MAXIM

3Msps/2Msps, 5V/3V, 2-Channel, True-Differential 12-Bit ADCs

MAX1332/MAX1333

General Description

The MAX1332/MAX1333 2-channel, serial-output, 12-bit, analog-to-digital converters (ADCs) feature two true-differential analog inputs and offer outstanding noise immunity and dynamic performance. Both devices easily interface with SPI™/QSPI™/MICROWIRE™ and standard digital signal processors (DSPs).

The MAX1332 operates from a single supply of +4.75V to +5.25V with sampling rates up to 3Msps. The MAX1333 operates from a single supply of +2.7V to +3.6V with sampling rates up to 2Msps. These devices feature a partial power-down mode and a full power-down mode that reduce the supply current to 3.3mA and 0.2µA, respectively. Also featured is a separate power supply input (DV$_{DD}$) that allows direct interfacing to +2.7V to +3.6V digital logic. The fast conversion speed, low power dissipation, excellent AC performance, and DC accuracy (±0.6 LSB INL) make the MAX1332/MAX1333 ideal for industrial process control, motor control, and base-station applications.

The MAX1332/MAX1333 are available in a space-saving (3mm x 3mm), 16-pin, TQFN package and operate over the extended (-40°C to +85°C) temperature range.

Applications

Data Acquisition

Bill Validation

Motor Control

Base Stations

High-Speed Modems

Optical Sensors

Industrial Process Control

Features

♦ **3Msps Sampling Rate (+5V, MAX1332)**

♦ **2Msps Sampling Rate (+3V, MAX1333)**

♦ **Separate Logic Supply: +2.7V to +3.6V**

♦ **Two True-Differential Analog Input Channels**

♦ **Bipolar/Unipolar Selection Input**

♦ **Only 38mW (typ) Power Consumption**

♦ **Only 2µA (max) Shutdown Current**

♦ **High-Speed, SPI-Compatible, 3-Wire Serial Interface**

♦ **2MHz Full-Linear Bandwidth**

♦ **71.4dB SINAD and -93dB THD at 525kHz Input Frequency**

♦ **No Pipeline Delays**

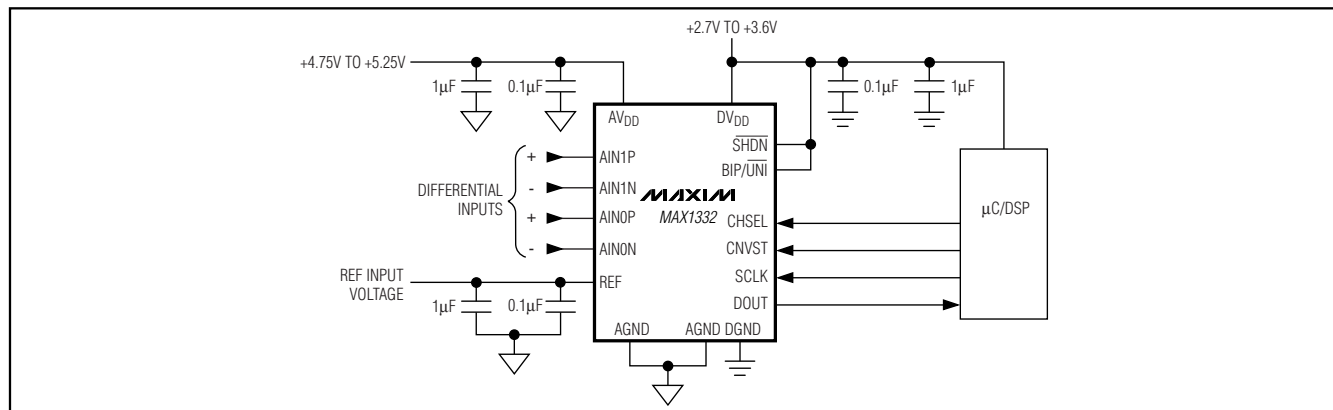♦ **Space-Saving (3mm x 3mm), 16-Pin, TQFN Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX1332ETE*	-40°C to +85°C	16 TQFN-EP** (3mm x 3mm)
MAX1333ETE	-40°C to +85°C	16 TQFN-EP** (3mm x 3mm)

Future product—contact factory for availability.

**EP = Exposed paddle.*

Selector Guide and Pin Configuration appear at end of data sheet.

Typical Operating Circuit

SPI/QSPI are trademarks of Motorola, Inc.

MICROWIRE is a trademark of National Semiconductor Corp.

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For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

3Msps/2Msps, 5V/3V, 2-Channel, True-Differential 12-Bit ADCs

ABSOLUTE MAXIMUM RATINGS

AV$_{DD}$ to AGND (MAX1332) ....-0.3V to +6V
AV$_{DD}$ to AGND (MAX1333) ....-0.3V to +4V
DV$_{DD}$ to DGND...-0.3V to +4V
AGND to DGND..-0.3V to +0.3V
SCLK, CNVST, $\overline{SHDN}$, CHSEL, BIP/$\overline{UNI}$,
   DOUT to DGND ....-0.3V to (DV$_{DD}$ + 0.3V)
AIN0P, AIN0N, AIN1P, AIN1N, REF to
   AGND..-0.3V to (AV$_{DD}$ + 0.3V)
Maximum Current into Any Pin ....±50mA

Continuous Power Dissipation (T$_A$ = +70°C)
   16-Pin TQFN (derate 17.5mW/°C above +70°C) 1398.6mW
Operating Temperature Range
   MAX133_ETE ....-40°C to +85°C
Junction Temperature ....+150°C
Storage Temperature Range ....-60°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (MAX1332)

(AV$_{DD}$ = +4.75V to +5.25V, DV$_{DD}$ = +2.7V to +3.6V, f$_{SCLK}$ = 48MHz, V$_{REF}$ = 4.096V, T$_A$ = T$_{MIN}$ to T$_{MAX}$, unless otherwise noted. Typical values are at T$_A$ = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY (BIP/$\overline{UNI}$ = DGND) (Note 1)						
Resolution	N		12			Bits
Integral Nonlinearity	INL			±0.6	±1.0	LSB
Differential Nonlinearity	DNL			±0.6	±1.0	LSB
Offset Error				±0.9	±3.0	LSB
Gain Error				±0.6	±6.0	LSB
Offset-Error Temperature Coefficient				±0.2		ppm/°C
Gain-Error Temperature Coefficient				±1.1		ppm/°C
DYNAMIC SPECIFICATIONS (A$_{IN}$ = -0.2dBFS, f$_{IN}$ = 525kHz, BIP/$\overline{UNI}$ = DV$_{DD}$, unless otherwise noted) (Note 1)						
Signal-to-Noise Ratio	SNR		70	71.5		dB
Signal-to-Noise Plus Distortion	SINAD		70	71.4		dB
Total Harmonic Distortion	THD			-93	-84	dBc
Spurious-Free Dynamic Range	SFDR		84	93		dBc
Channel-to-Channel Isolation				76		dB
Full-Linear Bandwidth		SINAD > 68dB		2		MHz
Full-Power Bandwidth				6		MHz
Small-Signal Bandwidth				6		MHz
CONVERSION RATE						
Minimum Conversion Time	t$_{CONV}$	Figure 5			271	ns
Maximum Throughput Rate			3			Msps
Minimum Track-and-Hold Acquisition Time	t$_{ACQ}$	Figure 5			52	ns

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ELECTRICAL CHARACTERISTICS (MAX1332) (continued)

(AV$_{DD}$ = +4.75V to +5.25V, DV$_{DD}$ = +2.7V to +3.6V, f$_{SCLK}$ = 48MHz, V$_{REF}$ = 4.096V, T$_A$ = T$_{MIN}$ to T$_{MAX}$, unless otherwise noted. Typical values are at T$_A$ = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Aperture Delay	t$_{AD}$	Figure 21		<10		ns
Aperture Jitter	t$_{AJ}$	Figure 21		<10		ps
DIFFERENTIAL ANALOG INPUTS (AIN0P, AIN0N, AIN1P, AIN1N)						
Differential Input Voltage Range (V$_{AIN\_P}$ - V$_{AIN\_N}$)	V$_{IN}$	BIP/$\overline{UNI}$ = DGND	0		V$_{REF}$	V
		BIP/$\overline{UNI}$ = DV$_{DD}$	-V$_{REF}$ / 2		+V$_{REF}$ / 2	
Absolute Input Voltage Range			AGND - 50mV		AV$_{DD}$ + 50mV	V
DC Leakage Current	I$_{LKG}$				±1	µA
Input Capacitance	C$_{IN}$			14		pF
REFERENCE INPUT (REF)						
REF Input Voltage Range	V$_{REF}$		1.0		AV$_{DD}$ + 50mV	V
REF Input Capacitance	C$_{REF}$			14		pF
REF DC Leakage Current	I$_{REF}$				±10	µA
DIGITAL INPUTS (SCLK, CNVST, $\overline{SHDN}$, CHSEL, BIP/$\overline{UNI}$)						
Input-Voltage Low	V$_{IL}$				0.3 x DV$_{DD}$	V
Input-Voltage High	V$_{IH}$		0.7 x DV$_{DD}$			V
Input Hysteresis				100		mV
Input Leakage Current	I$_{ILKG}$			±0.2	±5	µA
Input Capacitance	C$_{IN}$			15		pF
DIGITAL OUTPUT (DOUT)						
Output-Voltage Low	V$_{OL}$	I$_{SINK}$ = 5mA			0.4	V
Output-Voltage High	V$_{OH}$	I$_{SOURCE}$ = 1mA	DV$_{DD}$ - 0.5			V
Tri-State Leakage Current	I$_{LKGT}$	Between conversions, CNVST = DV$_{DD}$			±1	µA
Tri-State Output Capacitance	C$_{OUT}$	Between conversions, CNVST = DV$_{DD}$		15		pF
POWER REQUIREMENTS						
Analog Supply Voltage	AV$_{DD}$		4.75		5.25	V
Digital Supply Voltage	DV$_{DD}$		2.7		3.6	V
Analog Supply Current	I$_{AVDD}$	Normal mode; average current (f$_{SAMPLE}$ = 3MHz, f$_{SCLK}$ = 48MHz)		11	12	mA
		Partial power-down mode		3.5	6	
		Full power-down mode		0.1	2	µA

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ELECTRICAL CHARACTERISTICS (MAX1332) (continued)

(AV$_{DD}$ = +4.75V to +5.25V, DV$_{DD}$ = +2.7V to +3.6V, f$_{SCLK}$ = 48MHz, V$_{REF}$ = 4.096V, T$_A$ = T$_{MIN}$ to T$_{MAX}$, unless otherwise noted. Typical values are at T$_A$ = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Digital Supply Current	I$_{DVDD}$	Average current (f$_{SAMPLE}$ = 3MHz, f$_{SCLK}$ = 48MHz, zero-scale input)		4.5	7	mA
		Power-down (f$_{SCLK}$ = 48MHz), CNVST = DV$_{DD}$		15	30	µA
		Static; all digital inputs are connected to DV$_{DD}$ or DGND		0.2	2	
Power-Supply Rejection	PSR	AV$_{DD}$ = 4.75V to 5.25V, full-scale input			±2	mV

TIMING CHARACTERISTICS (MAX1332) (Figure 4)

(AV$_{DD}$ = +4.75V to +5.25V, DV$_{DD}$ = +2.7V to +3.6V, T$_A$ = T$_{MIN}$ to T$_{MAX}$, unless otherwise noted. Typical values are at T$_A$ = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Clock Period	t$_{CP}$		20.8			ns
SCLK Pulse Width	t$_{SPW}$		6			ns
CNVST Rise to DOUT Disable	t$_{CRDD}$		15			ns
CNVST Fall to DOUT Enable	t$_{CFDE}$		15			ns
CHSEL to CNVST Fall Setup	t$_{CHCF}$		40			ns
BIP/$\overline{UNI}$ to CNVST Fall Setup	t$_{BUCF}$		40			ns
CNVST Fall to CHSEL Hold	t$_{CFCH}$		0			ns
SCLK Fall to BIP/$\overline{UNI}$ Hold	t$_{CFBU}$		0			ns
DOUT Remains Valid After SCLK	t$_{DHOLD}$	C$_{LOAD}$ = 0pF (Note 2)	1	2		ns
SCLK Rise to DOUT Transition	t$_{DOT}$	C$_{LOAD}$ = 30pF			6	ns
CNVST to SCLK Rise	t$_{SETUP}$		6			ns
SCLK Rise to CNVST	t$_{HOLD}$		0			ns
CNVST Pulse Width	t$_{CSW}$		6			ns
Minimum Recovery Time (Full Power-Down)	t$_{FPD}$	From CNVST fall or $\overline{SHDN}$ rise			4	µs
Minimum Recovery Time (Partial Power-Down)	t$_{PPD}$	From CNVST fall			500	ns

Note 1: Tested with AV$_{DD}$ = 4.75V and DV$_{DD}$ = +2.7V.
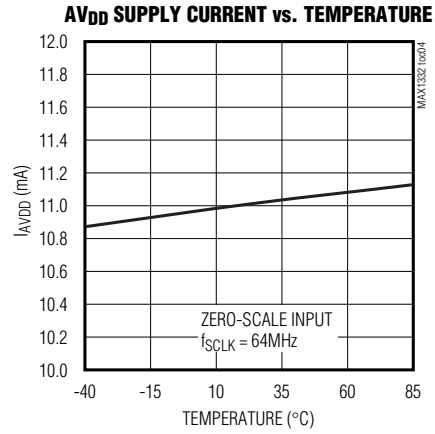**Note 2:** Guaranteed by design, not production tested.

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ELECTRICAL CHARACTERISTICS (MAX1333)

(AV$_{DD}$ = +2.7V to +3.6V, DV$_{DD}$ = +2.7V to AV$_{DD}$, f$_{SCLK}$ = 32MHz, V$_{REF}$ = 2.5V, T$_A$ = T$_{MIN}$ to T$_{MAX}$, unless otherwise noted. Typical values are at T$_A$ = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY (Note 3) (BIP/$\overline{\text{UNI}}$ = DGND)						
Resolution	N		12			Bits
Relative Accuracy	INL			±0.6	±1.0	LSB
Differential Nonlinearity	DNL			±0.6	±1.0	LSB
Offset Error				±0.9	±3.0	LSB
Gain Error				±0.6	±6.0	LSB
Offset-Error Temperature Coefficient				±1.1		ppm/°C
Gain-Error Temperature Coefficient				±0.2		ppm/°C
DYNAMIC SPECIFICATIONS (A$_{IN}$ = -0.2dBFS, f$_{IN}$ = 525kHz, BIP/$\overline{\text{UNI}}$ = DV$_{DD}$, unless otherwise noted) (Note 3)						
Signal-to-Noise Ratio	SNR		70	71.5		dB
Signal-to-Noise Plus Distortion	SINAD		70	71.4		dB
Total Harmonic Distortion	THD			-93	-86.5	dBc
Spurious-Free Dynamic Range	SFDR		83.5	93		dBc
Channel-to-Channel Isolation				76		dB
Full-Linear Bandwidth		SINAD > 68dB		1.7		MHz
Full-Power Bandwidth				5.5		MHz
Small-Signal Bandwidth				5		MHz
CONVERSION RATE						
Minimum Conversion Time	t$_{CONV}$	Figure 5			406	ns
Maximum Throughput Rate				2.0		Msps
Minimum Track-and-Hold Acquisition Time	t$_{ACQ}$	Figure 5			78	ns
Aperture Delay	t$_{AD}$	Figure 21		<10		ns
Aperture Jitter	t$_{AJ}$	Figure 21		<10		ps
DIFFERENTIAL ANALOG INPUTS (AIN0P, AIN0N, AIN1P, AIN1N)						
Differential Input Voltage Range (V$_{AIN\_P}$ - V$_{AIN\_N}$)	V$_{IN}$	BIP/$\overline{\text{UNI}}$ = DGND	0		V$_{REF}$	V
		BIP/$\overline{\text{UNI}}$ = DV$_{DD}$	-V$_{REF}$ / 2		+V$_{REF}$ / 2	
Absolute Input Voltage Range			AGND - 50mV		AV$_{DD}$ + 50mV	V
DC Leakage Current	I$_{LKG}$				±1	µA

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ELECTRICAL CHARACTERISTICS (MAX1333) (continued)

(AV$_{DD}$ = +2.7V to +3.6V, DV$_{DD}$ = +2.7V to AV$_{DD}$, f$_{SCLK}$ = 32MHz, V$_{REF}$ = 2.5V, T$_A$ = T$_{MIN}$ to T$_{MAX}$, unless otherwise noted. Typical values are at T$_A$ = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Capacitance	C$_{IN}$			14		pF
REFERENCE INPUT (REF)						
REF Input Voltage	V$_{REF}$		1.0		AV$_{DD}$ + 50mV	V
REF Input Capacitance	C$_{REF}$			14		pF
REF DC Leakage Current	I$_{REF}$				±10	µA
DIGITAL INPUTS (SCLK, CNVST, $\overline{SHDN}$, CHSEL, BIP/$\overline{UNI}$)						
Input-Voltage Low	V$_{IL}$				0.3 x DV$_{DD}$	V
Input-Voltage High	V$_{IH}$		0.7 x DV$_{DD}$			V
Input Hysteresis				100		mV
Input Leakage Current	I$_{ILKG}$			±0.2	±5	µA
Input Capacitance	C$_{IN}$			15		pF
DIGITAL OUTPUT (DOUT)						
Output-Voltage Low	V$_{OL}$	I$_{SINK}$ = 5mA			0.4	V
Output-Voltage High	V$_{OH}$	I$_{SOURCE}$ = 1mA	DV$_{DD}$ - 0.5			V
Tri-State Leakage Current	I$_{LKGT}$	Between conversions, CNVST = DV$_{DD}$			±1	µA
Tri-State Output Capacitance	C$_{OUT}$	Between conversions, CNVST = DV$_{DD}$		15		pF
POWER REQUIREMENTS						
Analog Supply Voltage	AV$_{DD}$		2.7		3.6	V
Digital Supply Voltage	DV$_{DD}$		2.7		AV$_{DD}$	V
Analog Supply Current	I$_{AVDD}$	Normal mode; average current (f$_{SAMPLE}$ = 2MHz, f$_{SCLK}$ = 32MHz)		9.5	11.5	mA
		Partial power-down mode		3.3	4	
		Full power-down mode		0.1	2	µA
Digital Supply Current	I$_{DVDD}$	Average current (f$_{SAMPLE}$ = 2MHz, f$_{SCLK}$ = 32MHz, zero-scale input)		3	5.4	mA
		Power-down (f$_{SCLK}$ = 32MHz, CNVST = DV$_{DD}$)		10	20	µA
		Static; all digital inputs are connected to DV$_{DD}$ or DGND		0.2	2	
Positive Supply Rejection	PSR	AV$_{DD}$ = 2.7V to 3.6V, full-scale input			±3	mV

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TIMING CHARACTERISTICS (MAX1333) (Figure 4)

(AV$_{DD}$ = +2.7V to +3.6V, DV$_{DD}$ = +2.7V to AV$_{DD}$, T$_A$ = T$_{MIN}$ to T$_{MAX}$, unless otherwise noted. Typical values are at T$_A$ = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Clock Period	t$_{CP}$		31.2			ns
SCLK Pulse Width	t$_{CPW}$		10			ns
CNVST Rise to DOUT Disable	t$_{CRDD}$		15			ns
CNVST Fall to DOUT Enable	t$_{CFDE}$		15			ns
CHSEL to CNVST Fall Setup	t$_{CHCF}$		50			ns
BIP/$\overline{UNI}$ to CNVST Fall Setup	t$_{BUCF}$		50			ns
CNVST Fall to CHSEL Hold	t$_{CFCH}$		0			ns
SCLK Fall to BIP/$\overline{UNI}$ Hold	t$_{CFBU}$		0			ns
DOUT Remains Valid After SCLK	t$_{DHOLD}$	C$_{LOAD}$ = 0pF (Note 4)	1	2		ns
SCLK Rise to DOUT Transition	t$_{DOT}$	C$_{LOAD}$ = 30pF			6	ns
CNVST to SCLK Rise	t$_{SETUP}$		6			ns
SCLK Rise to CNVST	t$_{HOLD}$		0			ns
CNVST Pulse Width	t$_{CSW}$		6			ns
Minimum Recovery Time (Full Power-Down)	t$_{FPD}$	From CNVST fall or $\overline{SHDN}$ rise			4	µs
Minimum Recovery Time (Partial Power-Down)	t$_{PPD}$	From CNVST fall			500	ns

Note 3: Tested with AV$_{DD}$ = DV$_{DD}$ = +2.7V.
Note 4: Guaranteed by design, not production tested.
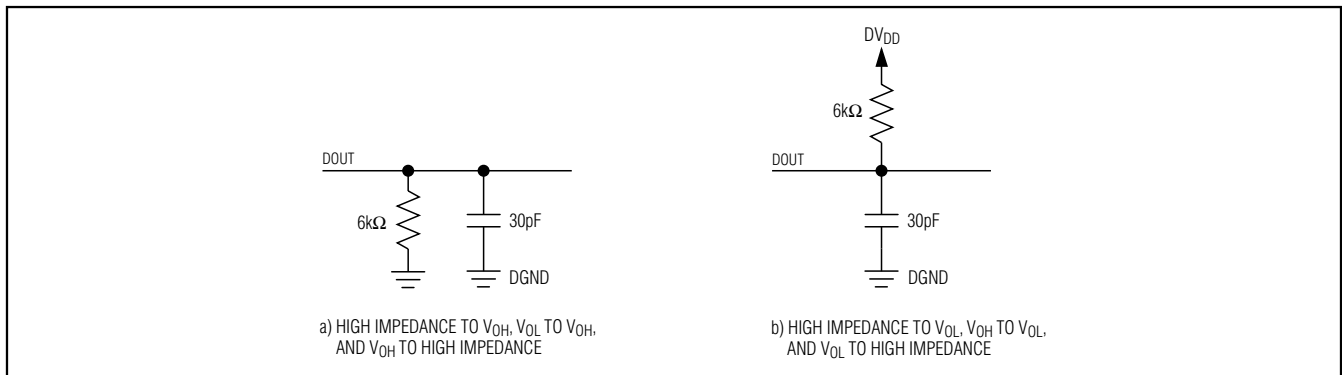
Figure 1. Load Circuits for Enable/Disable Times

3Msps/2Msps, 5V/3V, 2-Channel, True-Differential 12-Bit ADCs

Typical Operating Characteristics

(AV$_{DD}$ = +5V, DV$_{DD}$ = +3V, V$_{REF}$ = 4.096V, f$_{SCLK}$ = 64MHz. T$_A$ = +25°C, unless otherwise noted.)
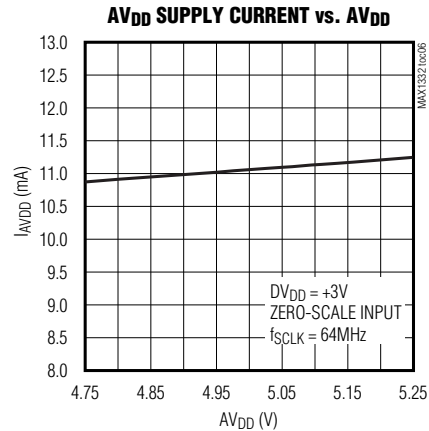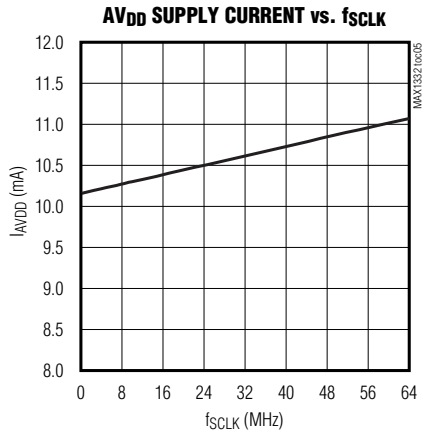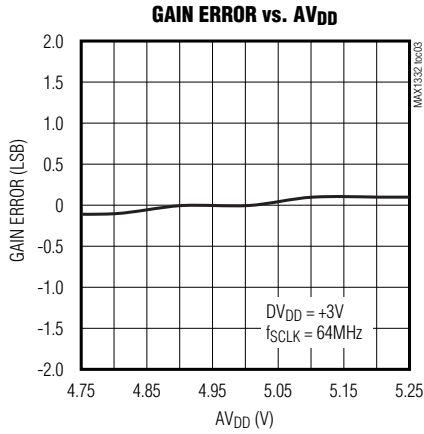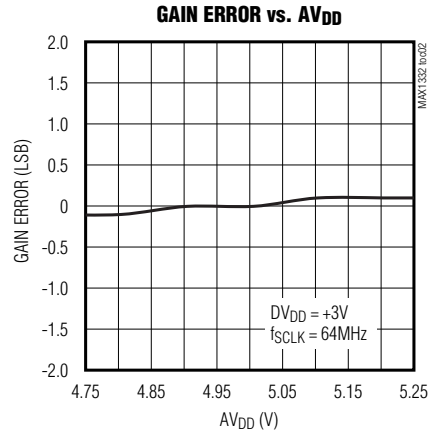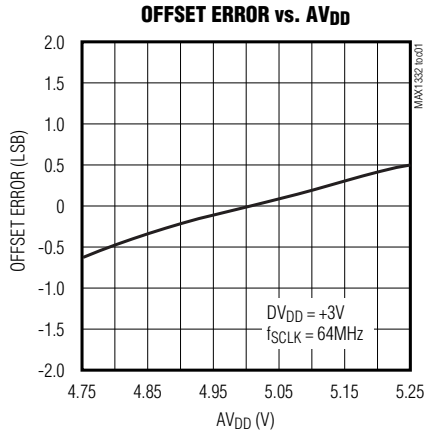
MAX1332

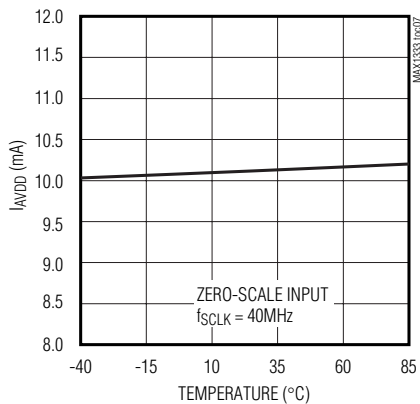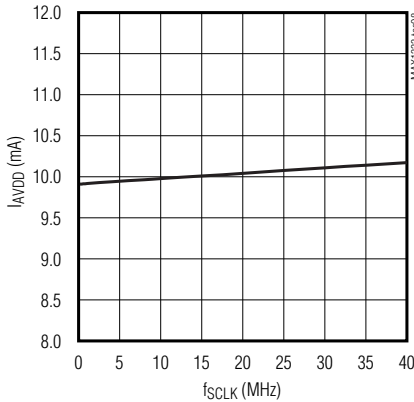OFFSET ERROR vs. AV$_{DD}$
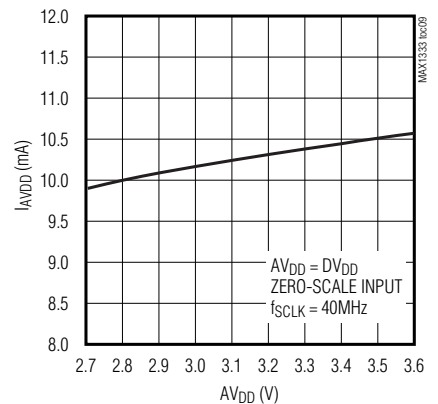
GAIN ERROR vs. AV$_{DD}$

GAIN ERROR vs. AV$_{DD}$

AV$_{DD}$ SUPPLY CURRENT vs. TEMPERATURE

AV$_{DD}$ SUPPLY CURRENT vs. f$_{SCLK}$
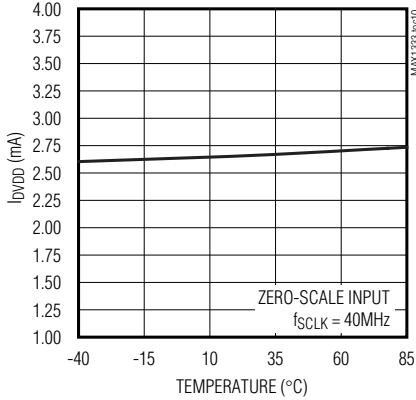
AV$_{DD}$ SUPPLY CURRENT vs. AV$_{DD}$

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Typical Operating Characteristics (continued)

(AV$_{DD}$ = +5V, DV$_{DD}$ = +3V, V$_{REF}$ = 4.096V, f$_{SCLK}$ = 64MHz. T$_A$ = +25°C, unless otherwise noted.)
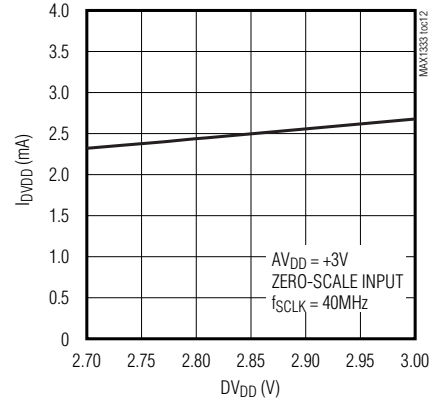
MAX1332

DV$_{DD}$ SUPPLY CURRENT vs. TEMPERATURE
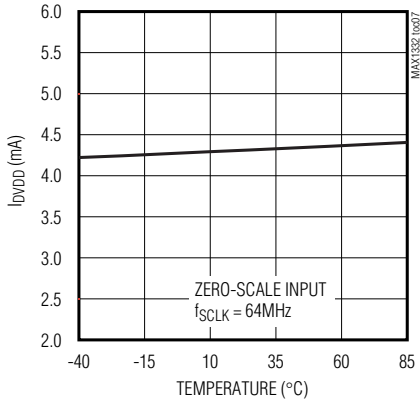
DV$_{DD}$ SUPPLY CURRENT vs. f$_{SCLK}$
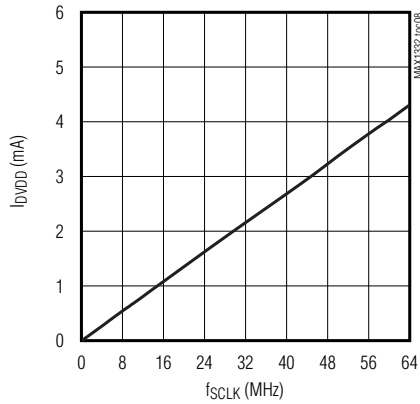
DV$_{DD}$ SUPPLY CURRENT vs. DV$_{DD}$
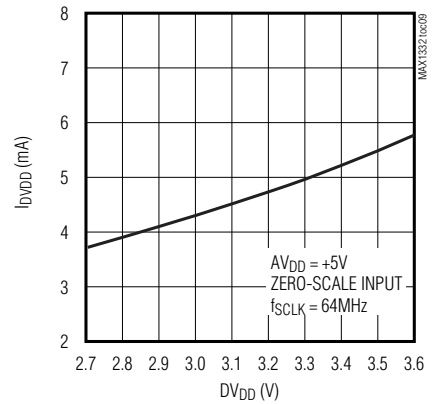
TOTAL SUPPLY CURRENT
vs. THROUGHPUT RATE
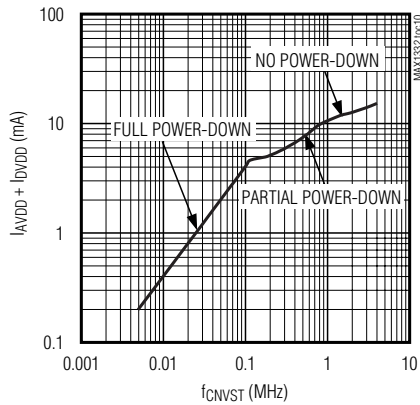
3Msps/2Msps, 5V/3V, 2-Channel, True-Differential 12-Bit ADCs

_____Typical Operating Characteristics (continued)

(AV$_{DD}$ = +3V, DV$_{DD}$ = +3V, V$_{REF}$ = 2.5V, f$_{SCLK}$ = 40MHz. T$_A$ = +25°C, unless otherwise noted.)

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INTEGRAL NONLINEARITY vs. OUTPUT CODE
f$_{SCLK}$ = 32MHz
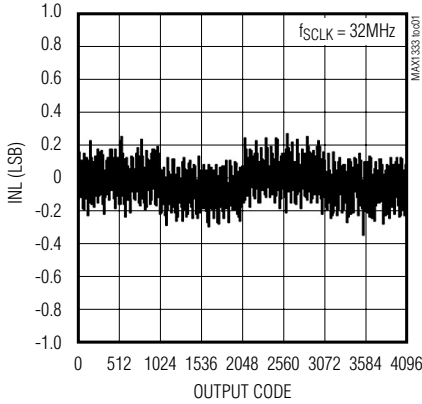
DIFFERENTIAL NONLINEARITY vs. OUTPUT CODE
f$_{SCLK}$ = 32MHz
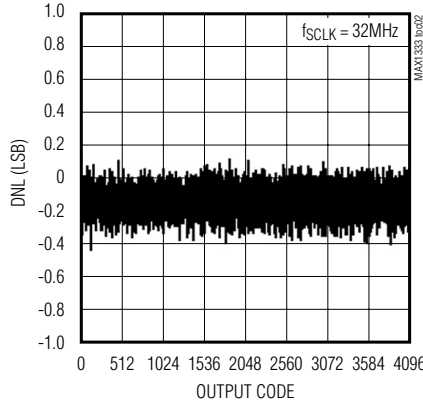
OFFSET ERROR vs. TEMPERATURE
AV$_{DD}$ = +3V

OFFSET ERROR vs. AV$_{DD}$
DV$_{DD}$ = AV$_{DD}$
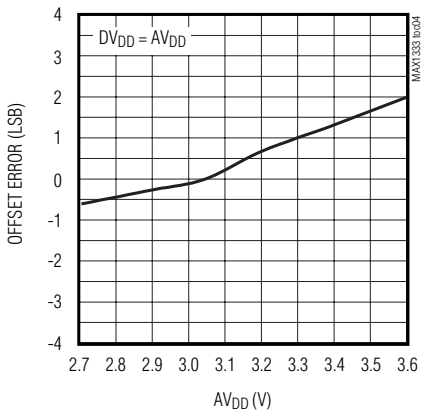
GAIN ERROR vs. TEMPERATURE
AV$_{DD}$ = +3V

GAIN ERROR vs. AV$_{DD}$
DV$_{DD}$ = AV$_{DD}$

AV$_{DD}$ SUPPLY CURRENT vs. TEMPERATURE
ZERO-SCALE INPUT
f$_{SCLK}$ = 40MHz

AV$_{DD}$ SUPPLY CURRENT vs. f$_{SCLK}$

AV$_{DD}$ SUPPLY CURRENT vs. AV$_{DD}$
AV$_{DD}$ = DV$_{DD}$
ZERO-SCALE INPUT
f$_{SCLK}$ = 40MHz

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Typical Operating Characteristics (continued)

$(AV_{DD} = +3V, DV_{DD} = +3V, V_{REF} = 2.5V, f_{SCLK} = 40MHz. T_A = +25°C$, unless otherwise noted.)
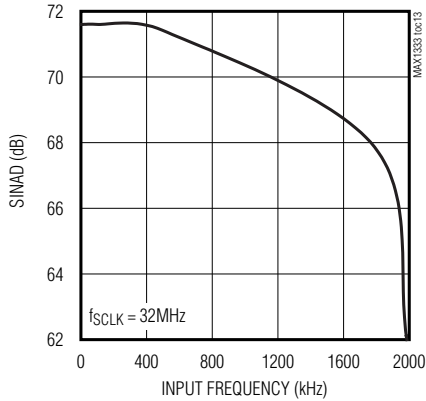
MAX1333

DV_DD SUPPLY CURRENT vs. TEMPERATURE

DV_DD SUPPLY CURRENT vs. f_SCLK
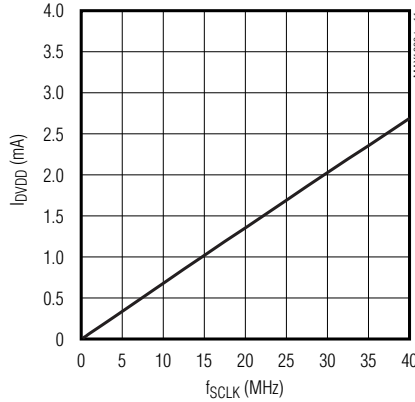
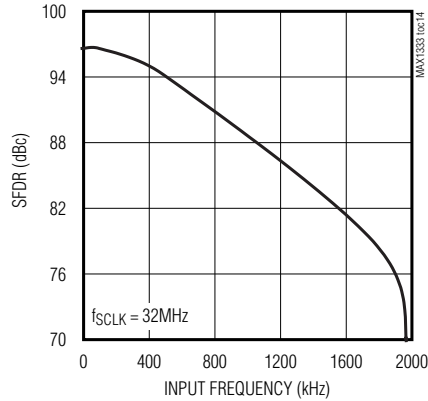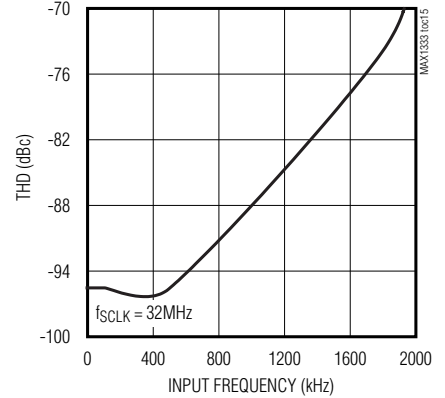
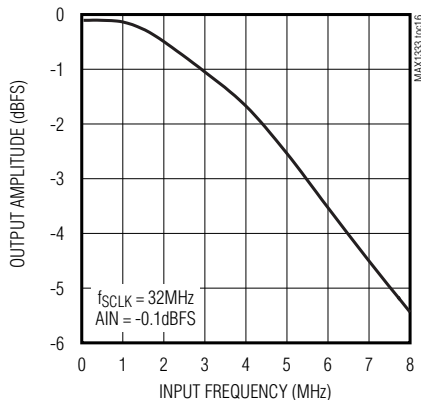DV_DD SUPPLY CURRENT vs. DV_DD

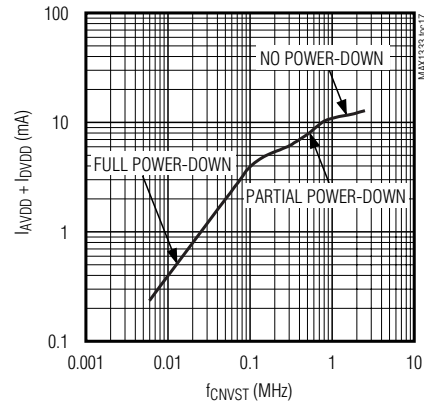SINAD vs. INPUT FREQUENCY

SFDR vs. INPUT FREQUENCY

THD vs. INPUT FREQUENCY

OUTPUT AMPLITUDE vs. INPUT FREQUENCY

TOTAL SUPPLY CURRENT vs. THROUGHPUT RATE

3Msps/2Msps, 5V/3V, 2-Channel, True-Differential 12-Bit ADCs

Pin Description

PIN	NAME	FUNCTION
1	AIN0P	Positive Analog-Input Channel 0
2	AIN0N	Negative Analog-Input Channel 0
3	AIN1P	Positive Analog-Input Channel 1
4	AIN1N	Negative Analog-Input Channel 1
5	REF	External Reference Voltage Input. V_{REF} = 1V to (AV_{DD} + 50mV). Bypass REF to AGND with a 0.1µF and a 1µF.
6	$\overline{SHDN}$	Shutdown Input. Pull $\overline{SHDN}$ low to enter full power-down mode. Drive $\overline{SHDN}$ high to resume normal operation regardless of previous software entered into power-down mode.
7	BIP/$\overline{UNI}$	Analog-Input-Mode Select. Drive BIP/$\overline{UNI}$ high to select bipolar-input mode. Pull BIP/$\overline{UNI}$ low to select unipolar-input mode.
8	AGND	Analog Ground. Connect all AGNDs and EP to the same potential.
9	CHSEL	Channel-Select Input. Drive CHSEL high to select channel 1. Pull CHSEL low to select channel 0.
10	CNVST	Conversion-Start Input. The first rising edge of CNVST powers up the MAX1332/MAX1333 and begins acquiring the analog input. A falling edge samples the analog input and starts a conversion. CNVST also controls the power-down mode of the device (see the *Partial Power-Down (PPD) and Full Power-Down (FPD) Mode* section).
11	SCLK	Serial-Clock Input. Clocks data out of the serial interface. SCLK also sets the conversion speed.
12	DOUT	Serial-Data Output. Data is clocked out on the rising edge of SCLK (see the *Starting a Conversion* section).
13	DV_{DD}	Positive-Digital-Supply Input. DV_{DD} is the positive supply input for the digital section of the MAX1332/MAX1333. Connect DV_{DD} to a 2.7V to 3.6V power supply. Bypass DV_{DD} to DGND with a 0.1µF capacitor in parallel with a 1µF capacitor. Place the bypass capacitors as close to the device as possible.
14	DGND	Digital Ground. Ensure that the potential difference between AGND and DGND is less than ±0.3V.
15	AV_{DD}	Positive-Analog-Supply Input. AV_{DD} is the positive supply input for the analog section of the MAX1332/MAX1333. Connect AV_{DD} to a 4.75V to 5.25V power supply for the MAX1332. Connect AV_{DD} to a 2.7V to 3.6V power supply for the MAX1333. Bypass AV_{DD} to AGND with a 0.1µF capacitor in parallel with a 1µF capacitor. Place the bypass capacitors as close to the device as possible.
16	AGND	Analog Ground. Connect all AGNDs and EP to the same potential.
—	EP	Exposed Paddle. Internally connected to AGND. Connect the exposed paddle to the analog ground plane.

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MAX1332/MAX1333

Detailed Description

The MAX1332/MAX1333 use an input track and hold (T/H) circuit along with a successive-approximation register (SAR) to convert a differential analog input signal to a digital 12-bit output. The serial interface requires only three digital lines (SCLK, CNVST, and DOUT) and provides easy interfacing to microcontrollers (µCs) and DSPs. Figure 2 shows the simplified block diagram for the MAX1332/MAX1333.

Power Supplies

The MAX1332/MAX1333 accept two power supplies that allow the digital noise to be isolated from sensitive analog circuitry. For both the MAX1332 and MAX1333, the digital power-supply input accepts a supply voltage of +2.7V to +3.6V. However, the supply voltage range for the analog power supply is different for each device. The MAX1332 accepts a +4.75V to +5.25V analog power supply, and the MAX1333 accepts a +2.7V to +3.6V analog power supply. See the *Layout, Grounding, and Bypassing* section for information on how to isolate digital noise from the analog power input.

The MAX1332/MAX1333s' analog power supply consists of one AV_{DD} input, two AGND inputs, and the exposed paddle (EP). The digital power input consists of one DV_{DD} input and one DGND input. Ensure that the potential on both AGND inputs is the same. Furthermore, ensure that the potential between AGND and DGND is limited to ±0.3V. Ideally there should be no potential difference between AGND and DGND. There are no power sequencing issues between AV_{DD} and DV_{DD}. The analog and digital power supplies are insensitive to power-up sequencing.

True-Differential Analog Input T/H

The equivalent input circuit of Figure 3 shows the MAX1332/MAX1333s' input architecture, which is composed of a T/H, a comparator, and a switched-capacitor DAC. On power-up, the MAX1332/MAX1333 enter full power-down mode. Drive CNVST high to exit full power-down mode and to start acquiring the input. The positive input capacitor is connected to AIN_P and the negative input capacitor is connected to AIN_N. The T/H enters its hold mode on the falling edge of CNVST and the ADC starts converting the sampled difference between the analog inputs. Once a conversion has been initiated, the T/H enters acquisition mode for the next conversion on the 13th falling edge of SCLK after CNVST has been transitioned from high to low.

The time required for the T/H to acquire an input signal is determined by how quickly its input capacitance is charged. If the input signal's source impedance is high,
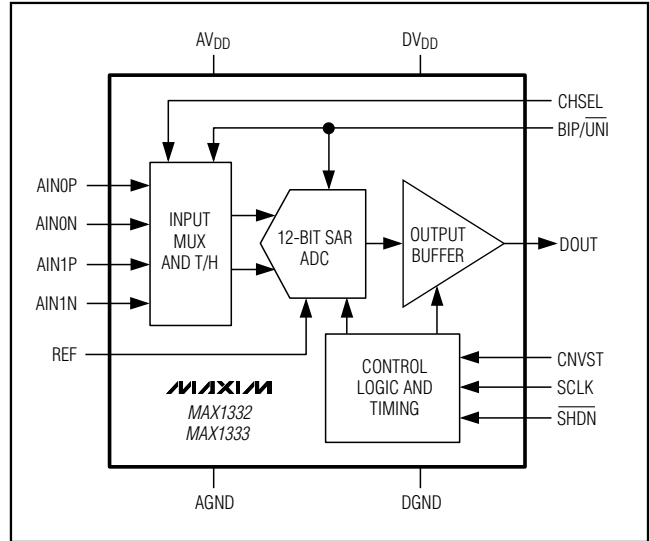

Figure 2. Simplified Functional Diagram

the acquisition time lengthens. The acquisition time, t_{ACQ}, is the minimum time needed for the signal to be acquired. It is calculated by the following equation:

$$t_{ACQ} \geq k \times (R_{SOURCE} + R_{IN}) \times C_{IN}$$

where:

$$k = 9 \approx \ln(2 \times 2N)$$

The constant k is the number of RC time constants required so that the voltage on the internal sampling capacitor reaches N-bit accuracy, i.e., so that the difference between the input voltage and the sampling capacitor voltage is equal to 0.5 LSB. N = 12 for the MAX1332/MAX1333.

R_{IN} = 250Ω is the equivalent differential analog input resistance, C_{IN} = 14pF is the equivalent differential analog input capacitance, and R_{SOURCE} is the source impedance of the input signal. Note that t_{ACQ} is never less than 52µs for the MAX1332 and 78µs for the MAX1333, and any source impedance below 160Ω does not significantly affect the ADC's AC performance.

Input Bandwidth

The ADC's input-tracking circuitry has a 5MHz small-signal bandwidth, making it possible to digitize high-speed transient events and measure periodic signals with bandwidths exceeding the ADC's sampling rate by using undersampling techniques. To avoid high-frequency signals being aliased into the frequency band

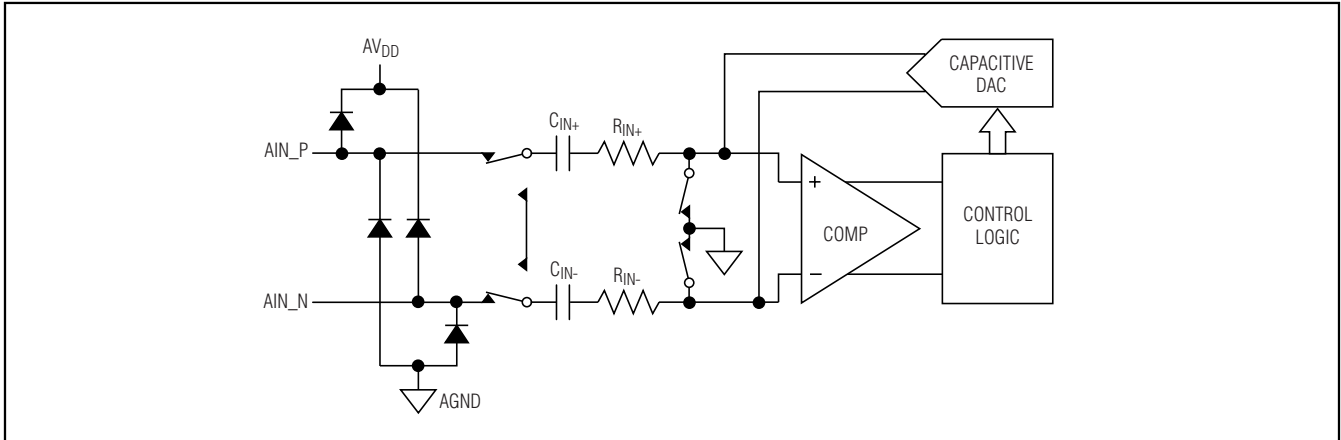# 3Msps/2Msps, 5V/3V, 2-Channel, True-Differential 12-Bit ADCs

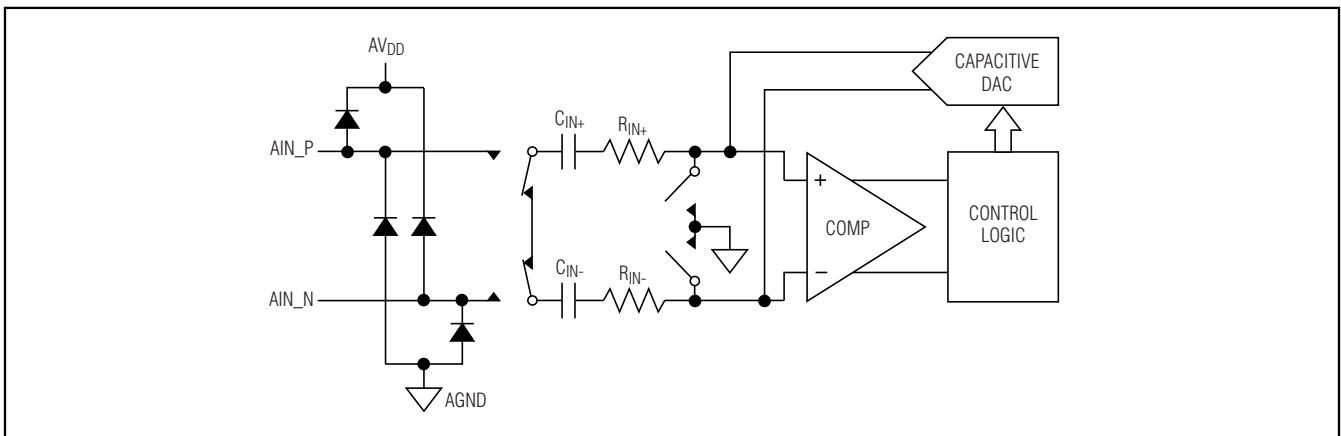Figure 3a. Equivalent Input Circuit (Acquisition Mode)

Figure 3b. Equivalent Input Circuit (Hold/Conversion Mode)

of interest, lowpass or bandpass filtering is recommended to limit the bandwidth of the input signal.

Input Buffer

To improve the input signal bandwidth under AC conditions, drive the input with a wideband buffer (>50MHz) that can drive the ADC's input capacitance (14pF) and settle quickly. Most applications require an input buffer to achieve 12-bit accuracy. Although slew rate and bandwidth are important, the most critical input buffer specification is settling time. The sampling requires an acquisition time of 52µs for the MAX1332 and 78µs for the MAX1333. At the beginning of the acquisition, the ADC internal sampling capacitors connect to the analog inputs, causing some disturbance. Ensure the amplifier is capable of settling to at least 12-bit accuracy during this interval. Use a low-noise, low-distortion, wideband amplifier that settles quickly and is stable with the ADC's 14pF input capacitance.

See the Maxim website (www.maxim-ic.com) for application notes on how to choose the optimum buffer amplifier for an ADC application. The MAX4430 is one of the devices that is ideal for this application.

Differential Analog Input Range and Protection

The MAX1332/MAX1333 produce a digital output that corresponds to the differential analog input voltage as long as the differential analog inputs are within the specified range. When operating in unipolar mode ($\overline{BIP}/\overline{UNI}$ = 0), the usable differential analog input range is from 0 to V_{REF}. When operating in bipolar mode ($\overline{BIP}/\overline{UNI}$ = 1), the differential analog input range is from -$V_{REF}/2$ to +$V_{REF}/2$. In both unipolar and bipolar
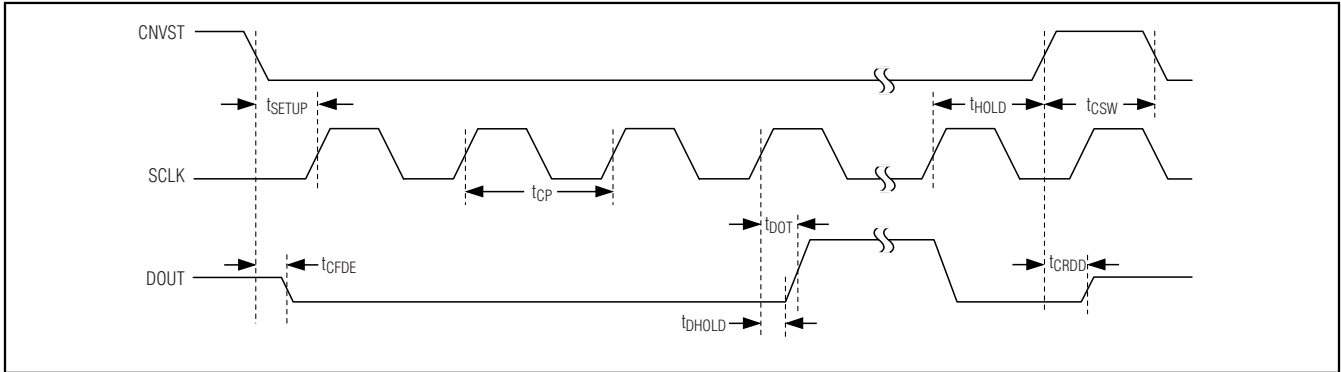
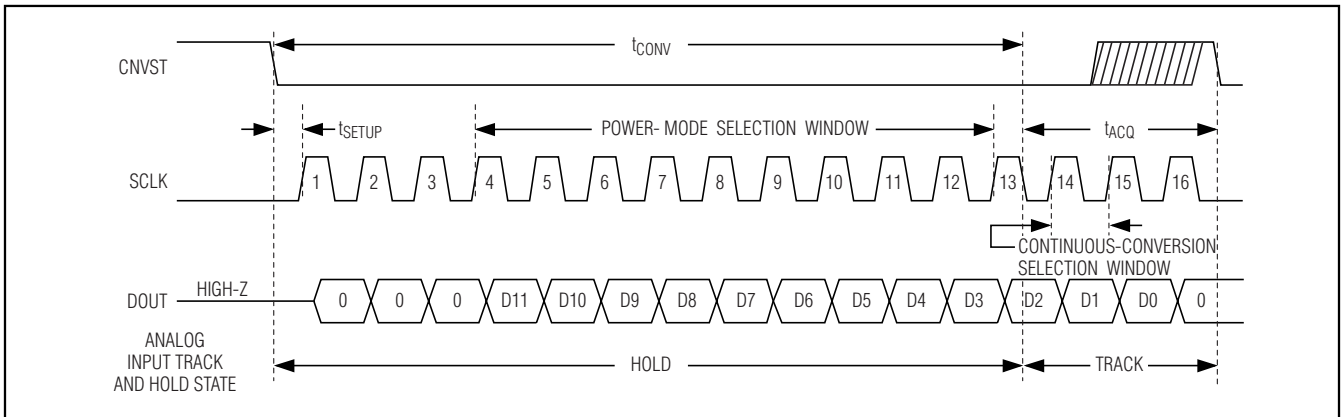**MAXIM**

Figure 4. Detailed Serial-Interface Timing

Figure 5. Interface Timing Sequence

modes, the input common-mode voltage can vary as long as the voltage at any single analog input (V_{AIN_P}, V_{AIN_N}) remains within 50mV of the analog power supply rails (AV_{DD}, AGND).

As shown in Figure 3, internal protection diodes confine the analog input voltage within the region of the analog power-supply rails (AV_{DD}, AGND) and allow the analog input voltage to swing from AGND - 0.3V to AV_{DD} + 0.3V without damage. Input voltages beyond AGND - 0.3V and AV_{DD} + 0.3V forward bias the internal protection diodes. In this situation, limit the forward diode current to 50mA to avoid damaging the MAX1332/MAX1333.

Serial Digital Interface

Timing and Control

Conversion-start and data-read operations are controlled by the CNVST and SCLK digital inputs. CNVST controls the state of the T/H as well as when a conversion is initiated. CNVST also controls the power-down mode of the device (see the *Partial Power-Down (PPD)* and *Full Power-Down (FPD) Mode* section). SCLK clocks data out of the serial interface and sets the conversion speed. Figures 4 and 5 show timing diagrams that outline the serial-interface operation.

Starting a Conversion

On power-up, the MAX1332/MAX1333 enter full power-down mode. The first rising edge of CNVST exits the full power-down mode and the MAX1332/MAX1333 begin acquiring the analog input. A CNVST falling edge initiates a conversion sequence. The T/H stage holds the input voltage; DOUT changes from high impedance to logic low; and the ADC begins to convert at the first SCLK rising edge. SCLK is used to drive the conversion process, and it shifts data out of DOUT. SCLK begins shifting out the data after the 4th rising edge of SCLK. DOUT transitions t_{DOT} after each SCLK's rising edge and remains valid for t_{DHOLD} after the next rising edge. The 4th rising clock edge produces the MSB of the conversion result at DOUT, and the MSB remains valid t_{DHOLD} after the 5th rising edge of SCLK. Sixteen

3Msps/2Msps, 5V/3V, 2-Channel, True-Differential 12-Bit ADCs
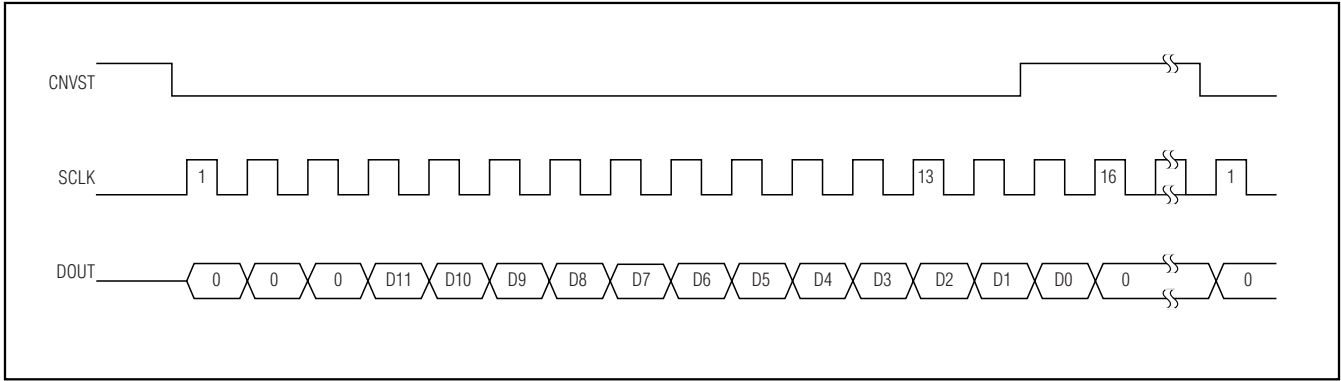

Figure 6. Continuous Conversion with Burst or Continuous Clock
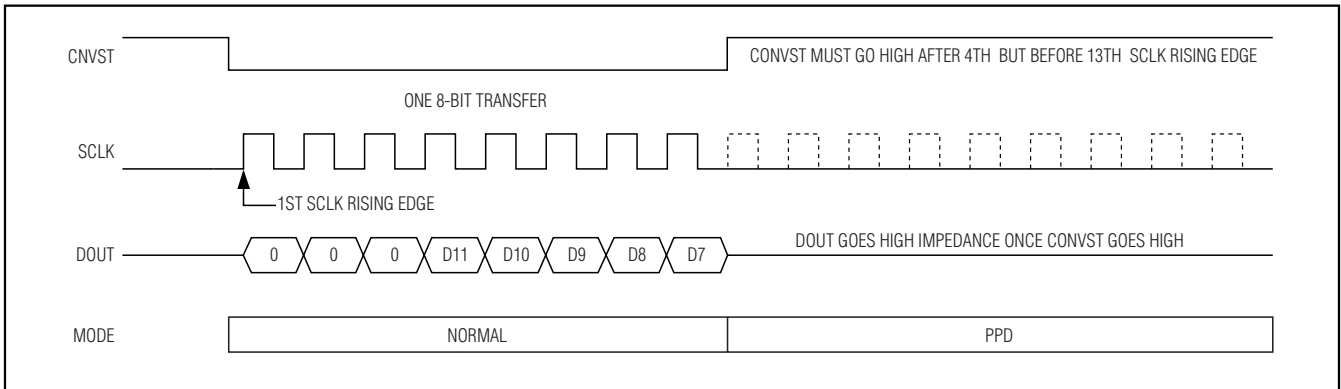

Figure 7. SPI Interface—Partial Power-Down

rising SCLK edges are needed to clock out the three leading zeros, 12 data bits, and a trailing zero. For continuous operation, pull CNVST high between the 14th and the 15th rising edges of SCLK. The highest throughput is achieved when performing continuous conversions. If CNVST is low during the rising edge of the 16th SCLK, the DOUT line goes to a high-impedance state on either CNVST's rising edge or the next SCLK's rising edge, enabling the serial interface to be shared by multiple devices. Figure 6 illustrates a conversion using a typical serial interface.

Partial Power-Down (PPD) and Full Power-Down (FPD) Mode

Power consumption is reduced significantly by placing the MAX1332/MAX1333 in either partial power-down mode or full power-down mode. Partial power-down mode is ideal for infrequent data sampling and fast wake-up time applications. Once CNVST is transitioned from high to low, pull CNVST high any time after the 4th rising edge of the SCLK but before the 13th rising edge of the SCLK to enter partial power-down mode (see Figure 7). Drive CNVST low and then drive high before the 4th SCLK to remain in partial power-down mode. This reduces the supply current to 3.3mA. Drive CNVST low and allow at least 13 SCLK cycles to elapse before driving CNVST high to exit partial power-down mode.

Full power-down mode reduces the supply current to 0.2μA and is ideal for infrequent data sampling. To enter full power-down mode, the MAX1332/MAX1333 must first be in partial power-down mode. While in partial power-down mode, repeat the sequence used to enter partial power-down mode to enter full power-down mode (see Figure 8). Drive CNVST low and allow at least 13 SCLK cycles to elapse before driving CNVST high to exit full power-down mode.

Maintain a logic low or a logic high on SCLK and all digital inputs at DV$_{DD}$ or DGND while in either partial power-down or full power-down mode to minimize power consumption.
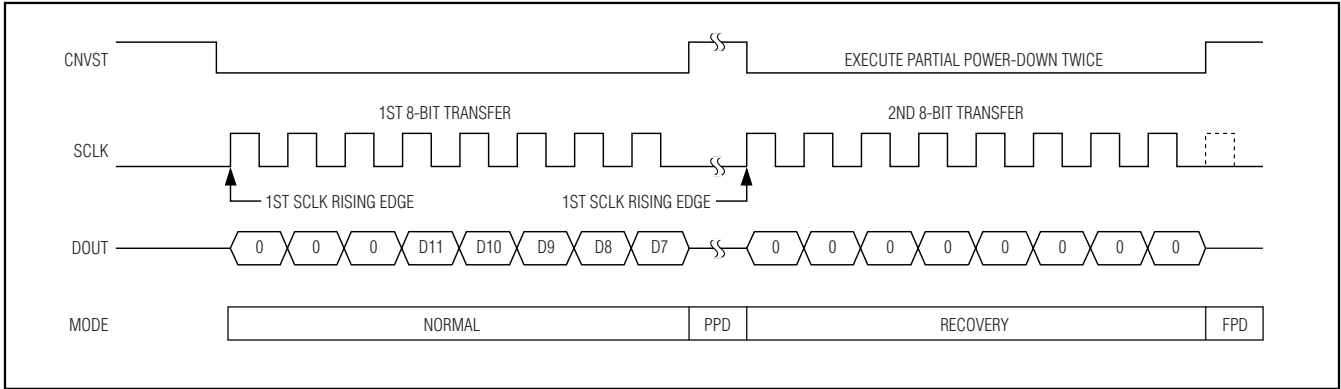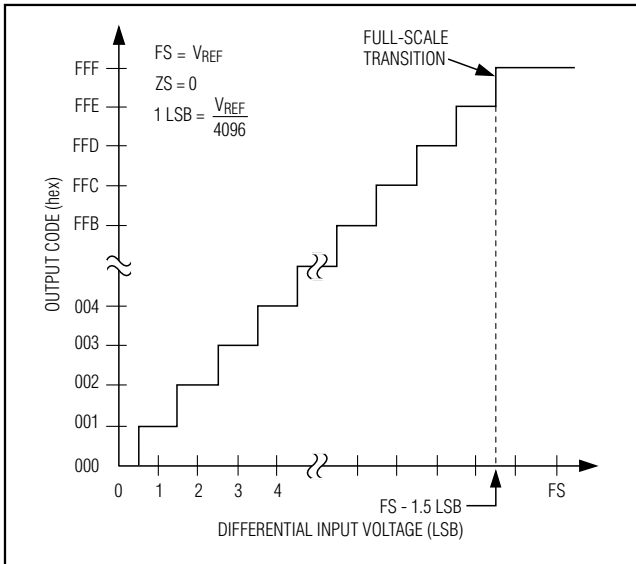
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Figure 8. SPI Interface—Full Power-Down

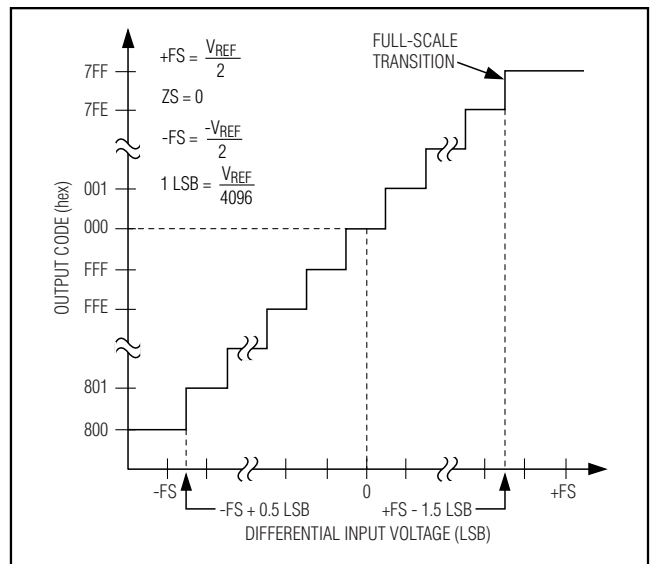Figure 9. Unipolar Transfer Function

Figure 10. Bipolar Transfer Function

Another way of entering the full power-down mode is using the $\overline{\text{SHDN}}$ input. Drive $\overline{\text{SHDN}}$ to a logic low to put the device into the full power-down mode. Drive $\overline{\text{SHDN}}$ high to exit full power-down mode and return to normal operating mode. $\overline{\text{SHDN}}$ overrides any software-controlled power-down mode and every time it is deasserted, it places the MAX1332/MAX1333 in its normal mode of operation regardless of its previous state.

Transfer Function

The MAX1332/MAX1333 output is straight binary in unipolar mode and is two's complement in bipolar mode. Figure 9 shows the unipolar transfer function for the MAX1332/MAX1333. Table 1 shows the unipolar relationship between the differential analog input voltage and the digital output code. Figure 10 shows the bipolar transfer function for the MAX1332/MAX1333. Table 2 shows the bipolar relationship between the differential analog input voltage and the digital output code.

3Msps/2Msps, 5V/3V, 2-Channel, True-Differential 12-Bit ADCs

Table 1. Unipolar Code Table (MAX1332)

BINARY DIGITAL OUTPUT CODE D11–D0	HEXADECIMAL EQUIVALENT OF D11–D0	DECIMAL EQUIVALENT OF D11–D0 (CODE$_{10}$)	DIFFERENTIAL INPUT VOLTAGE (V) (V$_{REF}$ = 4.096V)
1111 1111 1111	0xFFF	4095	+4.095 ±0.5 LSB
1111 1111 1110	0xFFE	4094	+4.094 ±0.5 LSB
1000 0000 0001	0x801	2049	+2.049 ±0.5 LSB
1000 0000 0000	0x800	2048	+2.048 ±0.5 LSB
0111 1111 1111	0x7FF	2047	+2.047 ±0.5 LSB
0000 0000 0001	0x001	1	+0.001 ±0.5 LSB
0000 0000 0000	0x000	0	+0.000 ±0.5 LSB

Table 2. Bipolar Code Table (MAX1332)

TWO's-COMPLEMENT DIGITAL OUTPUT CODE D11–D0	HEXADECIMAL EQUIVALENT OF D11–D0	DECIMAL EQUIVALENT OF D11–D0 (CODE$_{10}$)	DIFFERENTIAL INPUT VOLTAGE (V) (V$_{REF}$ = 4.096V)
0111 1111 1111	0x7FF	+2047	+2.047 ±0.5 LSB
0111 1111 1110	0x7FE	+2046	+2.046 ±0.5 LSB
0000 0000 0001	0x001	+1	+0.001 ±0.5 LSB
0000 0000 0000	0x000	0	0.000 ±0.5 LSB
1111 1111 1111	0xFFF	-1	-0.001 ±0.5 LSB
1000 0000 0001	0x801	-2047	-2.047 ±0.5 LSB
1000 0000 0000	0x800	-2048	-2.048 ±0.5 LSB

Determine the differential analog input voltage as a function of V$_{REF}$ and the digital output code with the following equation:

$$\Delta V_{AIN} = LSB \times CODE_{10} \pm 0.5 \times LSB$$

where:

$$\Delta V_{AIN} = V_{AIN\_P} - V_{AIN\_N}$$

$$LSB = \frac{V_{REF}}{2^{12}} = \frac{V_{REF}}{4096}$$

CODE$_{10}$ = the decimal equivalent of the digital output code (see Tables 1 and 2).

±0.5 x LSB represents the quantization error that is inherent to any ADC.

When using a 4.096V reference, 1 LSB equals 1.0mV. When using a 2.5V reference, 1 LSB equals 0.61mV.

_____Applications Information

External Reference

The MAX1332/MAX1333 use an external reference between 1V and (AV$_{DD}$ + 50mV). Bypass REF with a 1µF capacitor in parallel with a 0.1µF capacitor to AGND for best performance (see the _Typical Operating Circuit_).

Connection to Standard Interfaces

The MAX1332/MAX1333 serial interface is fully compatible with SPI, QSPI and MICROWIRE (see Figure 11). If a serial interface is available, set the µC's serial interface in master mode so the µC generates the serial clock. Choose a clock frequency based on the AV$_{DD}$ and DV$_{DD}$ amplitudes.

SPI and MICROWIRE

When using SPI or MICROWIRE, the MAX1332/MAX1333 are compatible with all four modes programmed with the CPHA and CPOL bits in the SPI or MICROWIRE control register. (This control register is in

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the bus master, not the MAX1332/MAX1333.) Conversion begins with a CNVST falling edge. DOUT goes low, indicating a conversion is in progress. Two consecutive 1-byte reads are required to get the full 12 bits from the ADC. DOUT transitions on SCLK rising edges and is guaranteed to be valid t_{DOT} later and remain valid until t_{DHOLD} after the following SCLK rising edge. When using CPOL = 0 and CPHA = 0 or CPOL = 1 and CPHA = 1, the data is clocked into the μC on the following or next SCLK rising edge. When using CPOL = 0 and CPHA = 1 or CPOL = 1 and CPHA = 0, the data is clocked into the μC on the next falling edge. See Figure 11 for connections and Figures 12 and 13 for timing. See the *Timing Characteristics* table to determine the best mode to use.

QSPI

Unlike SPI, which requires two 1-byte reads to acquire the 12 bits of data from the ADC, QSPI allows acquiring the conversion data with a single 16-bit transfer. The MAX1332/MAX1333 require 16 clock cycles from the μC to clock out the 12 bits of data. Figure 14 shows a transfer using CPOL = 1 and CPHA = 1. The conversion result contains three zeros, followed by the 12 data bits and a trailing zero with the data in MSB-first format.

DSP Interface to the TMS320C54_

The MAX1332/MAX1333 can be directly connected to the TMS320C54_ family of DSPs from Texas Instruments. Set the DSP to generate its own clocks or use external clock signals. Use either the standard or buffered serial port. Figure 15 shows the simplest interface between the MAX1332/MAX1333 and the TMS320C54_, where the transmit serial clock (CLKX) drives the receive serial clock (CLKR) and SCLK, and the transmit frame sync (FSX) drives the receive frame sync (FSR) and CNVST.

For continuous conversion, set the serial port to transmit a clock and pulse the frame sync signal for a clock period before data transmission. Use the serial port configuration (SPC) register to set up with internal frame sync (TXM = 1), CLKX driven by an on-chip clock source (MCM = 1), burst mode (FSM = 1), and 16-bit word length (FO = 0).

This setup allows continuous conversions provided that the data transmit register (DXR) and the data-receive register (DRR) are serviced before the next conversion. Alternately, autobuffering can be enabled when using the buffered serial port to execute conversions and read the data without μC intervention. Connect DV_{DD} to the TMS320C54_ supply voltage. The word length can be set to 8 bits with FO = 1 to implement the power-
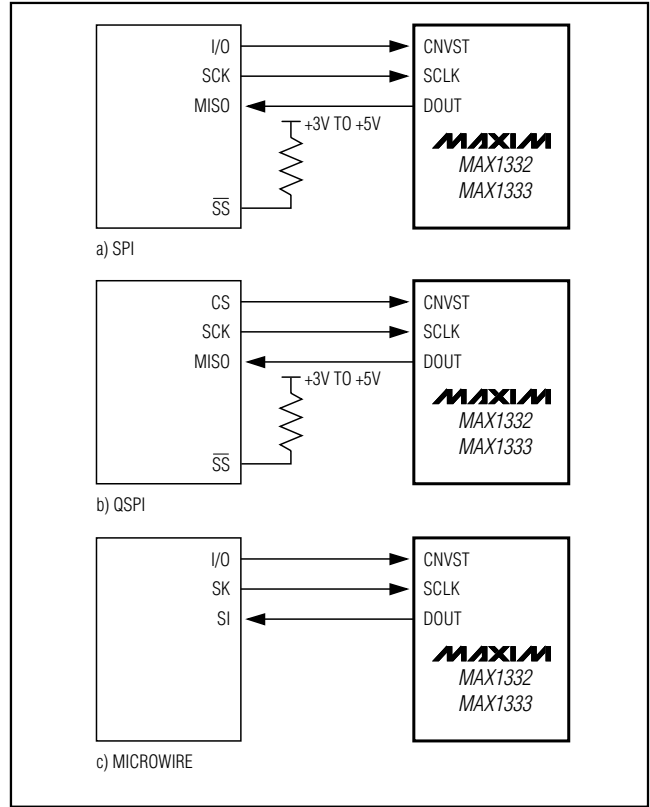

Figure 11. Common Serial-Interface Connections to the MAX1332/MAX1333

down modes. The CNVST pin must idle high to remain in either power-down state.

Another method of connecting the MAX1332/MAX1333 to the TMS320C54_ is to generate the clock signals external to either device. This connection is shown in Figure 16 where serial clock (CLOCK) drives the receive serial clock (CLKR) and SCLK, and the convert signal (CONVERT) drives the receive frame sync (FSR) and CNVST.

The serial port must be set up to accept an external receive clock and external receive frame sync. Write the serial port configuration (SPC) register as follows:

• TXM = 0, external frame sync

• MCM = 0, CLKX is taken from the CLKX pin

• FSM = 1, burst mode

• FO = 0, data transmitted/received as 16-bit words

This setup allows continuous conversion provided that the data-receive register (DRR) is serviced before the next conversion. Alternately, autobuffering can be
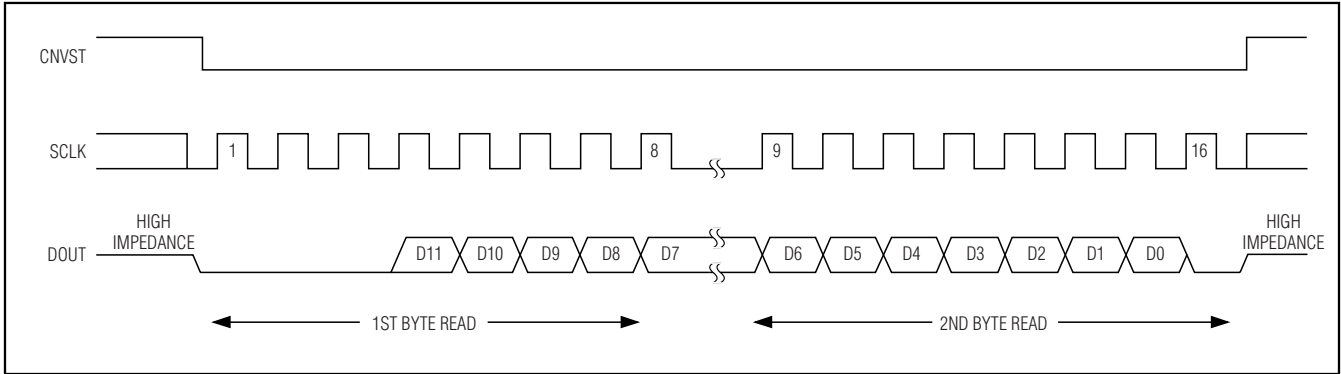
Figure 12. SPI/MICROWIRE Serial-Interface Timing—Single Conversion
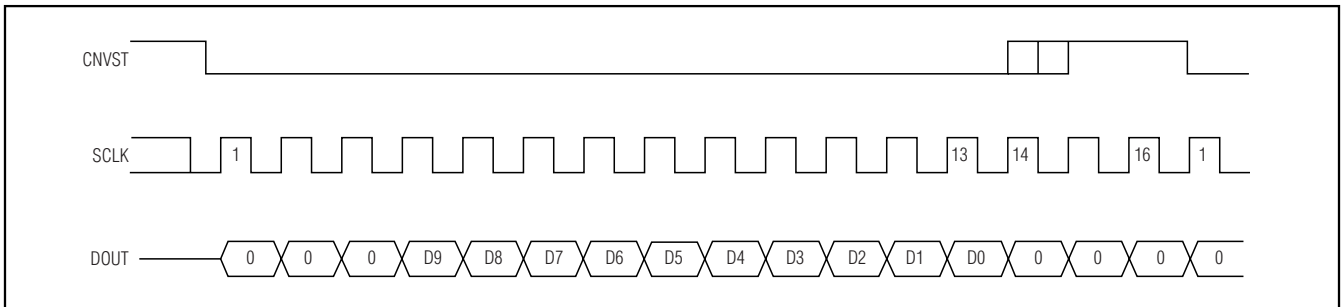

Figure 13. SPI/MICROWIRE Serial-Interface Timing—Continuous Conversion
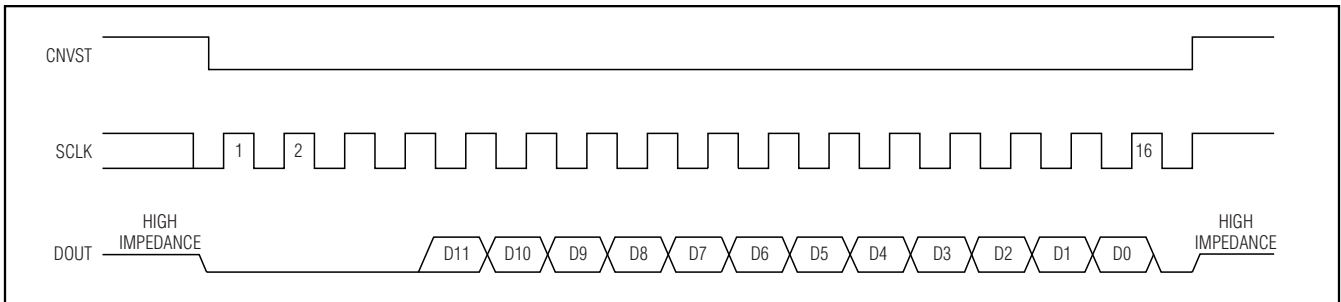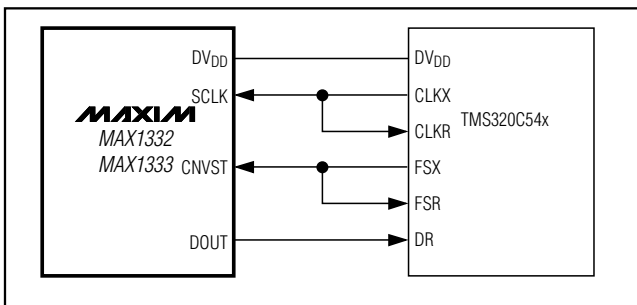

Figure 14. QSPI Serial-Interface Timing

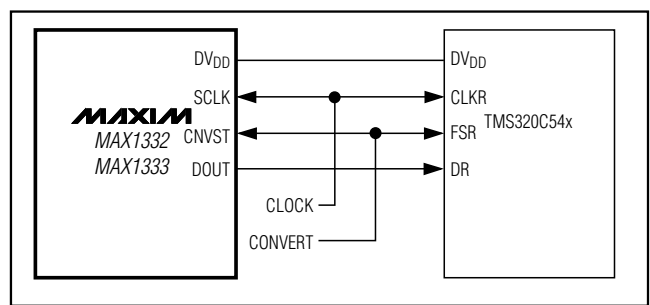

Figure 15. Interfacing to the TMS320C54_ Internal Clocks

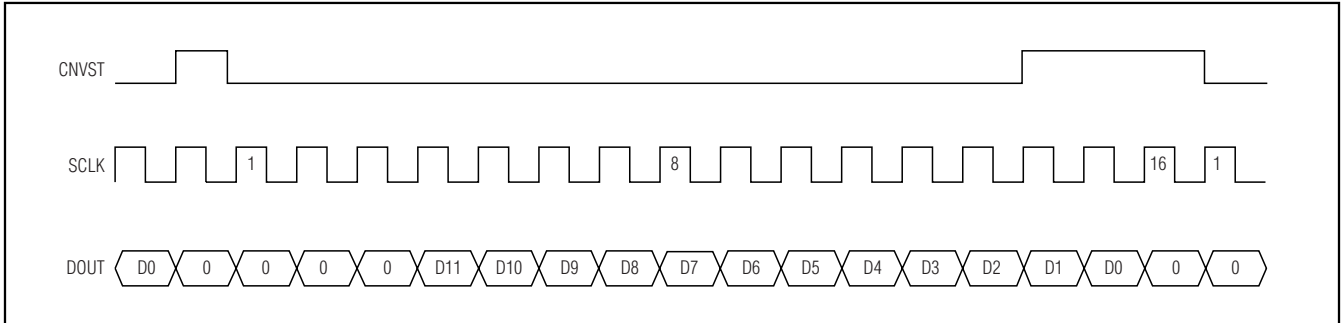Figure 16. Interfacing to the TMS320C54_ External Clocks

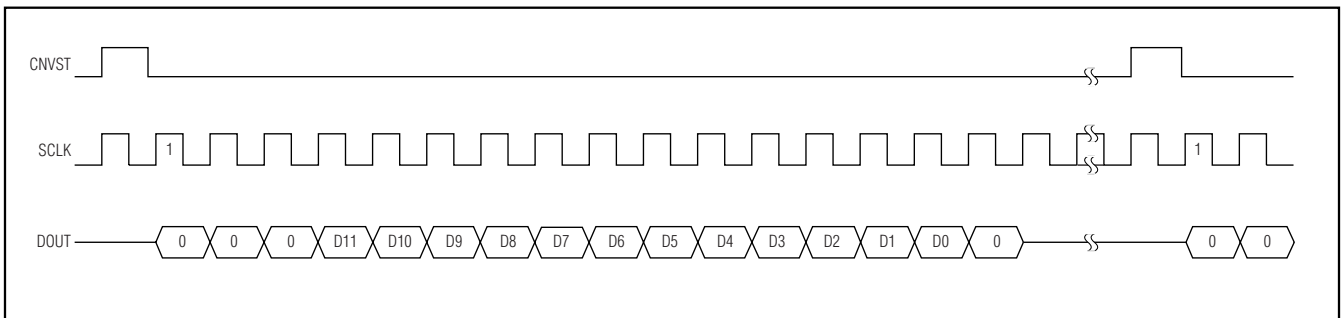*MAXIM*

Figure 17. DSP Interface—Continuous Conversion

Figure 18. DSP Interface—Single Conversion—Continuous/Burst Clock

enabled when using the buffered serial port to read the data without µC intervention. Connect DV_{DD} to the TMS320C54_ supply voltage.

The MAX1332/MAX1333 can also be connected to the TMS320C54_ by using the data transmit (DX) pin to drive CNVST and the transmit clock (CLKX) generated internally to drive SCLK. A pullup resistor is required on the CNVST signal to keep it high when DX goes high impedance and write (0001)h to the data transmit register (DXR) continuously for continuous conversions. The power-down modes can be entered by writing (00FF)h to the DXR (see Figures 17 and 18).

DSP Interface to the ADSP21_ _ _

The MAX1332/MAX1333 can be directly connected to the ADSP21_ _ _ family of DSPs from Analog Devices. Figure 19 shows the direct connection of the MAX1332/MAX1333 to the ADSP21_ _ _. There are two modes of operation that can be programmed to interface with the MAX1332/MAX1333. For continuous conversions, idle CNVST low and pulse it high for one clock cycle during the LSB of the previous transmitted word. Configure the ADSP21_ _ _ STCTL and SRCTL registers for early framing (LAFR = 0) and for an active-

high frame (LTFS = 0, LRFS = 0) signal. In this mode, the data-independent frame-sync bit (DITFS = 1) can be selected to eliminate the need for writing to the transmit data register more than once. For single conversions, idle CNVST high and pulse it low for the entire conversion. Configure the ADSP21_ _ _ STCTL and SRCTL registers for late framing (LAFR = 1) and for an active-low frame (LTFS = 1, LRFS = 1) signal. This is also the best way to enter the power-down modes by setting the word length to 8 bits (SLEN = 0111). Connect the DV_{DD} pin to the ADSP21_ _ _ supply voltage (see Figures 17 and 18).

Layout, Grounding, and Bypassing
For best performance, use PC boards. Wire-wrap boards must not be used. Board layout must ensure that digital and analog signal lines are separated from each other. Do not run analog and digital (especially clock) lines parallel to one another, or digital lines underneath the ADC package.

Figure 20 shows the recommended system ground connections. Establish an analog ground point at AGND and a digital ground point at DGND. Connect all other analog grounds to the analog ground point.

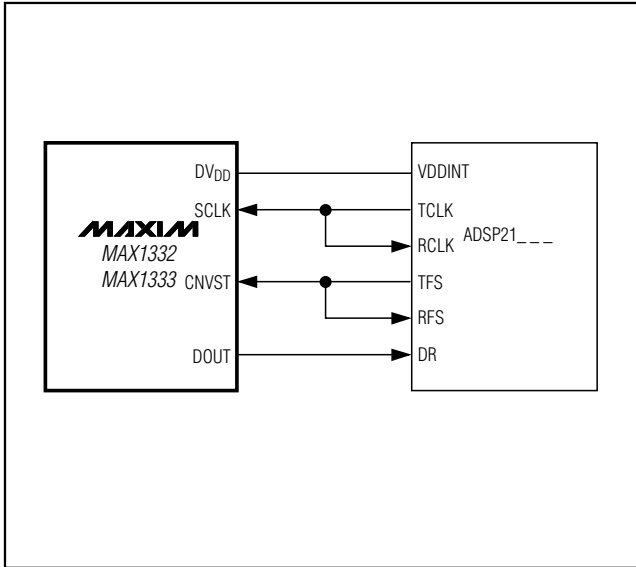# 3Msps/2Msps, 5V/3V, 2-Channel, True-Differential 12-Bit ADCs

Figure 19. Interfacing to the ADSP21_ _ _

Figure 20. Power-Supply Grounding Condition

Connect all digital grounds to the digital ground point. For lowest noise operation, make the power supply returns as low impedance and as short as possible. Connect the analog ground point to the digital ground point together at the IC.

High-frequency noise in the power supplies degrades the ADC's performance. Bypass AV_{DD} to AGND with 0.1µF and 1µF bypass capacitors. Likewise, bypass DV_{DD} to DGND with 0.1µF and 1µF bypass capacitors. Minimize capacitor lead lengths for best supply noise rejection. To reduce the effects of supply noise, a 10Ω resistor can be connected as a lowpass filter to attenuate supply noise (see Figure 20).

Exposed Paddle
The MAX1332/MAX1333 TQFN package has an exposed paddle on the bottom of the package, providing a very low thermal resistance path for heat removal from the IC, as well as a low-inductance path to ground. The pad is electrically connected to AGND on the MAX1332/MAX1333 and must be soldered to the circuit board analog ground plane for proper thermal and electrical performance. Refer to the Maxim Application Note HFAN-08.1: *Thermal Considerations for QFN and Other Exposed Pad Packages*, for additional information.

Definitions

Integral Nonlinearity (INL)
INL is the deviation of the values on an actual transfer function from a straight line. For the MAX1332/MAX1333, this straight line is between the end points of
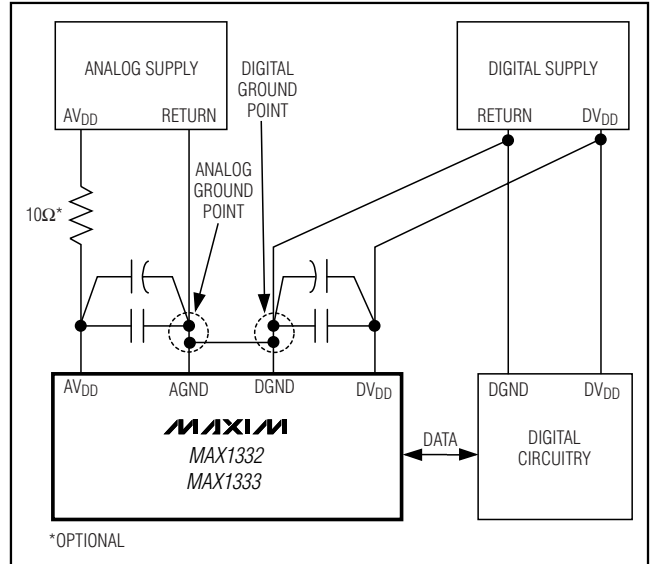
the transfer function once offset and gain errors have been nullified. INL deviations are measured at every step and the worst-case deviation is reported in the electrical characteristics table.

Differential Nonlinearity (DNL)
DNL is the difference between an actual step width and the ideal value of 1 LSB. A DNL error specification of less than 1 LSB guarantees no missing codes and a monotonic transfer function. For the MAX1332/MAX1333, DNL deviations are measured at every step and the worst-case deviation is reported in the electrical characteristics table.

Offset Error
Offset error is a figure of merit that indicates how well the actual transfer function matches the ideal transfer function at a single point. Typically, the point at which the offset error is specified is at or near the zero-scale of the transfer function or at or near the midscale of the transfer function.

For the MAX1332/MAX1333, operating with a unipolar transfer function, the ideal zero-scale digital output transition from 0x000 to 0x001 occurs at 0.5 LSB above AGND. Unipolar offset error is the amount of deviation between the measured zero-scale transition point and the ideal zero-scale transition point.

For the MAX1332/MAX1333, operating with a bipolar transfer function, the ideal midscale digital output transition from 0xFFF to 0x000 occurs at 0.5 LSB below AGND. Bipolar offset error is the amount of deviation
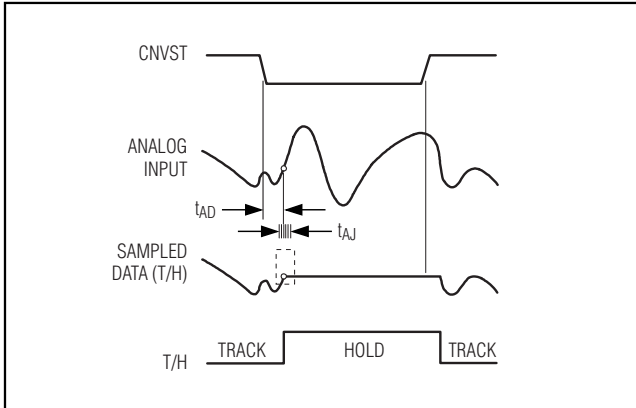
MAXIM

Figure 21. T/H Aperture Timing

between the measured midscale transition point and the ideal midscale transition point.

Gain Error

Gain error is a figure of merit that indicates how well the slope of the actual transfer function matches the slope of the ideal transfer function. For the MAX1332/MAX1333, the gain error is the difference of the measured full-scale and zero-scale transition points minus the difference of the ideal full-scale and zero-scale transition points.

For the unipolar input, the full-scale transition point is from 0xFFE to 0xFFF and the zero-scale transition point if from 0x000 to 0x001.

For the bipolar input, the full-scale transition point is from 0x7FE to 0x7FF and the zero-scale transition point is from 0x800 to 0x801.

Aperture Jitter

Aperture jitter (t_{AJ}) is the sample-to-sample variation in the aperture delay.

Aperture Delay

Aperture delay (t_{AD}) is the time defined between the falling edge of the CNVST and the instant when an actual sample is taken (Figure 21).

Signal-to-Noise Ratio (SNR)

SNR is a dynamic figure of merit that indicates the converter's noise performance.

For a waveform perfectly reconstructed from digital samples, the theoretical maximum SNR is the ratio of the full-scale analog input (RMS value) to the RMS quantization error (residual error). The ideal, theoretical minimum analog-to-digital noise is caused by quantiza-

tion error only and results directly from the ADC's resolution (N bits):

$$SNR_{dB[max]} = 6.02_{dB} \times N + 1.76_{dB}$$

In reality, there are other noise sources such as thermal noise, reference noise, and clock jitter that also degrade SNR.

For the MAX1332/MAX1333, SNR is computed by taking the ratio of the RMS signal to the RMS noise. RMS noise includes all spectral components to the Nyquist frequency excluding the fundamental, the first five harmonics, and the DC offset.

Signal-to-Noise Plus Distortion (SINAD)

SINAD is a dynamic figure of merit that indicates the converter's noise and distortion performance.

SINAD is computed by taking the ratio of the RMS signal to the RMS noise plus distortion. RMS noise plus distortion includes all spectral components to the Nyquist frequency excluding the fundamental and the DC offset:

$$SINAD(dB) = 20 \times \log \left[\frac{SIGNAL_{RMS}}{(NOISE + DISTORTION)_{RMS}} \right]$$

Effective Number of Bits (ENOB)

ENOB specifies the global accuracy of an ADC at a specific input frequency and sampling rate. An ideal ADC's error consists of quantization noise only. ENOB for a full-scale sinusoidal input waveform is computed from:

$$ENOB = \frac{SINAD - 1.76}{6.02}$$

Total Harmonic Distortion (THD)

THD is a dynamic figure of merit that indicates how much harmonic distortion the converter adds to the signal.

THD is the ratio of the RMS sum of the first five harmonics of the fundamental signal to the fundamental itself. This is expressed as:

$$THD = 20 \times \log \left(\frac{\sqrt{V2^2 + V3^2 + V4^2 + V5^2 + V6^2}}{V1} \right)$$

where V_1 is the fundamental amplitude, and V_2 through V_6 are the amplitudes of the 2nd- through 6th-order harmonics.

3Msps/2Msps, 5V/3V, 2-Channel, True-Differential 12-Bit ADCs

Spurious-Free Dynamic Range (SFDR)

SFDR is a dynamic figure of merit that indicates the lowest usable input signal amplitude. SFDR is the ratio of the RMS amplitude of the fundamental (maximum signal component) to the RMS value of the next-largest spurious component, excluding DC offset. SFDR is specified in decibels relative to the carrier (dBc).

Intermodulation Distortion (IMD)

IMD is the total power of the IM2 to IM5 intermodulation products to the Nyquist frequency relative to the total input power of the two input tones f_{IN1} and f_{IN2}. The individual input tone levels are at -7dBFS. The intermodulation products are as follows:

- 2nd-order intermodulation products (IM2): f_{IN1} + f_{IN2}, f_{IN2} - f_{IN1}

- 3rd-order intermodulation products (IM3): $2f_{IN1}$ - f_{IN2}, $2f_{IN2}$ - f_{IN1}, $2f_{IN1}$ + f_{IN2}, $2f_{IN2}$ + f_{IN1}

- 4th-order intermodulation products (IM4): $3f_{IN1}$ - f_{IN2}, $3f_{IN2}$ - f_{IN1}, $3f_{IN1}$ + f_{IN2}, $3f_{IN2}$ + f_{IN1}

- 5th-order intermodulation products (IM5): $3f_{IN1}$ - $2f_{IN2}$, $3f_{IN2}$ - $2f_{IN1}$, $3f_{IN1}$ + $2f_{IN2}$, $3f_{IN2}$ + $2f_{IN1}$

Channel-to-Channel Isolation

Channel-to-channel isolation is a figure of merit that indicates how well each analog input is isolated from the others. The channel-to-channel isolation for the MAX1332/MAX1333 is measured by applying a low-frequency 500kHz -0.5dBFS sine wave to the on channel while a high-frequency 900kHz -0.5dBFS sine wave is applied to the off channel. An FFT is taken for the on channel. From the FFT data, channel-to-channel crosstalk is expressed in dB as the power ratio of the 500kHz low-frequency signal applied to the on channel and the 900kHz high-frequency crosstalk signal from the off channel.

Full-Power Bandwidth

A large -0.5dB FS analog input signal is applied to an ADC, and the input frequency is swept up to the point where the amplitude of the digitized conversion result has decreased by -3dB. This point is defined as full-power input bandwidth frequency.

Full-Linear Bandwidth

Full-linear bandwidth is the frequency at which the signal-to-noise plus distortion (SINAD) is equal to 68dB. The amplitude of the analog input signal is -0.5dBFS.

Small-Signal Bandwidth

A small -20dBFS analog input signal is applied to an ADC in such a way that the signal's slew rate does not limit the ADC's performance. The input frequency is

then swept up to the point where the amplitude of the digitized conversion result has decreased by -3dB.

Power-Supply Rejection (PSR)

PSR is defined as the shift in offset error when the analog power supply is moved from 2.7V to 3.6V.

Pin Configuration
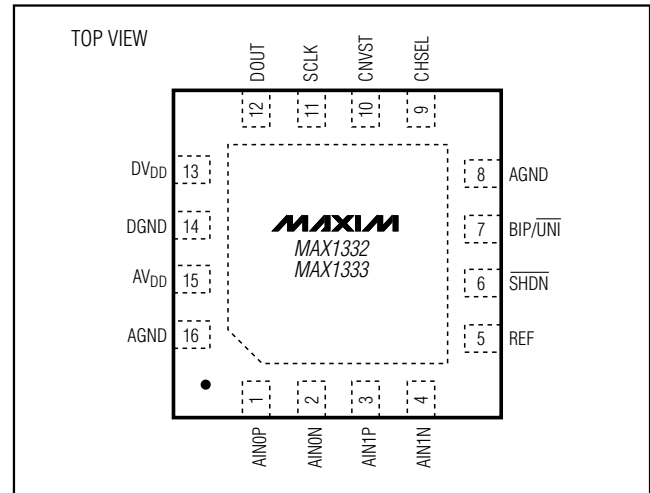
Selector Guide

PART	AV$_{DD}$ (V)	MAX SAMPLING RATE (Msps)
MAX1332ETE	+5	3
MAX1333ETE	+3	2

Chip Information

PROCESS: BiCMOS

MAXIM

MAX1332/MAX1333

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

12x16L QFN THIN.EPS

INDEX AREA (D/2 X E/2)

TOP VIEW

BOTTOM VIEW

PIN #1 ID

DETAIL A

SIDE VIEW

SEATING PLANE

(R IS OPTIONAL)

EVEN TERMINAL   ODD TERMINAL

TERMINAL TIP

DETAIL A

DALLAS SEMICONDUCTOR /Μ/ΑΧΙΜ/

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE 12, 16L, THIN QFN, 3x3x0.8mm

APPROVAL | DOCUMENT CONTROL NO. 21-0136 | REV. E | 1/2
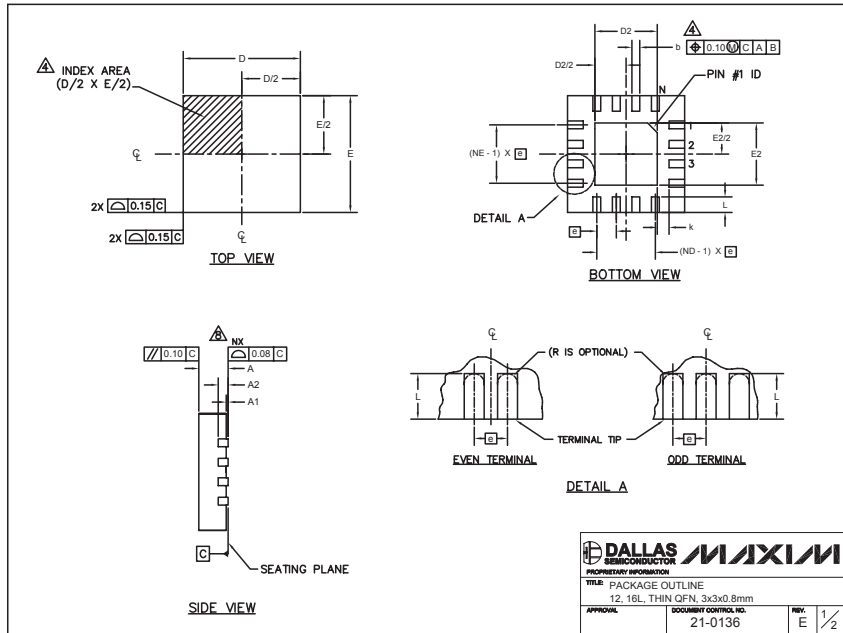
PKG	12L 3x3			16L 3x3		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80
b	0.20	0.25	0.30	0.20	0.25	0.30
D	2.90	3.00	3.10	2.90	3.00	3.10
E	2.90	3.00	3.10	2.90	3.00	3.10
e	0.50 BSC.			0.50 BSC.		
L	0.45	0.55	0.65	0.30	0.40	0.50
N	12			16		
ND	3			4		
NE	3			4		
A1	0	0.02	0.05	0	0.02	0.05
A2	0.20 REF			0.20 REF		
k	0.25	-	-	0.25	-	-

	EXPOSED PAD VARIATIONS							
PKG. CODES	D2			E2			PIN ID	JEDEC	DOWN BONDS ALLOWED
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.			
T1233-1	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1	NO
T1233-3	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1	YES
T1633-1	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2	NO
T1633-2	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2	YES
T1633F-3	0.65	0.80	0.95	0.65	0.80	0.95	0.225 x 45°		N/A
T1633-4	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2	NO

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.20 mm AND 0.25 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220 REVISION C.

DALLAS SEMICONDUCTOR /Μ/ΑΧΙΜ/

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE 12, 16L, THIN QFN, 3x3x0.8mm

APPROVAL | DOCUMENT CONTROL NO. 21-0136 | REV. E | 2/2