Sound Processors for Home Theater System

7.1ch Sound Processor

BD3452KS

No.10081EAT01

●Description

BD3452KS is a sound processor where the functions including Input Selector, 8ch Volume and Gain Amp required for applications such as AV receivers, home theater systems and mini-component systems are integrated into a single chip. Adopting the BiCMOS process achieves low distortion, low noise and a wide dynamic range.

●Features

1) Dynamic range: 132dB (VOL=MUTE, IHF-A)
2) Independent 8 channels for Master Volume (0 to -99 dB, MUTE 1dB/Step)
3) Supporting 2nd room entertainment
4) Low current consumption design achieved by adopting the BiCMOS process
5) Built-in Output Gain Amp useful for adjusting output signal voltages (0 to 15dB, 1dB/Step)
6) BD3841FS (9-input selector), BD3843FS (6-input selector) and BUS are common to be controlled simultaneously.
7) Built-in 2ch output port
8) 2-wire serial control (For both 3.3V and 5V)

●Applications

AV receivers, home theater systems and mini-component systems

●Absolute maximum ratings (Ta=25℃)

Parameter	Symbol	Ratings	Unit
Power Supply Voltage	VCC	7.5 *1	V
	VEE	-7.5	
Input Signal Voltage	VIN	VCC+0.3 to VEE-0.3	V
Power Dissipation	Pd	1300 *2	mW
Operating Temperature Range	Topr	-20 to +75	℃
Storage Temperature Range	Tastg	-55 to +125	℃

*1 Even in the specified range of Power Supply Voltage, applying voltage only to the VCC side may cause an excessive current to give a permanent damage to the IC.
When starting up power supplies, VEE and VCC should be powered on simultaneously or VEE first; then followed by VCC.

*2 Over Ta=25℃, reduce at the rate of 13mW/℃. When installed on the standard board (size: 70×70×1.6mm).

●Operating conditions

It must function normally at Ta=25℃.

Parameter	Symbol	Ratings			Unit
		Min.	Typ.	Max.	
Operating Supply Voltage	VCC	6.5	7	7.3	V
	VEE	-7.3	-7	-6.5	

●**Electrical characteristics**

Ta=25℃, VCC=7V, VEE=-7V, f=1kHz, Vin=1Vrms, RL=10kΩ, Rg=600Ω, Input Gain=0dB,
Master volume=0dB, Output gain=0dB, unless otherwise noted.

	Parameter		Symbol	Limits			Unit	Conditions
				Min.	Typ.	Max.		
Total Output	Circuit Current	VCC	IQ	-	20	40	mA	No signal
		VEE		-40	-20	-		
	Output Voltage Gain		Gv	-2	0	2	dB	Measure : Pin87,88
	Total Harmonic Distortion Ratio		THD	-	0.0006	0.03	%	Measure : Pin87,88 BW=400 to 30kHz
	Maximum Output Voltage		Vomax	3.6	4.2	-	Vrms	Measure : Pin87,88 THD=1%
	Output Noise Voltage		Vno	-	1.4	12	μVrms	Measure : Pin87,88, Rg=0Ω, BW=IHF-A
	Residual Noise Voltage		Vnor	-	1	8	μVrms	Measure : Pin87,88, Rg=0Ω, BW=IHF-A, Volume=MUTE
	Cross-talk between Channels		CTC	-	-95	-80	dB	Measure : Pin88(OUTFL),87 (OUTFR) Rg=0Ω, BW=IHF-A Reference : Pin87(OUTFR), 88(OUTFL)=1Vrms
	Cross-talk between Selectors		CTS	-	-95	-80	dB	Measure : Pin87,88 Rg=0Ω, BW=IHF-A
	Input Impedance		Rin	32	47	62	kΩ	
Volume Output	V Output Voltage Gain		GVV	-2	0	2	dB	Measure : Pin 81,82,83,84,85,86,87,88
	V Total Harmonic Distortion Ratio		THDV	-	0.0006	0.03	%	Measure : Pin 81,82,83,84,85,86,87,88 BW=400 to 30kHz
	V Residual Noise Voltage		VnorV	-	1	8	μVrms	Measure : Pin 81,82,83,84,85,86,87,88 BW=IHF-A, Rg=0Ω,Volume=MUTE
	Volume Setting Error		VOLE1	-0.5	0	0.5	dB	Measure : Pin 81,82,83,84,85,86,87,88 Volume=0dB, Vin=3Vrms
	Maximum Attenuation		VOLmin	-	-115	-105	dB	Measure : Pin 81,82,83,84,85,86,87,88 Vin=3Vrms, BW=IHF-A
Input Gain	Input Gain Control Range		GIG	10	12	14	dB	Measure : Pin 81,82,83,84,85,86,87,88 Input Gain=12dB, Vin=0.3Vrms
Output Gain	Output Gain Control Range		GOG	13	15	17	dB	Measure : Pin 81,82,83,84,85,86,87,88 Output Gain=15dB, Vin=0.3Vrms
	Output Gain Setting Error		GOE	-0.5	0	0.5	dB	Measure : Pin 81,82,83,84,85,86,87,88 Output Gain=0dB, Vin=0.3Vrms
REC Out	R Output Impedance		RoutR	-	20	100	Ω	Measure : Pin 44,45,46,47
	R Voltage Gain		GVR	-2	0	2	dB	Measure : Pin 44,45,46,47 (*)RL=10kΩ
	R Total Harmonic Distortion Ratio		THDR	-	0.005	0.09	%	Measure : Pin 44,45,46,47 BW=400 to 30kHz, (*)RL=10kΩ
Port	Port H Output		PH	4.0	4.9	5.4	V	Measure : Pin 62,63 RL=10kΩ
	Port Output Current		PI	-	-	1.0	mA	Measure : Pin 62,63

(*) If two RECOUTs are ON, total load resistances of these two (RL) should be 10 kΩ.

* This product is not of "anti radiation design".

●Timing chart

1) Signal Timing Conditions

・Data is read on the rising edge of the clock.
・Latch is read on the falling edge of the clock.
・Latch signal must terminate with the LOW state.

*To avoid malfunctions, clock and data signals must terminate with the LOW state.

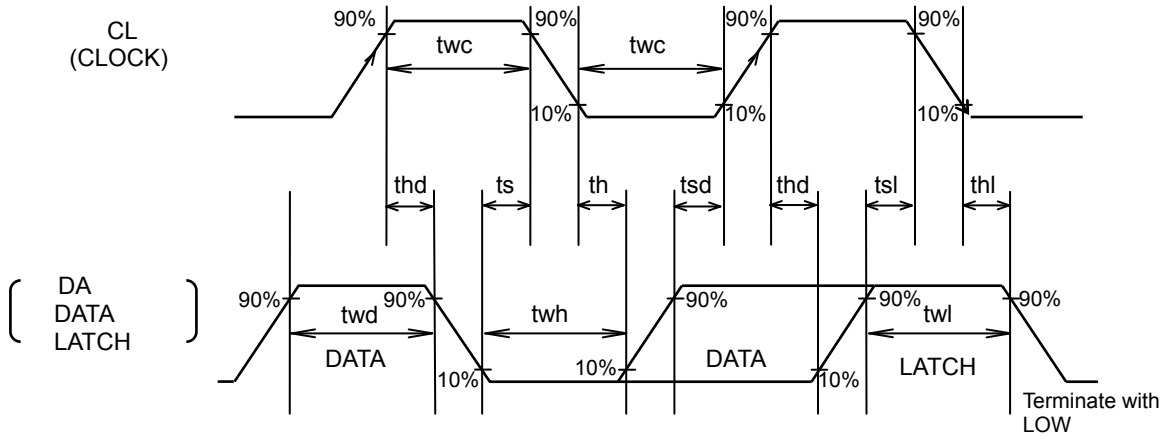


Fig.1

Parameter	Symbol	Limits			Unit
		Min.	Typ.	Max.	
Minimum Clock Width	twc	1.0	-	-	μs
Minimum Data Width	twd	1.0	-	-	μs
Minimum Latch Width	twl	1.0	-	-	μs
LOW Hold Width	twh	1.0	-	-	μs
Data Set-up Time (DATA→CLK)	tsd	0.5	-	-	μs
Data Hold Time (CLK→DATA)	thd	0.5	-	-	μs
Latch Set-up Time (CLK→LATCH)	tsl	0.5	-	-	μs
Latch Hold Time (DATA→LATCH)	thl	0.5	-	-	μs
Latch Low Set-up Time	ts	0.5	-	-	μs
Latch Low Hold Time	th	0.5	-	-	μs

2) Voltage Conditions for Control Signals

Parameter	Limits			Unit	Conditions
	Min.	Typ.	Max.		
“H” Input Voltage	2.2	—	5.5	V	Vcc = 6.5～7.3V VEE=-6.5～-7.3V
“L” Input Voltage	0	—	1.0	V	

3) Basic Configuration of Control Data Formats

← Input direction

	MSB																LSB
Data	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	Data														Select Address		

・Control Data Formats

← Input direction

															Select Address		
Data (1)	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	Input selector 1				Input selector 2				Input ATT		Input gain		*	*	0	0	0
Data (2)	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	FLR Input Selector			SBLR Input Selector			Multi Input Selector		REC A	REC B	Port A	Port B	*	0	0	0	1
Data (3)	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	Output gain 7ch				Output gain SWch				*	*	*	*	*	1	0	0	1
Data (4)	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	Master volume FLch								Master volume FRch						0	1	0
Data (5)	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	Master volume Cch								Master volume SWch						0	1	1
Data (6)	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	Master volume SLch								Master volume SRch						1	1	0
Data (7)	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	Master volume SBLch								Master volume SBRch						1	1	1

By changing the setting of Select Address, seven different control formats are selectable.
For Select Address, the values except those shown above must not be specified.
Each time of power-on, all of the address data must be initialized.
* indicates 0 or 1.

(Example)

← Input direction

MSB LSB	MSB LSB	MSB LSB	MSB LSB	MSB LSB	MSB LSB	MSB LSB
Data(1) L	Data(2) L	Data(3) L	Data(4) L	Data(5) L	Data(6) L	Data(7) L

"L" means latch.

After power-on, for the second and subsequent times, only the desired data can be selected for setting.

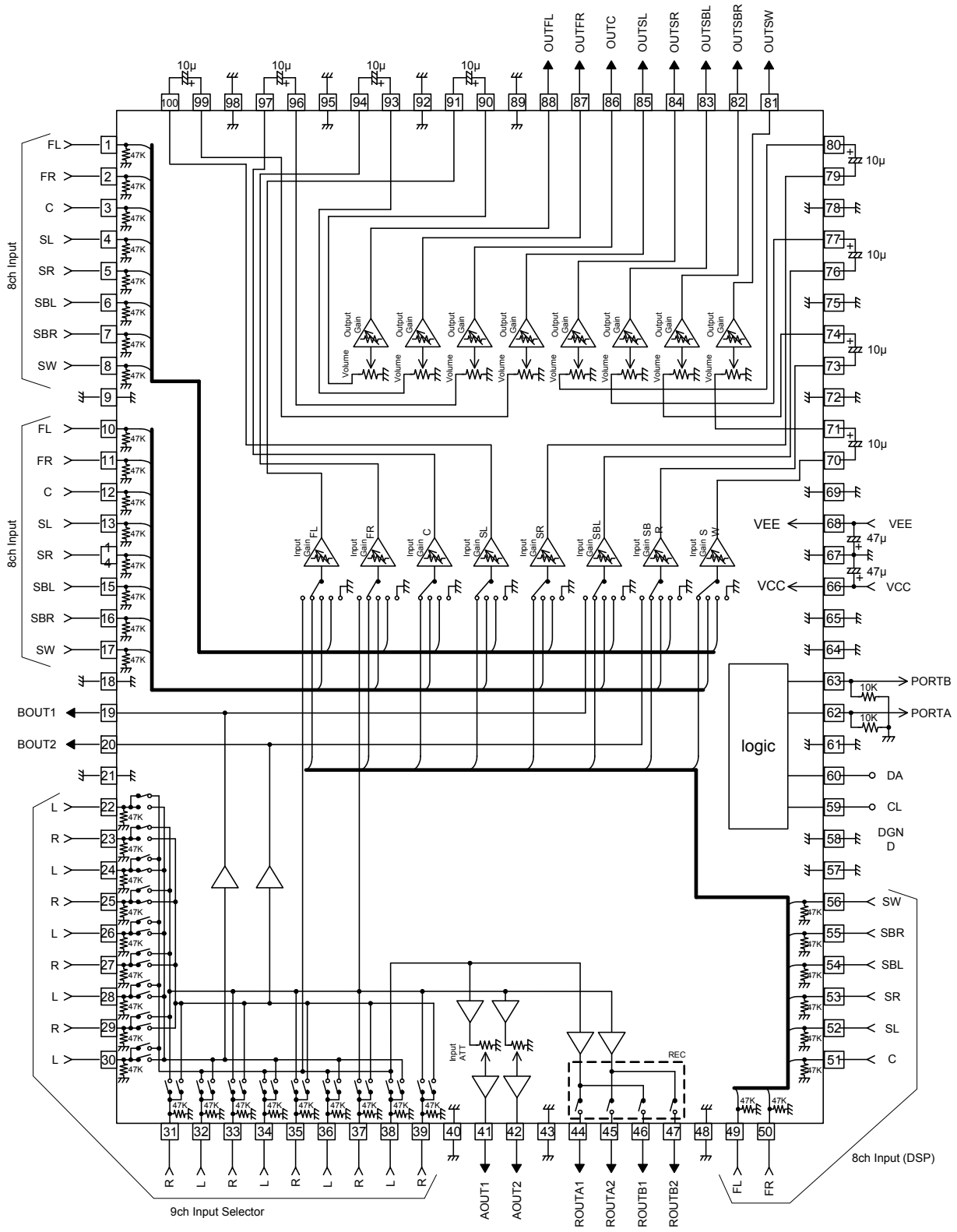
(Example) When changing Output Gain SWch,Input direction

← MSB LSB

Data(3)	L

"L" means latch.

●Application circuit



UNIT
RESISTOR : Ω
CAPACITOR : F

Fig.2

●Reference data

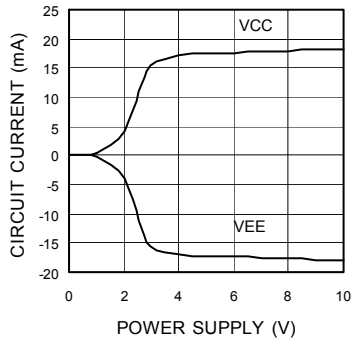


Fig.3 Circuit Current - Power Supply

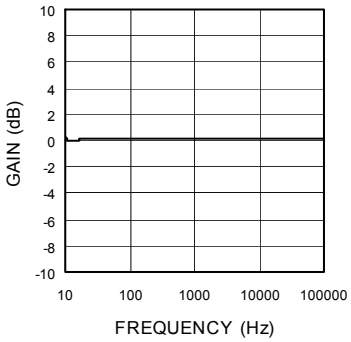


Fig.4 Voltage Gain - Frequency

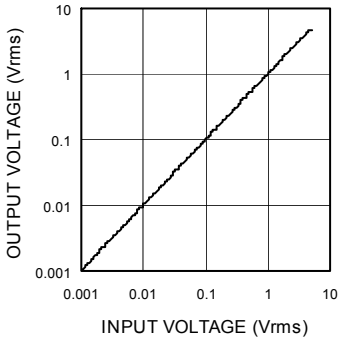


Fig.5 Output Voltage - Input Voltage

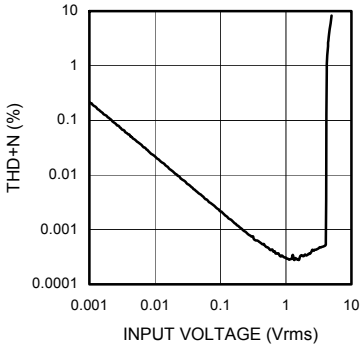


Fig.6 THD+N - Input Voltage

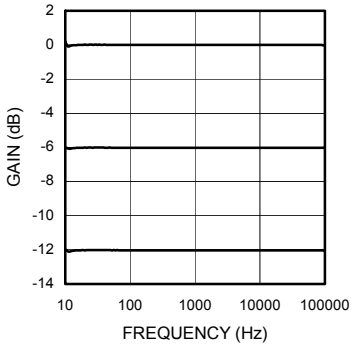


Fig.7 Input Attenuation - Frequency

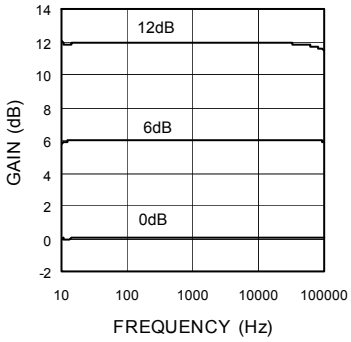


Fig.8 Input Gain - Frequency

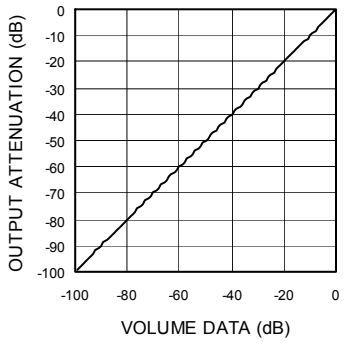


Fig.9 Volume Attenuation - Volume Settin

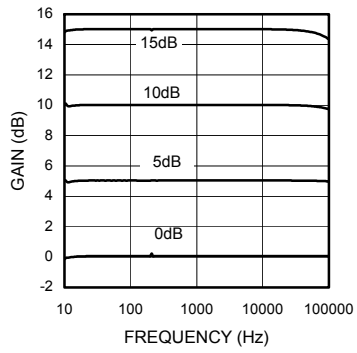


Fig.10 Output Gain - Frequency

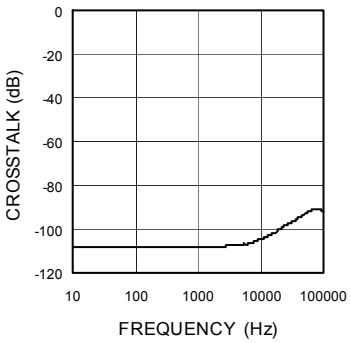


Fig.11 Cross-talk between Channels - Frequency

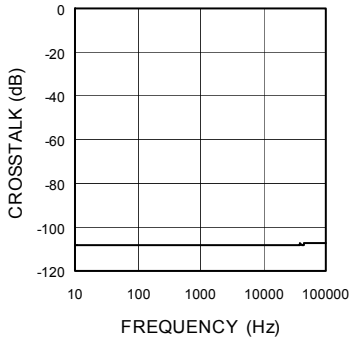


Fig.12 Cross-talk between Selectors - Frequency

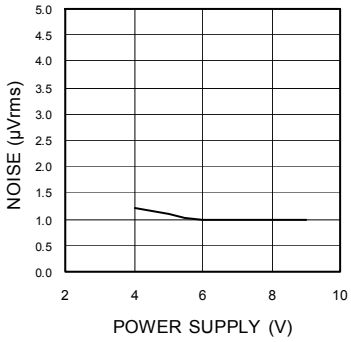


Fig.13 Output Noise Voltage - Power Supply Voltage

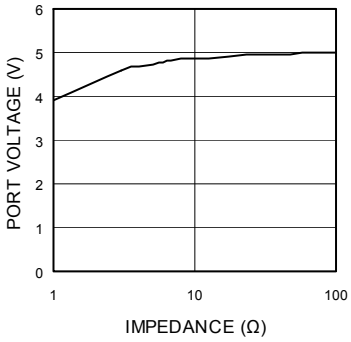


Fig.14 Port H Voltage – Load Resistance

●Notes for use

(1) Numbers and data in entries are representative design values and are not guaranteed values of the items.

(2) Although we are confident in recommending the sample application circuits, carefully check their characteristics further when using them. When modifying externally attached component constants before use, determine them so that they have sufficient margins by taking into account variations in externally attached components and the Rohm LSI, not only for static characteristics but also including transient characteristics.

(3) Absolute maximum ratings
If applied voltage, operating temperature range, or other absolute maximum ratings are exceeded, the LSI may be damaged. Do not apply voltages or temperatures that exceed the absolute maximum ratings. If you think of a case in which absolute maximum ratings are exceeded, enforce fuses or other physical safety measures and investigate how not to apply the conditions under which absolute maximum ratings are exceeded to the LSI.

(4) VEE potential
Make the VEE pin voltage such that it is the lowest voltage even when operating below it. Actually confirm that the voltage of each pin does not become a lower voltage than the VEE pin, including transient phenomena.

(5) Thermal design
Perform thermal design in which there are adequate margins by taking into account the allowable power dissipation in actual states of use.

(6) Shorts between pins and misinstallation
When mounting the LSI on a board, pay adequate attention to orientation and placement discrepancies of the LSI. If it is misinstalled and the power is turned on, the LSI may be damaged. It also may be damaged if it is shorted by a foreign substance coming between pins of the LSI or between a pin and a power supply or a pin and a GND.

(7) Operation in strong magnetic fields
Adequately evaluate use in a strong magnetic field, since there is a possibility of malfunction.

(8) About Operating Voltage Range and Operating Temperature Range
The circuit functional operations are guaranteed within the Operating Voltage Range and Operating Temperature Range. The standard values of electrical characteristics, however, are guaranteed under the specific conditions. Accordingly, careful consideration of the IC characteristic variations is required to design a set of circuit.

(9) About power ON/OFF
(a) At power ON/OFF, a shock sound will be generated and, therefore, use MUTE on the set.
(b) When turning on power supplies, VEE and VCC should be powered on simultaneously or VEE first;
then followed by VCC. If the VCC side is started up first, an excessive current may pass VCC through VEE.

(10) About serial control
For the CL and DA terminals, the patterned and other wirings should be routed not to cause interference with the analog-signal-related lines.

(11) About function switching
When switching Input Selector or Input Gain, use MUTE on Master Volume.

●**Thermal derating characteristic**

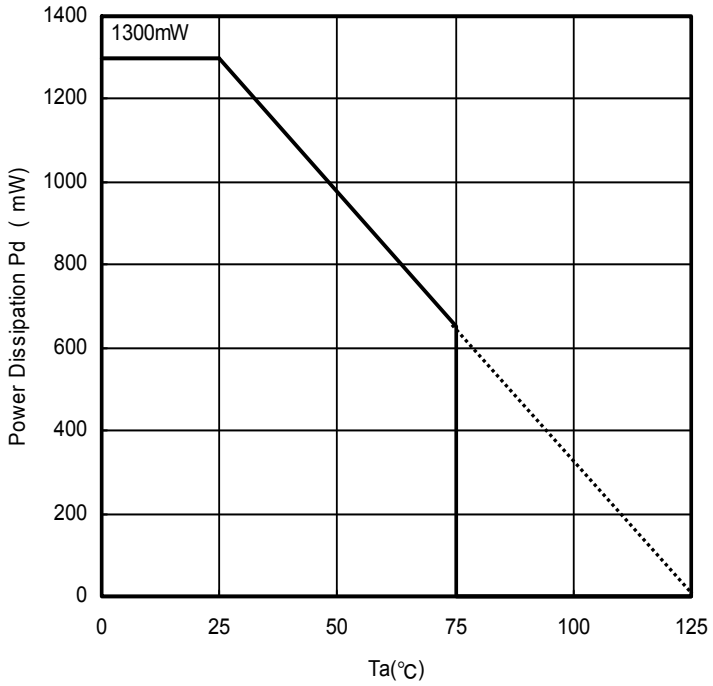


Fig.15

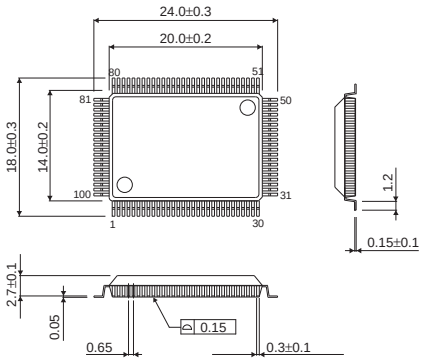
BD3452KS
ROHM standard board packaging time value
Board size: 70 x 70 x 1.6mm Raw material : FR4 glass epoxy board (copper area 3% or below)

●**Ordering part number**

B	D	3	4	5	2	K	S	-		

Part No. Part No. Package KS: SQFP100 Packaging and forming specification None :Tray

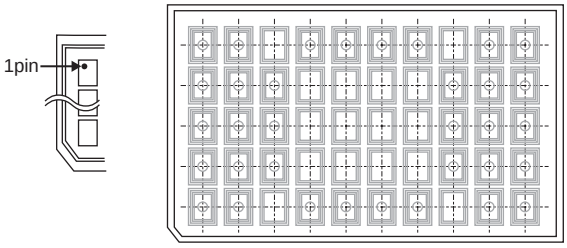
SQFP100



(Unit : mm)

<Tape and Reel information>

Container	Tray (with dry pack)
Quantity	500pcs
Direction of feed	Direction of product is fixed in a tray



∗Order quantity needs to be multiple of the minimum quantity.

Notes

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