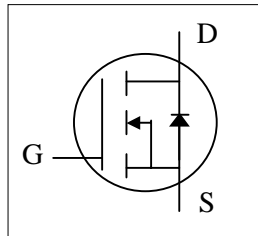




- ▼ Low Gate Charge
- ▼ Single Drive Requirement
- ▼ Fast Switching Performance

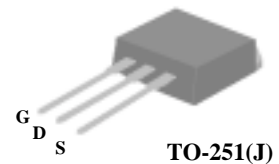
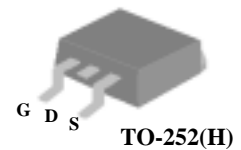


$BV_{DSS}$	80V
$R_{DS(ON)}$	45mΩ
$I_D$	21.3A

### Description

The Advanced Power MOSFETs from APEC provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-252 package is universally preferred for all commercial-industrial surface mount applications and suited for low voltage applications such as DC/DC converters. The through-hole version (AP9980J) are available for low-profile applications.



### Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	80	V
$V_{GS}$	Gate-Source Voltage	±25	V
$I_D @ T_C=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	21.3	A
$I_D @ T_C=100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	13.4	A
$I_{DM}$	Pulsed Drain Current <sup>1</sup>	80	A
$P_D @ T_C=25^\circ C$	Total Power Dissipation	41.7	W
	Linear Derating Factor	0.33	W/°C
$T_{STG}$	Storage Temperature Range	-55 to 150	°C
$T_J$	Operating Junction Temperature Range	-55 to 150	°C

### Thermal Data

Symbol	Parameter	Value	Units
Rthj-c	Thermal Resistance Junction-case	Max. 3.0	°C/W
Rthj-a	Thermal Resistance Junction-ambient	Max. 110	°C/W



# AP9980H/J

## Electrical Characteristics @T<sub>j</sub>=25°C (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250uA	80	-	-	V
ΔBV <sub>DSS</sub> /ΔT <sub>j</sub>	Breakdown Voltage Temperature Coefficient	Reference to 25°C, I <sub>D</sub> =1mA	-	0.07	-	V/°C
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =10V, I <sub>D</sub> =12A	-	-	45	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =8A	-	-	55	mΩ
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250uA	1	-	3	V
g <sub>fs</sub>	Forward Transconductance	V <sub>DS</sub> =10V, I <sub>D</sub> =12A	-	20	-	S
I <sub>DSS</sub>	Drain-Source Leakage Current (T <sub>j</sub> =25°C)	V <sub>DS</sub> =80V, V <sub>GS</sub> =0V	-	-	10	uA
	Drain-Source Leakage Current (T <sub>j</sub> =150°C)	V <sub>DS</sub> =64V, V <sub>GS</sub> =0V	-	-	100	uA
I <sub>GSS</sub>	Gate-Source Leakage	V <sub>GS</sub> =±25V	-	-	±100	nA
Q <sub>g</sub>	Total Gate Charge <sup>2</sup>	I <sub>D</sub> =12A	-	18	30	nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>DS</sub> =64V	-	5	-	nC
Q <sub>gd</sub>	Gate-Drain ("Miller") Charge	V <sub>GS</sub> =4.5V	-	11	-	nC
t <sub>d(on)</sub>	Turn-on Delay Time <sup>2</sup>	V <sub>DS</sub> =40V	-	11	-	ns
t <sub>r</sub>	Rise Time	I <sub>D</sub> =12A	-	20	-	ns
t <sub>d(off)</sub>	Turn-off Delay Time	R <sub>G</sub> =3.3Ω, V <sub>GS</sub> =10V	-	29	-	ns
t <sub>f</sub>	Fall Time	R <sub>D</sub> =3.3Ω	-	30	-	ns
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V	-	1810	2900	pF
C <sub>oss</sub>	Output Capacitance	V <sub>DS</sub> =25V	-	135	-	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	f=1.0MHz	-	96	-	pF
R <sub>g</sub>	Gate Resistance	f=1.0MHz	-	1.6	-	Ω

## Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V <sub>SD</sub>	Forward On Voltage <sup>2</sup>	I <sub>S</sub> =20A, V <sub>GS</sub> =0V	-	-	1.2	V
t <sub>rr</sub>	Reverse Recovery Time <sup>2</sup>	I <sub>S</sub> =12A, V <sub>GS</sub> =0V,	-	57	-	ns
Q <sub>rr</sub>	Reverse Recovery Charge	dI/dt=100A/μs	-	140	-	nC

### Notes:

1. Pulse width limited by safe operating area.
2. Pulse width ≤300us, duty cycle ≤2%.

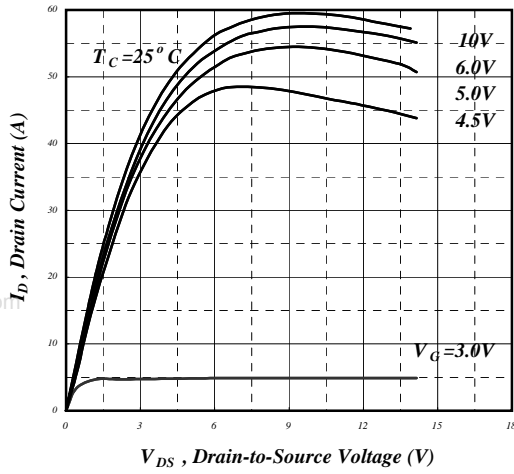


Fig 1. Typical Output Characteristics

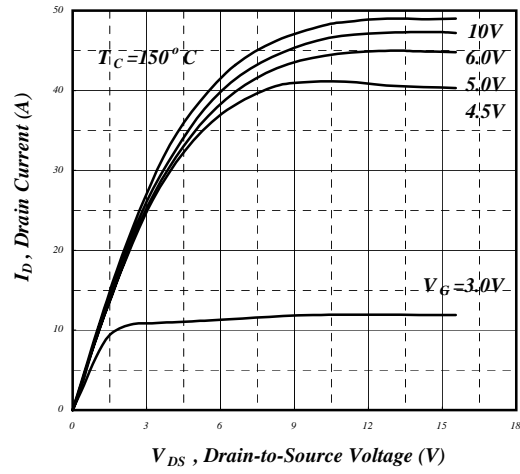


Fig 2. Typical Output Characteristics

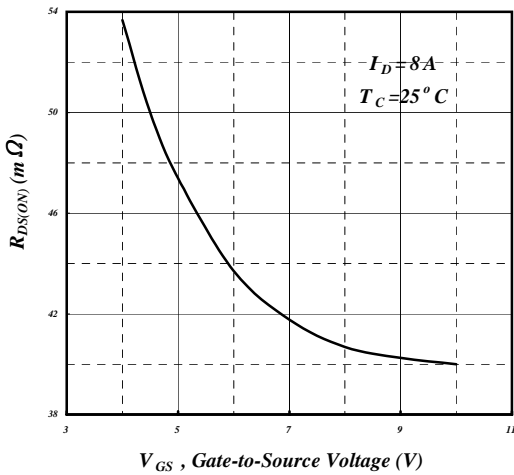


Fig 3. On-Resistance v.s. Gate Voltage

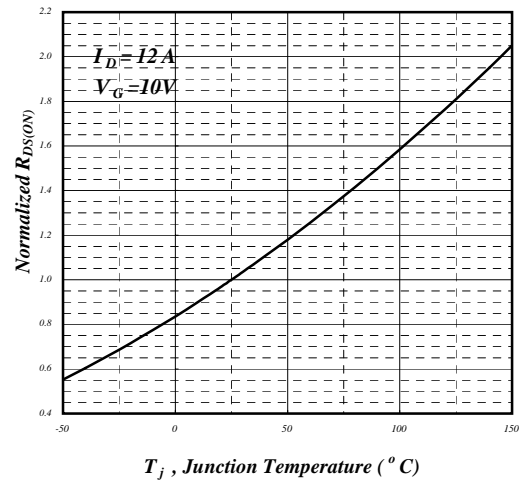


Fig 4. Normalized On-Resistance v.s. Junction Temperature

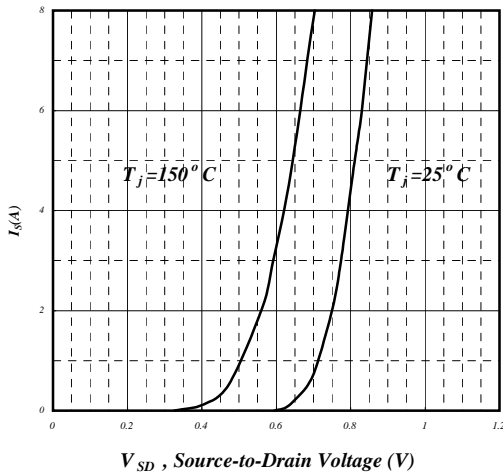


Fig 5. Forward Characteristic of Reverse Diode

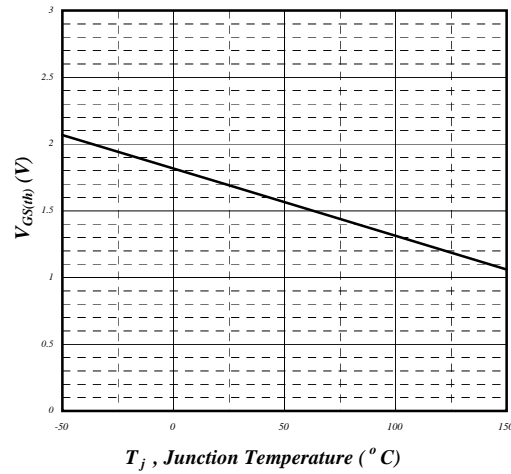


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

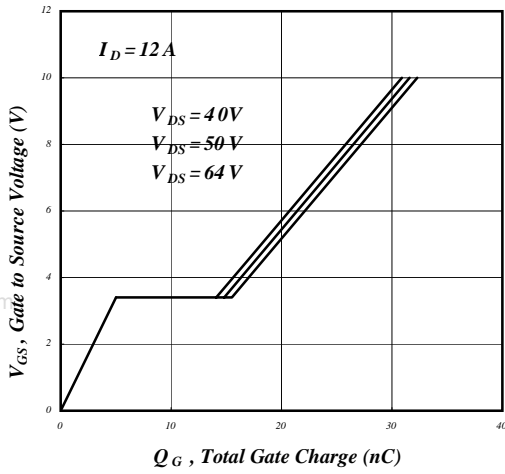


Fig 7. Gate Charge Characteristics

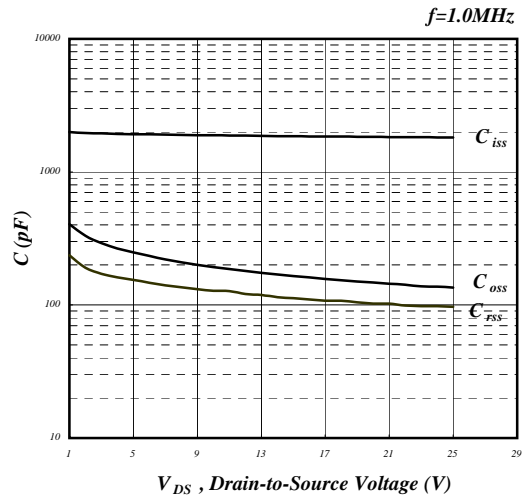


Fig 8. Typical Capacitance Characteristics

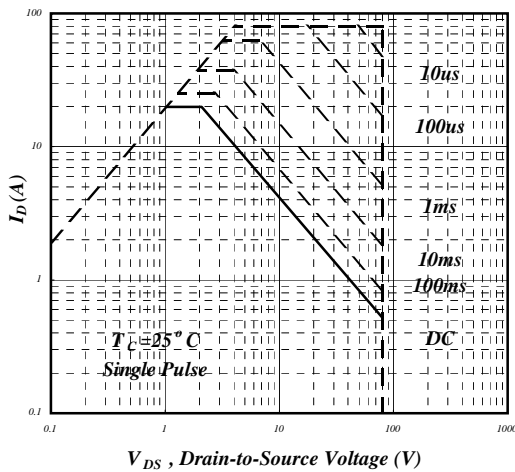


Fig 9. Maximum Safe Operating Area

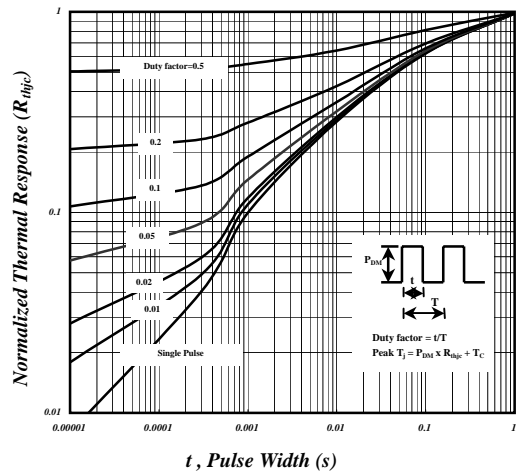


Fig 10. Effective Transient Thermal Impedance

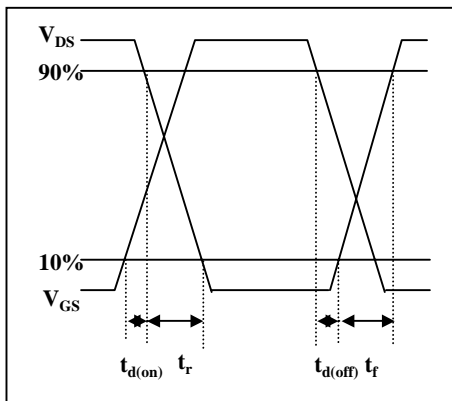


Fig 11. Switching Time Waveform

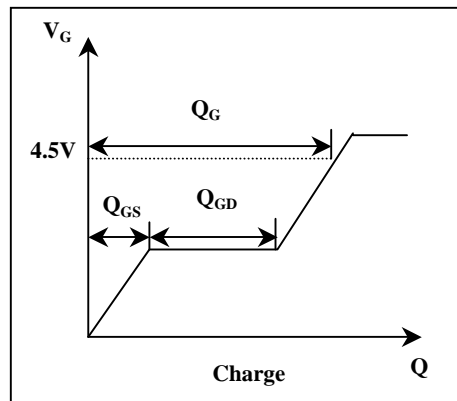


Fig 12. Gate Charge Waveform