
Features

- On-chip Control Functions are Available for System Gain Adjust (dB Linear versus DC Current)
- Low Noise LO Design
- ESD Protected

Benefits

- All Front-end Functions of a High-performance FM Receiver Except the RF Preamp are Integrated
- Improved Dynamic Range by High Current Double-balanced Mixer Design and a New AGC Conception with 3 Loops On-chip
- Improved Blocking and Intermod Behavior Due to a Unique “Interference” Sensor Controlling the AGC
- Easy Cascading of 3 IF Filters (Ceramic) Enabled by Two On-chip IF Preamp

Description

The IC U4065B is a bipolar integrated FM front-end circuit. It contains a mixer, an oscillator, two IF preamp and an unique interference sensor. The device is designed for high-performance car radio and home receiver applications.



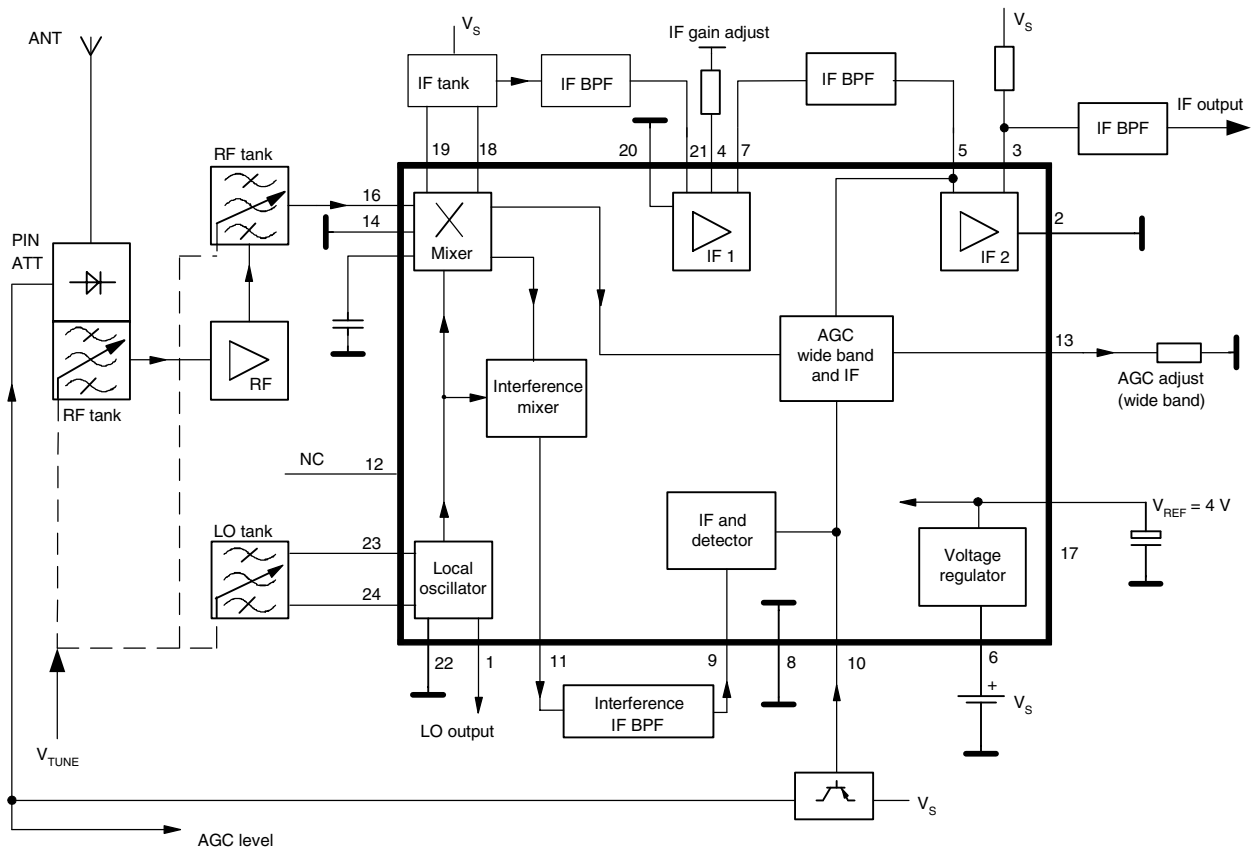
FM Receiver IC

U4065B

Rev. 4807A–AUDR–05/04

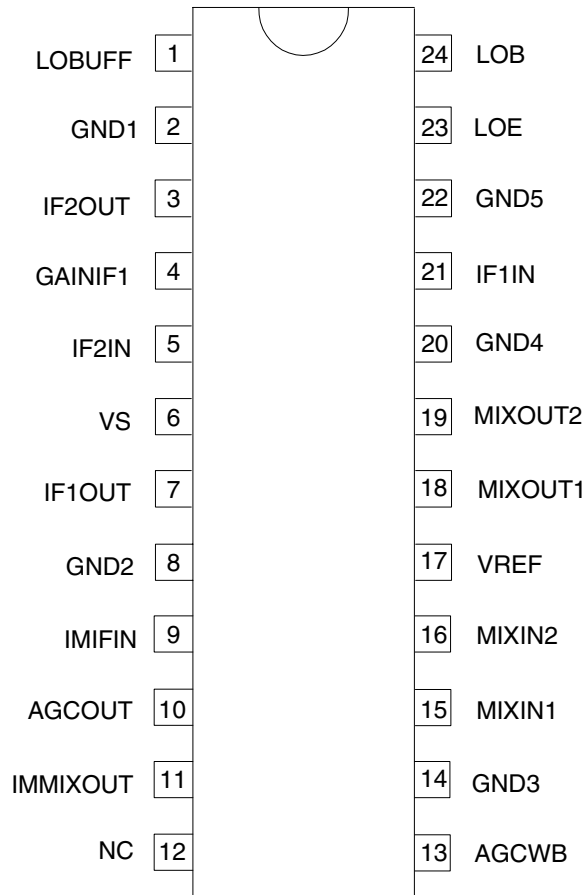


Figure 1. Block Diagram



Pin Configuration

Figure 2. Pinning SO24

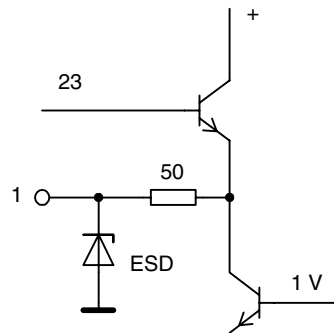


Pin Description

Pin	Symbol	Function
1	LOBUFF	Buffered local oscillator output
2	GND1	Ground of the second IF amplifier
3	IF2OUT	Output of the second IF amplifier
4	GAINIF1	Gain control of the first IF amplifier
5	IF2IN	Input of the second IF amplifier
6	VS	Supply voltage
7	IF1OUT	Output of the first IF amplifier
8	GND2	Ground
9	IMIFIN	Input of the amplifier for the IM sensor
10	AGCOUT	Output of the automatic gain control
11	IMMIXOUT	Output of the intermodulation mixer
12	NC	Not connected
13	AGCWB	Threshold adjustment of the wideband AGC
14	GND3	Mixer ground
15	MIXIN1	Input 1 of the double-balanced mixer
16	MIXIN2	Input 2 of the double-balanced mixer
17	VREF	Reference voltage output
18	MIXOUT1	Mixer output 1
19	MIXOUT2	Mixer output 2
20	GND4	Ground of the first IF amplifier
21	IF1IN	Input of the first IF amplifier
22	GND5	Oscillator ground
23	LOE	Local oscillator (emitter)
24	LOB	Local oscillator (base)

LOBUFF

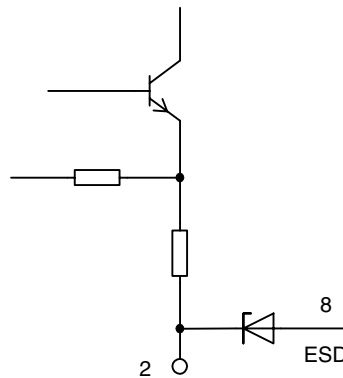
Figure 3. Buffered Local Oscillator Output



The buffered local oscillator used for output, drives the FM input of the PLL circuit (for example, U428xBM family). The typical parallel output resistance at 100 MHz is 70 Ω , the parallel output capacitance is about 10 pF. When using an external load of 500 Ω /10 pF, the oscillator swing is about 100 mV. The second harmonic of the oscillator frequency is less than -15 dBc.

GND1

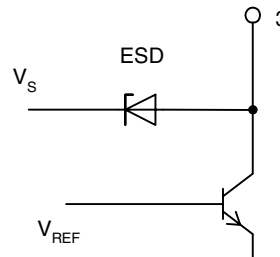
Figure 4. Ground of the Second IF Amplifier



There is no internal connection to the other ground pins.

IF2OUT

Figure 5. Output of the Second IF Amplifier

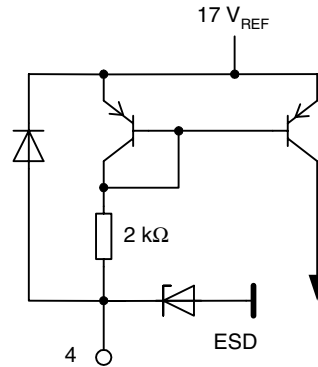


The parallel output capacitance to ground is about 7 pF. The external load resistance must be connected to V_S . The DC current into the pin is typically 3 mA.

Note: The supply voltage V_S has to be protected against IF distortion.

GAINIF1

Figure 6. Gain Control of the First IF Amplifier



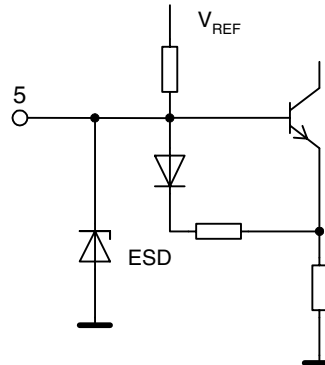
The gain of the first IF amplifier can be adjusted by a resistor to ground. This is useful, for example, to compensate for the insertion loss tolerances of the ceramic BPFs. It must be ensured that the output current of the pin does not exceed 150 μA in any case. Linear increasing in the current out of GAINIF1 results in a linear dB increase of the gain (0.15 dB/ μA).

$I_4 = 0$, thus, $G = G_{\min} = 2 \text{ dB}$

$I_4 = 140 \mu\text{A}$, thus, $G = G_{\max} = 22 \text{ dB}$

IF2IN

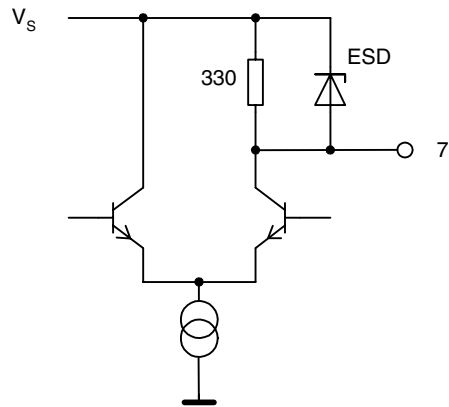
Figure 7. Input of the Second IF Amplifier



The parallel input resistance is 330 Ω . The parallel input capacitance is about 12 pF. No DC current is allowed. To avoid overload of this stage, an internal detector watches the input level and causes current at the AGCOUT pin.

IF1OUT

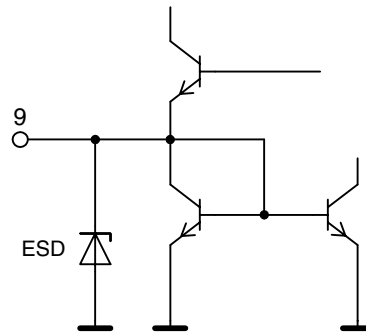
Figure 8. Output of the First IF Amplifier



The parallel output resistance is 330 Ω which allows the use of standard ceramic BPF. The parallel output capacitance is about 7 pF. The DC voltage at the pin is 0.5 V less than V_s .

IMIFIN

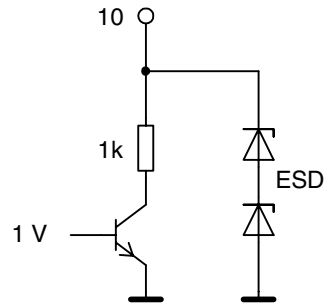
Figure 9. Input of the IF Amplifier for the IM Sensor



The parallel input resistance is 330 Ω . The amplifier is extremely sensitive to AC signals. An IF signal with a few hundred μV at this pin will cause current at the AGC output. Therefore, attention needs to be paid when connecting the standard ceramic filter between IMOUT and this pin. The reference point of the filter has to be free of any AC signal, no DC current shall appear at this pin.

AGCOUT

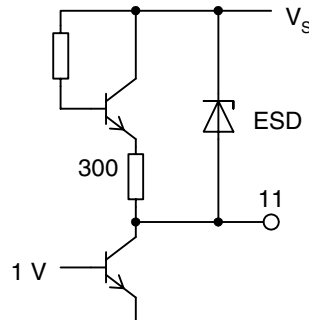
Figure 10. Output of the Automatic Gain Control



The AGC output is an open collector output. The current of the pin diode is this current multiplied by the current gain of the external PNP transistor. The DC voltage at the pin may vary from 2 V to V_S , therefore, this pin can easily be used as an indicator of the AGC regulation state.

IMMIXOUT

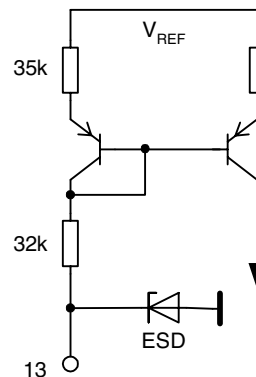
Figure 11. Output of the Intermodulation Mixer



The parallel output resistance is 330 Ω which allows the use of standard ceramic BPF without any further matching network. It must be ensured that the ground pin of the filter is free of AC signals.

AGCWB

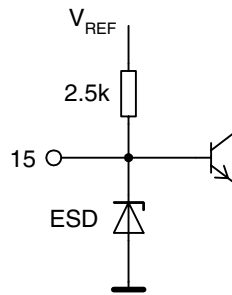
Figure 12. Threshold Adjustment of the Wideband AGC



The threshold of the wideband AGC can be adjusted by an external resistor to ground. The setting range is 10 dB. For minimum blocking, this pin is connected to ground. To set the threshold to lower levels, the resistance should have a value of up to a few hundred $k\Omega$.

MIXIN1

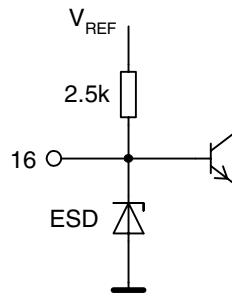
Figure 13. Input 1 of the Double-balanced Mixer



The parallel input resistance is 1.2 kΩ. The parallel input capacitance is about 9 pF. When using the mixer in an unbalanced way, this pin needs to be grounded for RF signals by an external capacitance of a few nF. DC current is not allowed.

MIXIN2

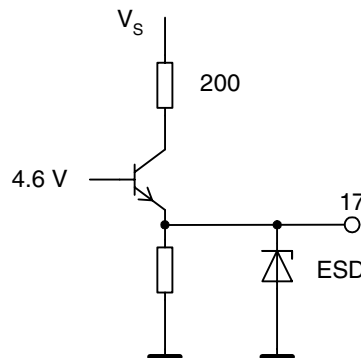
Figure 14. Input 2 of the Double-balanced Mixer



The parallel input resistance is 1.6 kΩ. The parallel input capacitance is about 7 pF. The double sideband noise figure of the unbalanced mixer is about 7 dB. If using the mixer in balanced mode, the noise figure will be reduced by about 0.8 dB.

VREF

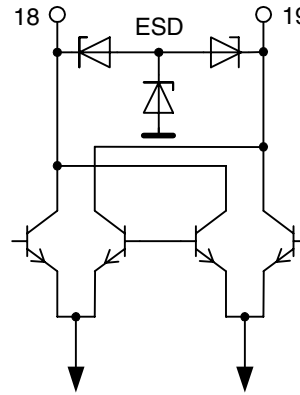
Figure 15. Reference Voltage Output



The internal temperature-compensated reference voltage is 3.9 V and it is used as bias voltage for most blocks. Therefore, the electrical characteristics of the U4065B are mainly independent of the supply voltage. The internal output resistance of the reference voltage is less than 10 Ω. To avoid internal coupling across this pin, external capacitors are required. The maximum output current is $I_{REF} = 5 \text{ mA}$.

MIXOUT1, MIXOUT2

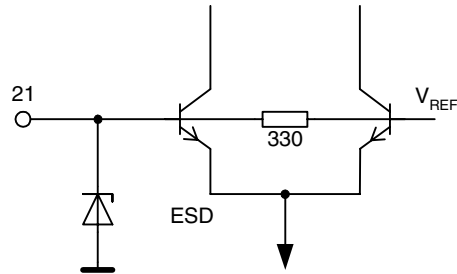
Figure 16. Mixer Output 1, 2



The mixer output is an open collector of a bipolar transistor. The minimum voltage at these pins is 5 V (V_S - voltage swing). The DC current into these pins is typically 9 mA. Good LO and RF suppression at the mixer output can be achieved by symmetrical load conditions at the pins MIXOUT1 and MIXOUT2.

IF1IN

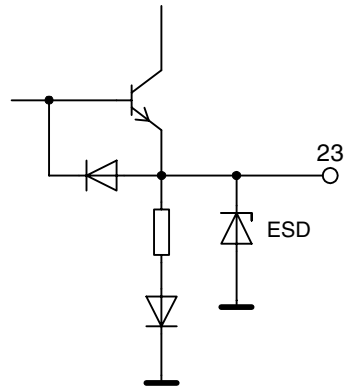
Figure 17. Input of the First IF Amplifier



The typical input resistance is 330 Ω . The DC voltage is almost identical to the reference voltage. DC current must be avoided at this pin.

LOE

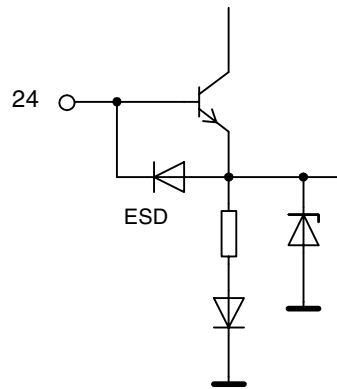
Figure 18. Emitter of the Local Oscillator



An external capacitor is connected between LOE and ground. The ground pin of this capacitor must be connected to pin GND5, the chip-internal ground of the local oscillator.

LOB

Figure 19. Base of the Local Oscillator



The tank of the local oscillator is connected at pin LOB. The ground pin of this tank needs to be connected to pin GND5, the chip-internal ground of the local oscillator's pin 24. The resonant resistance of the tank should be about 250 Ω . Minimum Q of the unloaded tank is 50.

Functional Description

The U4065B FM-frontend IC is the dedicated solution for high-end car radios. A new design philosophy enables to build up tuners with superior behavior. This philosophy is based on the fact that the sensitivity of state of the art designs is at the physical border and cannot be enhanced any more. On the other hand, the spectral power density in the FM-band increases. An improvement of reception can only be achieved by increasing the dynamic range of the receiver. This description is to give the designer an introduction to get familiar with this new product and its philosophy.

The Signal Path

The U4065B offers the complete signal path of an FM-frontend IC including a highly linear mixer and two IF preamplifiers. The mixer is a double-balanced, high-current Gilbert Cell. A high transit frequency of the internal transistors enables the use of the emitter grounded circuit with its favorable noise behavior. The full balanced output offers LO carrier reduction.

The first IF preamplifier has a dB-linear gain adjustment by DC means. Thus, different ceramic filter losses can be compensated and the overall tuner gain can be adapted to the individual requirements. The low noise design suppresses post stage noise in the signal path. Input and output resistance is 330 Ω to support standard ceramic filters. This is achieved without feedback, which would cause different input impedances when varying the output impedance.

The second IF preamplifier enables the use of three ceramic filters with real 330 Ω input- and output termination. Feedthrough of signals is kept low. The high level of output compression is necessary to keep up a high dynamic range.

Beneath the signal path the local oscillator part and the AGC signal generation can be found on chip. The local oscillator uses the collector grounded colpitts type. A low phase noise is achieved with this access. A mutual coupling in the oscillator coil is not necessary.

The AGC Concept

Special care was taken to design a unique AGC concept. It offers 3 AGC loops for different kinds of reception conditions. The most important loop is the interference sensor part.

In today's high-end car radios, the FM AGC is state of the art. It is necessary to reduce the influence of 3rd and higher order intermodulation to sustain reception in the presence of strong signals in the band. On one hand, it makes sense to reduce the desired signal level by AGC as few as possible to keep up stereo reception, on the other hand two or more strong out-of-channel signals may interfere and generate an intermodulation signal on the desired frequency. By introducing input attenuation, the level of the intermod signal decreases by a higher order, whereas the level of the desired signal shows only a linear dependency on the input attenuation. Therefore, input attenuation by pin diodes may keep up reception in the presence of strong signals.

The standard solution to generate the pin diode current is to pick up the RF-signal in front of the mixer. Because the bandwidth at that point is about 1.5 MHz, this is called wideband AGC. The threshold of AGC start is a critical parameter. A low threshold does not allow any intermodulation but has the disadvantage of blocking if there is only one strong station on the band or if the intermod signals do not cover the desired channel. A higher AGC threshold may tolerate a certain ground floor of intermodulation. This avoids blocking, but it has the disadvantage, that no reception is possible, if the interfering signals generate an intermod signal inside the desired channel. This contradiction could not be overcome in the past.

With the new U4065B IC, there is a unique access to this problem. This product has an interference sensor on chip. Thus, an input signal attenuation is only performed if the interfering signals do generate an intermod signal inside the desired channel. If they do not, the existing wideband AGC is active but up to 20 dB higher levels. The optimum AGC state is always generated.

The Figure 20 to Figure 23 on page 14 illustrate the situation. In Figure 20 the AGC threshold of a standard tuner is high to avoid blocking. But then the intermod signal suppresses the desired signal. The interference sensor of the U4065B ensures that the AGC threshold is kept low as illustrated in Figure 21 on page 14.

In Figure 22 on page 14 the situation is reversed. The AGC threshold of a standard tuner is kept low to avoid intermod problems. But then blocking makes the desired signal level drop below the necessary stereo level. In this case, the higher wideband AGC level of the U4065B enables perfect stereo reception.

By principle, this interference sensor is an element with a third order characteristic. For input levels of zero, the output level is zero, too. With increasing input level, the output level is increased with the power of three, thus preferring intermod signals compared to linear signals. At the same time, a down conversion to the IF level of 10.7 MHz is performed. If a corresponding 10.7 MHz IF filter selects the intermod signals, only an output is generated, if an intermod signal inside the 10.7 MHz channel is present.

The circuit blocks interference sensor and IF, and detector build up a second IF chain. In an FM system, the maximum deviation of a 3rd order intermod signal is the triple max deviation of the desired signal. Therefore, the ceramic IF BPF between pin 11 and pin 9 may be a large bandwidth type. This is all that is needed for this unique feature.

A further narrow band AGC avoids overriding the second IF amplifier. The amplitude information of the channel is not compressed in order to maintain multipath detection in the IF part of the receiver.

Figure 20. A High AGC Threshold Causes the Intermod Signal to Suppress the Desired Signal

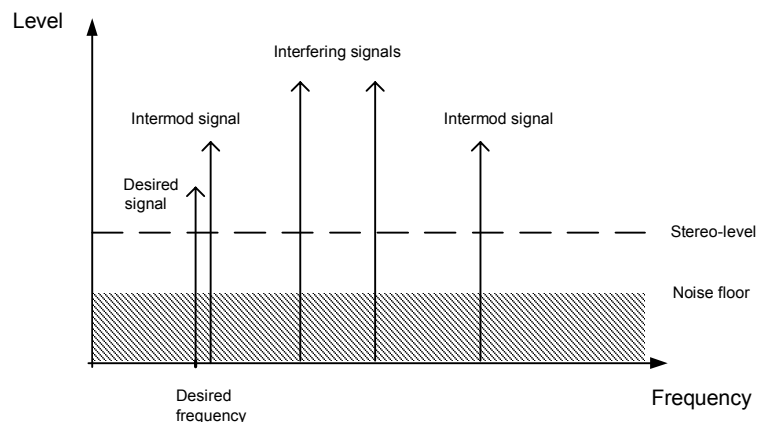


Figure 21. AGC Threshold Settings

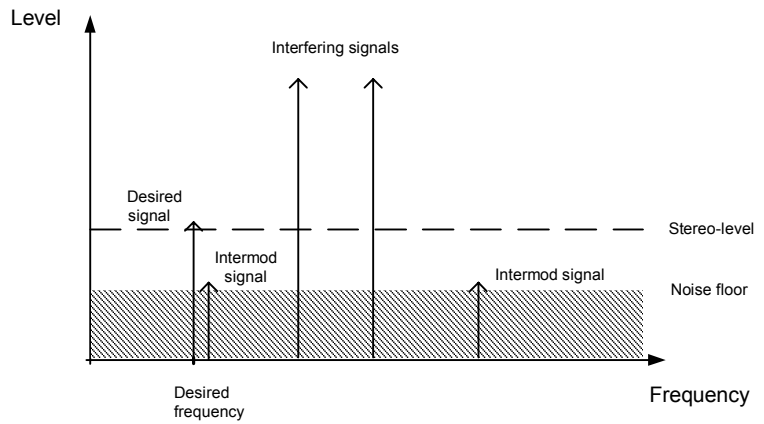


Figure 22. A Low AGC Threshold Causes the Blocking Signal to Suppress the Desired Signal

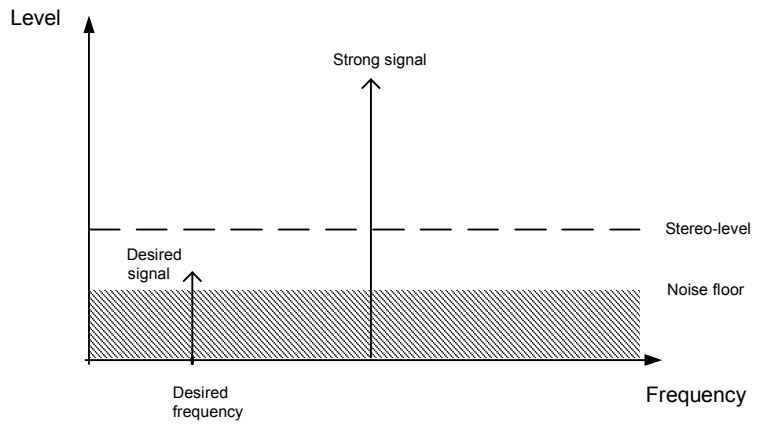
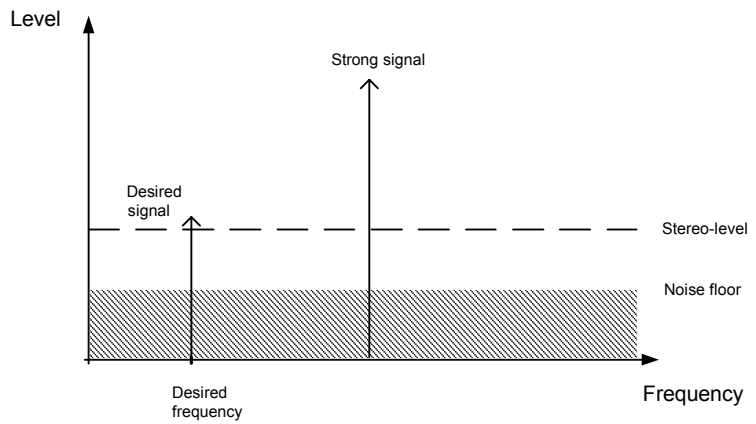


Figure 23. The Correct AGC Threshold Enables Optimum Reception



Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Reference point is ground (pins 2, 8, 14, 20 and 22)

Parameters	Symbol	Value	Unit
Supply voltage	V_S	10	V
Power dissipation at $T_{amb} = 85^\circ\text{C}$	P_{tot}	470	mW
Junction temperature	T_j	125	$^\circ\text{C}$
Ambient temperature range	T_{amb}	-30 to +85	$^\circ\text{C}$
Storage temperature range	T_{stg}	-50 to +125	$^\circ\text{C}$
Electrostatic handling: Human body model (HBM), all I/O pins tested against the supply pins	$\pm V_{ESD}$	2000	V

Thermal Resistance

Parameters	Symbol	Value	Unit
Thermal resistance	R_{thJA}	90	K/W

Electrical Characteristics

$V_S = 8.0\text{ V}$, $f_{RF} = 98\text{ MHz}$, $f_{OSC} \cong 108.7\text{ MHz}$, $f_{IF} = f_{OSC} - f_{RF} = 10.7\text{ MHz}$

Reference point is ground (pins 2, 8, 14, 20, and 22), $T_{amb} = 25^\circ\text{C}$, unless otherwise specified.

Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit
Supply voltage		3, 6, 10, 18, 19	V_S	7	8	10	V
Supply current		3, 6, 10, 18, 19	I_{tot}		37	47	mA
Oscillator (GND5 Has to be Connected to External Oscillator Components)							
Oscillator voltage	$R_{G24} = 220\ \Omega$, unloaded Q of $L_{OSC} = 70$, $R_{L1} = 520\ \Omega$	24 23 1	V_{LOB} V_{LOE} V_{LOBUFF}	70	160 100 90	220	mV
Harmonics		1				-15	dBc
Output resistance		1	R_{LO}		70		Ω
Voltage gain		Between 1 and 23			0.9		
Mixer (GND3 Has to be Separated from GND1, GND2 and GND4)							
Conversion power gain	Source impedance: $R_{G15,16} = 200\ \Omega$ Load impedance: $R_{L18,19} = 200\ \Omega$		G_C	5	7	10	dB
3rd-order input intercept			IP_3	4	6	14	dBm
Conversion transconductance			g_C		8		mA/V
Noise figure			NF_{DSB}		7		dB
Input resistance to ground	$f = 100\text{ MHz}$	15	R_{ignd15}		1.2		k Ω
Input capacitance to ground	$f = 100\text{ MHz}$	15	C_{ignd15}		9		pF
Input resistance to ground	$f = 100\text{ MHz}$	16	R_{ignd16}		1.6		k Ω
Input capacitance to ground	$f = 100\text{ MHz}$	16	C_{ignd16}		7		pF
Input-input resistance		Between 15 and 16	$R_{ii15,16}$		1.6		k Ω
Input-input capacitance		Between 15 and 16	$C_{ii15,16}$		5		pF
Output capacitance to GND		18 and 19	$C_{ignd18,19}$		9		pF

Electrical Characteristics (Continued)

$V_S = 8.0\text{ V}$, $f_{RF} = 98\text{ MHz}$, $f_{OSC} \cong 108.7\text{ MHz}$, $f_{IF} = f_{OSC} - f_{RF} = 10.7\text{ MHz}$

Reference point is ground (pins 2, 8, 14, 20, and 22), $T_{amb} = 25^\circ\text{C}$, unless otherwise specified.

Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit
First IF Preamp (IF 1)							
Gain control deviation by I_4		4		17	20	24	dB
Gain control slope		4	dG_{IF1}/dI_4		0.15		dB/ μA
External control current to ground At G_{min} At G_{nom} At G_{max}			I_{4min} I_{4nom} I_{4max}		0 70 140		μA
Power gain At I_{4min} At I_{4nom} At I_{4max}	Source impedance: $R_{G21} = 200\ \Omega$	Between 21 and 7	G_{min} G_{nom} G_{max}	-2.5 11 19	2 12 22	2.5 16 28	dB
Noise figure At G_{max} At G_{nom} At G_{min}	Load impedance: $R_{L7} = 200\ \Omega$	Between 21 and 7	NF_{min} NF_{nom} NF_{max}		7 9 15		dB
Temperature coefficient of the gain at G_{nom}			TKnom		+0.045		dB/K
1 dB compression at G_{nom}		7	V_{cnom}		70		mV
-3 dB cut-off frequency at G_{nom}		7	f_{cnom}		50		MHz
Input resistance	$f = 10\text{ MHz}$	21	R_{iIF1}	270	330	400	Ω
Input capacitance	$f = 10\text{ MHz}$	21	C_{iIF1}		5		pF
Output resistance	$f = 10\text{ MHz}$	7	R_{oIF1}	270	330	400	Ω
Output capacitance	$f = 10\text{ MHz}$	7	C_{oIF1}		7		pF
Second IF Preamp (IF 2)							
Power gain	Source impedance: $R_{G5} = 200\ \Omega$ Load impedance: $R_{L3} = 200\ \Omega$	Between 5 and 3	G_{IF2}	15	18	19	dB
Noise figure			NF_{IF2}		7		dB
1 dB compression		3	V_{comp}		500		mV
-3 dB cutoff frequency		3	f_c		50		MHz
Parallel input resistance	$f = 10\text{ MHz}$	5	R_{iIF2}	270	330	400	Ω
Parallel input capacitance	$f = 10\text{ MHz}$	5	C_{iIF2}		12		pF
Parallel output resistance	$f = 10\text{ MHz}$	3	R_{oIF2}		50		k Ω
Parallel output capacitance	$f = 10\text{ MHz}$	3	C_{oIF2}		7		pF
Voltage Regulator							
Regulated voltage		17	V_{ref}	3.7	3.9	4.9	V
Maximum output current		17	I_{ref}	5			mA
Internal differential resistance, dc_{17}/di_{17} when $I_{17} = 0$		17	r_{d17}		7	50	Ω
Power supply suppression	$f = 50\text{ Hz}$	17	psrr	36	50		dB

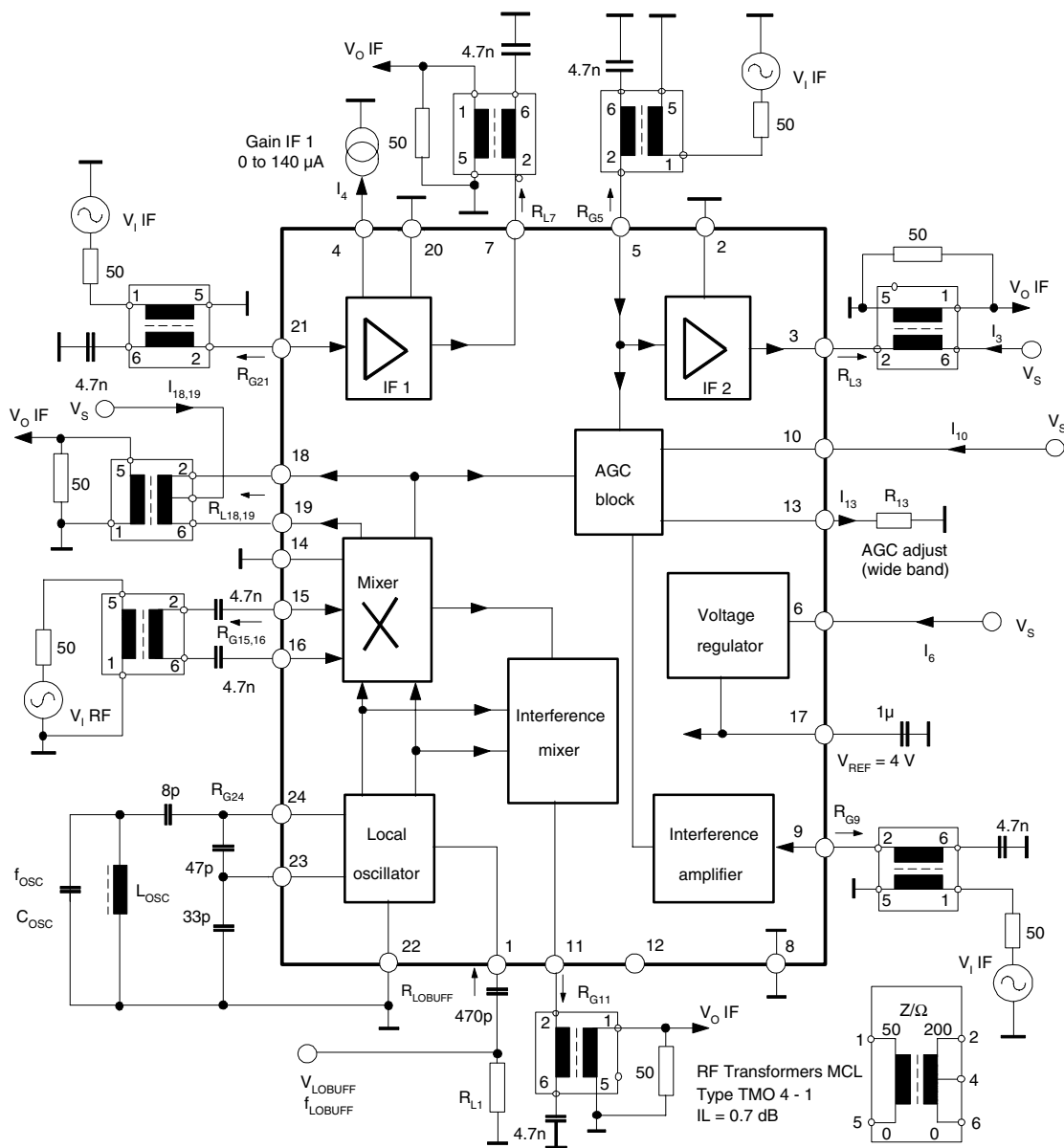
Electrical Characteristics (Continued)

$V_S = 8.0\text{ V}$, $f_{RF} = 98\text{ MHz}$, $f_{OSC} \cong 108.7\text{ MHz}$, $f_{IF} = f_{OSC} - f_{RF} = 10.7\text{ MHz}$

Reference point is ground (pins 2, 8, 14, 20, and 22), $T_{amb} = 25^\circ\text{C}$, unless otherwise specified.

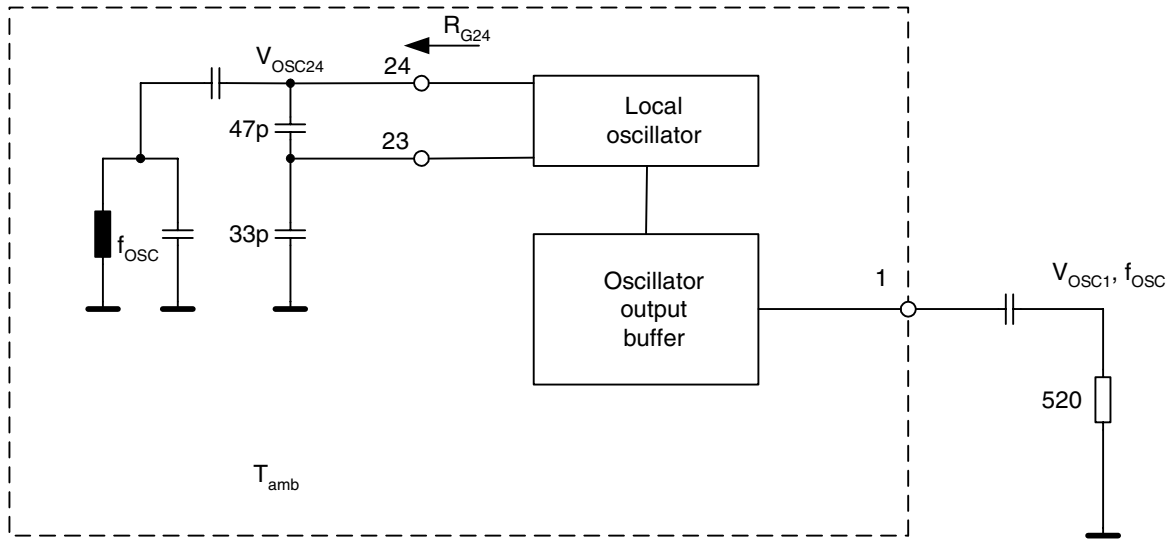
Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit
AGC Input Voltage Thresholds (AGC Threshold Current is 10 μA at Pin 10)							
IF2 input		5	V_{thIF2}	85	86	92	$\text{dB}\mu\text{V}$
IF and detector		9	V_{thIFD}	42	43	48	$\text{dB}\mu\text{V}$
Mixer input level of wideband sensor	$f_{iRF} = 100\text{ MHz}$ V at pin 13 = 0 V I through pin 13 = 0 A	Between 15 and 16	V_{thWB1}	95	98	100	$\text{dB}\mu\text{V}$
			V_{thWB2}	85	87	90	$\text{dB}\mu\text{V}$

Figure 24. Test Circuit



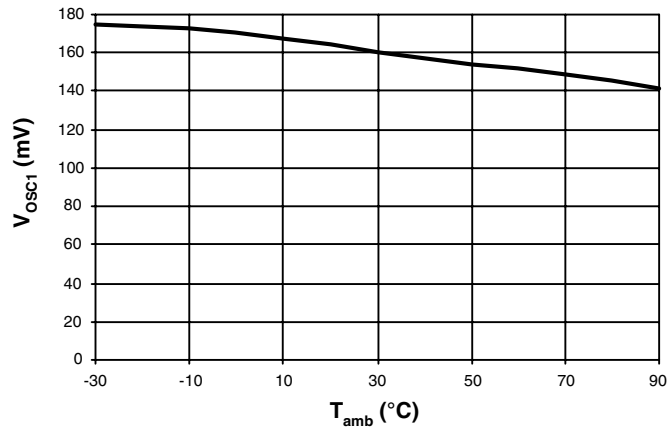
Local Oscillator

Figure 25. LO Principle Application



Free running oscillator frequency $f_{OSC} \approx 110$ MHz, $V_{OSC24} = 160$ mV, $R_{G24} = 220 \Omega$, $Q_L = 70$

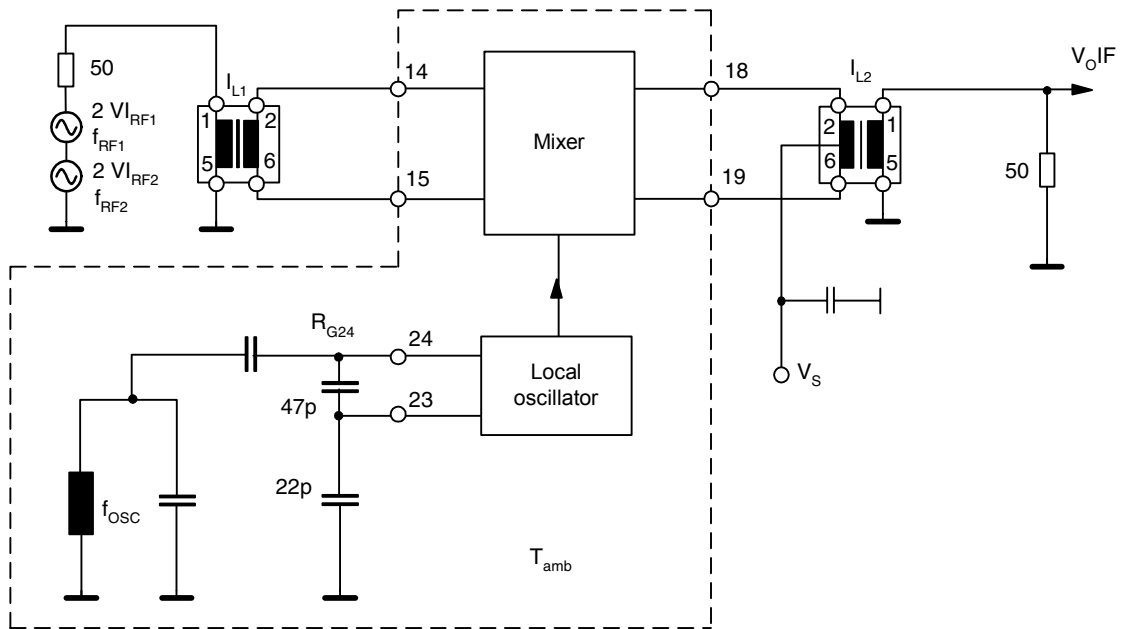
Figure 26. Oscillator Swing versus Temperature



Mixer

$$f_{OSC} = 110.7 \text{ MHz}, V_{OSC24} \cong 160 \text{ mV}, f_{IF} = 10.7 \text{ MHz}$$

Figure 27. Mixer Principle Application



Conversion power gain $G_c = 20 \log (V_{OIF}/V_{IF}) + I_{L1} \text{ (dB)} + I_{L2} \text{ (dB)}$
 I_{L1}, I_{L2} insertion loss of the RF transformers

Figure 28. Mixer Characteristic

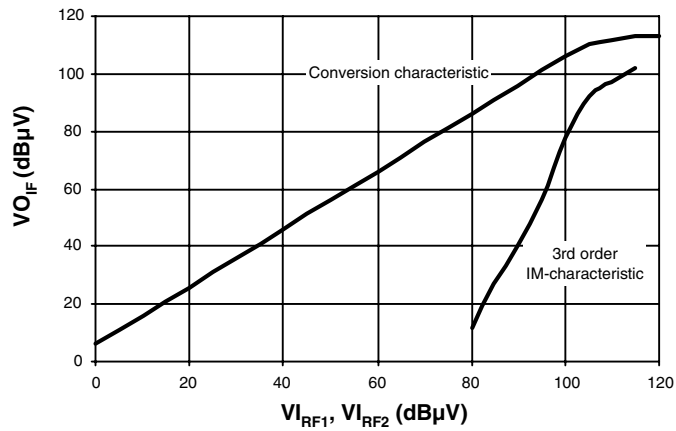


Figure 29. Conversion Power Gain of the Mixer Stage versus Temperature

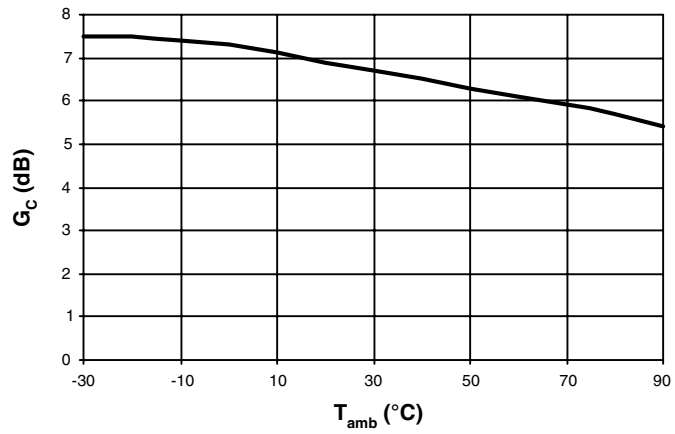
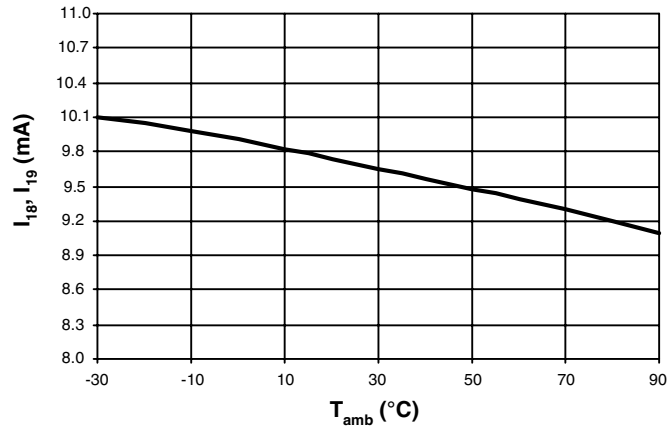
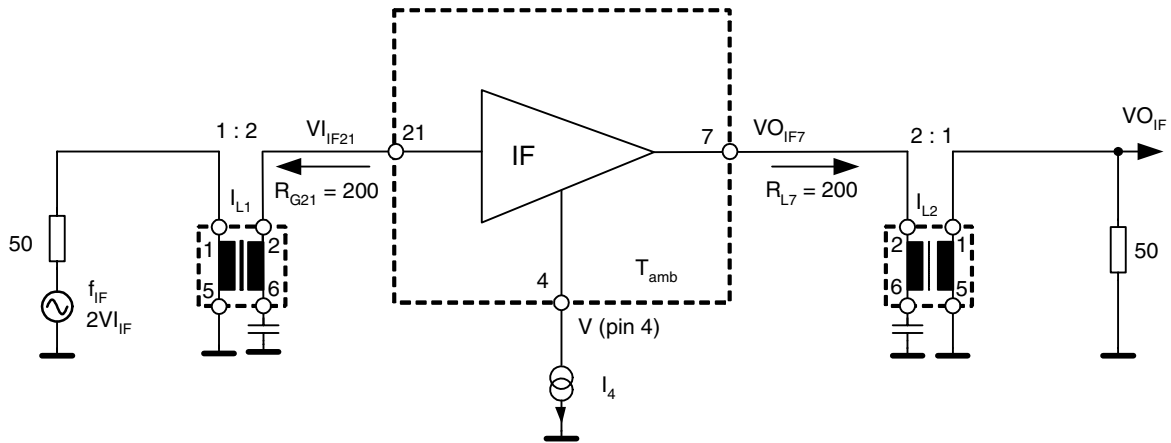


Figure 30. Current of the Mixer Stage versus Temperature



First IF Preampfier

Figure 31. First IF Preampfier Principle Application



Power gain $G_{IF} = 20 \log (V_{O_{IF}}/V_{I_{IF}}) + I_{L1} \text{ (dB)} + I_{L2} \text{ (dB)}$

I_{L1}, I_{L2} = insertion loss of the RF transformers

Figure 32. Power Gain of the First IF Amplifier versus I_4

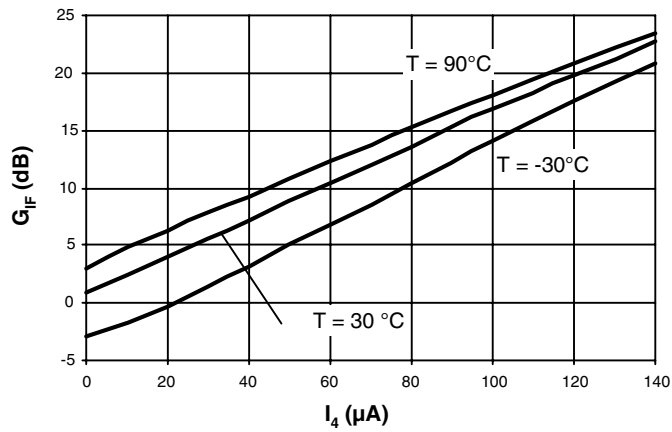


Figure 33. Power Gain of the First IF Amplifier versus Frequency

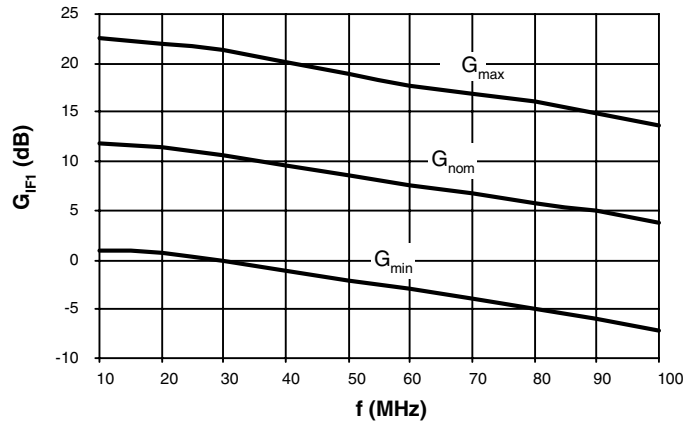
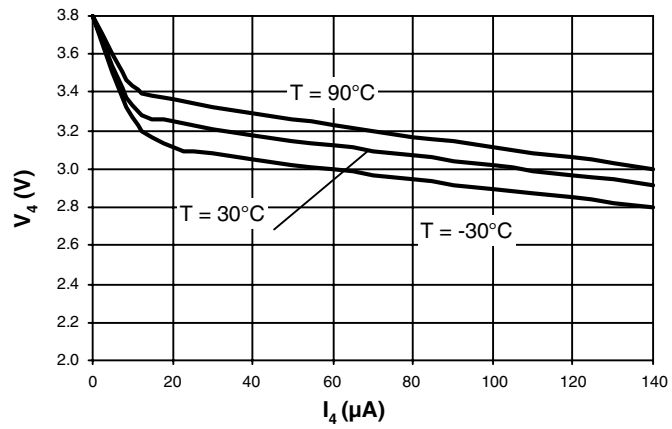
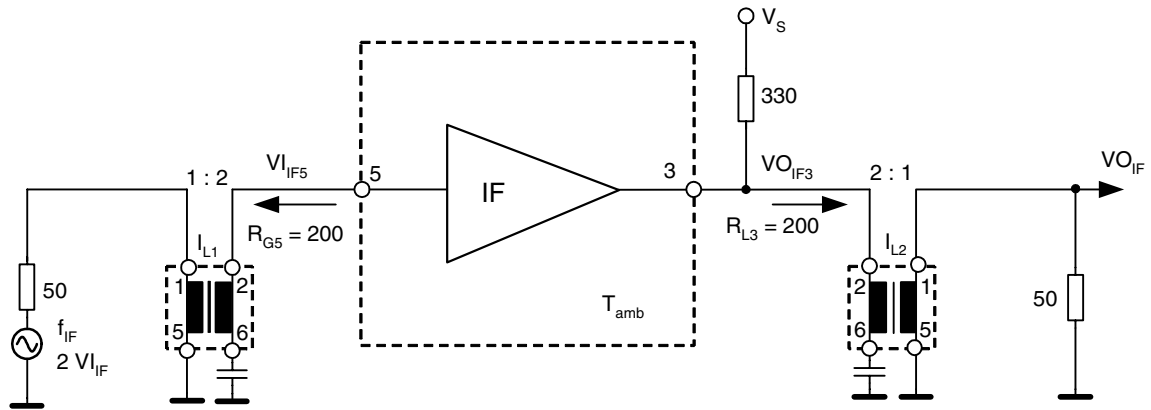


Figure 34. V₄ (Pin 4) versus I₄



Second IF Preamplifier

Figure 35. Second IF Preamplifier Principle Application



Power gain $G_{IF} = 20 \log (V_{O_{IF}}/V_{I_{IF}}) + I_{L1} \text{ (dB)} + I_{L2} \text{ (dB)}$
 $I_{L1}; I_{L2}$ = insertion loss of the RF transformers

Figure 36. Power Gain of the Second IF Amplifier versus Temperature

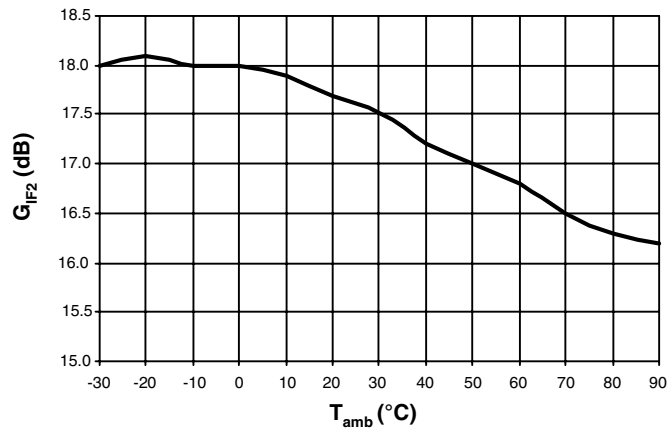


Figure 37. Power Gain of the Second IF Amplifier versus Frequency

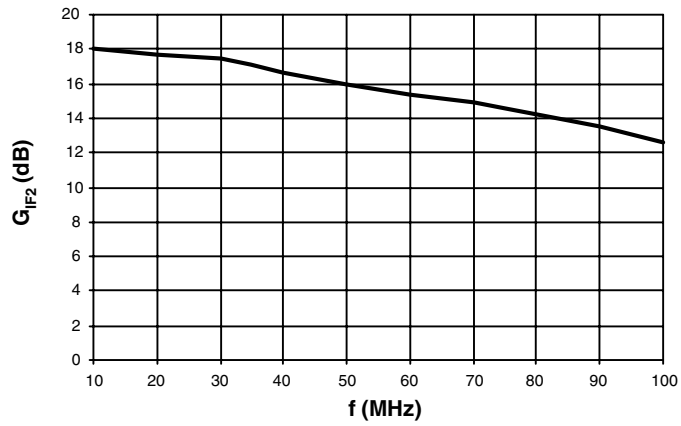


Figure 38. AGC Threshold (110 = 1 μ A) of the Second IF Amplifier versus Temperature

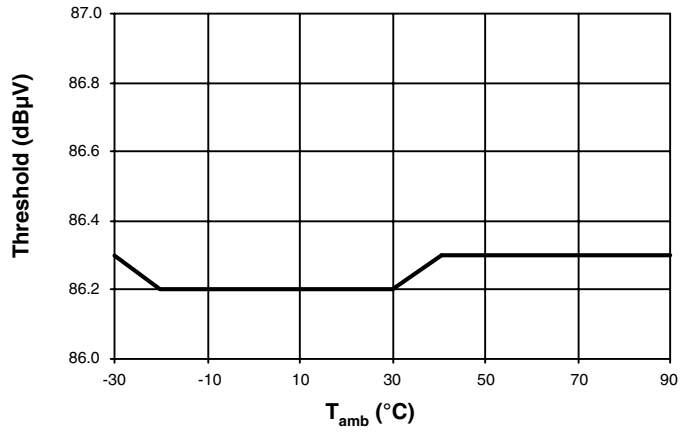
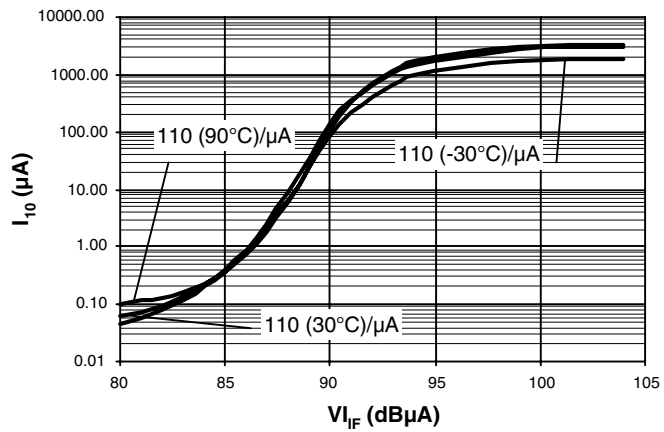
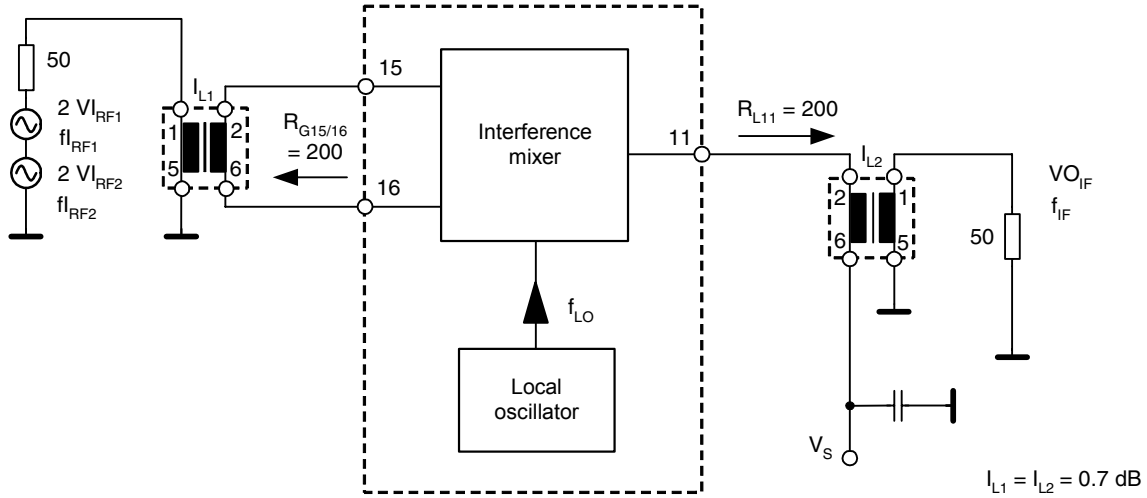


Figure 39. AGC Characteristic of the Second IF Amplifier Input



Interference Sensor (Mixer)

Figure 40. Interference Sensor Principle Application



Test conditions for characteristic VO_{IF} versus VI_{RF1} :

$$f_{LO} = 100 \text{ MHz}, f_{RF1} = 89.3 \text{ MHz}, VI_{RF2} = 0, f_{IF} = f_{LO} - f_{RF1} = 10.7 \text{ MHz}$$

Test conditions for 3rd order IM-characteristic VO_{IF} versus VI_{RF1} , VI_{RF2} :

$$f_{LO} = 100 \text{ MHz}, f_{RF1} = 89.4 \text{ MHz}, f_{RF2} = 89.5 \text{ MHz}, f_{IF} = f_{LO} - (2 f_{RF1} - 1 f_{RF2}) = 10.7 \text{ MHz}$$

I_{L1} , I_{L2} = insertion loss of the RF transformer

Figure 41. Characteristics of the Interference Sensor (Mixer)

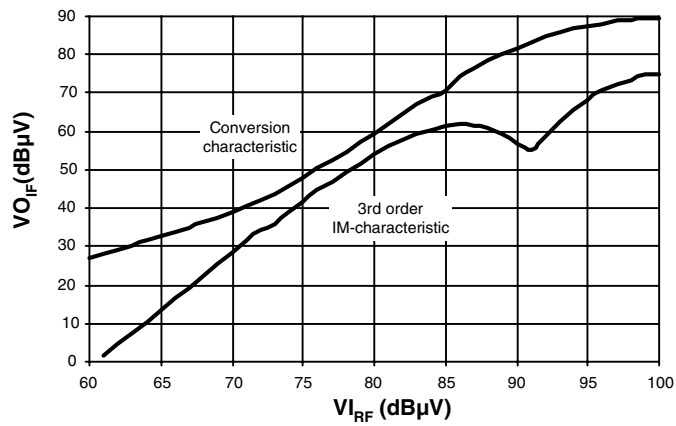


Figure 42. Conversion Characteristic of the Interference Sensor (Mixer)

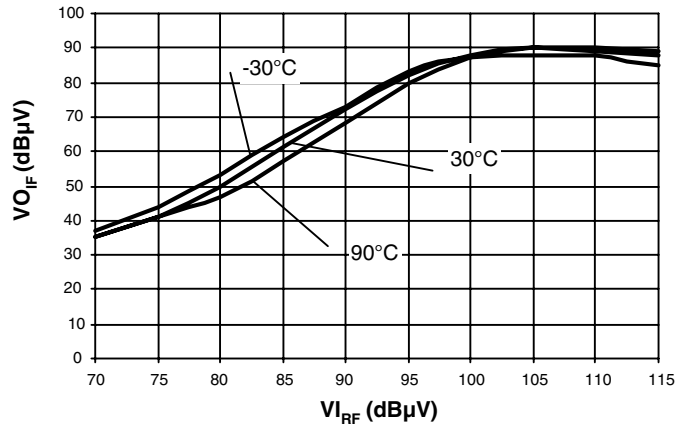
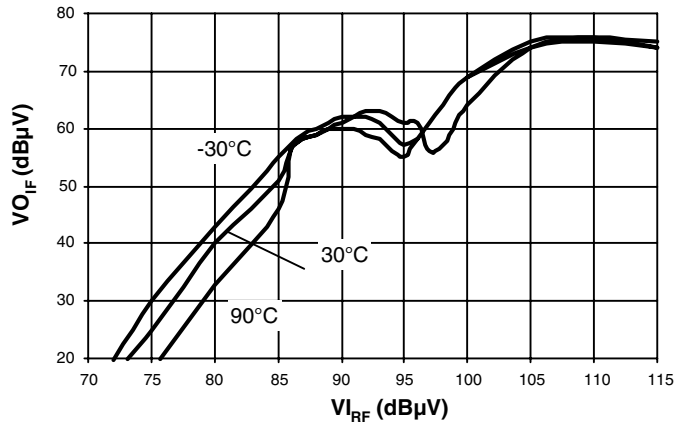
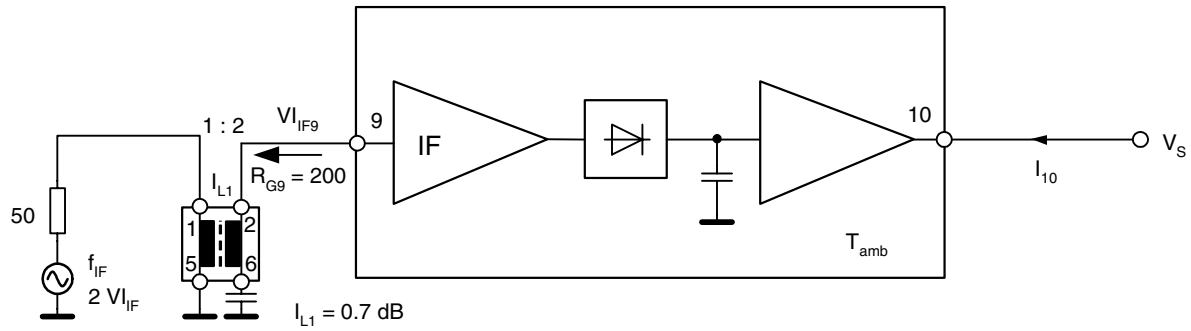


Figure 43. Third-order Interference Characteristic of the Interference Sensor (Mixer)



Interference Sensor (Amplifier)

Figure 44. Interference Sensor Principle Application



AGC Thresholds

Figure 45. AGC Threshold of the Interference IF Amplifier versus Temperature

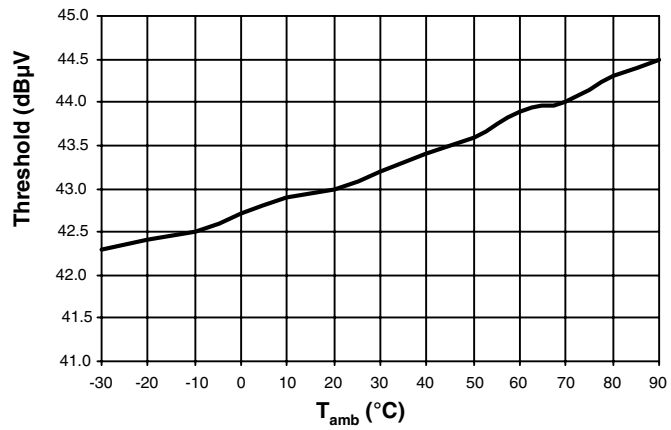


Figure 46. Wideband AGC Threshold ($I_{10} = 1 \mu A$) versus I_{13}

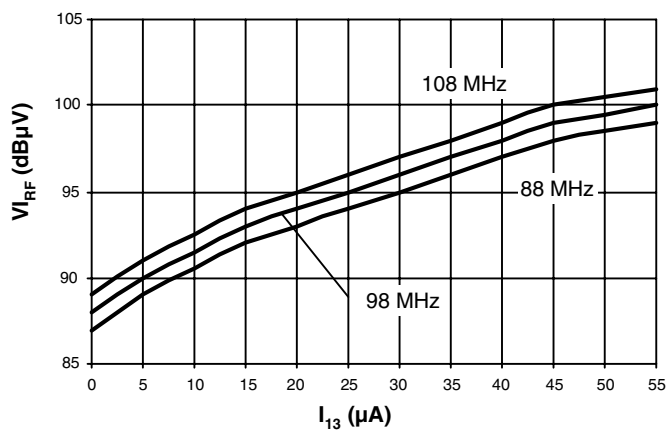
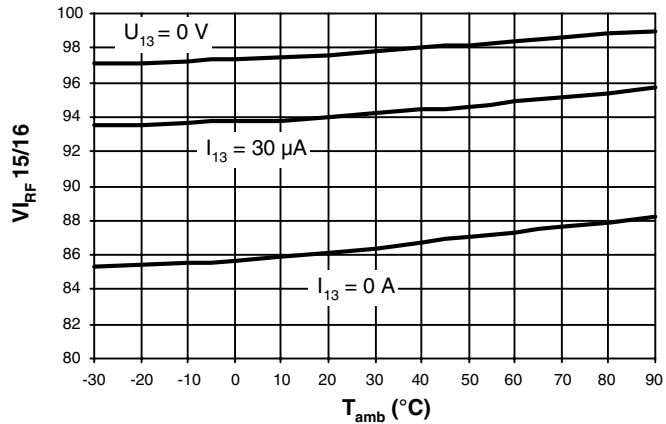


Figure 47. Wideband AGC Threshold ($I_{10} = 1 \mu\text{A}$) versus Temperature



AGC Characteristics

Figure 48. AGC Characteristic of the Interference IF and Detector Block

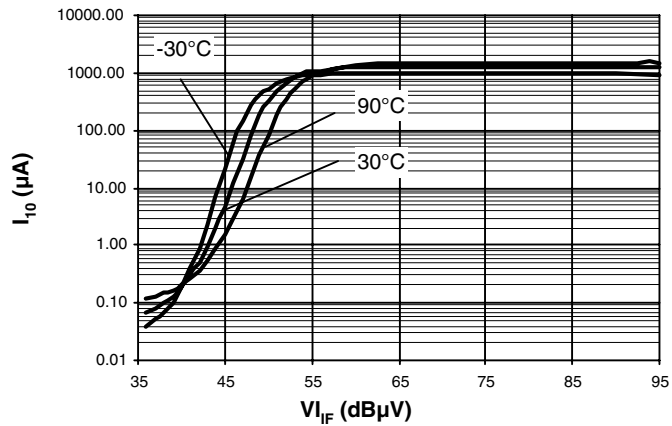


Figure 49. Characteristic of the Wideband AGC ($I_{13} = 0\text{ V}$)

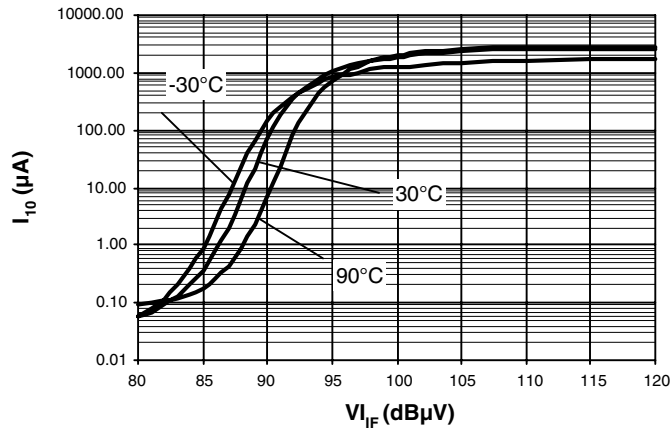
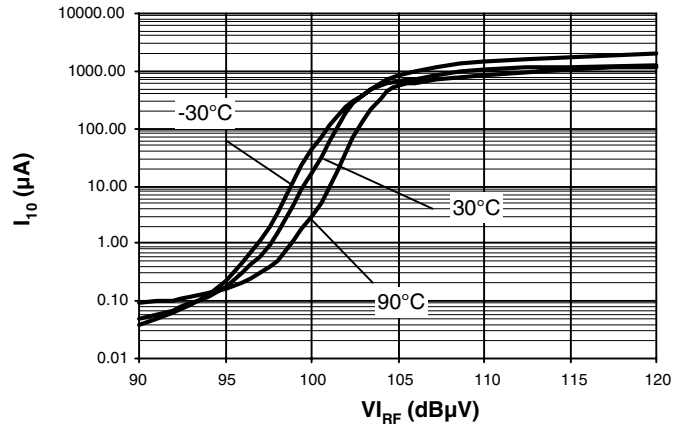


Figure 50. Characteristic of the Wideband AGC ($V_{13} = 0$ V)



DC Characteristics

Figure 51. Supply Current versus Supply Voltage

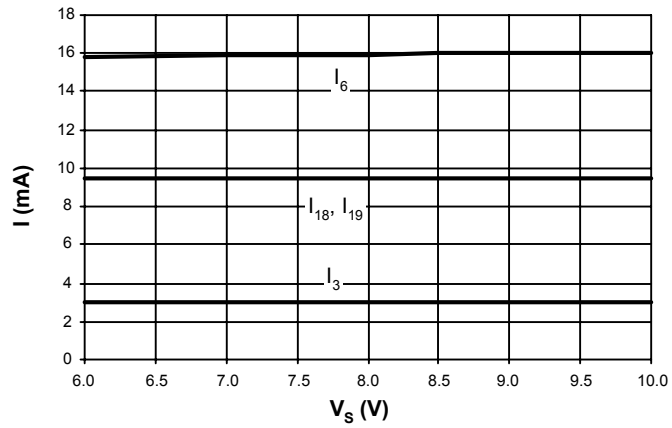


Figure 52. Reference Voltage versus Temperature

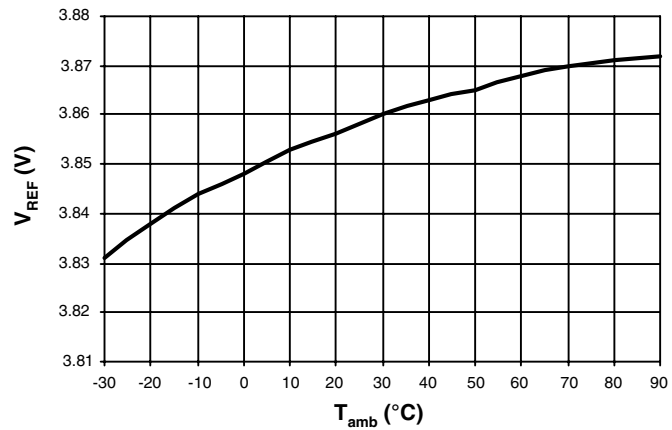


Figure 53. Supply Current versus Temperature

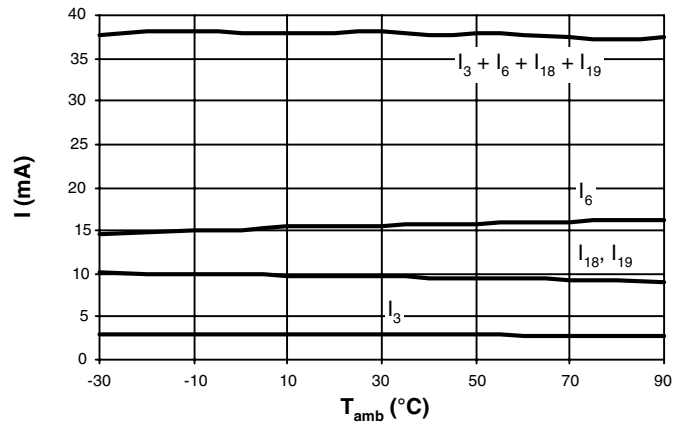


Figure 54. Reference Voltage versus I_{17}

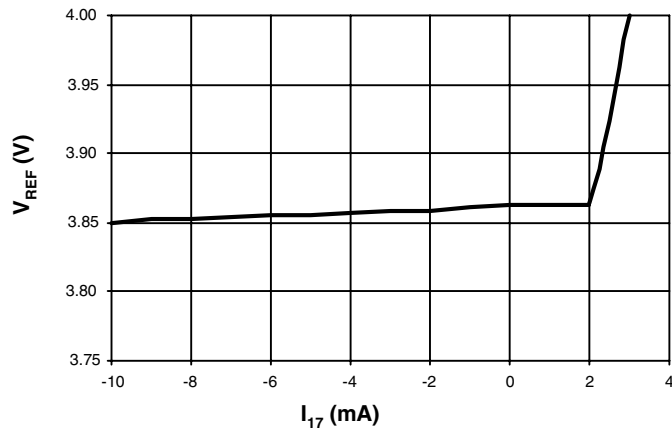
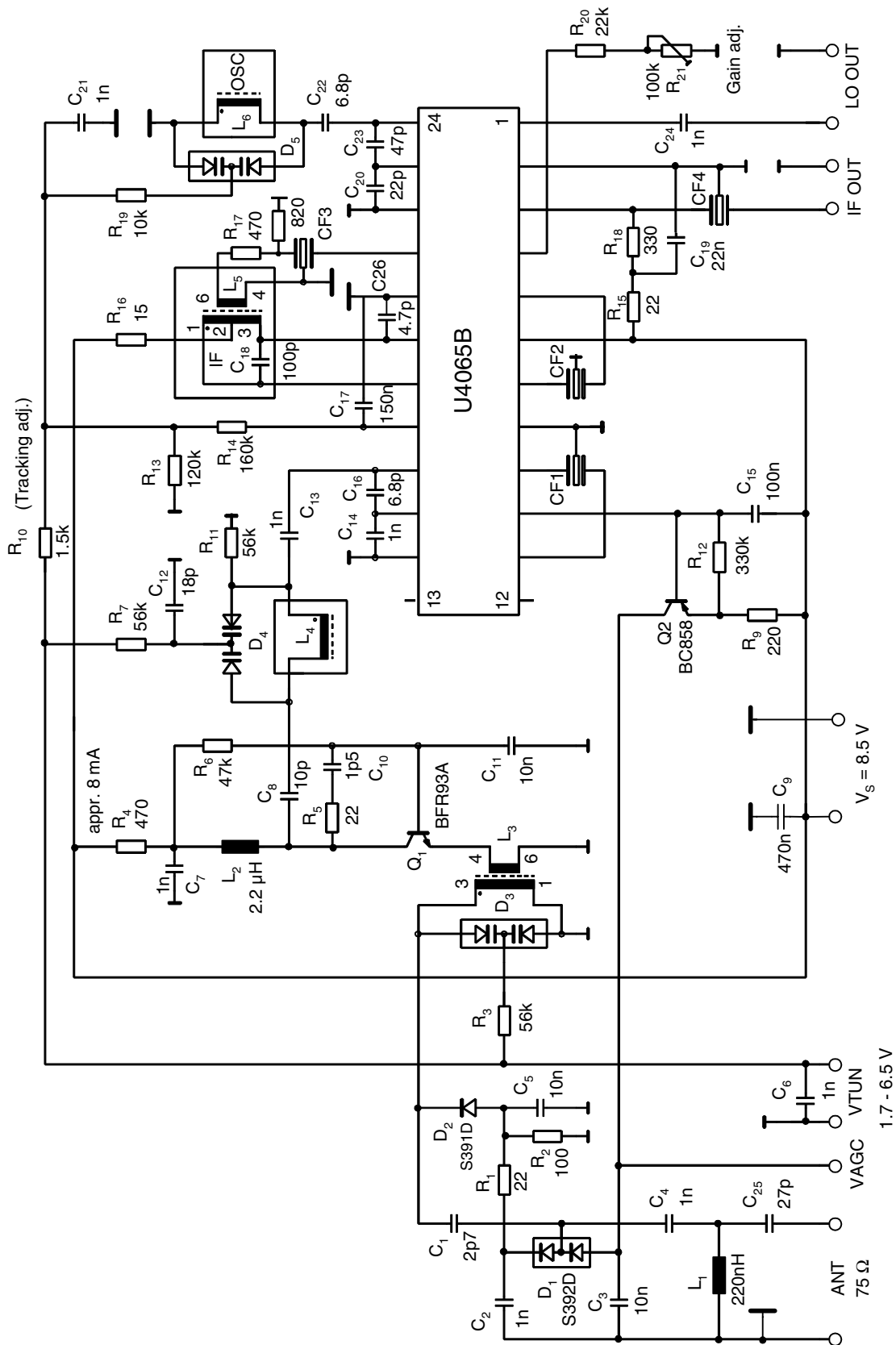


Figure 55. Application Diagram



Part List

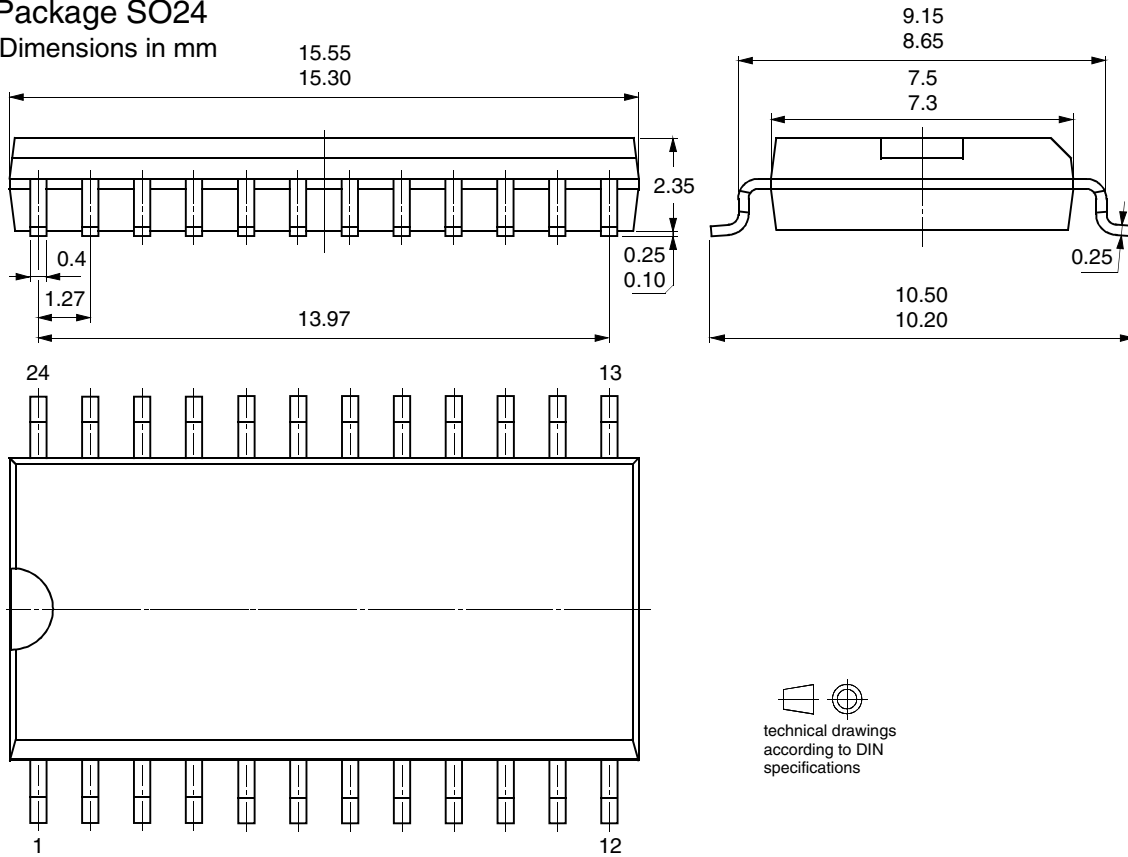
Item	Description
Q1	BFR93AR (BFR93A)
Q2	BC858
D1	S392D
D2	S391D
D3, D4, D5	BB804
L1	11 turns, 0.35 mm wire, 3 mm diameter (approximately 220 nH)
L2	2.2 mH (high Q type)
L3	TOKO® 7KL-type, # 600ENF-7251x
L4	TOKO 7KL-type, # 291ENS 2341IB
L5	TOKO 7KL-type, # M600BCS-1397N
L6	TOKO 7KL-type, # 291ENS 2054IB
CF1	TOKO type SKM 2 (230 KHZ)
CF2, CF3, CF4	TOKO type SKM 3 (180 KHZ)


Ordering Information

Extended Type Number	Package	Remarks
U4065B-AFL	SO24 plastic	–
U4065B-AFL3	SO24 plastic	Taping according to ICE-286-3

Package Information

Package SO24
Dimensions in mm




technical drawings
according to DIN
specifications



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Fax: (49) 71-31-67-2340

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