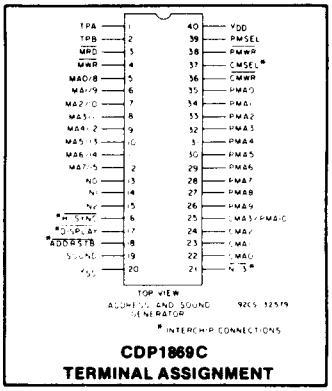
CDP1869C, CDP1870C, CDP1876C

Advance Information/
Preliminary Data



CDP1869C
TERMINAL ASSIGNMENT

Video Interface System (VIS)

Features:

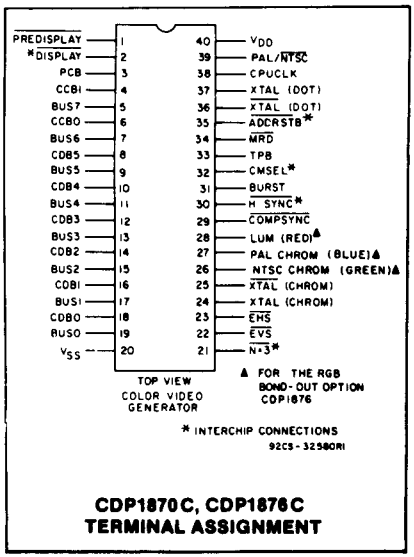
- *DOT frequency=5.67 MHz (PAL=5.626 MHz). Easily adaptable for RF (antenna) input*
- *CPU clock independent (½ DOT rate provided)*
- *CPU not involved in screen refresh*
- *Non-interlaced*
- *Graphics and motion*
- *Up to 256 different characters*
- *Character memory may be any combination of ROM or RAM Programmable for 12/24 rows x 20/40 char/row*
- *6 x 8 or 6 x 16 char. matrix (6 x 9 for PAL)*
- *Character generation approach minimizes memory*
- *PAL and NTSC compatible*
- *Page memory is accessed as extension of CPU memory during non-display time*
- *Composite sync, luminance, and chrominance outputs*
- *Programmable background color*
- *Hardware scroll capability*
- *Audio generator (576 selectable tones covering 8 octaves) and white noise generator*
- *Both tones and white noise can be enveloped from 0 to 0.78 V_{DD} in 16 steps*
- *External horizontal and vertical sync inputs allow for integration into existing chassis for character-on-picture overlays*
- *Teletext compatible format*
- *RGB bond-out option available (CDP1876C)*

The RCA-CDP1869C and CDP1870C video interface system is designed for use in CDP1800-Series Microprocessor systems. It consists of the CDP1869C address and sound generator and the CDP1870C color video generator. These two LSI CMOS circuits interface directly with the CDP1802 and CDP1804A microprocessor/microcomputer families.

The VIS offers a variety of formats for the display and modification of data under software control, with either NTSC or PAL compatible output signals. The display device can be a video monitor or a standard TV receiver with an RF modulator. Composite sync, luminance, and chrominance are combined externally to form a single system-output. (With the RGB Bond-Out option [CDP1876C], Red, Green, and Blue outputs are provided to drive the CRT color amplifiers directly.) External sync inputs are also provided to allow picture overlays in existing TV chassis.

A sound output provides white noise and eight octaves of programmable tones. The output amplitude is variable in 16 steps from 0 V to 0.78 V_{DD}. This output is particularly useful in video game applications.

All are supplied in 40-lead hermetic dual-in-line ceramic packages (D suffix) and in 40-lead dual-in-line plastic packages (E suffix).



CDP1870C, CDP1876C
TERMINAL ASSIGNMENT

CDP1869C, CDP1870C, CDP1876C

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
Voltage referenced to V_{SS} Terminal)
CDP1869C, CDP1870C, CDP1876C ..... -0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ± 10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A=-40 to +60°C (PACKAGE TYPE E) ..... 500 mW
For T_A=+60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 12 mW/°C to 200 mW
For T_A=-55 to +100°C (PACKAGE TYPE D) ..... 500 mW
For T_A=+100 to 125°C (PACKAGE TYPE D) ..... Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
For T_A=FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE D ..... -55 to +125°C
PACKAGE TYPE E ..... -40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

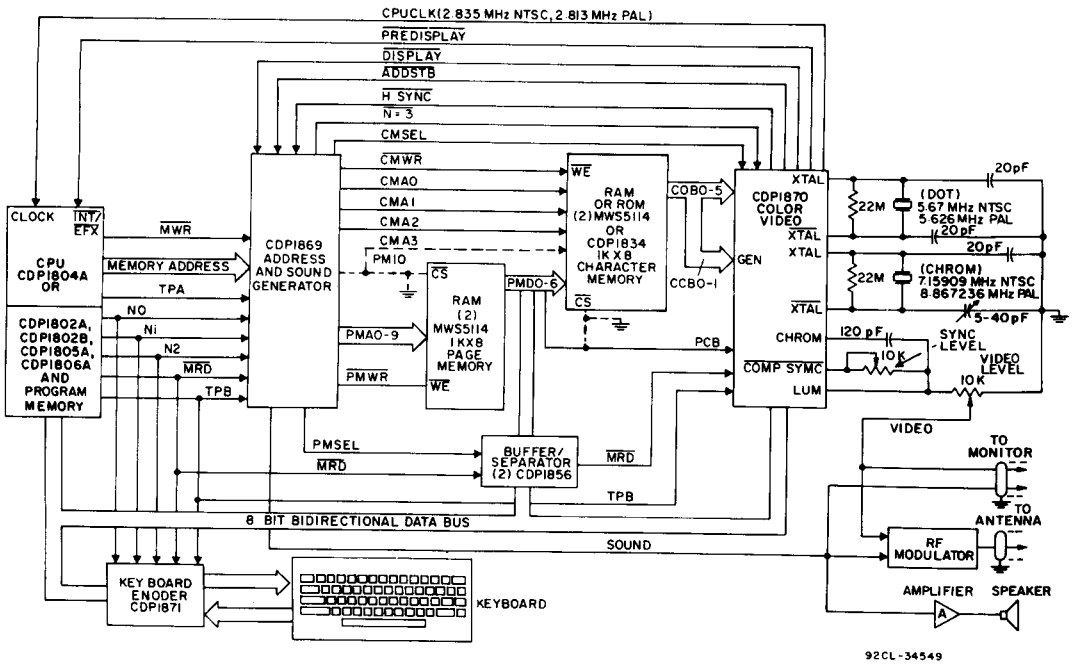


Fig. 1(a) - System diagram using CDP1869C and CDP1870C (Composite Outputs). See Fig. 1(b) using CDP1876C (RGB Bond Option Outputs).

CDP1869C, CDP1870C, CDP1876C

RECOMMENDED OPERATING CONDITIONS at T_A=25°C Unless Otherwise Specified

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC		V_{DD} (V)	LIMITS CDP1869C CDP1870C		UNITS
			Min.	Max.	
Supply-Voltage Range (At T_A=Full Package-Temperature Range)		—	4	6.5	V
Input Voltage Range		—	V_{SS}	V_{DD}	V
Input Signal Rise or Fall Time	t_r,t_f	5	—	5	μs
Clock Input Frequency (DOT)	f_{CL}	5	5.67 (5.626 PAL)		MHz

STATIC CHARACTERISTICS at T_A=−40 to +85°C, V_{DD} ± 5%, Except as noted

CHARACTERISTIC		CONDITIONS V_O (V)	V_{IN} (V)	V_{DD} (V)	LIMITS CDP1869C CDP1870C Min.	Typ.*	Max.	UNITS
Quiescent Device Current	I_{DD}	—	0, 5	5	—	100	500	μA
Output Low Drive (Sink) Current (Except $\overline{XTAL}$)	I_{OL}	0.4	0, 5	5	2	2.4	—	mA
$\overline{XTAL}$ Output	I_{OL}	0.4	5	5	75	150	—	μA
Output High Drive (Source) Current (Except $\overline{XTAL}$)	I_{OH}	4.6	0, 5	5	-1.6	-1.8	—	mA
$\overline{XTAL}$ Output	I_{OH}	4.6	0	5	-38	-75	—	μA
Output Voltage Low-Level	V_{OL}	—	0, 5	5	—	0	0.05	V
Output Voltage High Level	V_{OH}	—	0, 5	5	4.95	5	—	
Input Low Voltage	V_{IL}	0.5, 4.5	—	5	—	—	1.5	V
Input High Voltage	V_{IH}	0.5, 4.5	—	5	3.5	—	—	
Input Leakage Current	I_{IN}	Any Input	0, 5	5	—	±0.1	±1	μA
3-State Output Leakage Current	I_{OUT}	0, 5	0, 5	5	—	±0.2	±2	μA

*Typical values are for T_A=25°C.

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OPERATION

The CPU is clock independent of the VIS and is not involved in screen refresh, although a CPU clock output (½ DOT rate) is provided. At this clock rate 787 instructions (1080 for PAL) can be executed during non-display time. $\overline{\text{PRE-DISPLAY}}$ provides synchronization between the CPU and the VIS. Various system configurations for the CDP1869C/CDP1870C VIS are easiy implemented due to:

PAGE MEMORY
- 20 Characters x 12 Lines—Requires 240 Bytes of RAM
- 40 Characters x 24 Lines—Requires 960 Bytes of RAM

Character Memory—Can be RAM or ROM
- 32 Different (or any Combination of) Characters—Requires 256 Bytes (NTSC)
- 64 Different Characters—Requires 512 Bytes (NTSC)
- 128 Different Characters—Requires 1024 Bytes (NTSC)
- 256 Different Characters—Requires 2048 Bytes (NTSC)

Character memory requirements for PAL are the same as NTSC in most alphanumeric applications, but are 12.5% higher for graphics applications due to the larger character matrix (6x9) used for PAL.

Color

Color information may be stored in the two extra bits in each character byte (characters are only six dots wide), providing a choice of up to four colors for each character. With 128 different characters, only seven bits are required in the page memory and the eighth bit expands the choice of colors up to eight.

Graphics and Motion

Graphics and motion may be accomplished with two basic techniques. The first is by character selection. In this approach the desired graphics and motion symbols are stored in ROM or RAM. In a system where the character memory is all ROM, all the possible required positions within a character space are stored in the ROM. Graphics are accomplished by selecting the appropriate graphic character for each screen position. If the character memory is RAM then not all combinations need be stored in the character memory since they can be modified as required during operation. Motion in increments as small as one character space are possible.

A second technique may be used for more sophisticated motion, in which it is desired to move the displayed object in increments smaller than a normal character space. In this technique the object is moved within a character space using a bit-map approach, with object stored in the RAM character memory. The object is moved by rewriting the dots of the character space matrix, thereby continuously repositioning the object within its character space. As the object reaches the "edge" of its character space, that character space is moved and the object is repositioned. For example, if the object reaches the left edge of the character space, then that character space is moved to the left via the page memory and the object is rewritten on the right side of the character space.

Thus, the object moves smoothly across the screen one pixel at a time. Objects larger than one character space may also be moved using a similar technique.

Bit Map Operation

The VIS may be used to display data in a bit-map format, offering a high resolution display (up to 46,080 pixels) with up to 7,680 color blocks (8 colors). In this mode, the character memory addresses and the page memory addresses are used to address a single bit-map memory, instead of separate PAGE and CHARACTER memories. X-Y coordinates are located by implementing the appropriate software.

RGB Bond-Out Option (CDP1876C)—The CDP1870C may be ordered with an alternate pin-out to provide direct drive to the internal TV chassis red, green, and blue amplifiers. For the CDP1876C, the LUM, PAL CHROM, and NTSC CHROM outputs become the RED, BLUE, and GREEN outputs, respectively.

In the RGB mode of operation, the RF, IF, and color demodulator circuits of the TV chassis are bypassed and the composite sync, video, and color information are supplied directly to the appropriate chassis sections. Since no color subcarrier is used, the CHROM crystal is not needed, although the XTAL CHROM input must be term inated (Fig. 1(b)). The CDP1876C, RGB Bond-Out option, offers higher color resolution and simpler interfacing than the CDP1870C composite interface systems when used with direct internal TV chassis systems.

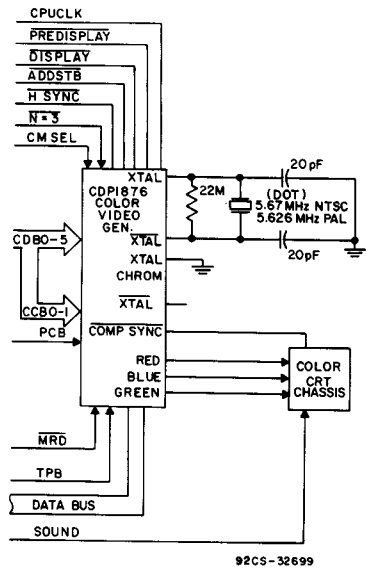

Fig. 1(b) - System diagram (same as that shown in Fig. 1(a) using CDP1876C (RGB Bond-Out Option).

CDP1869C - Address and Sound Generator—This circuit formats and controls sound, page-memory addressing, and character-memory addressing. This is accomplished by software instructions, data from the CPU, and hardware interaction with the CDP1870C timing signals.

OPERATION (Cont'd)

Control and multiplexing is determined by four command registers in the CDP1869C. A register-based output technique is used to transfer information from the CPU to the CDP1869C. This method allows 16 bits of data, from any of the 16 general-purpose registers of the CPU, to be loaded into the CDP1869C command registers with a single I/O instruction.

Data to the command registers are loaded from the 8 multiplexed address inputs (MA0/8-MA7/15). The high-order byte (MA8-MA15) is latched by the high-to-low transition of TPA, to provide up to 16 internal data bits. The I/O instruction N-Line Codes are latched by the high-to-low transition of TPB (Fig. 2).

OUT 4 Instruction—This instruction uses 15 data bits (MA0-MA14) to control the tone output function. (Bit 15 is unused, but must be programmed.) Bits MA0-MA3 control the tone output amplitude using an on-chip binary R/2R ladder network to produce a variable output amplitude in 16 steps. Bits MA4-MA6 control the tone output frequency range. Eight octaves are available (Table 1). Within each range the input frequency is divided by the N + 1 value on bits MA8-MA14, producing up to 128 different frequencies. This frequency is then divided by two in the output flip-flop, providing a square-wave signal that is gated on or off by bit MA7. A high on MA7 turns the tone output off. If both the tone and white noise are turned off, the sound output impedance is equal to 2.5R (R ≈ 1 to 2 kΩ).

OUT 5 Instruction—This instruction uses 13 data bits. (Bits MA1, MA2, and MA4 are unused and need not be programmed). The higher-order byte (MA8-MA15) is used to control the white noise output function. Bits MA8-MA11 control the white noise output amplitude using an on-chip binary R/2R ladder network to provide a variable output amplitude in 16 steps. Bits MA12-MA14 control the white noise output frequency range. Eight ranges are available (Table 2). The white noise output is gated on or off by bit MA15. The result is an explosion-type sound effect useful in TV game systems. A high on MA15 turns the white noise output off. If both the tone and white noise are on, a combined amplitude and frequency output results.

The lower-order byte of the OUT 5 Instruction (MA0-MA7) provides screen format control. The CMEM ACCESS MODE Bit (MA0) is used in conjunction with the OUT 6 Instruction to control the character memory READ/WRITE functions. A high on MA0 enables the character access mode.

The $\overline{\text{9-LINE}}$ bit (MA3) is used to select either 8-line or 9-line character matrix operation. A low on MA3 selects 9-line operation, which is normally used with PAL compatible signal timing.

The 16-LINE HI-RES bit (MA5) is used to define the vertical resolution of each character by selective control of the CMA3/PMA10 output. A low on MA5 defines each character as a 6x8 dot matrix and PMA10 is available to extend the page memory addressing. A high on MA5 defines each character as a 6x16 dot matrix by using CMA3 to extend the character memory line addressing. Each of the 16 character matrix lines may contain different data. The 16-LINE HI-RES bit (MA5) must be low if the DOUBLE-PAGE bit (MA6) is high. (During PAL operation, where each character is normally a 6x9 dot matrix, the 16-LINE HI-RES mode is not available and MA5 should be programmed low).

The DOUBLE-PAGE bit (MA6) is used to select the function of the CMA3/PMA10 output. A low on MA6 selects the single-page mode, in which the page memory can be a maximum of 960 bytes. In this mode, the CMA3/PMA10 output is available as CMA3 to expand the character-memory addressing if the 16-LINE HI-RES bit is high. A high on MA6 selects the double-page mode.

In which the page-memory can be a maximum of 1920 bytes. In this mode, the CMA3/PMA10 output is used as PMA10 to expand the page-memory addressing (the 16-LINE HI-RES bit must be low).

Various roll and scroll operations (Table 8) are possible as described under the OUT 7 Instruction.

In PAL systems, the double-page function is normally useful only for certain text and graphic applications, since the CMA3/PMA10 output would have to be used as PMA10 and would not be available as CMA3 to address the ninth line in the normal 9-line PAL character matrix. Although these double-page display combinations are not shown in Table 8 under the PAL formats, they are possible with the restriction that character line 0 in the character matrix is repeated at character line 8.

The FRES VERT bit (MA7) controls the full screen vertical resolution of the display. A high on MA7 sets the maximum resolution to 24 rows of characters. A low on MA7 sets the maximum resolution of 12 rows of characters, with each of the 8 adjacent lines within a character displayed twice.

All valid vertical and horizontal display format combinations are shown in Table 8, along with the page and character-memory requirements. Fig. 9 shows the relative character matrix sizes.

OUT 6 Instruction—As shown in Fig. 2, the page-memory outputs (PMA0-PMA10) and the character-memory outputs (CMA0-CMA3) originate from two sources, with four modes of operation:

1. **DISPLAY REFRESH MODE**—This mode of operation provides automatic screen refreshing and has priority over the other modes during the display time. The internal refresh address counter is incremented on each high-to-low transition of $\overline{\text{ADDSTB}}$, during display time, and its outputs are multiplexed via the internal RCA0-RCA3 and RPA0-RPA10 bus to the page and character memory outputs (CMA0-CMA3, PMA0-PMA10).
2. **PAGE-MEMORY ACCESS MODE**—This mode of operation is used to read or write data in the page-memory. During non-display time, with the CMEM ACCESS MODE bit (OUT 5 Instruction) reset (low), the address inputs (MA0/8-MA7/15) from CPU are transferred directly through the page-memory address register and are multiplexed via the internal MA0-MA10/PRA0-PRA10 Bus to the page-memory outputs (PMA0-PMA10).

   The page-memory functions as an extension of the CPU memory in this mode, when it is selected at address space $F800_{16}$-$FFFF_{16}$, and the OUT 6 Instruction is not required. The PMWR and PMSEL outputs are also enabled at this time. As shown in Fig. 1, the PMWR output is connected to the WRITE input of the page-memory and the PMSEL output is connected to the SELECT input of the data bus buffer/separator, which prevents CPU bus contention.
3. **CHARACTER-MEMORY ACCESS MODE (WITH DISPLAY DISTURB)**—This mode of operation is used to read or write data in the character-memory, when the user is not concerned with the possibility of the current display data being disturbed. (NOTE: This mode is useful only if RAM exists in the entire 1024-byte

CDP1869C, CDP1870C, CDP1876C

OPERATION (Cont'd)

address space in the SINGLE-PAGE MODE or in the entire 2048-byte address space in the DOUBLE-PAGE MODE.

When the CMEM ACCESS MODE bit is set high, the address inputs (MA0/8-MA7/15) from the CPU that are present during the OUT 5 Instruction are latched in the page-memory address register via the internal MA0-MA10 bus and are multiplexed to the page-memory outputs (PMA0-PMA10), during non-display time. The data in the page-memory address register, which remains latched until an OUT 6 Instruction is executed or until the CMEM ACCESS MODE bit is reset, provides a stable address to the page memory, which essentially reduces it to a single location. This location is read from or written to by selecting the page-memory at address space $F800_{16}$-$FFFF_{16}$, with the data supplied over the CPU 8-bit data bus. (The actual location within $F800_{16}$-$FFFF_{16}$ is unimportant since the page-memory address is already latched.) The OUT 6 Instruction is not required in this mode.

The page-memory data outputs (PMD0-PMD7) provide the character-memory "Column" addresses, which select a particular character. Since the page-memory address location is latched, the address inputs (MA0/8-MA7/15) from the CPU are available to access the character-memory via the internal MA0-3 bus, which is multiplexed to the character-memory outputs (CMA0-CMA3) during non-display time. The CMA0-CMA3 outputs provide the character-memory "Row" addresses, which select a particular line of dots within a character. The character-memory is selected at address space $F400_{16}$-$F7FF_{16}$. Although 1024 bytes of address space is decoded, only 8 memory locations (16 locations in the 16-LINE HI-RES mode) are required and the character-memory addressing will wrap (repeat) for the rest of the 1K address space. The $\overline{CMWR}$ output, which is connected to the $\overline{WRITE}$ input of the character-memory, and the CMSEL output, which is connected to the CDP1870C CMSEL input, are also enabled at this time. The data to be read from or written to the character-memory is multiplexed through the CDP-1870C internal 8-bit data bus via the BUS0-BUS7 inputs from the CPU.

This mode of operation is useful to initially load the character-set into the RAM character-memory since fewer program instructions are required than with the following Character-Memory Access Mode.

4. **CHARACTER-MEMORY ACCESS MODE (Without Display Disturb)**—This mode is used to read or write data in the character-memory, without disturbing the current display data. Operation is the same as the Character-Memory Access Mode (with Display Disturb), with the following exceptions.

   After the CMEM ACCESS MODE bit is set high, the OUT 6 Instruction is used to load the page-memory address register with the address input (MA0/8-MA7/15) from the CPU via the internal MA0-MA10 bus. These 11 data bits (PMA0-PMA10) are multiplexed via the internal MA0-MA10/PRA0-PRA10 bus to the page-memory outputs (PMA0-PMA10), during non-display time. The address remains latched until a new OUT 6 Instruction is executed, to latch new data, or until the CMEM ACCESS MODE bit is reset.

   This mode provides a means to select a page-memory location that is not part of the current display or a location that is outside of the display window in the page-memory, rather than a random location, as in MODE 3 (above). Reading and writing to the character-memory remains the same as in MODE 3.

In both MODE 3 and MODE 4, the character-memory access mode is disabled by programming the CMEM ACCESS MODE bit low (reset), using the OUT 5 Instruction. When accessing the page-memory, if the DOUBLE-PAGE bit is not set (low), PMA10 is not used and does not have to be programmed. When accessing the character-memory, during double-page operation (DOUBLE-PAGE bit set high), CMA3 is not used and does not have to be programmed.

OUT 7 Instruction—This instruction uses 9 data bits to load the home-address register bits (HMA2-HMA10) via the internal MA2-MA10 bus. The home-address register outputs (HMA2-HMA10) are transferred to the refresh-address counter at the end of each display frame. The home address determines which row of characters from the page-memory is used to start the display at the top left-hand corner of the screen. In the FULL RES HORZ MODE (CDP1870), the home address must be an even multiple of 40. In the HALF RES HORZ MODE (CDP1870C), the home address must be an even multiple of 20. Therefore, the HMA0 and HMA1 bits are automatically set low internally and do not have to be programmed.

The OUT 7 Instruction is used to define a display window which can be moved through multiple pages of display RAM in various roll and scroll operations. As shown in Table 8, the total characters displayed per frame can be less than the maximum display page-memory size. The OUT 7 Instruction is used to display the remaining page-memory up to the maximum display page-memory size using a scroll technique.

For example, using line 4 in Table 8, 480 characters will be displayed as 24 rows of 20 characters. However, the maximum display page-memory size is 960. If the home address was initially set to zero, the last row of characters on the screen will begin at page-memory location 460. To display the next row of characters in the remaining 480 locations of page memory, an OUT 7 Instruction is executed with the home address set at $20(14_{16})$. The last row of characters now displayed will begin at location 480, the start of the second 480 locations of page-memory. This sequence can be continued with successive multiples of 20 loaded into the home-address register up to the maximum display page-memory size minus 20 (940). The display window appears to scroll through the page-memory with old data shifted off the top of the screen, but retained in page-memory, as new data is presented at the bottom of the screen. During this sequence when the final page-memory address count (as determined by the maximum display page-memory size) is reached, prior to the end of the display window, zero is loaded into the refresh address counter and the next row of characters displayed will be the first row in page-memory. Thus, the display will appear to have rolled around from the beginning of the page-memory to the bottom of the screen.

The roll operation is automatic when the final page-memory address count is reached prior to the end of the display window. The scroll operation occurs when the OUT 7 Instruction is executed, but is automatic in that the display window data does not have to be rewritten in the page-memory as the display window changes. The home-address modes in Table 8 indicate which operations (scroll, roll) are possible with each format combination.

OPERATION (Cont'd)

CDP1870 - Color Video Generator

This circuit formats and controls the TV sync, video, and color information. It also provides synchronization timing to the CDP1869C and the CPU. The character-memory data I/O lines are multiplexed through the CDP1870C to the CPU 8-bit bidirectional data bus. This is accomplished by software instructions, data from the CPU, and hardware interaction with the CDP1869C timing signals. Control and multiplexing is determined by a single internal command register, which is loaded by a CPU I/O instruction. Data to the command register are loaded from the 8-bit bidirectional data bus, which is latched by the high-to-low transition of TPB when the $\overline{MRD}$ and the $\overline{N=3}$ inputs are at a logic 0 (Fig. 3).

OUT 3 Instruction—This instruction uses 8 data bits to control the internal format and timing functions. The BKG GREEN, BKG BLUE, BKG RED bits (BUS0-BUS2) provide a binary selection of eight screen background colors, as shown in Table 5. The CFC bit (BUS 3) selects the color format control function (Table 4). When the CFC bit is low, the background luminance and chrominance are selected by the BKG GREEN, BKG BLUE, and BKG RED control bits. The dot chrominance and luminance are selected by the CCB0, CCB1, and PCB inputs. Operation is the same when the CFC bit is high, except that the dot chrominance is now selected by the BKG GREEN, BKG BLUE, and BKG RED control bits to provide a tone-on-tone color display. The DISP OFF bit (BUS 4) is used to turn the screen display off. When the DISP-OFF bit is high, the PAL CHROM, NTSC CHROM, and LUM outputs are held at the background color and the $\overline{ADDSTB}$, $\overline{PREDISPLAY}$, and $\overline{DISPLAY}$ outputs are held at a high level. However, the $\overline{COMP\text{-}SYNC}$, $\overline{HSYNC}$, and $\overline{CPUCLK}$ outputs continue to supply synchronization timing. This display-off condition allows the CPU to access the VIS, page memory, and character memory asynchronously. Any change in this bit is only recognized at the end of the frame. The COLB0 and COLB1 bits (BUS5, BUS 6) provide a binary selection of 3 character-color control modes, as shown in Table 3. These 3 modes control which color bit inputs (CCB0, CCB1, PCB) select a particular character color (Table 5). The FRES HORZ bit (BUS 7) controls the full screen horizontal resolution of the display. A high on BUS 7 sets the maximum resolution to 40 characters per row. The 6 dots per character are shifted out of the CDP1870C parallel/serial shift register to the screen at the dot-clock rate (Fig. 4(a)). The MSB is shifted out first (CDB5=MSB). A low on BUS 7 sets the maximum resolution to 20 characters per row. The 6 dots per character are shifted out to the screen at ½ the dot-clock rate, thereby, doubling the dot width. All valid display format combinations are shown in Table 8.

The CDP1870C uses two separate input frequencies. On-chip oscillators are provided, requiring only external crystal circuits. One oscillator circuit provides the dot-clock frequency, from which SYNC and $\overline{ADDSTB}$ timing is derived. The DOT frequency, divided by two, provides a CPU CLK output. The other oscillator circuit provides the color reference and chrominance frequencies. The NTSC CHROM, PALCHROM, and LUM outputs include on-chip summing resistors to reduce the external components required. The outputs are connected to the $\overline{COMPSYNC}$ output to provide a single video signal, which may be used to drive a video monitor directly or a standard TV receiver through an RF modulator circuit.

(With the RGB Bond-Out option, CDP1876C, the color crystal is not used and the LUM, NTSC CHROM, and PAL CHROM become the RED, BLUE, and GREEN outputs, respectively.)

The $\overline{EVS}$ and $\overline{EHS}$ inputs may be used to sync the VIS from an existing TV chassis to provide picture overlay and teletext operations. When the VIS is used in this mode of operation, the DOT XTAL is replaced with a simple external LC oscillator circuit that is gated on with the $\overline{EHS}$ signal.

The VIS does not provide for an external system reset. All command and format instructions must be executed before proper operation is initiated. Command and format information may be changed at any time (asynchronous) with respect to screen refresh, although certain format changes will not be executed until the end of a display frame. The CDP1869C and CDP1870C, CDP1876C command registers are write-only registers and may not be read by CPU.

The page and character memory READ/WRITE operations may only be performed during non-display time, with the $\overline{PREDISPLAY}$ or $\overline{DISPLAY}$ outputs used to provide synchronization between the CPU and the VIS.

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OPERATION (Cont'd)

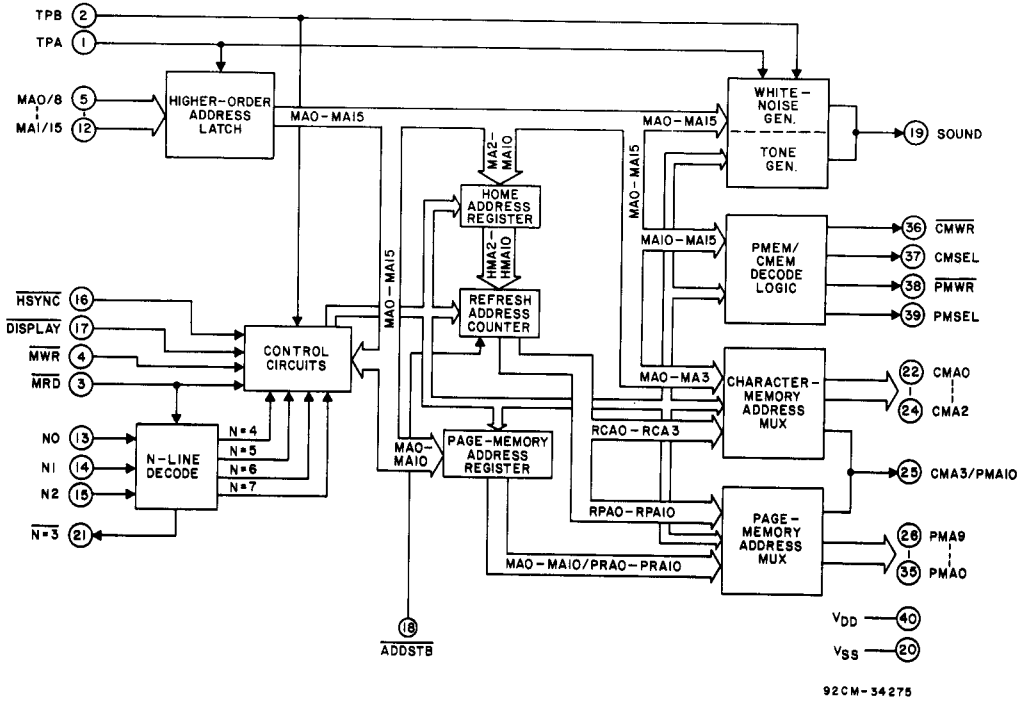


Fig. 2 - CDP1869C block diagram.

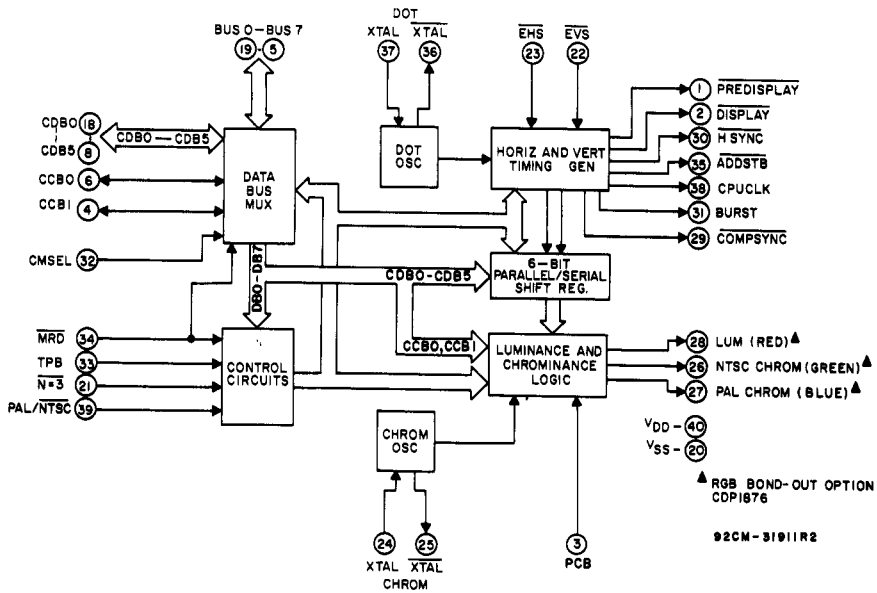


Fig. 3 - CDP1870C and CDP1876C block diagram.

CDP1869C, CDP1870C, CDP1876C

FUNCTIONAL DESCRIPTION OF CDP1869C TERMINALS

TPA (Input):
An active high pulse from the CPU that occurs once in each machine cycle. The trailing edge of TPA is used to latch the higher-order byte of the 16-bit memory address. TPA is also one of the frequency generator input clocks.

TPB (Input):
An active high pulse from the CPU that occurs once in each machine cycle, following TPA. It is used to latch the various internal command registers. TPB is also one of the frequency generator input clocks.

$\overline{MRD}$ (Input):
An active low pulse from the CPU, indicating a memory read cycle. It is used to provide various latch and control functions.

$\overline{MWR}$ (Input):
An active low pulse from the CPU, appearing in a memory write cycle after the address lines have stabilized. It is used to gate various latch and control functions.

MA0/8-MA7/15 (Inputs):
The 8 memory address lines. The higher-order byte of a 16-bit CDP1802 or CDP1804 memory address appears on the memory address lines MA0-MA7 first, and is latched by the high-to-low transition of TPA. These 8 lines serve a dual purpose. They can be used to provide direct address information to the page or character memories or they can be used to provide data to the command registers.

N0 to N2 (Inputs):
These lines are used to issue command codes during an I/O instruction from the CPU. Their state is the same as the corresponding bits in the CPU N register. The three N bits are internally decoded with $\overline{MRD}$ to provide various latch and control functions.

$\overline{HSYNC}$ (Input):
Active low horizontal sync signal from the CDP1870C. This signal provides synchronization between the CDP1869C and the CDP1870C timing signals.

$\overline{DISPLAY}$ (Input):
Active low signal from the CDP1870C that indicates that a screen refresh is in progress. This signal provides synchronization between the CDP1869C and the CDP1870C timing signals.

$\overline{ADDSTB}$ (Input):
Active low pulses from the CDP1870C that provide page and character-memory address clock timing. $\overline{ADDSTB}$=DOT clock ÷ 6 (40-character display). $\overline{ADDSTB}$=DOT clock ÷ 12 (20-character display). Only 40 or 20 pulses are generated per horizontal line, and no pulses occur during non-display time.

SOUND (Output):
This output provides two types of frequency signals that can be selected either individually or in combination. The first type provides single-frequency tones in 8 selectable ranges, with 128 different tones in each range (Table 1). The second type provides a white-noise output in 8 selectable ranges, with the white noise consisting of all 128 tones of each range (Table 2). Both tone and white-noise outputs are programmable from 0 volts to 0.78 V_{DD} in 16 steps.

V_{SS}:
Ground

$\overline{N=3}$ (Output):
Active low output from the internally decoded N bits that is normally connected to the CDP1870C. It is used to select the CDP1870C command register.

CMA0-CMA2—CHARACTER-MEMORY ADDRESS (Outputs):
The character-memory address outputs. These three outputs function as character-line selects. During a screen refresh the address data are provided by an internal counter, which is controlled by $\overline{HSYNC}$, to provide character information in one of eight formats (Fig. 9). During non-refresh periods the address data are provided by the MA0-MA2 inputs as an extension of the CPU memory.

CMA3/PMA10 (Output):
This output signal serves a dual purpose. In the 16-LINE HI-RES character mode (command bit 5=1) this output represents CMA3 and its function is identical to the CMA0-CMA2 outputs. In the 9-LINE mode (command bit 3=0), this signal represents CMA3 in both the low-and-high-resolution modes (command bit 5=0 or 1), and is used to select the ninth line of the character matrix. In the double-page mode (command bit 6=1), this output represents PMA10 and its function is identical to the PMA0-PMA9 outputs.

PMA0-PMA9—PAGE-MEMORY ADDRESS (Outputs):
These ten page-memory address outputs access the page-memory data (PMD0-6), 7 bits of which are used to address the character memory. The spare bit (PCB) may be used to expand the color information. During a screen refresh the address data are provided by an internal counter, which is controlled by ADDSTB to provide page-memory information in one of four formats (Table 8). During non-refresh periods the address data are provided by the MA0/8-MA9/15 inputs as an extension of the CPU memory.

$\overline{CMWR}$—CHARACTER-MEMORY WRITE (Output):
$\overline{CMWR}$ is an active low output signal that is connected to the WRITE input of the character memory. This output provides a delayed $\overline{MWR}$ pulse during non-display periods, when the character memory is selected by the MA10-MA15 inputs (F400-F7FF).

CMSEL—CHARACTER-MEMORY SELECT (Output):
CMSEL is an active high output signal that is connected to the CDP1870C CMSEL input. This output provides a delayed positive pulse during non-display periods, when the character memory is selected by the MA10-MA15 inputs (F400-F7FF) and $\overline{MRD}$ or $\overline{MWR}$ is low.

$\overline{PMWR}$—PAGE-MEMORY WRITE (Output):
$\overline{PMWR}$ is an active low output signal that is connected to the WRITE input of the page memory. This output provides a delayed MWR pulse during non-display periods, when the page memory is selected by the MA11-MA15 inputs (F800FFFF).

PMSEL—PAGE-MEMORY SELECT (Output):
PMSEL is an active high output signal that is connected to an external bus separator. This output provides a delayed positive chip-enable pulse during non-display periods, when the page memory is selected by the MA11-MA15 inputs (F800-FFFF) and $\overline{MRD}$ or $\overline{MWR}$ is low.

V_{DD}
Positive supply voltage.

CDP1869C, CDP1870C, CDP1876C

FUNCTIONAL DESCRIPTION OF CDP1870C TERMINALS

$\overline{\text{PREDISPLAY}}$ (Output):
An output signal that goes low one horizontal line before the start of the display field. This output may be connected to the CPU to provide advance warning of a refresh operation.

$\overline{\text{DISPLAY}}$ (Output):
An output signal that is low during the display field. This signal is connected to the CDP1869C to provide synchronization timing during a screen refresh.

PCB—PAGE-MEMORY COLOR BIT (Input):
The page-memory color bit expands the character color information to 3 bits (8 colors, Table 3). It may also be used to expand the character-memory addressing when only 4 dot colors are required.

CCB0, CCB1—CHARACTER-MEMORY COLOR BITS (I/O):
The character-memory color bit inputs provide character color data. These two inputs select one of four colors (Table 3). When the CMSEL input is high during non-display periods, CCB0 and CCB1 are multiplexed to the CPU data bus (BUS 6, BUS 7) to provide character memory READ/WRITE data.

CDB0-CDB5—CHARACTER-MEMORY DATA BITS (I/O):
The character-memory data bit inputs provide character data during screen refresh periods. When the CMSEL input is high during non-display periods, CDB0-CDB5 are multiplexed to the CPU data bus (BUS0-BUS5) to provide character memory READ/WRITE data.

BUS 0-BUS 7 (I/O):
The 8-bit bidirectional data bus that is normally connected directly to the CPU. During non-display periods, these I/O lines serve a dual function. If the CMSEL input is high, BUS 0-BUS 7 provide character-memory READ/WRITE data. If the $\overline{\text{N=3}}$ input (OUT 3 instruction) is low, BUS 0-BUS 7 provide input data to the CDP1870C command register. These data are latched on the high-to-low transition of TPB when $\overline{\text{MRD}}$ is low.

V_{SS}:
Ground.

$\overline{\text{N=3}}$ (Input):
An input signal from the CDP1869C that is low during an OUT 3 instruction from the CPU. This input is used to select the CDP1870C command register.

$\overline{\text{EVS}}$, $\overline{\text{EHS}}$—EXTERNAL VERTICAL SIGNAL, EXTERNAL HORIZONTAL SIGNAL (Inputs):
The active low external vertical and horizontal sync signals synchronize the VIS to an external system. When not used, these inputs must be connected high.

XTAL (Input), $\overline{\text{XTAL}}$ (Output)—CHROM COLOR CHROMINANCE CRYSTAL
The color chrominance crystal inputs are normally connected to a 7.15909-MHz crystal (NTSC) or an 8.867236-MHz crystal (PAL) to provide a burst and color data input clock. The XTAL input may be connected to an external generator. (With the RGB Bond-Out option, CDP1876C, the chrominance crystal is not required although the XTAL input must be terminated.)

NTSC CHROM (Output):
The United States National Television System Committee (NTSC), standard color video output signal. This output provides a composite signal containing chrominance information and 11 cycles of the color reference signal. (With the RGB Bond-Out option, CDP1876C, this output provides the GREEN drive.)

PAL CHROM (Output):
The European Phase Alternation Line (PAL), standard color video output signal. This output provides a composite signal containing chrominance information and 14 cycles of the color reference signal. (With the RGB Bond-Out option, CDP1876C, this output provides the BLUE drive.)

LUM—LUMINANCE (Output):
The luminance output signal provides video dot brightness information. (With the RGB Bond-Out option, CDP1876C, this output provides the RED drive.)

$\overline{\text{COMPSYNC}}$ (Output):
The composite TV synchronization signal provides active low pulses at the line (horizontal) and frame (vertical) rates.

$\overline{\text{HSYNC}}$ (Output):
The horizontal synchronization signal provides an active low pulse at the TV line rate. It is connected to the CDP1869C to control timing synchronization.

BURST (Output):
This output provides an active high pulse following the horizontal sync pulse. It indicates when the color reference signal is being output, however, it is not required for normal operation.

CMSEL—CHARACTER-MEMORY SELECT (Input):
The character-memory select input, from the CDP1869C, indicates a character-memory READ/WRITE operation. When CMSEL is high, the 8-bit bidirectional data bus from the CPU is multiplexed to the CCB0, CCB1, and CDB0-CDB5 I/O lines to provide character-memory data. This input is active only during non-display periods.

TPB (Input):
An active high pulse from the CPU that occurs once in each machine cycle, following the TPA pulse. This input pulse is used to latch the CDP1870C command register data on the high-to-low transition, when the $\overline{\text{N=3}}$ and $\overline{\text{MRD}}$ inputs are low.

$\overline{\text{MRD}}$—MEMORY READ (Input):
An active low pulse from the CPU indicating a memory READ cycle. This signal enables the command register clock and selects the direction of data flow in the data bus multiplexer. When this signal is low, a CPU READ operation is in progress.

$\overline{\text{ADDSTB}}$—MEMORY ADDRESS STROBE (Output):
The $\overline{\text{ADDSTB}}$ output signal is connected to the CDP1869C to provide the page and character-memory address counter clock during display time.

XTAL (Input), $\overline{\text{XTAL}}$ (Output)—DOT CRYSTAL:
The dot crystal inputs are normally connected to a 5.67-MHz crystal (NTSC) or a 5.626-MHz crystal (PAL) that is used to provide horizontal, vertical, and control timing. The XTAL input may be connected to an external generator.

CPUCLK—CLOCK (Output):
A clock output equal to ½ the DOT frequency. It may be connected to the CPU CLOCK input terminal. At this frequency, 2947 instructions per frame are available, with 787 instructions occurring during the non-display period.

PAL/$\overline{\text{NTSC}}$ (Input):
This input selects either PAL or NTSC operation. When the PAL/$\overline{\text{NTSC}}$ input is high, the VIS provides PAL compatible output signals. When the PAL/$\overline{\text{NTSC}}$ input is low, the VIS provides NTSC compatible output signals.

V_{DD}:
Positive supply voltage.

TABLE 1 TONE RANGE SELECT

TONE FREQ SEL2	TONE FREQ SEL1	TONE FREQ SEL0	INPUT FREQUENCY (kHz)	CPU CLK *
0	0	0	5.5371093	÷ 512
0	0	1	11.074218	÷ 256
0	1	0	22.148437	÷ 128
0	1	1	44.296875	÷ 64
1	0	0	88.593750	÷ 32
1	0	1	177.18750	÷ 16
1	1	0	354.37500	÷ 8
1	1	1	708.75000	÷ 4

* CPUCLK = 2.835 MHz

TABLE 2 WHITE NOISE RANGE SELECT

WN FREQ SEL2	WN FREQ SEL1	WN FREQ SEL0	TOP-OF-RANGE FREQUENCY (kHz)	CPU CLK *
0	0	0	0.69213867	÷ 4096
0	0	1	1.3842773	÷ 2048
0	1	0	2.7685546	÷ 1024
0	1	1	5.5371093	÷ 512
1	0	0	11.074218	÷ 256
1	0	1	22.148437	÷ 128
1	1	0	44.296875	÷ 64
1	1	1	88.593750	÷ 32

* CPUCLK = 2.835 MHz

TABLE 3 CHARACTER COLOR CONTROL

COLB1	COLB0	RED	BLUE	GREEN
0	0	CCB0	CCB1	PCB
0	1	CCB0	PCB	CCB1
1	0	PCB	CCB0	CCB1
1	1	PCB	CCB0	CCB1

TABLE 4 COLOR FORMAT CONTROL

CFC	BKG CHR	BKG LUM	DOT CHR	DOT LUM
0	BKG R,B,G	BKG R,B,G	CCB0/CCB1 PCB	CCB0/CCB1 PCB
1	BKG R,B,G	BKG R,B,G,	BKG R,B,G	CCB0/CCB1 PCB

TABLE 5 COLOR SELECT

CHAR OR BKG COLOR DATA BITS			OUTPUT COLOR	% OF MAX LUMINANCE
RED	BLUE	GREEN		
0	0	0	BLACK	0
0	0	1	GREEN	59
0	1	0	BLUE	11
0	1	1	CYAN	70
1	0	0	RED	30
1	0	1	YELLOW	89
1	1	0	MAGENTA	41
1	1	1	WHITE	100

CDP1869C, CDP1870C, CDP1876C

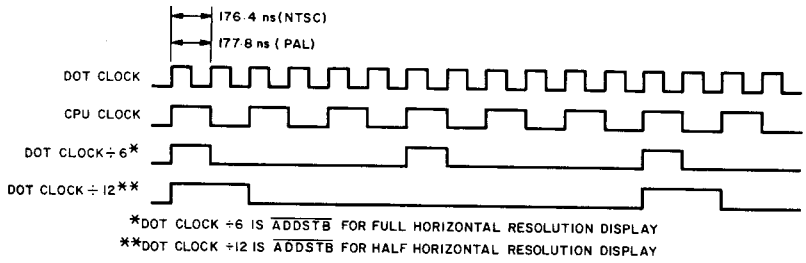


Fig. 4(a) - ADDSTB timing diagram.

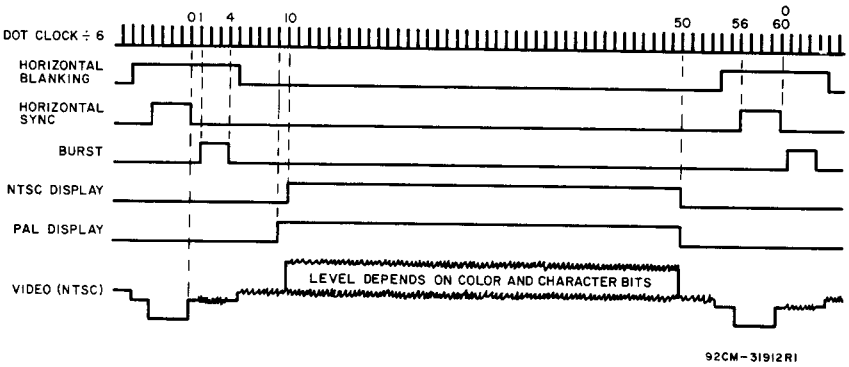


Fig. 4(b) - Horizontal timing diagram.

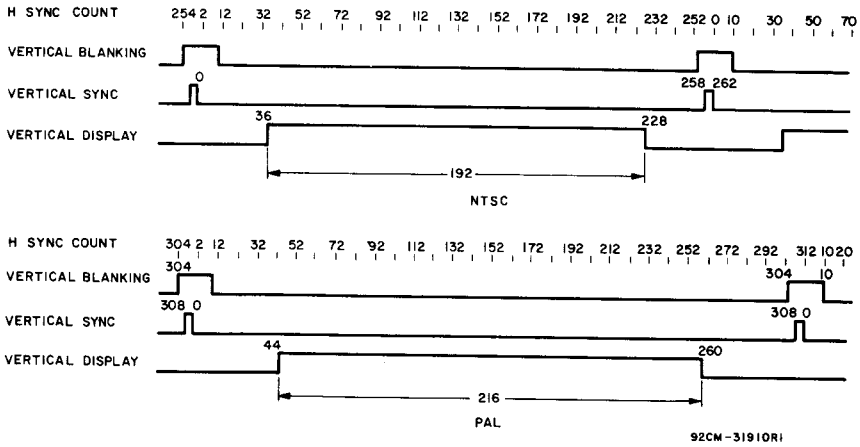


Fig. 4(c) - Vertical timing diagram.

CDP1869C, CDP1870C, CDP1876C

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A=-40° to 85°C, C_L=50 pF
V_{DD} ± 5%, Except as noted

CHARACTERISTIC		V_{DD} (V)	LIMITS CDP1869C CDP1870C, CDP1876C Min.	Typ.*	Max.	UNITS
CPU Interface Timing - See Fig. 5						
Address Set-up Time From TPA	t_{SU}	5	—	50	—	ns
Address Hold Time From TPA	t_H	5	—	50	—	
Page Memory Address Delay From TPA	t_{PMD}	5	—	380	—	
Character Memory Address Delay From TPA	t_{CMD}	5	—	380	—	
Page Memory Select Delay From TPA	t_{PSD}	5	—	320	—	
Character Memory Select Delay From TPA	t_{CSD}	5	—	350	—	
Page Memory Write Delay From $\overline{MWR}$	t_{PWHL}	5	—	120	—	
	t_{PWLH}	5	—	120	—	
Character Memory Write Delay From $\overline{MWR}$	t_{CWHL}	5	—	120	—	
	t_{CWLH}	5	—	120	—	
MA0-MA7 Set-up Time From TPB	t_{BSU}	5	—	30	—	

*Typical values are for T_A=25°C and nominal V_{DD}.

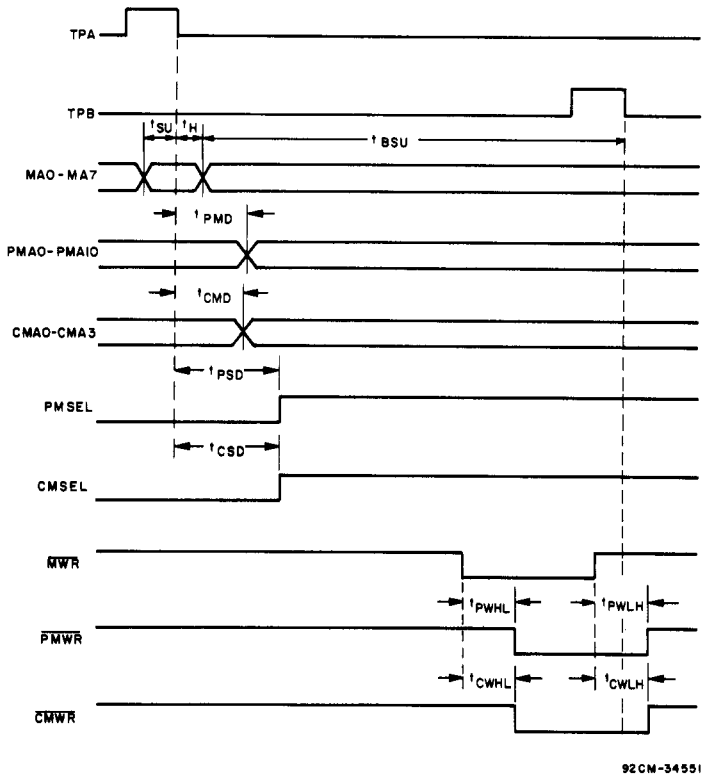


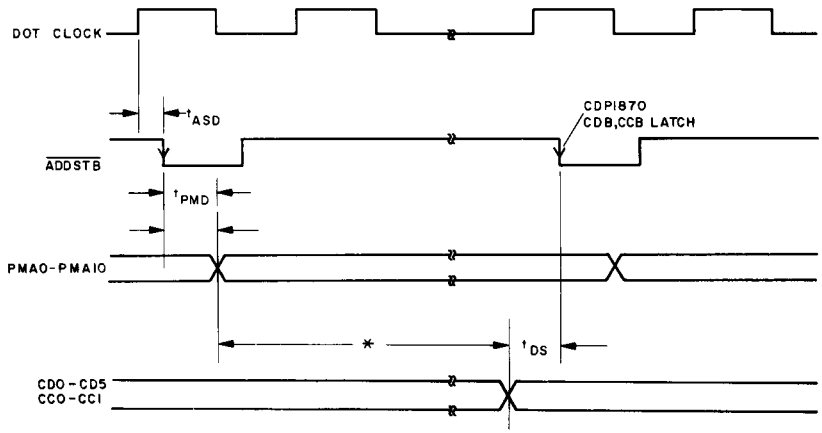
Fig. 5 - CPU interface timing waveforms.

CDP1869C, CDP1870C, CDP1876C

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A=-40° to 85°C, C_L=50 pF
V_{DD} ± 5%, Except as noted

CHARACTERISTIC		V_{DD} (V)	LIMITS CDP1869C CDP1870C, CDP1876C Min.	Typ.*	Max.	UNITS
Refresh Memory Timing - See Fig. 6						
$\overline{\text{ADDSTB}}$ Delay Time From DOT Clock	t_{ASD}	5	—	215	—	ns
Page Memory Address Delay From $\overline{\text{ADDSTB}}$	t_{PMD}	5	—	300	—	ns
Character Data and Color Bits Set-up Time	t_{DS}	5	—	250	—	ns

*Typical values are for T_A=25°C and nominal V_{DD}.



* AVAILABLE PAGE AND CHARACTER MEMORY ACCESS TIME
FULL HORZ RESOLUTION=(DOT CLK x 6)-t_{PMD}-t_{DS}
HALF HORZ RESOLUTION=(DOT CLK x 12)-t_{PMD}-t_{DS}
TYPICAL AVAILABLE ACCESS TIME (NTSC, 5 V):
(176.4 x 6)-300-250=508.4 ns (FULL RES.)
(176.4 x 12)-300-250=1.117 μs (HALF RES.)

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Fig. 6 - Refresh memory timing waveforms.

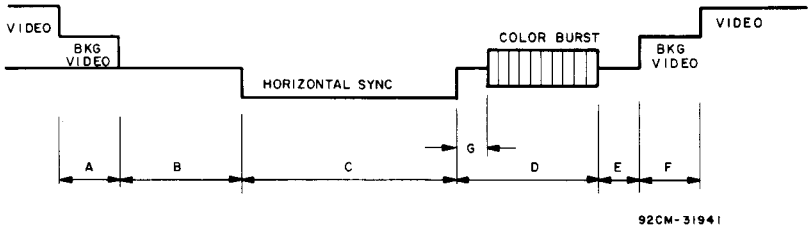

Fig. 7 - Horizontal sync timing (see Table 6).

TABLE 6 HORIZONTAL TIMING STANDARDS

DIAGRAM	NTSC STANDARD	NTSC VIS 5.67 MHz XTAL	PAL STANDARD	PAL VIS 5.626 MHz XTAL
A	NA	3.7 μs	NA	4.8 μs
B	0.02H MIN 1.27 μs MIN	2.12 μs	1.55 μs	2.12 μs
C	0.07H-.08H 4.45-5.08 μs	4.23 μs	4.7 μs	4.27 μs
D	0.045H-0.55H 8-11 CYCLES 3.58 MHz	3.174 μs 11 CYCLES 3.58 MHz	11 CYCLES 4.433 MHz	3.199μs 14 CYCLES 4.433 MHz
E	0.02H MIN 1.27 μs MIN	1.41 μs	2.07μs	1.07 μs
F	NA	6 μs	NA	4.98 μs
G	0.006H 0.381 μs	0.352 μs	0.70 μs	0.355 μs
HORIZONTAL FREQUENCY	15,734.264 Hz (COLOR) 15,750 Hz (B&W)	15,750 Hz	15,625 Hz	15,628 Hz

H = 63.5 μs NA = NOT APPLICABLE

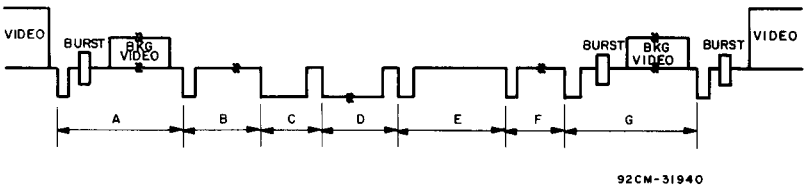

Fig. 8 - Vertical sync timing (see Table 7).

TABLE 7 VERTICAL TIMING STANDARDS

DIAGRAM	NTSC STANDARD	NTSC VIS 5.67 MHz XTAL	PAL STANDARD	PAL VIS 5.626 MHz XTAL
A	NA	26H	NA	44H
B*	3H	4H	2.5H	4H
C	1H	1H	1H	1H
D	2H	3H	1.5H	3H
E	1H	1H	1H	1H
F	2H	9H	19H	9H
G	9H-12H	26H	NA	34H
HORIZONTAL PERIOD (H)	63.5 μs	63.5 μs	64 μs	64 μs
VERTICAL FREQUENCY	59.94 Hz (COLOR) 60 Hz (B&W)	60.115 Hz	50 Hz	50.09 Hz

* = NO BKG VIDEO, NO BURST NA = NOT APPLICABLE

CDP1869C, CDP1870C, CDP1876C

Table 8
DISPLAY FORMAT COMBINATIONS (FULL COLOR SYSTEM)

COMMAND DATA								
CDP1870C FRES HORZ	CDP1869C FRES VERT	CDP1869C DOUBLE PAGE	CDP1869C 16-LINE HI-RES	CDP1869C 9-LINE	CHAR DISPLAY MATRIX	CHAR/ ROW	CHAR ROWS/ FRAME	TOTAL CHAR/ FRAME
0	0	0	0	1	6 x 8	20	12	240
0	0	0	1	1	6 x 16	20	6	120
0	0	1	0	1	6 x 8	20	12	240
0	1	0	0	1	6 x 8	20	24	480
0	1	0	1	1	6 x 16	20	12	240
0	1	1	0	1	6 x 8	20	24	480
1	0	0	1	1	6 x 16	40	6	240
1	0	1	0	1	6 x 8	40	12	480
1	1	0	0	1	6 x 8	40	24	960
1	1	0	1	1	6 x 16	40	12	480
1	1	1	0	1	6 x 8	40	24	960
0	0	0	0	0	6 x 9	20	12	240
0	1	0	0	0	6 x 9	20	24	480
1	1	0	0	0	6 x 9	40	24	960

NOTE: ALL OTHER COMMAND COMBINATIONS ARE INVALID AND WILL RESULT IN IMPROPER DISPLAY OPERATION.
*NTSC Format **PAL Format. ■=7 BITS FOR CHARACTER ADDRESS DATA, 1 BIT FOR COLOR DATA

Table 9
CDP1869 COMMAND REGISTER CODES

CPU I/O INSTRUCTION	MA15	MA14	MA13	MA12	MA11	MA10	MA9	MA8
OUT 4	0*	TONE ÷ 2^6	TONE ÷ 2^5	TONE ÷ 2^4	TONE ÷ 2^3	TONE ÷ 2^2	TONE ÷ 2^1	TONE ÷ 2^0
OUT 5	WN OFF	WN FREQ SEL2	WN FREQ SEL1	WN FREQ SEL0	WN AMP 2^3	WN AMP 2^2	WN AMP 2^1	WN AMP 2^0
OUT 6	X	X	X	X	X	PMA10 REG	PMA9 REG	PMA8 REG
OUT 7	X	X	X	X	X	HMA10 REG	HMA9 REG	HMA8 REG

X=DON'T CARE
*=MUST BE PROGRAMMED LOW
**=ALWAYS SET LOW INTERNALLY
***=MUST BE PROGRAMMED LOW DURING 9-LINE OPERATION

DISPLAY/MEMORY COMBINATIONS				
MAX. DISPLAY PAGE MEM. SIZE■	MAX. DISPLAY CHAR. MEM. SIZE§	CHAR SIZE •	HOME ADDRESS MODE	COMMENTS
240 x 8	128 x 8 x 8	4	ROLL	REPEATS EACH LINE AND COL TWICE*
240 x 8	128 x 16 x 8	8	SCROLL ROLL	REPEATS EACH LINE AND COL TWICE,* 16 DIFFERENT LINES/CHARACTER
1200 x 8	128 x 8 x 8	4	SCROLL ROLL	REPEATS EACH LINE AND COL TWICE*
960 x 8	128 x 8 x 8	2	SCROLL ROLL	REPEATS EACH COL TWICE*
960 x 8	128 x 16 x 8	6	SCROLL ROLL	REPEATS EACH COL TWICE* 16 DIFFERENT LINES/CHARACTER
1920 x 8	128 x 8 x 8	2	SCROLL ROLL	REPEATS EACH COL TWICE*
240 x 8	128 x 16 x 8	7	ROLL	REPEATS EACH LINE TWICE* 16 DIFFERENT LINES/CHARACTER
1200 x 8	128 x 8 x 8	3	SCROLL ROLL	REPEATS EACH LINE TWICE*
960 x 8	128 x 8 x 8	1	ROLL	HIGHEST RESOLUTION*
960 x 8	128 x 16 x 8	5	SCROLL ROLL	HIGHEST RESOLUTION,* 16 DIFFERENT LINES/CHARACTER
1920 x 8	128 x 8 x 8	1	SCROLL ROLL	HIGHEST RESOLUTION*
240 x 8	128 x 9 x 8	4	ROLL	REPEATS EACH LINE AND COL TWICE**
960 x 8	128 x 9 x 8	2	SCROLL ROLL	REPEATS EACH COL TWICE**
960 x 8	128 x 9 x 8	1	ROLL	HIGHEST RESOLUTION**

§=6 BITS FOR CHARACTER DATA, 2 BITS FOR COLOR DATA

•SEE FIG. 9.

MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0
TONE OFF	TONE FREQ SEL2	TONE FREQ SEL1	TONE FREQ SEL0	TONE AMP 2^3	TONE AMP 2^2	TONE AMP 2^1	TONE AMP 2^0
FRES VERT	DOUBLE PAGE ***	16 LINE HI-RES ***	X	9-LINE	X	X	CMEM ACCESS MODE
PMA7 REG	PMA6 REG	PMA5 REG	PMA4 REG	PMA3 REG	PMA2 REG	PMA1 REG	PMA0 REG
HMA7 REG	HMA6 REG	HMA5 REG	HMA4 REG	HMA3 REG	HMA2 REG	X**	X**

CDP1869C, CDP1870C, CDP1876C

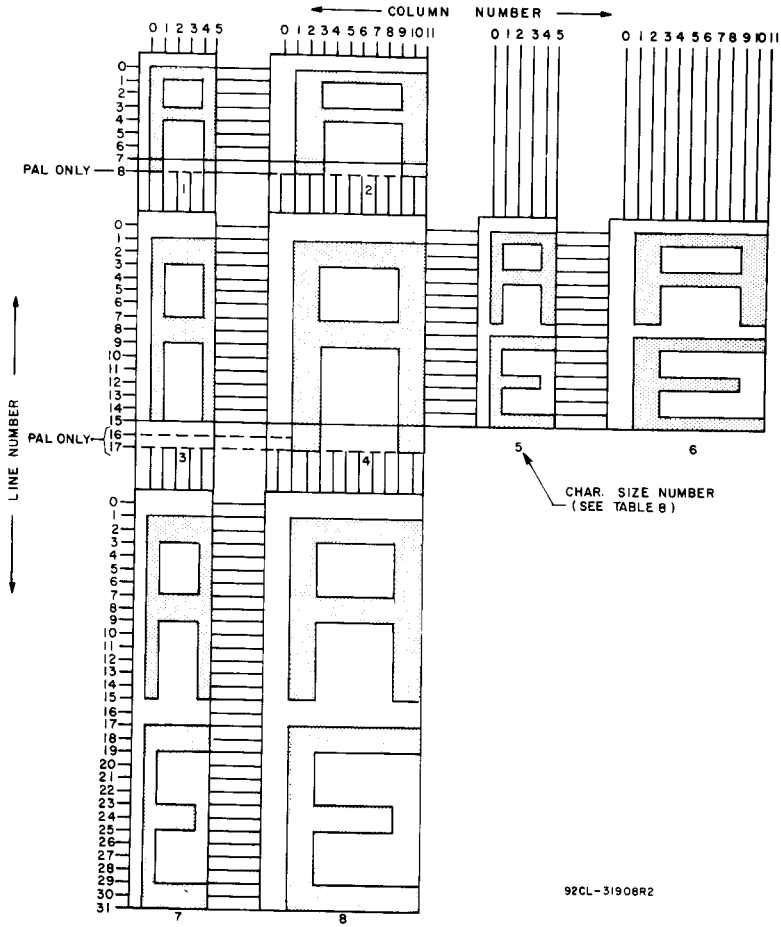

Fig. 9 - Character display matrix size.

Table 10
CDP1870C COMMAND REGISTER CODE

CPU I/O INSTRUCTION	BUS 7	BUS 6	BUS 5	BUS 4	BUS 3	BUS 2	BUS 1	BUS 0
OUT 3	FRES HORZ	COLB1	COLB0	DISP OFF	CFC	BKG RED	BKG BLUE	BKG GREEN

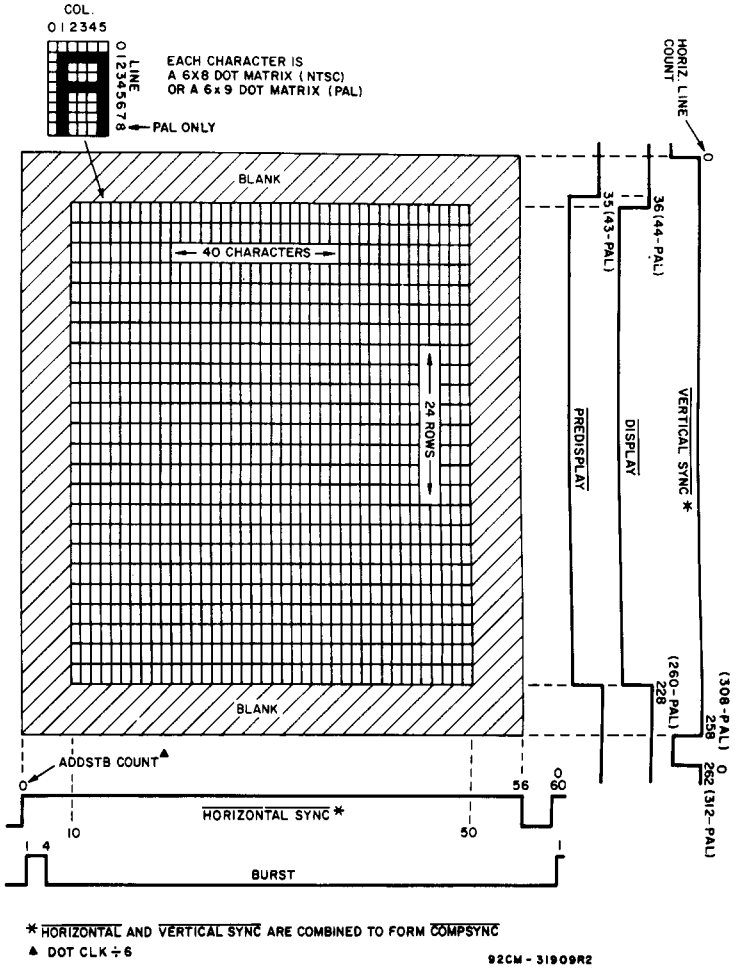

Fig. 10 - 40 x 24-character display.