



SANYO Semiconductors

DATA SHEET

LA72714VA

Monolithic Linear IC

For JPN TV

Multi Channel Television Sound Decoder IC

Overview

The LA72714VA is a JPN MTS (Multi Channel Television Sound) Decoder IC.

Features

- With SIF circuit, alignment-free* STEREO channel separation.
* In Base Band signal input mode, separation is adjusted by input level.
- Three I²C slave-addresses are prepared.
- The maximum output level is as large as 4.2dBV.
(Frequency = 1kHz, distortion = less than 3%, V_{CC} = 5V, TYP)
- The external clock is unnecessary.
- A couple of external input terminal is prepared.

Functions

- Stereo & Bilingual demodulation.
- Stereo & Bilingual detection.
- JUST CLOCK OUT.

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum power supply voltage	V _{CC} max		7.0	V
Allowable power dissipation	Pd max	Ta ≤ 70°C *	203	mW
Operating temperature	Topr		-20 to +70	°C
Storage temperature	Tstg		-55 to +150	°C

* When mounted on a 114.3mm×76.1mm×1.6mm glass epoxy board.

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SANYO Semiconductor Co., Ltd.

TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

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Operating Ranges at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended operating voltage	V _{CC}		5.0	V
Allowable operating voltage range	V _{CC op}		4.5 to 5.5	V

Electrical Characteristics at Ta = 25°C, V_{DD} = 5V

[Condition of input signal at pin 5]

BASE BAND input

[Output] L-ch : pin 18, R-ch : pin 17

Parameter	Symbol	Conditions	Ratings			unit
			min	typ	max	
Current dissipation	I _{CC1}	No signal, Inflow current at Pin 19	18	26	34	mA
MONO output level	V _{OMN1}	fm = 1kHz, 100% Mod, Pre-Emphasis OFF	-6	-4.5	-3	dBV
			501	595	708	mVrms
MONO L/R level difference	ΔV _{OMN1}	fm = 1kHz, 100% Mod, Pre-Emphasis OFF	-1	0	1	dB
MONO distortion	THDM1	fm = 1kHz, 100% Mod, Pre-Emphasis OFF		0.2	0.5	%
MONO frequency characteristics	FCM1	fm = 10kHz/1kHz, 100% Mod, 15kHz LPF Pre-Emphasis OFF	-18	-13.5		dB
MONO S/N	SNM1	Non Mod, 15kHz LPF	60	65		dB
STEREO output level	V _{OST1}	fm = 1kHz, 100% Mod, Cue (Stereo), 15kHz LPF	-6	-4.5	-3	dBV
			501	595	708	mVrms
STEREO distortion	THDS1	fm = 1kHz, 100% Mod, Cue (Stereo), 15kHz LPF		0.5	1	%
STEREO S/N	SNS1	Sub Carrier (Non Mod), Cue (Stereo), 15kHz LPF	50	60		dB
Main output level	V _{OMA1}	fm = 1kHz, 100% Mod, Cue (Bilingual), 15kHz LPF	-6	-4.5	-3	dBV
			501	595	708	mVrms
Main distortion	THDMA1	fm = 1kHz, 100% Mod, Cue (Bilingual), 15kHz LPF		0.2	0.5	%
Main S/N	SNMA1	Sub Carrier (Non Mod), Cue (Bilingual), 15kHz LPF	60	65		dB
SUB output level	V _{OSU1}	fm = 1kHz, 100% Mod, Cue (Bilingual), 15kHz LPF	-6	-4.5	-3	dBV
			501	595	708	mVrms
SUB distortion	THDSU1	fm = 1kHz, 100% Mod, Cue (Bilingual), 15kHz LPF		0.7	1.5	%
SUB frequency characteristics	FCSU1	fm = 10kHz/1kHz, 60% Mod, Cue (Bilingual), 15kHz LPF, Pre-Emphasis OFF	-18	-14.5		dB
SUB Main S/N	SNSU1	Sub Carrier (Non Mod), Cue (Bilingual), 15kHz LPF	50	60		dB
STEREO separation L → R	SEPR1	fm = 1kHz (L-only), 60% Mod, Cue (Stereo), 15kHz LPF	35	43		dB
STEREO separation R → L	SEPL1	fm = 1kHz (R-only), 60% Mod, Cue (Stereo), 15kHz LPF	35	43		dB
Stay behind carrier level (SUB)	CLSU1	Main = 0%, Sub = 0% (Carrier) Cue (Bilingual)		-50	-40	dBV
Stay behind carrier level (MAIN)	CLMA1	Main = 0%, Sub = 0% (Carrier) Cue (Bilingual)		-55	-45	dBV
Cross-talk MAIN → SUB	CTSUB1	Main : fm = 1kHz, 100% modulation, Cue (Bilingual), 15kHz LPF	55	62		dB
Cross-talk SUB → MAIN	CTMA1	Sub : fm = 1kHz, 100% modulation, Cue (Bilingual), 15kHz LPF	55	62		dB
MODE output MONO	MODMO1	Input = Mono Signal	0	1	1.3	V
MODE output STEREO	MODST1	Input = Stereo Signal	1.7	2	2.3	V
MODE output BILINGUAL	MODBI1	Input = Bilingual Signal	2.7	3	3.3	V
Just Clock output High volt	JCH1	f = 400Hz (mono), 25%Mod	4			V
Just Clock output Low volt	JCL1	f = 400Hz (mono), 10%Mod			1	V
Max Output level	MOL1	f = 1kHz, distortion = 3%	3.3	4.2		dBV
			1462	1622		mVrms
EXTERNAL input level	EXTIN1	f = 1kHz, (pin 12 & pin 13 input)		-14.5		dBV
				188.4		mVrms

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[Condition of input signal at pin 5]

Deviation of SIF input MONO : (fm = 1kHz) 100% → 4.5MHz ± 25kHz Pre-Emphasis ON

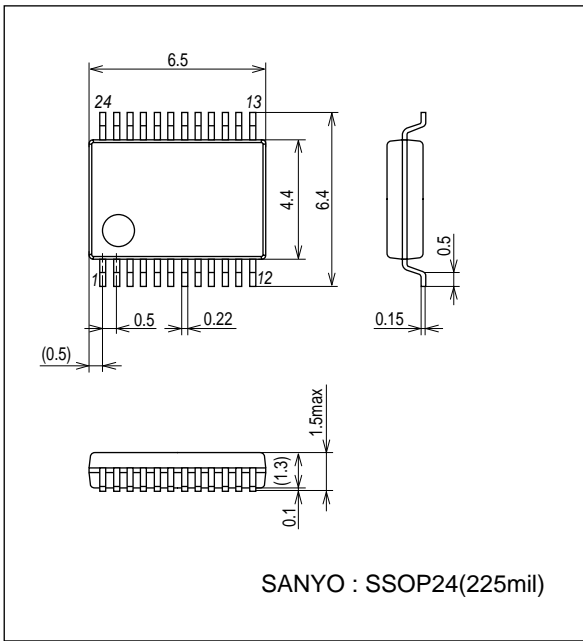
[Output] L-ch : pin 18, R-ch : pin 17

Parameter	Symbol	Conditions	Ratings			unit
			min	typ	max	
Current dissipation	I_{CC2}	No signal, Inflow current at Pin 19	20	28	36	mA
Input sensitivity level	V_{SIN}	fc = 4.5MHz	70	90	110	dB μ V
			3.16	31.62	316.2	mVrms
MONO output level	V_{OMN2}	fm = 1kHz, 100% Mod, Pre-Emphasis OFF	-6	-4.5	-3	dBV
			501	595	708	mVrms
MONO L/R level difference	ΔV_{OMN2}	fm = 1kHz, 100% Mod, Pre-Emphasis OFF	-1	0	1	dB
MONO distortion	THDM2	fm = 1kHz, 100% Mod, Pre-Emphasis OFF		0.2	0.5	%
MONO frequency characteristics	FCM2	fm = 10kHz/1kHz, 100% Mod, 15kHz LPF Pre-Emphasis OFF	-18	-13.5		dB
MONO S/N	SNM2	Non Mod, 15kHz LPF	55	60		dB
STEREO output level	V_{OST2}	fm = 1kHz, 100% Mod, Cue (Stereo), 15kHz LPF	-6	-4.5	-3	dBV
			501	595	708	mVrms
STEREO distortion	THDS2	fm = 1kHz, 100% Mod, Cue (Stereo), 15kHz LPF		0.5	1	%
STEREO S/N	SNS2	Sub Carrier (Non Mod), Cue (Stereo), 15kHz LPF	50	57		dB
Main output level	V_{OMA2}	fm = 1kHz, 100% Mod, Cue (Bilingual), 15kHz LPF	-6	-4.5	-3	dBV
			501	595	708	mVrms
Main distortion	THDMA2	fm = 1kHz, 100% Mod, Cue (Bilingual), 15kHz LPF		0.2	0.5	%
Main S/N	SNMA2	Sub Carrier (Non Mod), Cue (Bilingual), 15kHz LPF	55	60		dB
SUB output level	V_{OSU2}	fm = 1kHz, 100% Mod, Cue (Bilingual), 15kHz LPF	-6	-4.5	-3	dBV
			501	595	708	mVrms
SUB distortion	THDSU2	fm = 1kHz, 100% Mod, Cue (Bilingual), 15kHz LPF		0.7	1.5	%
SUB frequency characteristics	FCSU2	fm = 10kHz/1kHz, 60% Mod, Cue (Bilingual), 15kHz LPF, Pre-Emphasis OFF	-18	-14.5		dB
SUB Main S/N	SNSU2	Sub Carrier (Non Mod), Cue (Bilingual), 15kHz LPF	50	58		dB
STEREO separation L → R	SEPR2	fm = 1kHz (L-only), 60% Mod, Cue (Stereo), 15kHz LPF	35	38		dB
STEREO separation R → L	SEPL2	fm = 1kHz (R-only), 60% Mod, Cue (Stereo), 15kHz LPF	35	38		dB
Stay behind carrier level (SUB)	CLSU2	Main = 0%, Sub = 0% (Carrier) Cue (Bilingual)		-50	-40	dBV
Stay behind carrier level (MAIN)	CLMA2	Main = 0%, Sub = 0% (Carrier) Cue (Bilingual)		-55	-45	dBV
Cross-talk MAIN → SUB	CTSUB2	Main : fm = 1kHz, 100% modulation, Cue (Bilingual), 15kHz LPF	55	62		dB
Cross-talk SUB → MAIN	CTMA2	Sub : fm = 1kHz, 100% modulation, Cue (Bilingual), 15kHz LPF	55	62		dB
MODE output MONO	MODMO2	Input = Mono Signal	0	1	1.3	V
MODE output STEREO	MODST2	Input = Stereo Signal	1.7	2	2.3	V
MODE output BILINGUAL	MODBI2	Input = Bilingual Signal	2.7	3	3.3	V
Just Clock output High volt	JCH2	f = 400Hz (mono), 25%Mod	4			V
Just Clock output Low volt	JCL2	f = 400Hz (mono), 10%Mod			1	V
Max Output level	MOL2	f = 1kHz, distortion = 3%	3.3	4.2		dBV
			1462	1622		mVrms
EXTERNAL input level	EXTIN2	f = 1kHz, (pin 12 & pin 13 input)		-14.5		dBV
				188.4		mVrms

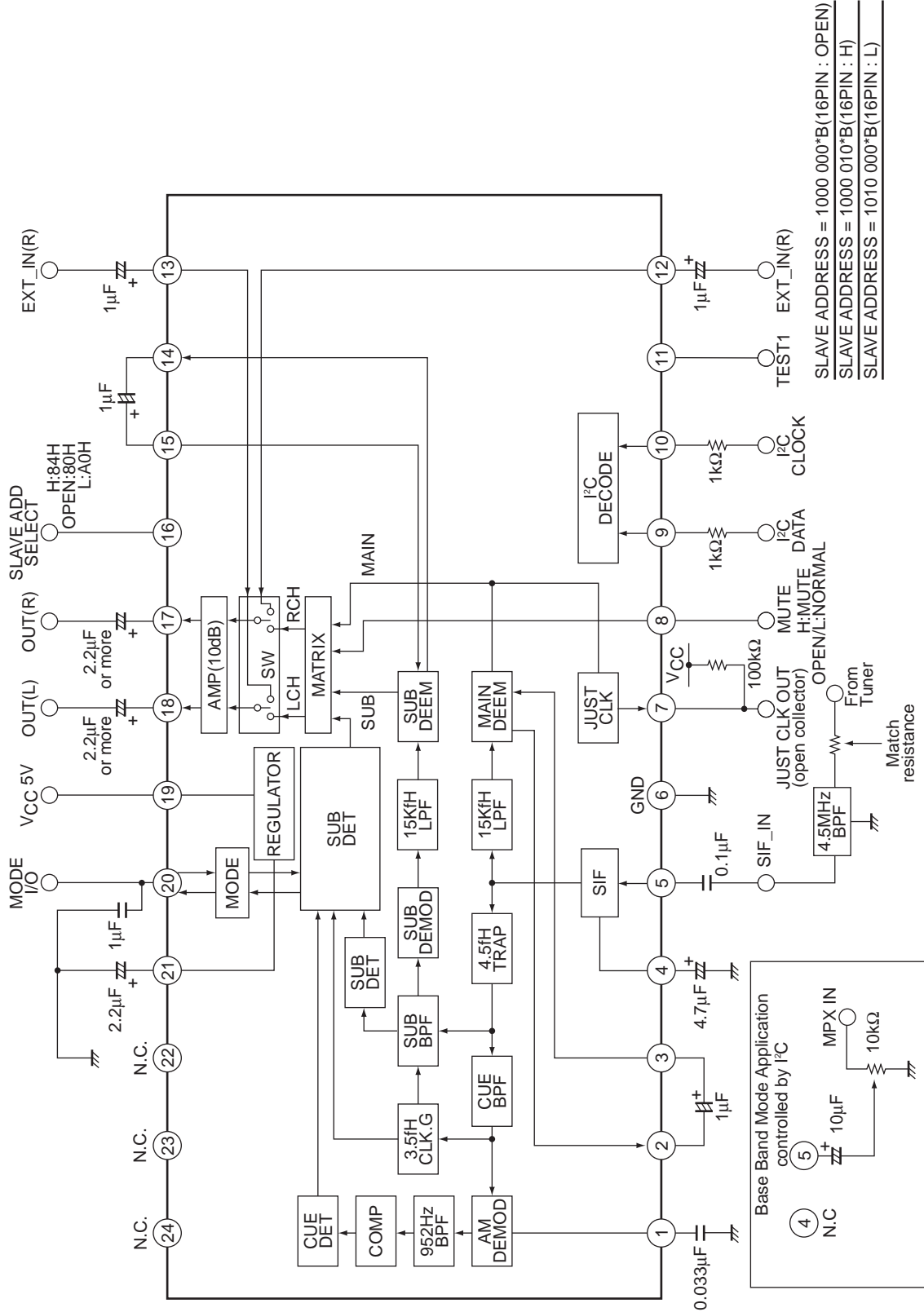
Package Dimensions

unit : mm (typ)

3287



Block Diagram and Application



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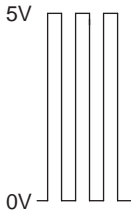
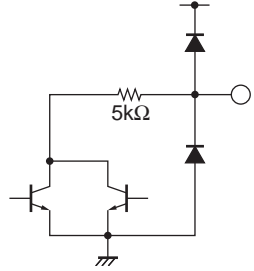
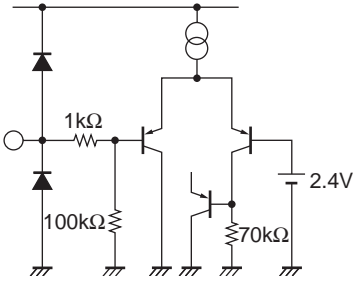
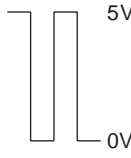
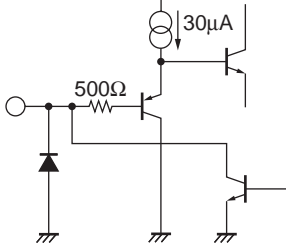
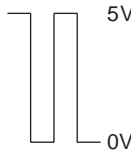
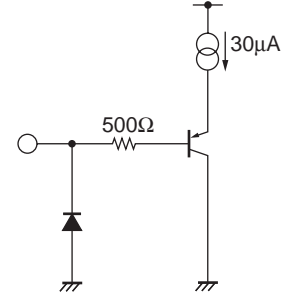
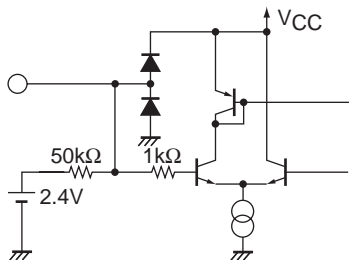
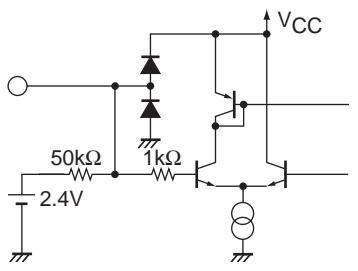
Pin Functions

Pin No.	Pin Name	Function	DC voltage AC level	Equivalent Circuit
1	AM DETECTOR	Reference terminal of AM detection.	DC : 2.3V	
2 14	DC FILTER OUT	Absorbing the DC offset of signal line by external capacity.	2pin DC : 2.6V 14pin DC : 2.1V	
3 15	DC FILTER IN	Absorbing the DC offset of signal line by external capacity.	DC : 2.4V	
4	FM FILTER	Filter terminal for making stable DC voltage of FM detection output in SIF part. Normally, use a condenser of 4.7μF. Increase the capacity value with concerning frequency characteristics of low level.	DC : 2.9V	
5	SIF INPUT	Input terminal for SIF. The input impedance is about 5kΩ. Be care for about pattern layout of the input circuit, because of causing buzz-beat and buzz by leaking noise signal into the input terminal. (The noise signal depending on sound is particularly video signal and chroma signal and so on. VIF carrier becomes noise signal.)	DC : 2.4V	
6	GND			

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Pin No.	Pin Name	Function	DC voltage AC level	Equivalent Circuit
7	JUST CLOCK OUT	Rectangle wave output for JUST CLOCK. (OPEN Collector) 100kΩ Pull-up		
8	MUTE	MUTE control pin. MUTE : 3.0V to	DC : 0V	
9	SDA	Serial data input/output pin. High : 2.5V to 5V Low : 0V to 1.5V		
10	SCL	Serial clock input pin. High : 2.5V to 5V Low : 0V to 1.5V		
11	TEST1			
12	EXTIN R	EXT input Rch not used : OPEN	DC : 2.4V -14.5dBV	
13	EXTIN L	EXT input Lch not used : OPEN	DC : 2.4V -14.5dBV	
16	TEST2			

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Pin No.	Pin Name	Function	DC voltage AC level	Equivalent Circuit
17 18	Line Out (R) Line Out (L)	Line output pin.	DC : 2.4V AC : -14.5dBV	
19	V _{CC} 5V			
20	MTS MODE OUT	Detection output for M.T.S. signal. BILINGUAL :3.0V STEREO :2.0V MONO :1.0V	No signal DC : 1.0V	
21	REG FILT	Filter terminal of reference voltage source	DC : 2.4V	
22 23 24	NC			

I²C BUS serial interface specification

(1) Data Transfer Manual

This IC adopts control method(I²C-BUS) with serial data, and controlled by two terminals which called SCL(serial clock) and SDA (serial data).At first, set up^{*1} the condition of starting data transfer, and after that, input 8 bit data to SDA terminal with synchronized SCL terminal clock. The order of transferring is first, MSB (the Most Scale of Bit), and save the order. The 9th bit takes ACK (Acknowledge) period, during SCL terminal takes ‘H’, this IC pull down the SDA terminal. After transferred the necessary data, two terminals lead to set up and of^{*2} data transfer stop condition, thus the transfer comes to close.

*1 Defined by SCL rise down SDA during ‘H’ period.

*2 Defined by SCL rise up SDA during ‘H’ period.

(2) Transfer Data Format

After transfer start condition, transfers slave address (1000 000*) to SDA terminal, control data, then, stop condition (See figure 1).

Slave address is made up of 7bits, 8th bit^{*3} shows the direction of transferring data, if it is ‘L’ takes write mode (As this IC side, this is input operation mode), and in case of ‘H’ reading mode (As this IC side, this is output operation mode). Data works with all of bit, transfer the stop condition before stop 8bit transfer, and to stop transfer, it will be canceled the transfer dates.

*3 It is called R/W bit.

Fig.1 DATA STRUCTURE “WRITE” mode

START Condition	Slave Address	R/W _L	ACK	Control data	ACK	STOP condition
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Fig.2 DATA STRUCTURE “READ” mode

START condition	Slave Address	R/W _H	ACK	Internal Data *	ACK	STOP condition
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* Output data as follows ;

bit8 is result of STERO DET (H : STEREO)

bit7 is result of BILINGUAL DET (H : BILINGUAL)

bit6 is Initial Condition ‘H’

bit5 to bit1 are fixed to ‘L’

(3) Initialize

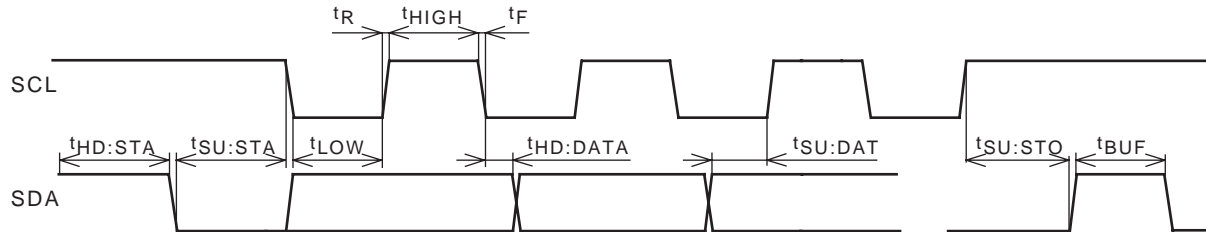
This LSI is initialized for circuit protection. Initial condition is “01h (Main-Mode)”.

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I²C Timing Specifications

Parameter	Symbol	min	max	unit
LOW level input voltage	V_{IL}	-0.5	1.5	V
HIGH level input voltage	V_{IH}	2.5	5.5	V
LOW level output current	I_{OL}		3.0	mA
SCL clock frequency	f_{SCL}	0	100	kHz
Set-up time for a repeated START condition	$t_{SU : STA}$	4.7		μs
Hold time START condition. After this period, the first clock pulse is generated	$t_{HD : STA}$	4.0		μs
LOW period of the SCL clock	t_{LOW}	4.7		μs
Rise time of both SDA and SDL signals	t_R	0	1.0	μs
HIGH period of the SCL clock	t_{HIGH}	4.0		μs
Fall time of both SDA and SDL signals	t_F	0	1.0	μs
Data hold time :	$t_{HD : DAT}$	0		μs
Data set-up time	$t_{SU : DAT}$	250		ns
Set-up time for STOP condition	$t_{SU : STO}$	4.0		μs
BUS free time between a STOP and START condition	t_{BUF}	4.7		μs

Definition of timing



LA72714VA

I²C Control/LA72714VA Group number is OMLY 1 (Normal Use).

Grp-1

D8	D7	D6	D5	D4	D3	D2	D1	Condition
						0	0	Bilingual
*						0	1	Main
						1	0	Sub
						1	1	(Prohibit)
*					0			Normal
					1			Forced MONO
*				0				Normal (MUTE Off)
				1				MUTE
*			0					TV Mode (SW Normal)
			1					EXT Mode (SW EXT)
*		0						JUST CLOCK Off
		1						JUST CLOCK On
*	0							SIF Mode
	1							BASE BAND Mode
*	0							Fix
1								Prohibit (TEST Mode)

*:Initial condition

Read out data

D8	D7	D6	D5	D4	D3	D2	D1	Condition
			0	0	0	0	0	Fixed
0								Normal
1								Stereo det
	0							Normal
	1							Bilingual det
		0						Except an initial condition
		1						Initial condition

Test mode condition

When STOP condition transform at Grp-1 data-end, controlled NORMAL mode.

Grp-2 (Only test condition : Normally, this group is hidden group)

D8	D7	D6	D5	D4	D3	D2	D1	Condition/Moniter position
0	0	0	0	0	0	0	0	-
0	0	0	0	0	0	0	1	TEST-01 SIF out
0	0	0	0	0	0	1	0	TEST-02 SUB FIL out
0	0	0	0	0	0	1	1	TEST-03 CUE FIL out
0	0	0	0	0	1	0	0	TEST-04 SUD DET out
0	0	0	0	0	1	0	1	TEST-05 CUE DC1 out
0	0	0	0	0	1	1	0	TEST-06 SUB DET2 out
0	0	0	0	0	1	1	1	TEST-07 110K out
0	0	0	0	1	0	0	0	TEST-08 28K out
0	0	0	0	1	0	0	1	TEST-09 CUE PLS out
0	0	0	0	1	0	1	0	TEST-10 FIL ZAP LEVEL

SLAVE ADDRESS 80H (16pin : OPEN)

SLAVE ADDRESS 84H (16pin : V_{CC})

SLAVE ADDRESS A0H (16pin : GND)

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Mode Select (pin & I²C setting)

Broadcast signal	MUTE PIN setting	I ² C					OUTPUT MODE			READ MODE OUT		MODE I/O
	pin8	D5	D4	D3	D2	D1	LCH (pin18)	RCH (pin17)	MODE	D8	D7	Pin20
Bilingual	L or OPEN	0	0	0	0	0	MAIN	SUB	BOTH	0	1	3V
	L or OPEN	0	0	0	0	1	MAIN	MAIN	MAIN	0	1	
	L or OPEN	0	0	0	1	0	SUB	SUB	SUB	0	1	
	L or OPEN	0	0	1	*	*	MAIN	MAIN	MONO	0	1	
	*	*	1	*	*	*	MUTE	MUTE	MUTE	0	1	
	H	*	*	*	*	*	MUTE	MUTE	MUTE	0	1	
	L or OPEN	1	0	*	*	*	EXT L	EXT R	EXT	0	1	
STEREO	L or OPEN	0	0	0	*	*	L	R	STEREO	1	0	2V
	L or OPEN	0	0	1	*	*	L+R	L+R	MONO	1	0	
	*	*	1	*	*	*	MUTE	MUTE	MUTE	1	0	
	H	*	*	*	*	*	MUTE	MUTE	MUTE	1	0	
	L or OPEN	1	0	*	*	*	EXT L	EXT R	EXT	1	0	
MONO	L or OPEN	0	0	*	*	*	L+R	L+R	MONO	0	0	1V
	*	*	1	*	*	*	MUTE	MUTE	MUTE	0	0	
	H	*	*	*	*	*	MUTE	MUTE	MUTE	0	0	
	L or OPEN	1	0	*	*	*	EXT L	EXT R	EXT	0	0	

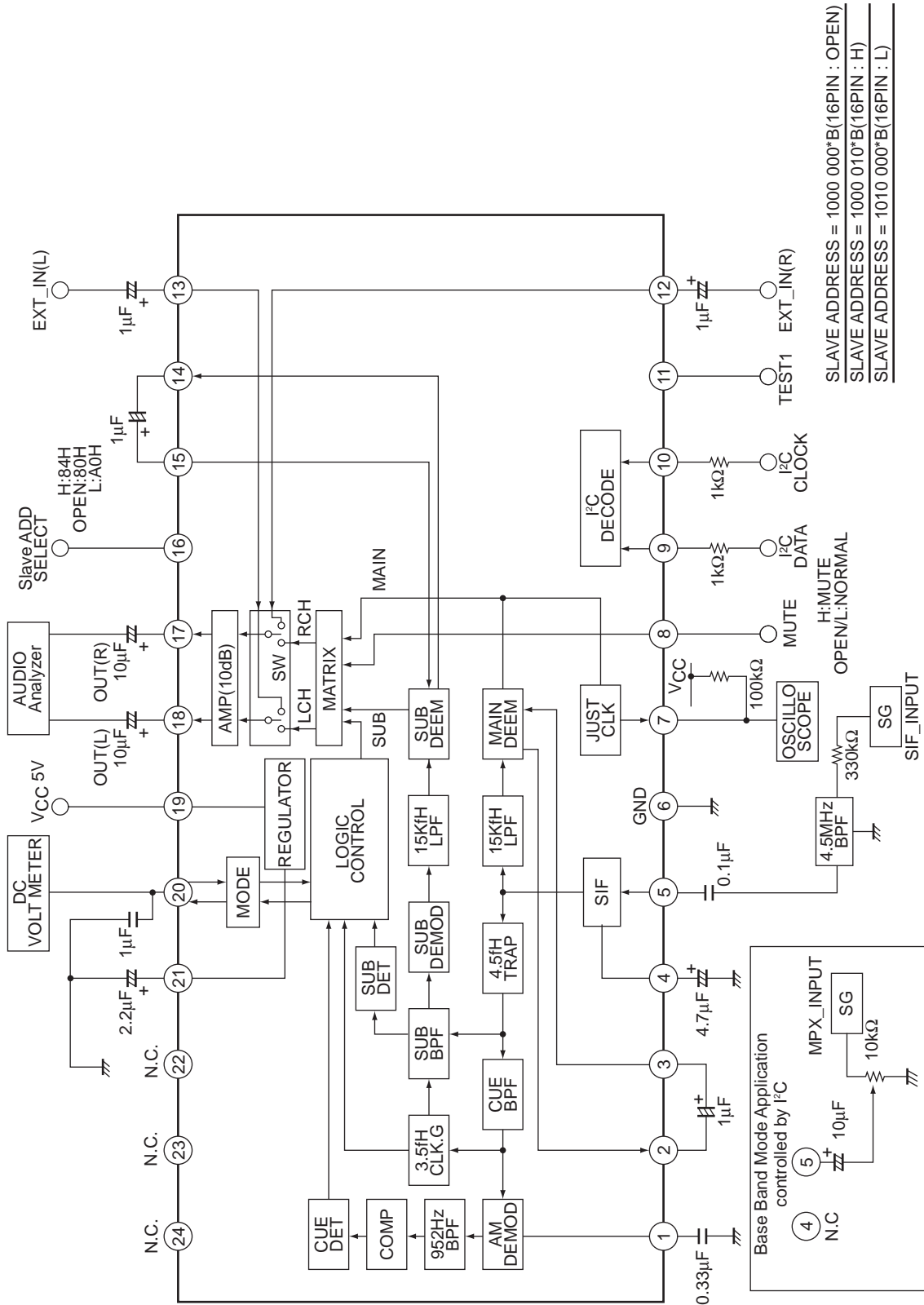
*: Don't care. 16pin : Slave address select. 0V to 1.5V : A0H, OPEN : 80H, 3.0V to V_{CC} : 84H

Serial Data Specification (I²C bus communication)

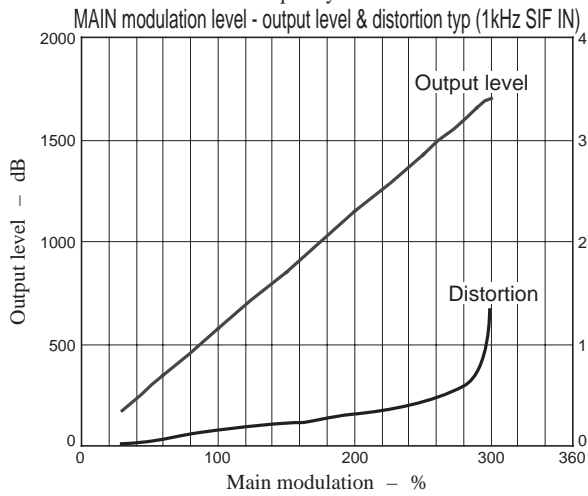
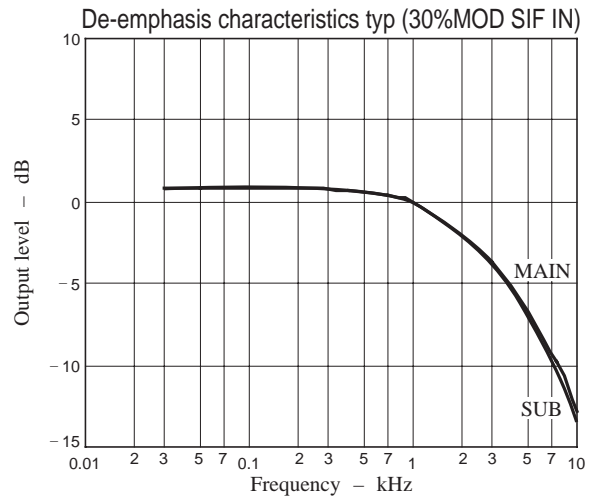
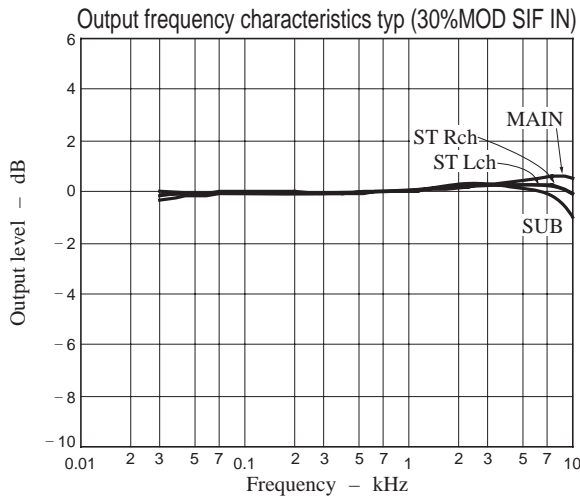
Data bit							
MSB D8	D7	D6	D5	D4	D3	D2	LSB D1
TEST	SIF or BASE BAND	JUST CLK	EXT SOURCE SELECT	NORMAL OUT MUTE	Forced MONO	(Bilingual mode select)	
<u>0</u> : OFF 1 : ON	<u>0</u> : SIF 1 : BASE BAND	0 : OFF 1 : ON	<u>0</u> : OFF(TV) 1 : EXT	<u>0</u> : OFF 1 : ON	<u>0</u> : OFF 1 : ON	00: BILINGUAL <u>01: MAIN</u> 10: SUB 11: Unusable	

Note : Underline shows default setting

Test Circuit



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