FLASH ROM MODULE

8M x 16 Flash ROM
Model No. HT8CF8M16FWCA

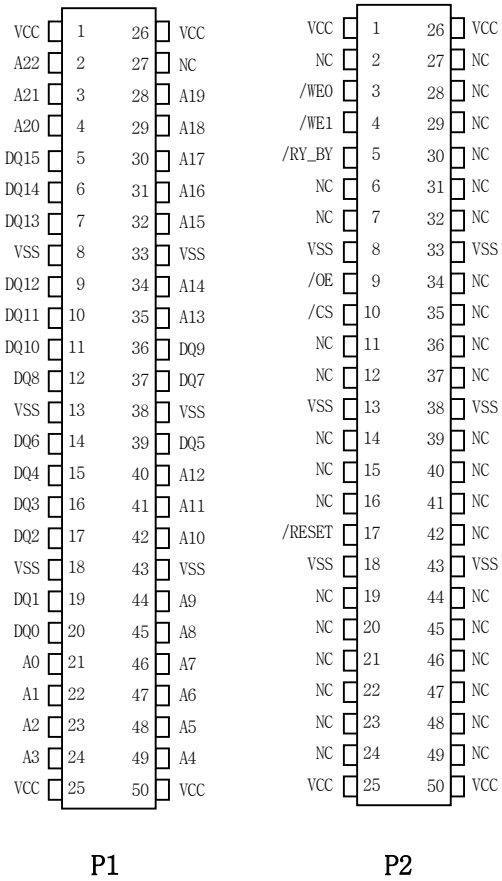
Features

- Single +3V ±0.3V power supply
- access time : 90ns
- High-density 16Mbyte design
- High-reliability, low-power design
- All input and output TTL-compatible
- Minimum 1,000,000 write/erase cycles guaranteed
- Sector erase architecture
- sector group protection
- Temporary sector group unprotection
- 100-pin design

  50-pin Fine Pitch SMT Stacking Connector(x2):P1,P2
- Connector
  - Bottom : 50-pin 0.6mm Pitch Free Height Receptacles (AMP 316077-3)
- Part Identification
  - HT8CF8M16FWCA-90 : 100-pin FH design

    /CE0, /CE1, /CE2, /CE3, /WE0, /WE1

Pin configuration



Option Marking

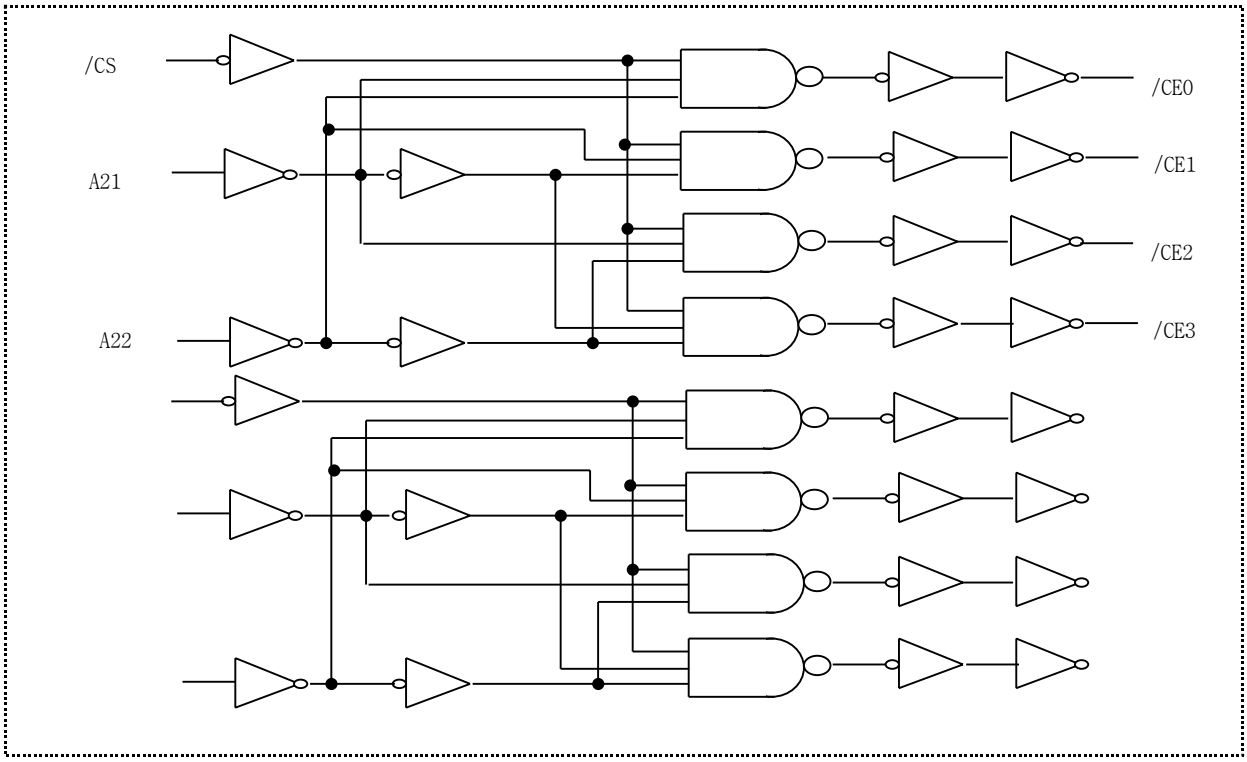
- Timing

90ns access	-90
120ns access	-120

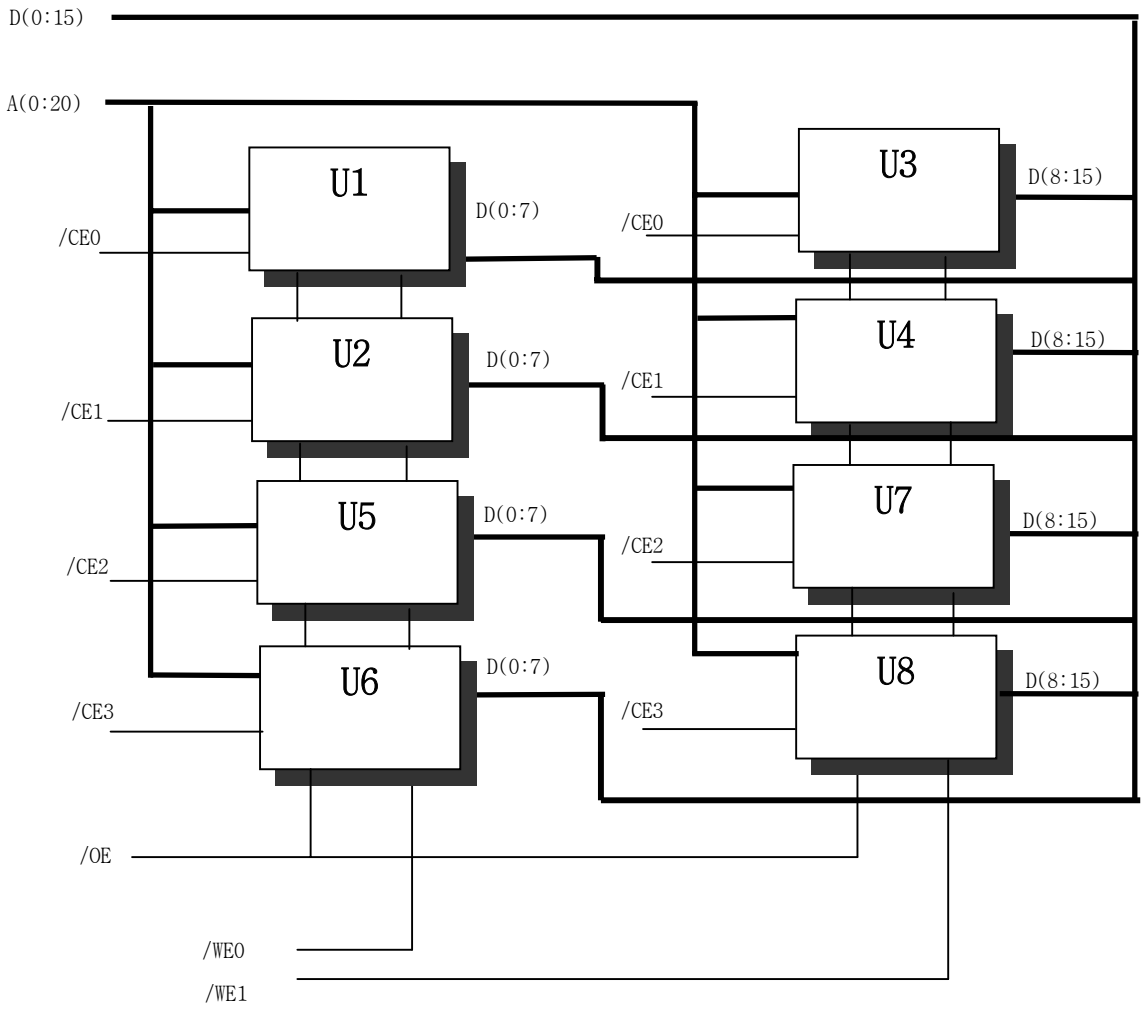
General Description

The HT8CF8M16FWCA-90 is a high-speed flash read only memory(FROM) module containing 8M words organized in a x16bit configuration. The module consists of eight 2M x 8bit FROM mounted on a 100-pin, FR4-printed circuit board. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from 12.0V flash or EPROM devices. Four write enable inputs, (/WE0, /WE1) are used to enable the module's 4 bytes independently. Output enable(/OE) and write enable(/WE) can set the memory input and output. Chip enable input /CE0, /CE1, /CE2, /CE3 is used to Enable FROM, write enable inputs(/WE0, /WE1) are used to write to the modules 4 bytes independently When FROM module is disable condition the module is becoming power standby mode, system designer can get low-power design. All module components may be powered from a single +3.3V DC power supply and all inputs and outputs are TTL-compatible.

74LVT139 (U9)



Functional block Diagram



Command Definitions (Byte Operation)

Command Sequence	Cycle	1st Cycle		2nd Cycle		3rd Cycle		4th Cycle		5th Cycle		6th Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read	1	RA	RD										
Reset	1	XXX	F0										
Autoselect Manufacturer ID	4	AAA	AA	555	55	AAA	90	X00	01	AMD			
									EC	SAMSUNG			
Autoselect Device ID	4	AAA	AA	555	55	AAA	90	X02	49	AMD			
									4F	SAMSUNG			
Autoselect Protect Verify	4	AAA	AA	555	55	AAA	90	SA X04	00	unprotect			
									01	protect			
Program	4	AAA	AA	555	55	AAA	A0	PA	PD				
Chip Erase	6	AAA	AA	555	55	AAA	80	AAA	AA	555	55	AAA	10
Block Erase	6	AAA	AA	555	55	AAA	80	AAA	AA	555	55	SA	30
Erase Suspend	1	AAA	B0										
Erase Resume	1	XXX	30										

Notes :

X : Don't care

RA : Address of the memory location to be read.

RD : Data read from location RA during read operation.

PA : Address of the memory location to be programmed.
Addresses latch on the falling edge of the WE# or CE# pulse, whichever Happens later.

PD : Data to be prigrammed at location PA.
Data latches on the rising edge of WE# or CE# pulse, whichever happens first.

SA : Address of the sector to be verified(in autoselect mode) or erased, Address bits A19-A12 select a unique sector.

※ The fourth cycle of the autoselect command sequence is a read cycle.

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Rating	Unit
Voltage on any pin relative to Vss	A9, $\overline{\text{Reset}}$	V_{IN}	-0.5 to +12.5	V
	All Other Pins		-0.5 to V_{CC}+0.5V	
Temperature Under Bias	Commercial	T_{bias}	-10 to +125	°C
	Industrial		-40 to +125	
Storage Temperature		T_{stg}	-65 to +150	°C
Short Circuit Output Current		I_{OS}	5	mA
Operating Temperature		T_A (Commercial Temp.)	0 to +70	°C
		T_A (Industrial Temp.)	-40 to + 85	°C

Notes :

1. Minimum DC voltage is -0.5V on Input/ Output pins. During transitions, this level may fall to -2.0V for periods <20ns. Maximum DC voltage on input / output pins is Vcc+0.5V which, during transitions, may overshoot to Vcc+2.0V for periods <20ns.
2. Minimum DC voltage is -0.5V on A9, $\overline{\text{Reset}}$ pins. During transitions, this level may fall to -2.0V for periods <20ns. Maximum DC voltage on A9, $\overline{\text{Reset}}$ pins is 12.5V which, during transitions, may overshoot to 14.0V for periods <20ns.
3. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to GND)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	V_{CC}	2.7	3.0	3.6	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS
CMOS Compatible

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN}=V_{SS} to V_{CC}, V_{CC}=V_{CCmax}		-1.0	1.0	µA
A9,$\overline{\text{Reset}}$ Input Leakage Current	I_{LIT}	V_{CC}=V_{CC}max, A9,$\overline{\text{Reset}}$=12.5V		-	35	µA
Output Leakage Current	I_{LO}	V_{OUT}=V_{SS} to V_{CC}, V_{CC}=V_{CCmax}		-1.0	1.0	µA
Active Read Current (1)	I_{CC1}	$\overline{CE}$=V_{IL}, $\overline{OE}$=V_{IL} All outputs open	5MHz	-	16	mA
			1MHz	-	4	
Active Write Current (2)	I_{CC2}	$\overline{CE}$=V_{IL}, $\overline{OE}$=V_{IH}		-	30	mA
Read While Program Current (3)	I_{CC3}	$\overline{CE}$=V_{IL}, $\overline{OE}$=V_{IH}		-	45	mA
Read While Erase Current (3)	I_{CC4}	$\overline{CE}$=V_{IL}, $\overline{OE}$=V_{IH}		-	45	mA
Program While Erase Suspend Current	I_{CC5}	$\overline{CE}$=V_{IL}, $\overline{OE}$=V_{IH}		-	30	mA
Standby Current	I_{SB1}	V_{CC}=V_{CCmax}, $\overline{CE}$=V_{CC}± 0.3V $\overline{\text{Reset}}$=V_{CC}± 0.3V		-	5	µA
Standby Current During Reset	I_{SB2}	V_{CC}=V_{CCmax}, $\overline{\text{Reset}}$=Vss± 0.3V		-	5	µA
Automatic Sleep Mode	I_{SB3}	V_{IH}=V_{CC} ± 0.3V, V_{IL}=V_{SS}± 0.3V		-	5	µA
Input Low Level	V_{IL}			-0.5	0.8	V
Input High Level	V_{IH}			0.7 x Vcc	V_{CC} + 0.3	V
Voltage for Autoselect and Block Protect	V_{ID}			11.5	12.5	V
Output Low Level	V_{OL}	I_{OL}=4.0mA, V_{CC}=V_{CCmin}		-	0.4	V
Output High Level	V_{OH1}	I_{OH}=-2.0mA, Vcc=V_{CCmin}		0.85 x Vcc	-	V
	V_{OH2}	I_{OH}=-100 uA, Vcc = V_{CCmin}		V_{CC} - 0.4	-	V
Low VCC Lock-out Voltage (4)	V_{LKO}			2.3	2.5	V

Notes :
1. The I_{CC} current listed includes both the DC operating current and the frequency dependent component(at 5 MHz).
   The read current is typically 9 mA (@ V_{CC}=3.0V , $\overline{OE}$ at V_{IH}.)
2. I_{CC} active during Internal Routine(program or erase) is in progress.
3. I_{CC} active during Read while Write is in progress.
4. Not 100% tested.

CAPACITANCE(T_A = 25 °C, V_{CC} = 3.3V, f = 1.0MHz)

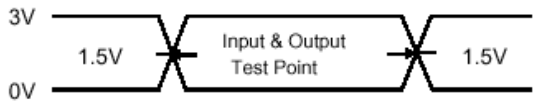
Item	Symbol	Test Condition	Min	Max	Unit
Input/Output Capacitance	$C_{I/O}$	V_{IL}=0V	-	10	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	10	pF

Note : Capacitance is periodically sampled and not 100% tested.

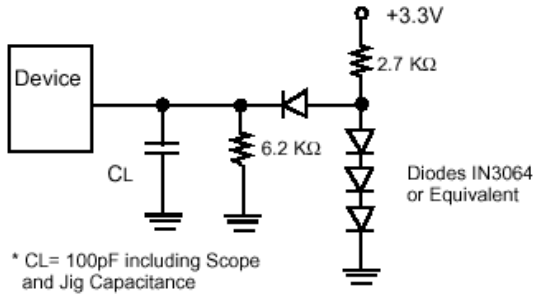
AC TEST CONDITION

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	1TTL and C_L = 100pF

Note : T_A = 0 °C to + 70 °C, V_{CC} = 2.7V - 3.6V, unless otherwise noted.



Input Pulse and Test Point



Output Load

AC CHARACTERISTICS

Read Operations

Parameter	Symbol	C_L = 100pF						Unit
		-9		-10		-12		
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	90		100		120		ns
Address Access Time	t_{AA}		90		100		120	ns
Chip Enable Access Time	t_{CE}		90		100		120	ns
Output Enable Time	t_{OE}		35		40		50	ns
$\overline{CE}$ & $\overline{OE}$ Disable Time	t_{DF} (*)		30		30		30	ns
Output Hold Time from Address, $\overline{CE}$ or $\overline{OE}$	t_{OH} (*)	0		0		0		ns
$\overline{Reset}$ Pin Low To Read Mode (Note)	t_{READY} (*)		20		20		20	μs

*. **Note** : Not 100% tested.

AC CHARACTERISTICS
Write(Erase/Program)Operations
Alternate $\overline{WE}$ Controlled Write

Parameter		Symbol	C_L = 100pF						Unit
			-9		-10		-12		
			Min	Max	Min	Max	Min	Max	
Write Cycle Time (1)		t_{WC}	90	-	100	-	120	-	ns
Address Setup Time		t_{AS}	0	-	0	-	0	-	ns
Address Setup Time to $\overline{OE}$ low during toggle bit polling		t_{ASO}	15	-	15	-	15	-	ns
Address Hold Time		t_{AH}	45	-	45	-	50	-	ns
Address Hold Time from $\overline{CE}$ or $\overline{OE}$ high during toggle bit polling		t_{AHT}	0	-	0	-	0	-	ns
Data Setup Time		t_{DS}	45	-	45	-	50	-	ns
Data Hold Time		t_{DH}	0	-	0	-	0	-	ns
Output Enable Setup Time (1)		t_{OES}	0	-	0	-	0	-	ns
Output Enable Hold Time	Read (1)	t_{OEH}	0	-	0	-	0	-	ns
	Toggle and $\overline{Data}$ Polling (1)		10	-	10	-	10	-	ns
$\overline{CE}$ Setup Time		t_{CS}	0	-	0	-	0	-	ns
$\overline{CE}$ Hold Time		t_{CH}	0	-	0	-	0	-	ns
Write Pulse Width		t_{WP}	45	-	45	-	50	-	ns
Write Pulse Width High		t_{WPH}	30	-	30	-	30	-	ns
Programming Operation	Word	t_{PGM}	11(typ.)		11(typ.)		11(typ.)		µs
	Byte		9(typ.)		9(typ.)		9(typ.)		µs
Block Erase Operation (2)		t_{BERS}	0.7(typ.)		0.7(typ.)		0.7(typ.)		sec
V_{CC} Set Up Time		t_{VCS}	50	-	50	-	50	-	µs
Write Recovery Time from RY/$\overline{BY}$		t_{RB}	0	-	0	-	0	-	ns
$\overline{Reset}$ High Time Before Read		t_{RH}	50	-	50	-	50	-	ns
$\overline{Reset}$ to Power Down Time		t_{RPD}	20	-	20	-	20	-	µs
Program/Erase Valid to RY/$\overline{BY}$ Delay		t_{BUSY}	90	-	90	-	90	-	ns
$\overline{CE}$ to $\overline{BYTE}$ Switching Low or High		t_{ELFL}/t_{ELFH}		5		5		5	ns
$\overline{BYTE}$ Switching Low to Output HIGH-Z		t_{FLQZ}	30	-	30	-	30	-	ns
$\overline{BYTE}$ Switching High to Output Active		t_{FHQV}	30	-	30	-	30	-	ns
V_{ID} Rising and Falling Time		t_{VID}	500	-	500	-	500	-	ns
$\overline{Reset}$ Pulse Width		t_{RP}	500	-	500	-	500	-	ns
$\overline{Reset}$ Low to RY/$\overline{BY}$ High		t_{RRB}	-	20	-	20	-	20	µs
$\overline{Reset}$ Setup Time for Temporary Unprotect		t_{RSP}	1	-	1	-	1	-	µs
$\overline{Reset}$ Low Setup Time		t_{RSTS}	500	-	500	-	500	-	ns
$\overline{Reset}$ High to Address Valid		t_{RSTW}	200	-	200	-	200	-	ns
Read Recovery Time Before Write		t_{GHWL}	0	-	0	-	0	-	ns
$\overline{CE}$ High during toggling bit polling		t_{CEPH}	20	-	20	-	25	-	ns
$\overline{OE}$ High during toggling bit polling		t_{OEPH}	20	-	20	-	25	-	ns

Notes : 1. Not 100% tested.
2. The duration of the Program or Erase operation varies and is calculated in the internal algorithms.

AC CHARACTERISTICS
Write(Erase/Program)Operations
Alternate $\overline{CE}$ Controlled Writes

Parameter		Symbol	C_L = 100pF						Unit
			-9		-10		-12		
			Min	Max	Min	Max	Min	Max	
Write Cycle Time (1)		t_{WC}	90	-	100	-	120	-	ns
Address Setup Time		t_{AS}	0	-	0	-	0	-	ns
Address Setup Time to $\overline{OE}$ low during toggle bit polling		t_{ASO}	15	-	15	-	15	-	ns
Address Hold Time		t_{AH}	45	-	45	-	50	-	ns
Address Hold Time from $\overline{CE}$ or $\overline{OE}$ high during toggle bit polling		t_{AHT}	0	-	0	-	0	-	ns
Data Setup Time		t_{DS}	45	-	45	-	50	-	ns
Data Hold Time		t_{DH}	0	-	0	-	0	-	ns
Output Enable Setup Time (1)		t_{OES}	0	-	0	-	0	-	ns
Output Enable Hold Time	Read (1)	t_{OEH}	0	-	0	-	0	-	ns
	Toggle and $\overline{Data}$ Polling (1)		10	-	10	-	10	-	ns
$\overline{WE}$ Setup Time		t_{WS}	0	-	0	-	0	-	ns
$\overline{WE}$ Hold Time		t_{WH}	0	-	0	-	0	-	ns
$\overline{CE}$ Pulse Width		t_{CP}	45	-	45	-	50	-	ns
$\overline{CE}$ Pulse Width High		t_{CPH}	30	-	30	-	30	-	ns
Programming Operation	Word	t_{PGM}	11(typ.)		11(typ.)		11(typ.)		µs
	Byte		9(typ.)		9(typ.)		9(typ.)		µs
Block Erase Operation (2)		t_{BERS}	0.7(typ.)		0.7(typ.)		0.7(typ.)		sec
$\overline{BYTE}$ Switching Low to Output HIGH-Z		t_{FLQZ}	30	-	30	-	30	-	ns

Notes : 1. Not 100% tested.
2.This does not include the preprogramming time.

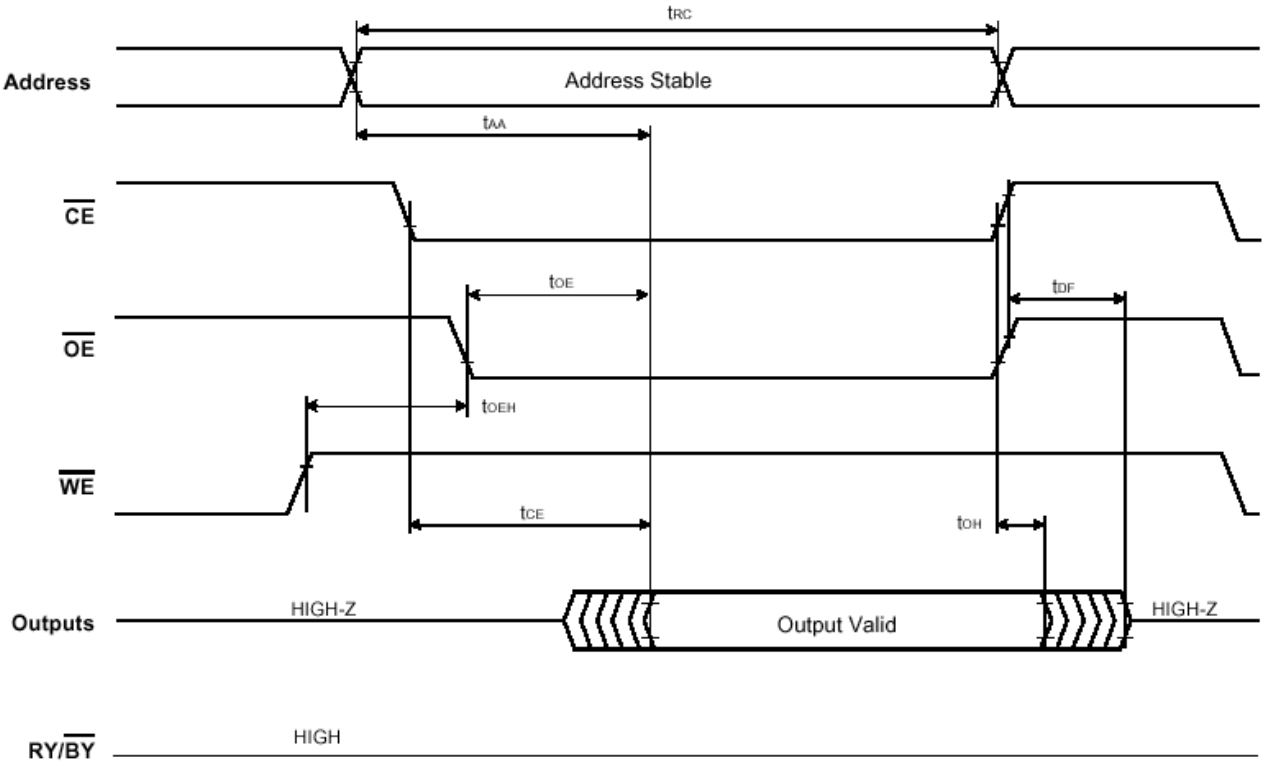
ERASE AND PROGRAM PERFORMANCE

Parameter		Limits			Unit	Comments
		Min	Typ	Max		
Block Erase Time			0.7	15	sec	Excludes 00H programming prior to erasure
Chip Erase Time			27		sec	
Word Programming Time			11	360	µs	Excludes system-level overhead
Byte Programming Time			9	300	µs	Excludes system-level overhead
Chip Programming Time	Word Mode		12	36	sec	Excludes system-level overhead
	Byte Mode		18	54	sec	
Erase/Program Endurance		100,000			cycles	Minimum 100,000 cycles guaranteed

Notes : 1. 25 °C, V_{CC} = 3.0 V 100,000 cycles, typical pattern.
2. System-level overhead is defined as the time required to execute the four bus cycle command necessary to program each byte. In the preprogramming step of the Internal Erase Routine, all bytes are programmed to 00H before erasure.

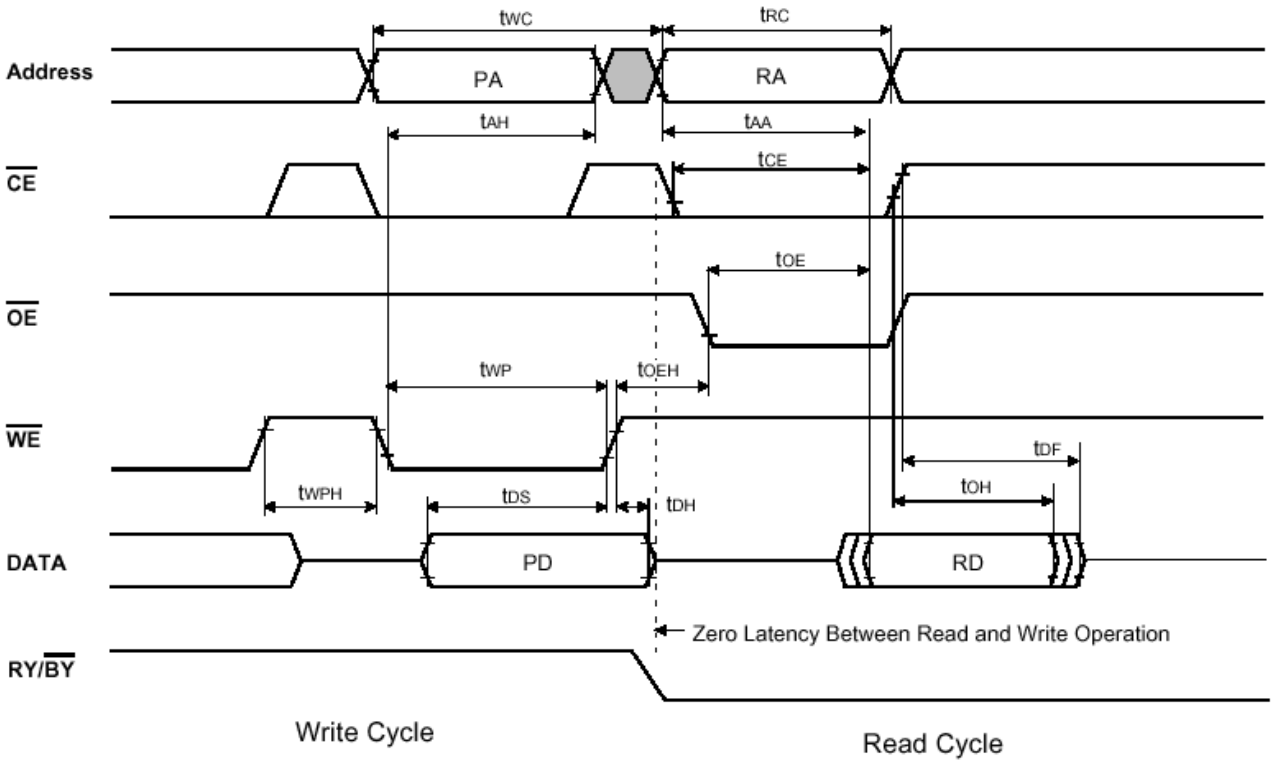
SWITCHING WAVEFORMS

Read Operations



Parameter	Symbol	-9		-10		-12		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	90		100		120		ns
Address Access Time	t_{AA}		90		100		120	ns
Chip Enable Access Time	t_{CE}		90		100		120	ns
Output Enable Time	t_{OE}		35		40		50	ns
$\overline{CE}$ & $\overline{OE}$ Disable Time	t_{DF}		30		30		30	ns
Output Hold Time from Address, $\overline{CE}$ or $\overline{OE}$	t_{OH}	0		0		0		ns
Output Enable Hold Time	t_{OEH}	0		0		0		ns

SWITCHING WAVEFORMS
Read While Write Operations

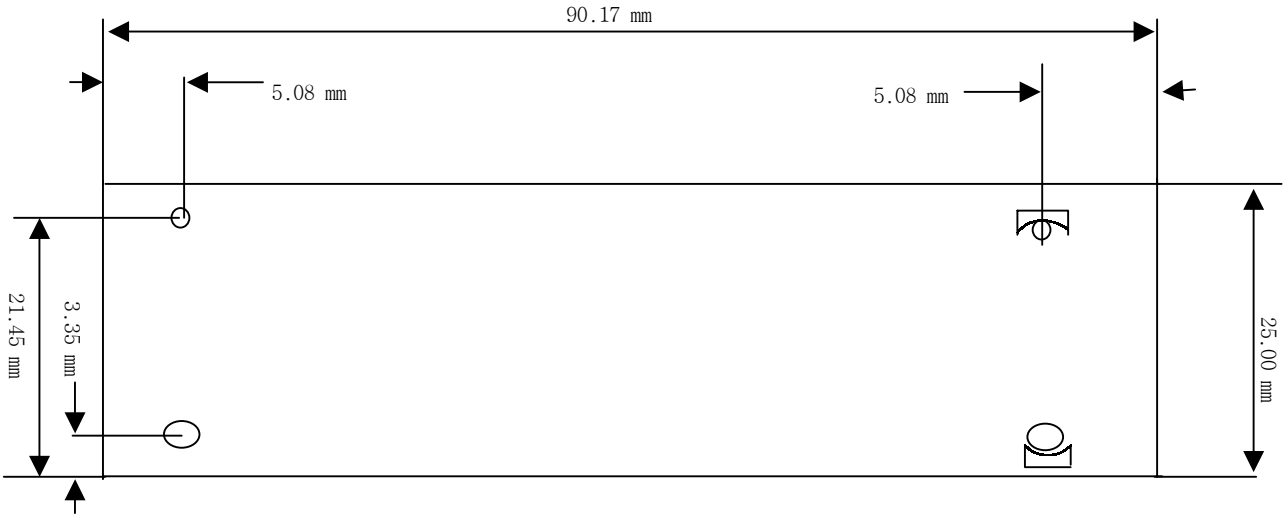


Note : PA = Program Address at one bank , RA = Read Address at the other bank , PD = Program Data In , RD = Read Data Out

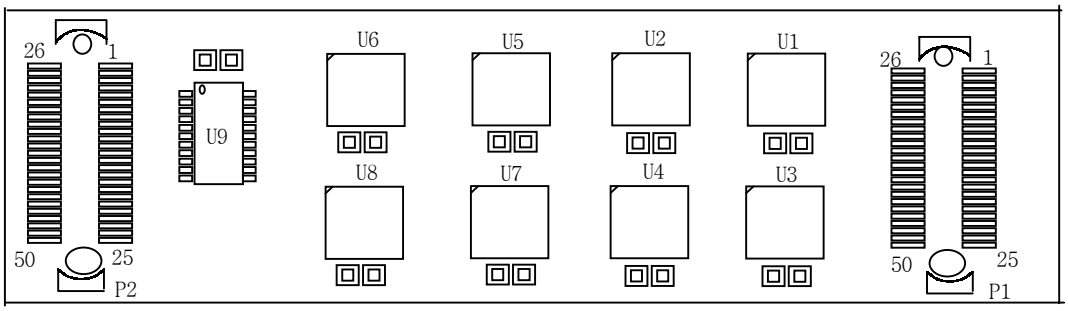
Parameter	Symbol	-9		-10		-12		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	tWC	90	-	100	-	120	-	ns
Write Pulse Width	tWP	45	-	45	-	50	-	ns
Write Pulse Width High	tWPH	30	-	30	-	30	-	ns
Address Hold Time	tAH	45	-	45	-	50	-	ns
Data Setup Time	tDS	45	-	45	-	50	-	ns
Data Hold Time	tDH	0	-	0	-	0	-	ns
Read Cycle Time	tRC	90	-	100	-	120	-	ns
Chip Enable Access Time	tCE	-	90	-	100	-	120	ns
Address Access Time	tAA	-	90	-	100	-	120	ns
Output Enable Access Time	tOE	-	35	-	40	-	50	ns
Output Enable Hold Time	tOEH	10	-	10	-	10	-	ns
$\overline{CE}$ & $\overline{OE}$ Disable Time	tDF	-	30	-	30	-	30	ns
Output Hold Time from Address,$\overline{CE}$ or $\overline{OE}$	tOH	0	-	0	-	0	-	ns

Package Information

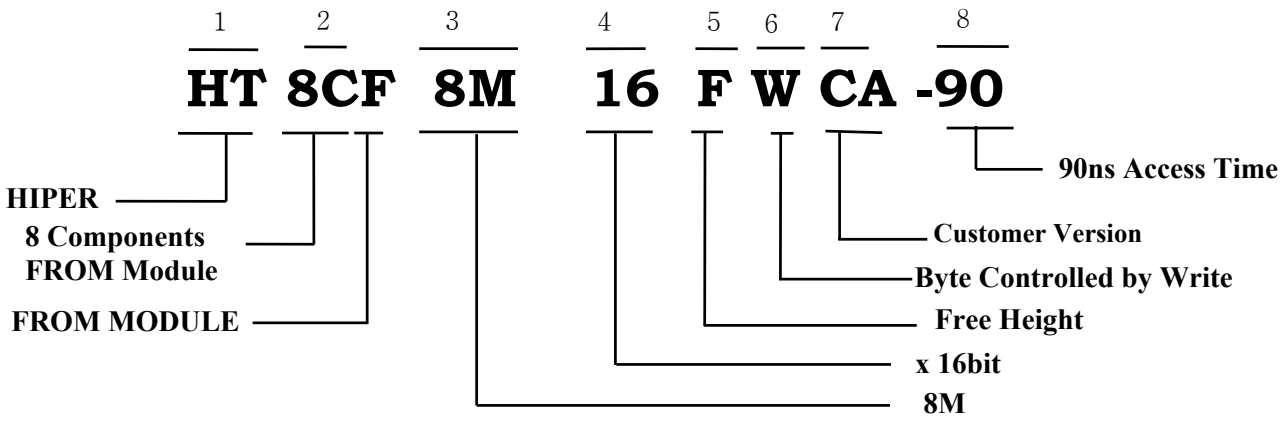
<TOP VIEW>



<BOTTOM VIEW>



Current Component Expanded Numbering System



1. - Product Line Identifier
HIPER Technology ---------- HT
2. - Number of memory components
3. - Depth : 8M
4. - Width : x 16bit
5. - Package Code
Free Height SMD Connector
6. - Empty : Byte Controlled by Chip enable Signal(CEx)
W : Byte Controlled by Write enable Signal(WEx)
7. - Customer Version ---------- CA
8. - Access time
70 ---------- 70ns
90 ---------- 90ns
120 ---------- 120ns