HD66704

(Graphics LCD Controller/Driver with Two 16-Character Lines and 160 Segments)

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Description

The HD66704 LCD controller and driver LSI is used to display alphanumeric characters, katakana, hiragana, a variety of symbols, and seven-segment numerals. It can be connected to a high-performance microcomputer via a high-speed clock-synchronized serial connection or on a four-bit bus. The HD66704 is capable of displaying two 16-character lines and 160 segments or one 16-character line and 240 segments in its character mode. The HD66704 has 432 built-in fonts for character display and supports double-height display. In its segment mode, it can drive up to 320 segments (at a duty cycle of 1/4). Segment-by-segment control of a blinking state, as well as the on/off state, is available.

The HD66704 applies various techniques for reducing the power consumption of an LCD system. These include low-voltage operation at 1.8 V or less, a booster to generate a maximum of triple the LCD-drive voltage from the supplied voltage, and voltage-followers to decrease the flow of direct current into the LCD-drive bleeder-resistors.

The HD66704 has a slim-chip configuration and interface-signal alignment that make it appropriate for chip-on-glass (COG) mounting. It is suitable for any product in which an LCD display may be used, such as facsimiles, telephones, pagers, audio equipment, video tape recorders, and electronic wallets.

Features

- Two 16-character lines (5-by-8-dot fonts) and 160 segments
- 320 segments with blinking control (at 1/4-duty drive)
- Wide range of operating voltages
    — V_{CC} = 1.8 to 5.5 V (LCD drive voltage: V_{LCD} = 3.0 to 6.5 V)
- Double or triple step-up circuit for LCD drive voltage
- 1/2- to 1/5-bias bleeder-resistors and voltage followers for LCD-drive power supply
- 25-level electronic potentiometer
- High-speed clock-synchronized serial interface (5 MHz) and high-speed 4-bit bus interface
- Continuous writing of data thanks to the zero instruction-execution time (wait-free writing)
- 80×8-bit display data RAM (80 characters max)
- 17,280-bit (5×8 dots : 432 characters) character generator ROM

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- 16×5-bit (two characters) character generator RAM
- Vertical double-height display
- Selectable CGROM memory bank (max. 432 fonts)
- Wide range of instruction functions (in character mode):
  — Clear display, display on/off control, icon and mark control, character blink, black-white reversed blinking cursor, return home, cursor on/off, black-white reversed raster-row
- Low-/high-speed blinking control of each segment (in segment mode)
- Power-save functions such as the standby mode and sleep mode
- Internal oscillation (with external or built-in resistor) hardware reset
- Shift change of segment and common driver
- Slim chip with bumps for chip-on-glass (COG) mounting

Table 1 Progammable Display Sizes and Duty Ratios

Duty Ratio	Drive Bias	Optimum Frame Frequency (at 32-kHz operation)	Segment Mode		Character Mode	
			Segment	7 Segments	Character	Segment
1/2	1/2	88 Hz	160	20 characters	-	-
1/3	1/3	88 Hz	240	30 characters	-	-
1/4	1/3	88 Hz	320	40 characters	-	-
1/11	1/4	91 Hz	-	-	1×16-character lines	240
1/18	1/5	88 Hz	-	-	2×16-character lines, 1×32-character line	160

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Total Current Consumption Characteristics (V_{CC} = 3 V, fosc = 32 kHz, TYP Conditions, LCD Drive Power Current Included)

| Character Display Size | Duty Ratio | Optimum Drive Bias | Frame Frequency | Total Power Consumption | | | Sleep Mode | Standby Mode |
| | | | | Normal Display Operation | | | | |
				Internal Logic	LCD Power	Total*		
Segment	1/3	1/3	88 Hz	15 µA	15 µA	45 µA	11 µA	0.1 µA
Character	1/18	1/5	88 Hz	20 µA	15 µA	50 µA	11 µA	

Note : When a double booster is used:
the total power consumption = Internal logic current + LCD power current × 2
When a triple booster is used:
the total power consumption = Internal logic current + LCD power current × 3

Type Name

Types	External Dimensions	Operation Voltages	Internal Fonts
HD66704A03BP	Au-bumped chip	1.8 V to 5.5 V	Katakana, alphanumerics, symbols, and European fonts

LCD Specification Comparison

Items	HD66704	HD66724	HD66725
Character display sizes	16 characters x 2 lines	12 characters x 3 lines	16 characters x 3 lines
Graphic display sizes	—	72 x 26 dots	96 x 26 dots
Multiplexing icons	160 to 320	144	192
Annunciator	1/2 to 1/4 duty	1/2 duty: 144	1/2 duty: 192
Key scan control	—	8 x 4	8 x 4
LED control ports	—	—	—
General output ports	—	3	3
Operating power voltages	1.8 V to 5.5 V	1.8 V to 5.5 V	1.8 V to 5.5 V
Liquid crystal drive voltages	3 V to 6.5 V	3 V to 6.5 V	3 V to 6.5 V
Serial bus	Clock-synchronized serial	Clock-synchronized serial	Clock-synchronized serial
Parallel bus	4 bits	4 bits, 8 bits	4 bits, 8 bits
Expansion driver control	Impossible	Impossible	Impossible
Liquid crystal drive duty ratios	1/2, 3, 4, 11, 18	1/2, 10, 18, 26	1/2, 10, 18, 26
Liquid crystal drive biases	1/2 to 1/5	1/4 to 1/6.5	1/4 to 1/6.5
Liquid crystal drive waveforms	B	B	B
Liquid crystal voltage booster	Double or triple	Single, double or triple	Single, double, or triple
Bleeder-resistor for liquid crystal drive	Incorporated	Incorporated (external)	Incorporated (external)
Liquid crystal drive operational amplifier	Incorporated	Incorporated	Incorporated
Liquid crystal contrast adjuster	Incorporated	Incorporated	Incorporated
Horizontal smooth scroll	—	3-dot unit	3-dot unit
Vertical smooth scroll	—	Line unit	Line unit
Double-height display	Yes	Yes	Yes
DDRAM	80 x 8	80 x 8	80 x 8
CGROM	17,280	20,736	20,736
CGRAM	16 x 5	384 x 8	384 x 8
SEGRAM	—	72 x 8	96 x 8
No. of CGROM fonts	240 + 192	240 + 192	240 + 192
No. of CGRAM fonts	2	64	64
Font sizes	5 x 8	6 x 8	6 x 8
Bit map area	—	72 x 26	96 x 26
R-C oscillation resistor/ oscillation frequency	External resistor, incorporated (32 kHz)	External resistor, incorporated (32 kHz)	External resistor, incorporated (32 kHz)
Reset function	External	External	External
Low power control	Partial display off Display off Oscillation off Liquid crystal power off	Partial display off Display off Oscillation off Liquid crystal power off Key wake-up interrupt	Partial display off Display off Oscillation off Liquid crystal power off Key wake-up interrupt
SEG/COM direction switching	SEG, COM	SEG, COM	SEG, COM
QFP package	—	—	—
TQFP package	—	—	—
TCP package	—	TCP-146	TCP-170
Bare chip	—	—	—
Bumped chip	Yes	Yes	Yes
No. of pins	126	146	170
Chip sizes	8.81 x 1.79	10.34 x 2.51	10.97 x 2.51
Pad intervals	70 µm	80 µm	80 µm

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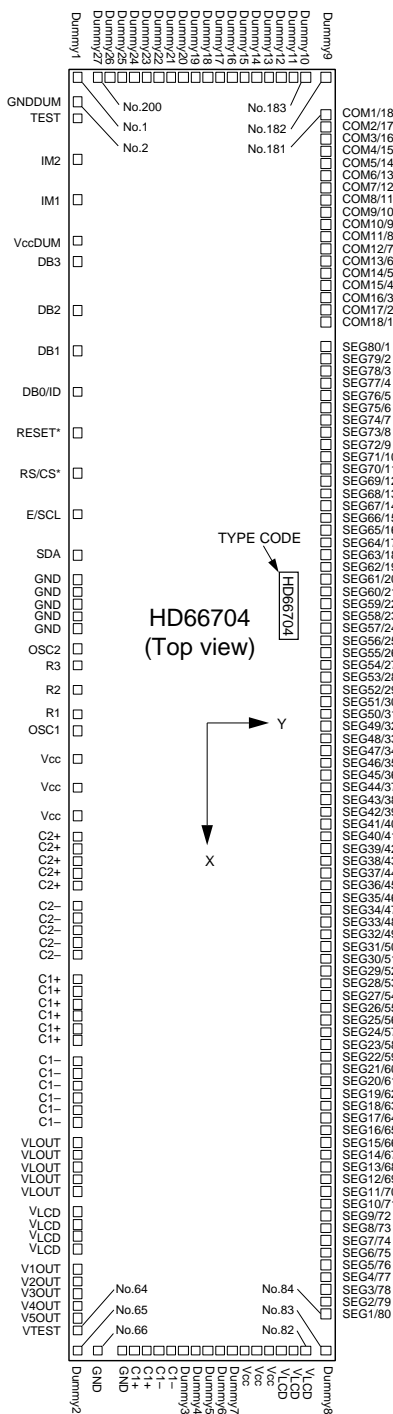## LCD-II Family Comparison (cont)

Items	HD66726	HD66728
Character display sizes	16 characters x 5 lines	16 characters x 10 lines
Graphic display sizes	96 x 42 dots	112 x 80 dots
Multiplexing icons	192	—
Annunciator	1/2 duty: 192	—
Key scan control	8 x 4	8 x 4
LED control ports	—	—
General output ports	3	3
Operating power voltages	1.8 V to 5.5 V	1.8 V to 5.5 V
Liquid crystal drive voltages	4.5 V to 11 V	4.5 V to 15 V
Serial bus	Clock-synchronized serial	Clock-synchronized serial
Parallel bus	4 bits, 8 bits	4 bits, 8 bits
Expansion driver control	Impossible	Impossible
Liquid crystal drive duty ratios	1/2, 10, 18, 26, 34, 42	1/8, 16, 24, 32, 40, 48, 56, 64, 72, 80
Liquid crystal drive biases	1/2 to 1/8	1/4 to 1/10
Liquid crystal drive waveforms	B	B, C
Liquid crystal voltage booster	Single, double, triple, or quadruple	Triple, quadruple, or quintuple
Bleeder-resistor for liquid crystal drive	Incorporated (external)	Incorporated (external)
Liquid crystal drive operational amplifier	Incorporated	Incorporated
Liquid crystal contrast adjuster	Incorporated	Incorporated
Horizontal smooth scroll	—	—
Vertical smooth scroll	Line unit	Line unit
Double-height display	Yes	Yes
DDRAM	80 x 8	160 x 8
CGROM	20,736	20,736
CGRAM	480 x 8	1,120 x 8
SEGRAM	96 x 8	—
No. of CGROM fonts	240 + 192	240 + 192
No. of CGRAM fonts	64	64
Font sizes	6 x 8	6 x 8
Bit map areas	96 x 42	112 x 80
R-C oscillation resistor/ oscillation frequency	External resistor (50 kHz)	External resistor (70 to 90 kHz)
Reset function	External	External
Low power control	Partial display off Display off Oscillation off Liquid crystal power off Key wake-up interrupt	Partial display off Display off Oscillation off Liquid crystal power off Key wake-up interrupt
SEG/COM direction switching	SEG, COM	SEG, COM
QFP package	—	—
TQFP package	—	—
TCP package	TCP-188	TCP-243
Bare chip	Yes	—
Bumped chip	Yes	Yes
No. of pins	188	243
Chip sizes	13.13 x 2.51	13.67 x 2.78
Pad intervals	100 µm	70 µm

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HD66704 Block Diagram
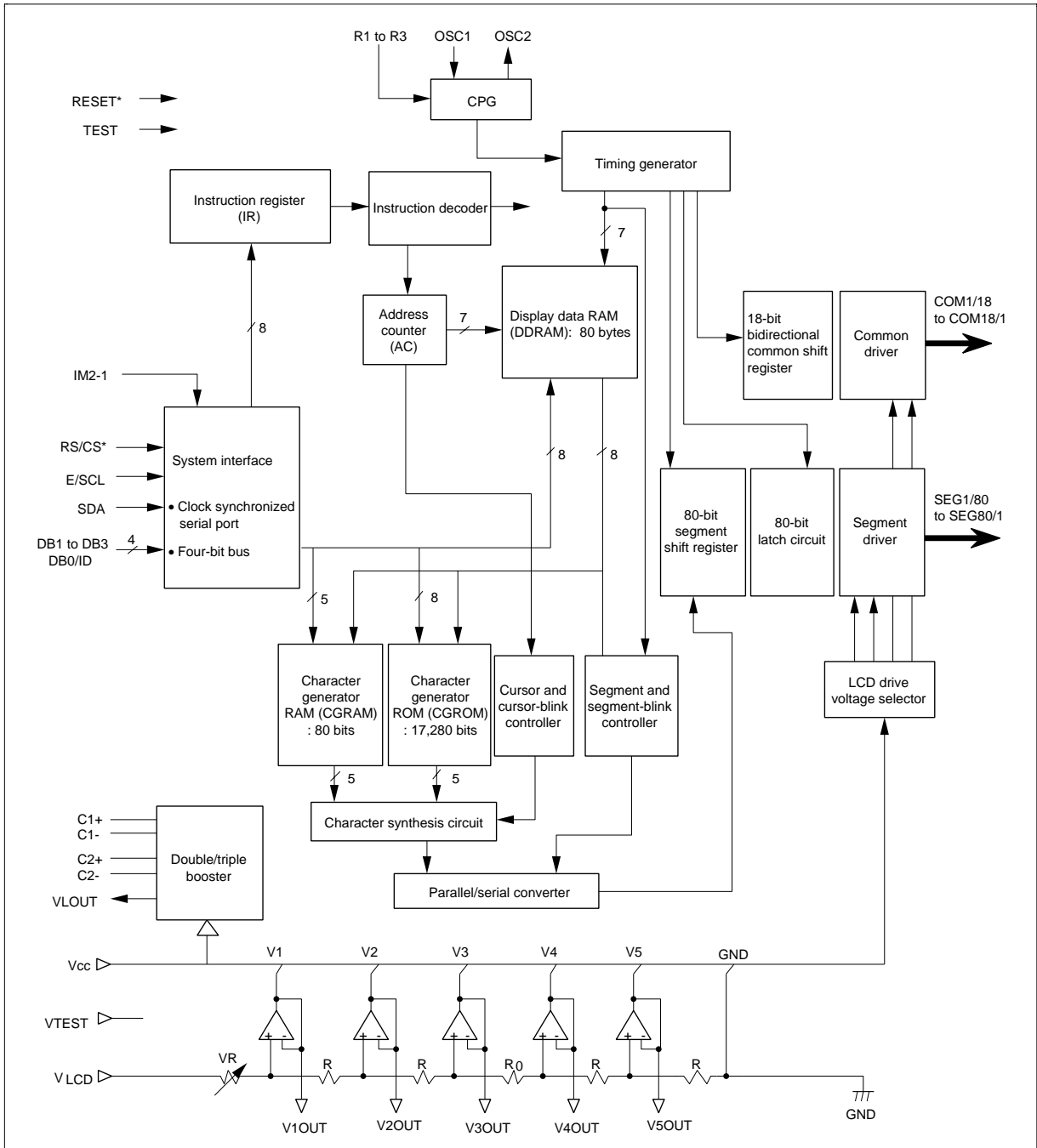
HD66704 Pad Arrangement

- Chip size: 8.81 mm × 1.79 mm
- Chip thickness: 550 μm (typ)
- PAD coordinates: PAD center
- Coordinate origin: Chip center
- Au bump size (pin number is shown in the blacket)
  (a) 70 μm × 70 μm
    Dummy1 (1), Dummy2 (65),
    Dummy8 (83), Dummy9 (182),
    (Chip corner pin)
  (b) 50 μm × 70 μm
    GNDDUM (2) to VTEST (64),
    GND (66) to VLCD (82),
    SEG1/80 (84) to COM1/18 (181),
    Dummy10 (183) to Dummy27 (200)
- Au bump pitch: 70 μm (min.)
- Au bump height: 20 μm (typ.)
- No cross recognition mark

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(Top view)

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Left side pads (top to bottom): GNDDUM, TEST, IM2, IM1, VccDUM, DB3, DB2, DB1, DB0/ID, RESET*, RS/CS*, E/SCL, SDA, GND, GND, GND, GND, OSC2, R3, R2, R1, OSC1, Vcc, Vcc, Vcc, C2+, C2+, C2+, C2+, C2+, C2−, C2−, C2−, C2−, C2−, C1+, C1+, C1+, C1+, C1+, C1+, C1−, C1−, C1−, C1−, C1−, C1−, VLOUT, VLOUT, VLOUT, VLOUT, VLOUT, VLCD, VLCD, VLCD, VLCD, V1OUT, V2OUT, V3OUT, V4OUT, V5OUT, VTEST

Top pads: Dummy1, Dummy27, Dummy26, Dummy25, Dummy24, Dummy23, Dummy22, Dummy21, Dummy20, Dummy19, Dummy18, Dummy17, Dummy16, Dummy15, Dummy14, Dummy13, Dummy12, Dummy11, Dummy10, Dummy9

No.200, No.1, No.2 — No.183, No.182, No.181

Right side pads (top to bottom): COM1/18, COM2/17, COM3/16, COM4/15, COM5/14, COM6/13, COM7/12, COM8/11, COM9/10, COM10/9, COM11/8, COM12/7, COM13/6, COM14/5, COM15/4, COM16/3, COM17/2, COM18/1, SEG80/1, SEG79/2, SEG78/3, SEG77/4, SEG76/5, SEG75/6, SEG74/7, SEG73/8, SEG72/9, SEG71/10, SEG70/11, SEG69/12, SEG68/13, SEG67/14, SEG66/15, SEG65/16, SEG64/17, SEG63/18, SEG62/19, SEG61/20, SEG60/21, SEG59/22, SEG58/23, SEG57/24, SEG56/25, SEG55/26, SEG54/27, SEG53/28, SEG52/29, SEG51/30, SEG50/31, SEG49/32, SEG48/33, SEG47/34, SEG46/35, SEG45/36, SEG44/37, SEG43/38, SEG42/39, SEG41/40, SEG40/41, SEG39/42, SEG38/43, SEG37/44, SEG36/45, SEG35/46, SEG34/47, SEG33/48, SEG32/49, SEG31/50, SEG30/51, SEG29/52, SEG28/53, SEG27/54, SEG26/55, SEG25/56, SEG24/57, SEG23/58, SEG22/59, SEG21/60, SEG20/61, SEG19/62, SEG18/63, SEG17/64, SEG16/65, SEG15/66, SEG14/67, SEG13/68, SEG12/69, SEG11/70, SEG10/71, SEG9/72, SEG8/73, SEG7/74, SEG6/75, SEG5/76, SEG4/77, SEG3/78, SEG2/79, SEG1/80

No.64, No.65, No.66 — No.84, No.83, No.82

Bottom pads: Dummy2, GND, C1+, C1+, C1−, C1−, GND, Dummy3, Dummy4, Dummy5, Dummy6, Vcc, Vcc, Vcc, VLCD, VLCD, Dummy7, VLCD, Dummy8

X, Y

Note: Although the pads for GND, VLCD, and V_{CC} pins are available on two sides of the chip, they are connected in the LSI. Supply the power to the pads on a single side.

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HD66704 Pad Coordinates

No.	Pad Name	X	Y	No.	Pad Name	X	Y	No.	Pad Name	X	Y	No.	Pad Name	X	Y	No.	Pad Name	X	Y
1	Dummy1	-4210	-706	41	C1+	2036	-673	81	VLCD	4183	529	121	SEG38/43	930	707	161	SEG78/3	-2295	707
2	GNDDUM	-4064	-706	42	C1+	2116	-673	82	VLCD	4183	600	122	SEG39/42	850	707	162	SEG79/2	-2376	707
3	TEST	-3984	-706	43	C1+	2196	-673	83	Dummy8	4183	707	123	SEG40/41	769	707	163	SEG80/1	-2456	707
4	IM2	-3731	-706	44	C1-	2306	-673	84	SEG1/80	3914	707	124	SEG41/40	689	707	164	COM18/1	-2618	707
5	IM1	-3478	-706	45	C1-	2386	-673	85	SEG2/79	3833	707	125	SEG42/39	608	707	165	COM17/2	-2698	707
6	VccDUM	-3225	-706	46	C1-	2466	-673	86	SEG3/78	3753	707	126	SEG43/38	527	707	166	COM16/3	-2779	707
7	DB3	-3144	-706	47	C1-	2546	-673	87	SEG4/77	3672	707	127	SEG44/37	447	707	167	COM15/4	-2860	707
8	DB2	-2891	-706	48	C1-	2626	-673	88	SEG5/76	3592	707	128	SEG45/36	366	707	168	COM14/5	-2940	707
9	DB1	-2638	-706	49	C1-	2706	-673	89	SEG6/75	3511	707	129	SEG46/35	285	707	169	COM13/6	-3021	707
10	DB0/ID	-2385	-706	50	VLOUT	2816	-673	90	SEG7/74	3430	707	130	SEG47/34	205	707	170	COM12/7	-3102	707
11	RESET*	-2132	-706	51	VLOUT	2896	-673	91	SEG8/73	3350	707	131	SEG48/33	124	707	171	COM11/8	-3182	707
12	RS/CS*	-1879	-706	52	VLOUT	2976	-673	92	SEG9/72	3269	707	132	SEG49/32	43	707	172	COM10/9	-3263	707
13	E/SCL	-1626	-706	53	VLOUT	3057	-673	93	SEG10/71	3188	707	133	SEG50/31	-37	707	173	COM9/10	-3344	707
14	SDA	-1373	-706	54	VLOUT	3137	-673	94	SEG11/70	3108	707	134	SEG51/30	-118	707	174	COM8/11	-3424	707
15	GND	-1119	-706	55	VLCD	3246	-673	95	SEG12/69	3027	707	135	SEG52/29	-199	707	175	COM7/12	-3505	707
16	GND	-1016	-706	56	VLCD	3327	-673	96	SEG13/68	2946	707	136	SEG53/28	-279	707	176	COM6/13	-3585	707
17	GND	-912	-706	57	VLCD	3407	-673	97	SEG14/67	2866	707	137	SEG54/27	-360	707	177	COM5/14	-3666	707
18	GND	-809	-706	58	VLCD	3487	-673	98	SEG15/66	2785	707	138	SEG55/26	-440	707	178	COM4/15	-3747	707
19	GND	-705	-706	59	V1OUT	3597	-673	99	SEG16/65	2705	707	139	SEG56/25	-521	707	179	COM3/16	-3827	707
20	OSC2	-452	-706	60	V2OUT	3677	-673	100	SEG17/64	2624	707	140	SEG57/24	-602	707	180	COM2/17	-3908	707
21	R3	-336	-706	61	V3OUT	3757	-673	101	SEG18/63	2543	707	141	SEG58/23	-682	707	181	COM1/18	-3989	707
22	R2	-181	-706	62	V4OUT	3837	-673	102	SEG19/62	2463	707	142	SEG59/22	-763	707	182	Dummy9	-4210	707
23	R1	-25	-706	63	V5OUT	3917	-673	103	SEG20/61	2382	707	143	SEG60/21	-844	707	183	Dummy10	-4210	600
24	OSC1	109	-706	64	VTEST	3997	-673	104	SEG21/60	2301	707	144	SEG61/20	-924	707	184	Dummy11	-4210	529
25	Vcc	478	-706	65	Dummy2	4183	-706	105	SEG22/59	2221	707	145	SEG62/19	-1005	707	185	Dummy12	-4210	459
26	Vcc	634	-706	66	GND	4183	-601	106	SEG23/58	2140	707	146	SEG63/18	-1086	707	186	Dummy13	-4210	389
27	Vcc	789	-706	67	GND	4183	-487	107	SEG24/57	2059	707	147	SEG64/17	-1166	707	187	Dummy14	-4210	319
28	C2+	935	-673	68	C1+	4183	-383	108	SEG25/56	1979	707	148	SEG65/16	-1247	707	188	Dummy15	-4210	249
29	C2+	1015	-673	69	C1+	4183	-313	109	SEG26/55	1898	707	149	SEG66/15	-1328	707	189	Dummy16	-4210	178
30	C2+	1095	-673	70	C1-	4183	-243	110	SEG27/54	1817	707	150	SEG67/14	-1408	707	190	Dummy17	-4210	108
31	C2+	1176	-673	71	C1-	4183	-173	111	SEG28/53	1737	707	151	SEG68/13	-1489	707	191	Dummy18	-4210	38
32	C2+	1256	-673	72	Dummy3	4183	-102	112	SEG29/52	1656	707	152	SEG69/12	-1569	707	192	Dummy19	-4210	-32
33	C2-	1365	-673	73	Dummy4	4183	-32	113	SEG30/51	1576	707	153	SEG70/11	-1650	707	193	Dummy20	-4210	-102
34	C2-	1446	-673	74	Dummy5	4183	38	114	SEG31/50	1495	707	154	SEG71/10	-1731	707	194	Dummy21	-4210	-173
35	C2-	1526	-673	75	Dummy6	4183	108	115	SEG32/49	1414	707	155	SEG72/9	-1811	707	195	Dummy22	-4210	-243
36	C2-	1606	-673	76	Dummy7	4183	178	116	SEG33/48	1334	707	156	SEG73/8	-1892	707	196	Dummy23	-4210	-313
37	C2-	1686	-673	77	Vcc	4183	249	117	SEG34/47	1253	707	157	SEG74/7	-1973	707	197	Dummy24	-4210	-383
38	C1+	1796	-673	78	Vcc	4183	319	118	SEG35/46	1172	707	158	SEG75/6	-2053	707	198	Dummy25	-4210	-453
39	C1+	1876	-673	79	Vcc	4183	389	119	SEG36/45	1092	707	159	SEG76/5	-2134	707	199	Dummy26	-4210	-524
40	C1+	1956	-673	80	VLCD	4183	459	120	SEG37/44	1011	707	160	SEG77/4	-2215	707	200	Dummy27	-4210	-594

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Example of COG Wiring

- Clock-synchronized serial
- Doubling-voltage booster used
- Internal operational amplifier used
- Internal oscillation resistor used

HD66704
(Top view)

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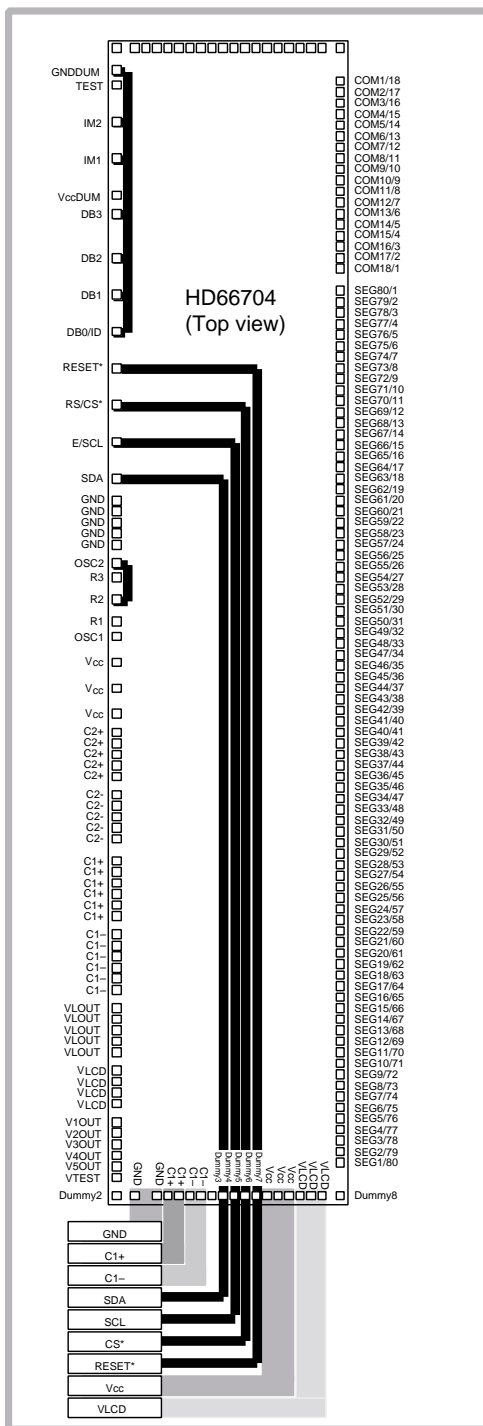
Pin Functions

Table 2 Pin Functional Description

Signals	Number of Pins	I/O	Connected to	Functions
IM2, IM1	2	I	V_{CC} or GND	Selects the MPU interface mode:

IM2	IM1	MPU interface mode
"GND"	"GND"	Clock-synchronized serial interface
"GND"	"Vcc"	68-system 4-bit bus interface
"Vcc"	"GND"	Setting inhibited
"Vcc"	"Vcc"	Setting inhibited

Signals	Number of Pins	I/O	Connected to	Functions
RS/CS*	1	I	MPU	Selects the register for a 4-bit bus interface. Low: Instruction High: RAM access. Selects the HD66704 for a serial interface. Low: HD66704 is selected and can be accessed. High: HD66704 is not selected and cannot be accessed. The start byte is transferred immediately after the signal level on this line is switched from high to low.
E/SCL	1	I	MPU	Enables the data write signal for a 4-bit bus interface. High: Enable. Inputs the serial transfer clock for a serial interface. Fetches data at the rising edge of a clock.
SDA	1	I	MPU	Not used for a 4-bit bus interface. Fix to V_{CC} or GND. Serves as the serial transfer data for a serial interface.
DB1 to DB3, DB0/ID	4	I	MPU	Serves as the write-only data bus for the four-bit bus interface. Fix these bits to V_{CC} or GND when using a serial interface. Since DB0/ID sets the ID bit for a serial interface, set it to GND or V_{CC} to select the ID.
COM1/18– COM18/1	18	O	LCD	Common output signals: COM1 to COM8 for the character display, and COM9 to COM11 for the segment display in the one-line character mode. COM1 to COM16 for the character display, and COM17 and COM18 for the segment display in the two-line character mode. COM1 to COM4 drive the LCDs in the segment mode. All the unused pins output deselection waveforms. In the sleep mode (SLP = 1) or standby mode (STB = 1), all pins output GND level. The CMS bit can change the shift direction of the common signal. For example, if CMS = 0, COM1/18 is COM1. If CMS = 1, COM1/18 is COM18.

Table 2 Pin Functional Description (cont)

Signals	Number of Pins	I/O	Connected to	Functions
SEG1/80–SEG80/1	80	O	LCD	Segment output signals for segment-icon display and character/graphics display. In the sleep mode (SLP = 1) or standby mode (STB = 1), all pins output GND level. The SGS bit can change the shift direction of the segment signal. For example, if SGS = 0, SEG1/80 is SEG1. If SGS = 1, SEG1/80 is SEG80.
V1OUT–V5OUT	5	O	Open	Used for output from the internal operational amplifiers. If the display quality is poor, attach a capacitor to stabilize the output.
V_{LCD}	7	—	Power supply	Power supply for LCD drive. V_{LCD} – GND = 6.5 V max. Input a voltage greater than V_{CC}.
Vcc	6	—	Power supply	V_{CC} = +1.8 V to +5.5 V
GND	8	—	GND	GND (logic) = 0 V
OSC1, OSC2	2	I or O	Oscillation resistor or clock	For R-C oscillation using an external resistor, connect an external resistor. For R-C oscillation using an internal resistor, connect R1-R3 to OSC2 and leave OSC1 disconnected. For external clock supply, input clock pulses to OSC1.
R1–R3	3	O	OSC2	For R-C oscillation using an internal resistor, adjust the internal resistor value. Fluctuation of the resistor value is _30% of the reference value. Care must be taken to avoid fluctuation of the frame frequency in crystal display drive operation.
VLOUT	5	O	V_{LCD} pin/booster capacitance	Potential difference between V_{CC} and GND is boosted twice or three times and then output.
C1+, C1–	16	—	Booster capacitance	External capacitance should be connected here when using the double or triple booster.
C2+, C2–	10	—	Booster capacitance	External capacitance should be connected here when using the triple booster. Must be left disconnected only when using the double booster.
RESET*	1	I	MPU or external R-C circuit	Reset pin. Initializes the LSI when low. Must reset after power-on.
VccDUM	1	O	Input pins	Outputs the internal V_{CC} level; shorting this pin sets the adjacent input pin to the V_{CC} level.
GNDDUM	1	O	Input pins	Outputs the internal GND level; shorting this pin sets the adjacent input pin to the GND level.
TEST	1	I	GND	Test pin. Must be fixed at GND level.
VTEST	1	I	Open	Test pin for the operational amplifier. Must be left disconnected.

Block Function Description

System Interface

The HD66704 has two types of system interfaces: a clock-synchronized serial interface and an E-clock-synchronized 4-bit bus. The interface mode is selected by the IM2/1 pin.

The HD66704 has two 8-bit registers: an instruction register (IR) and a data register (DR).

The IR stores instruction codes, such as clear display and display control, and address information for the display data RAM (DDRAM) and character generator RAM (CGRAM).

The DR temporarily stores the data to be written to and read from the DDRAM or CGRAM. When RS is high, RAM data can be written to the DR. The data written to the DR from the MPU is automatically written to the DDRAM or CGRAM.

Execution time for instruction excluding clear display is 0 clock cycle and instructions can be written in succession.

Address Counter (AC)

The address counter (AC) assigns addresses to DDRAM or CGRAM. When an address set instruction is written into the IR, the address information is sent from the IR to the AC. Selection of DDRAM and CGRAM is also determined concurrently by the RAM select bit (RM).

After writing into (reading from) DDRAM or CGRAM, the AC is automatically incremented by 1 (or decremented by 1). The cursor display position is determined by the address counter value.

Display Data RAM (DDRAM)

The display data RAM (DDRAM) stores data for display as 8-bit character codes in the character display mode. Its capacity is 80×8 bits, or 80 characters, which is equivalent to 20 characters $\times$ 4 lines. One or two lines of character-based display can be selected by software. In the mixed display modes, the remaining two- or three-line DDRAM, which is not used for the character display, is used for 160- or 240-segment displays. The segment display mode allows control of 320 segments. In all three modes, the assignment of DDRAM addresses is the same for all display modes.

The display data RAM (DDRAM) stores data that indicates whether each segment is light or dark, and whether it should blink. In segment-only mode, it carries display data for 80 segments $\times$ 4 common lines since two bits of information are required per segment.

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Character Generator ROM (CGROM)

The character generator ROM (CGROM) generates 5×8-dot character patterns from 8-bit character codes. It is equipped with a memory bank to generate 240 character patterns or 192 character patterns, which can be switched according to applications. For details, see the CGROM Bank Switching Function section. Tables 8 and 9 illustrate the relation between character codes and character patterns for the Hitachi standard CGROM. User-defined character patterns are also available using a mask-programmed ROM (see the Modifying Character Patterns section).

The CGROM cannot be used for the segment mode.

Character Generator RAM (CGRAM)

The character generator RAM (CGRAM) allows the user to redefine the character patterns in the character mode. Two character patterns of 5×8-dot characters can be simultaneously displayed. The DDRAM-specified character code can be selected to display one of these user font patterns.

The CGRAM cannot be used for the segment mode.

Timing Generator

The timing generator generates timing signals for the operation of internal circuits such as DDRAM, CGROM, and CGRAM. The RAM read timing for display and internal operation timing by MPU access are generated separately to avoid interference with one another. This prevents flickering in areas other than the display area when writing the data to the DDRAM, for example.

Cursor/Blink Control Circuit

The cursor/blink (or black-white reversed) control is used to create a cursor or a flashing area on the display in a position corresponding to the location stored in the address counter (AC).

Note: The cursor/blink or black-white reversed control is also active when the address counter indicates the CGRAM. However, it has no effect on the display.
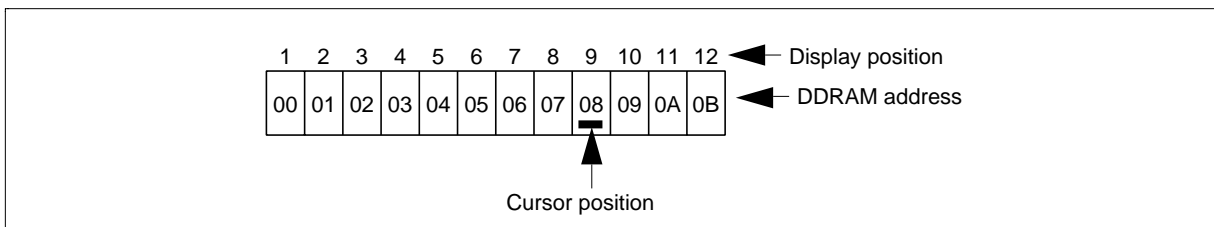
Figure 1 Cursor Position and DDRAM Address (When AC = 08H)

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Oscillation Circuit (OSC)

The HD66704 can provide R-C oscillation simply through the addition of an external oscillation-resistor between the OSC1 and OSC2 pins. The appropriate oscillation frequency for operating voltage, display size, and frame frequency can be obtained by adjusting the external-resistor value. Internal resistors can be used for R-C oscillation. If this is done, care must be taken due to variations in the oscillation frequency caused by fluctuations in internal-resistor values. Clock pulses can also be supplied externally. Since R-C oscillation stops during the standby mode, current consumption can be reduced. For details, see the Oscillation Circuit section.

Liquid Crystal Display Driver Circuit

The liquid crystal display driver circuit consists of 18 common signal drivers (COM1 to COM18) and 80 segment signal drivers (SEG1 to SEG80). When the number of lines are selected by a program, the required common signal drivers automatically output drive waveforms, while the other common signal drivers continue to output deselection waveforms.

The character pattern data is sent serially through a 80-bit shift register and latched when all needed data has arrived. The latched data then enables the segment signal drivers to generate drive waveform outputs.

The shift direction of 80-bit data can be changed by the SGS bit. The shift direction for the common driver can also be changed by the CMS bit by selecting an appropriate direction for the device mounting configuration.

When multiplexing drive is not used, or during the standby or sleep mode, all the above common and segment signal drivers output the GND level, halting the display.

Booster (DC-DC Converter)

The booster doubles or triples a voltage input to the V_{CC} pin. With this, both the internal logic units and LCD drivers can be controlled with a single power supply. For details, see the Power Supply for Liquid Crystal Display Drive section.

V-Pin Voltage Follower

A voltage follower for each voltage level (V1 to V5) reduces current consumption by the LCD drive power supply circuit. No external resistors are required because of the internal bleeder-resistor, which generates different levels of LCD drive voltage. This internal bleeder-resistor can be software-specified from 1/2 bias to 1/5 bias, according to the liquid crystal display drive duty value. The voltage followers can be turned off while multiplexing drive is not being used. For details, see the Power Supply for Liquid Crystal Display Drive section.

Contrast Adjuster

The contrast adjuster can be used to adjust LCD contrast in 25 steps by varying the LCD drive voltage by software. This can be used to select an appropriate LCD brightness or to compensate for temperature.

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DDRAM Address Map

Table 3 DDRAM Addresses and Display Positions in Character Mode (NL2 = 1)

Display Line	Display Digit																(Note 3)			
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
First line	"00"	"01"	"02"	"03"	"04"	"05"	"06"	"07"	"08"	"09"	"0A"	"0B"	"0C"	"0D"	"0E"	"0F"	"10"	"11"	"12"	"13"
Second line	"20"	"21"	"22"	"23"	"24"	"25"	"26"	"27"	"28"	"29"	"2A"	"2B"	"2C"	"2D"	"2E"	"2F"	"30"	"31"	"32"	"33"
third line	"40"	"41"	"42"	"43"	"44"	"45"	"46"	"47"	"48"	"49"	"4A"	"4B"	"4C"	"4D"	"4E"	"4F"	"50"	"51"	"52"	"53"
fourth line	"60"	"61"	"62"	"63"	"64"	"65"	"66"	"67"	"68"	"69"	"6A"	"6B"	"6C"	"6D"	"6E"	"6F"	"70"	"71"	"72"	"73"

(Note 1)

Note: 1. When one line of characters is displayed (NL2-0 = 100), the DDRAM area for the second to fourth lines produces a segment-based display. When two lines of characters are displayed (NL2-0 = 101/110), the DDRAM area for the third to fourth lines produces a segment-based display. When NL2-0 = 110, the font display in the second line is mirror-inverted.

2. When SGS = 0, SEG1/80 to SEG5/76 appear at the first character at the extreme left of the screen. When SGS = 1, SEG80/1 to SEG76/5 appear at the first character at the extreme left of the screen.

3. The 17th to 20th characters are not displayed.

Table 4 Character Display Line and DDRAM Addresses

Display Line	Duty	Display	Common Pin	DDRAM Address
One-line mode (NL = 100)	1/11	Character	COM1-8	00H to 13H
		Segment	COM9	20H to 33H
			COM10	40H to 53H
			COM11	60H to 73H
Two-line mode (NL = 101)	1/18	Character	COM1-8	00H to 13H
			COM9-16	20H to 33H
		Segment	COM17	40H to 53H
			COM18	60H to 73H

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Table 5 DDRAM Addresses and Display Positions in Segment Mode (NL2 = 0)

Common	Segment																			
	1-4	5-8	9-12	13-16	17-20	21-24	25-28	29-32	33-36	37-40	41-44	45-48	49-52	53-56	57-60	61-64	65-68	69-72	73-76	76-80
COM1	"00"	"01"	"02"	"03"	"04"	"05"	"06"	"07"	"08"	"09"	"0A"	"0B"	"0C"	"0D"	"0E"	"0F"	"10"	"11"	"12"	"13"
COM2	"20"	"21"	"22"	"23"	"24"	"25"	"26"	"27"	"28"	"29"	"2A"	"2B"	"2C"	"2D"	"2E"	"2F"	"30"	"31"	"32"	"33"
COM3	"40"	"41"	"42"	"43"	"44"	"45"	"46"	"47"	"48"	"49"	"4A"	"4B"	"4C"	"4D"	"4E"	"4F"	"50"	"51"	"52"	"53"
COM4	"60"	"61"	"62"	"63"	"64"	"65"	"66"	"67"	"68"	"69"	"6A"	"6B"	"6C"	"6D"	"6E"	"6F"	"70"	"71"	"72"	"73"

Note: 1. When SGS = 0, SEG1/80 pin is SEG1.
         When SGS = 1, SEG80/1 pin is SEG1.
       2. COM1 and COM2 are used for a duty cycle of 1/2.
          COM1, COM2, and COM3 are used for a duty cycle of 1/3.

Table 6 DDRAM Data and Segment Display at No Blinking (SB = 0)

DDRAM Data Settin				Segment LCD-Display Control
D7	D6	D5	D4	
0	0	0	0	0 (Always light)
1	1	1	1	1 (Always dark)
SEG1, 5, 9, 13, 17, 21, 25, 29, 33, 37, 41, 45, 49, 53, 57, 61, 65, 69, 73, 77	SEG2, 6, 10, 14, 18, 22, 26, 30, 34, 38, 42, 46, 50, 54, 58, 62, 66, 70, 74, 78	SEG3, 7, 11, 15, 19, 23, 27, 31, 35, 39, 43, 47, 51, 55, 59, 63, 67, 71, 75, 79	SEG4, 8, 12, 16, 20, 24, 28, 32, 36, 40, 44, 48, 52, 56, 60, 64, 68, 72, 76, 80	Segment driver

Note: 1. After the upper four bits have been written to a location, the AC is automatically incremented or
          decremented by 1.
       2. Any setting in the four lower-order bits (D3 to D0) is ignored.

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Table 7 DDRAM Data and Segment Display at Blinking (SB = 1)

DDRAM Data Setting								Segment LCD-Display Control
D7	D3	D6	D2	D5	D1	D4	D0	
0	0	0	0	0	0	0	0	0 (Always light)
0	1	0	1	0	1	0	1	Blinking Display (Note 1)
1	0	1	0	1	0	1	0	Blinking Display in Inverse Mode (Note 2)
1	1	1	1	1	1	1	1	1 (Always dark)
SEG1, 5, 9, 13, 17, 21, 25, 29, 33, 37, 41, 45, 49, 53, 57, 61, 65, 69, 73, 77		SEG2, 6, 10, 14, 18, 22, 26, 30, 34, 38, 42, 46, 50, 54, 58, 62, 66, 70, 74, 78		SEG3, 7, 11, 15, 19, 23, 27, 31, 35, 39, 43, 47, 51, 55, 59, 63, 67, 71, 75, 79		SEG4, 8, 12, 16, 20, 24, 28, 32, 36, 40, 44, 48, 52, 56, 60, 64, 68, 72, 76, 80		Segment driver

Note: 1. Blinking is the repeated activation (darkening) or deactivation (lightening) of a segment for 32 or 64 frames. The blinking cycle (number of frames) is selected by the BL bit.

2. During a blink in normal mode, the segment is activated (darkened). In inverse mode, it is deactivated (lightened).

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Table 8 CGROM Memory Bank 0 (ROM Bit = 0)

Lower Upper	x0	x1	x2	x3	x4	x5	x6	x7	x8	x9	xA	xB	xC	xD	xE	xF
0y	CGRAM (1)	CGRAM (2)	CGRAM (1)	CGRAM (2)	CGRAM (1)	CGRAM (2)	CGRAM (1)	CGRAM (2)	CGRAM (1)	CGRAM (2)	CGRAM (1)	CGRAM (2)	CGRAM (1)	CGRAM (2)	CGRAM (1)	CGRAM (2)
1y																
2y																
3y																
4y																
5y																
6y																
7y																
8y																
9y																
Ay																
By																
Cy																
Dy																
Ey																
Fy																

Table 9 CGROM Memory Bank 1 (ROM Bit = 1)

Lower Upper	x0	x1	x2	x3	x4	x5	x6	x7	x8	x9	xA	xB	xC	xD	xE	xF
0y	CGRAM (1)	CGRAM (2)	CGRAM (1)	CGRAM (2)	CGRAM (1)	CGRAM (2)	CGRAM (1)	CGRAM (2)	CGRAM (1)	CGRAM (2)	CGRAM (1)	CGRAM (2)	CGRAM (1)	CGRAM (2)	CGRAM (1)	CGRAM (2)
1y	CGRAM (1)	CGRAM (2)	CGRAM (1)	CGRAM (2)	CGRAM (1)	CGRAM (2)	CGRAM (1)	CGRAM (2)	CGRAM (1)	CGRAM (2)	CGRAM (1)	CGRAM (2)	CGRAM (1)	CGRAM (2)	CGRAM (1)	CGRAM (2)
2y																
3y																
4y																
5y																
6y																
7y																
8y	CGRAM (1)	CGRAM (2)	CGRAM (1)	CGRAM (2)	CGRAM (1)	CGRAM (2)	CGRAM (1)	CGRAM (2)	CGRAM (1)	CGRAM (2)	CGRAM (1)	CGRAM (2)	CGRAM (1)	CGRAM (2)	CGRAM (1)	CGRAM (2)
9y	CGRAM (1)	CGRAM (2)	CGRAM (1)	CGRAM (2)	CGRAM (1)	CGRAM (2)	CGRAM (1)	CGRAM (2)	CGRAM (1)	CGRAM (2)	CGRAM (1)	CGRAM (2)	CGRAM (1)	CGRAM (2)	CGRAM (1)	CGRAM (2)
Ay																
By																
Cy																
Dy																
Ey																
Fy																

CGRAM Address Map

Table 10 Relationship between Character Mode and CGRAM Address

Font Bank	Memory Bank: ROM = 0, 1															
Character Code	"00"H	"01"H	"02"H	"03"H	"04"H	"05"H	"06"H	"07"H	"08"H	"09"H	"0A"H	"0B"H	"0C"H	"0D"H	"0E"H	"0F"H
CGRAM Address (HEX)	"00"H to "07"H	"08"H to "0F"H	"00"H to "07"H	"08"H to "0F"H	"00"H to "07"H	"08"H to "0F"H	"00"H to "07"H	"08"H to "0F"H	"00"H to "07"H	"08"H to "0F"H	"00"H to "07"H	"08"H to "0F"H	"00"H to "07"H	"08"H to "0F"H	"00"H to "07"H	"08"H to "0F"H
Font Bank	Memory Bank: ROM = 1															
Character Code	"10"H "80"H "90"H	"11"H "81"H "91"H	"12"H "82"H "92"H	"13"H "83"H "93"H	"14"H "84"H "94"H	"15"H "85"H "95"H	"16"H "86"H "96"H	"17"H "87"H "97"H	"18"H "88"H "98"H	"19"H "89"H "99"H	"1A"H "8A"H "9A"H	"1B"H "8B"H "9B"H	"1C"H "8C"H "9C"H	"1D"H "8D"H "9D"H	"1E"H "8E"H "9E"H	"1F"H "8F"H "9F"H
CGRAM Address (HEX)	"00"H to "07"H	"08"H to "0F"H	"00"H to "07"H	"08"H to "0F"H	"00"H to "07"H	"08"H to "0F"H	"00"H to "07"H	"08"H to "0F"H	"00"H to "07"H	"08"H to "0F"H	"00"H to "07"H	"08"H to "0F"H	"00"H to "07"H	"08"H to "0F"H	"00"H to "07"H	"08"H to "0F"H

Note: In the character mode, CGRAM font pattern is displayed using character codes set to DDRAM as per the above table.

Table 11 Relationship between CGRAM Address and Character Pattern (CGRAM Data)

Character Code	"00"H					Character Code	"01"H				
CGRAM Address	D4	D3	D2	D1	D0	CGRAM Address	D4	D3	D2	D1	D0
"00"H	0	1	1	1	0	"08"H	1	1	1	1	0
"01"H	1	0	0	0	1	"09"H	1	0	0	0	1
"02"H	1	0	0	0	1	"0A"H	1	0	0	0	1
"03"H	1	0	0	0	1	"0B"H	1	1	1	1	0
"04"H	1	1	1	1	1	"0C"H	1	0	0	0	1
"05"H	1	0	0	0	1	"0D"H	1	0	0	0	1
"06"H	1	0	0	0	1	"0E"H	1	1	1	1	0
"07"H	0	0	0	0	0	"0F"H	0	0	0	0	0

Notes: 1. The 8th raster-row is the cursor position and its display is formed by a logical OR with the cursor.
2. A set bit in the CGRAM data corresponds to display selection 1 (darkened) and 0 to non-selection (lightened).

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Modifying Character Patterns

Character Pattern Development Procedure

User | Hitachi

Start

Determine character patterns (1)

Create EPROM address and data listing (2)

Write EPROM (3)

EPROM → Hitachi (4)

Computer processing

Create character pattern listing (5)

Evaluate character patterns

OK ? No / Yes

Art work

Masking

Trial

Sample

Sample evaluation (6)

OK ? No / Yes

Mass production
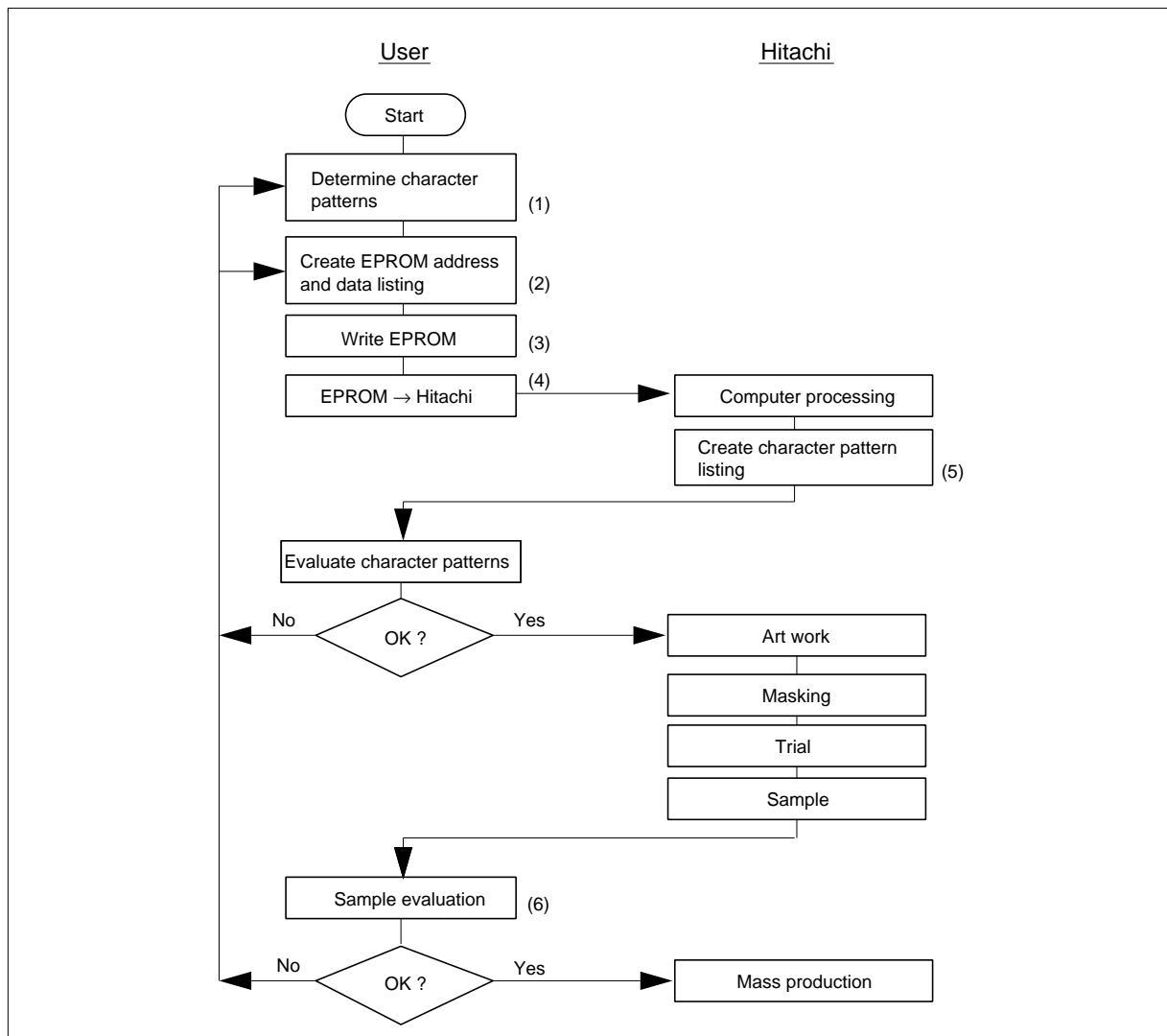
Figure 2 Character Pattern Development Procedure

The following operations correspond to the numbers listed in figure 2:

1. Determine the correspondence between character codes and character patterns.
2. Create a listing indicating the correspondence between EPROM addresses and data.
3. Program the character patterns into an EPROM.
4. Send the EPROM to Hitachi.

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5. Computer processing of the EPROM is performed at Hitachi to create a character pattern listing, which is sent to the user.

6. If there are no problems within the character pattern listing, a trial LSI is created at Hitachi and samples are sent to the user for evaluation. When the user confirms that the character patterns are correctly written, Hitachi will commence LSI mass production.

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Programming Character Patterns

This section explains the correspondence between addresses and data used to program character patterns in EPROM.

Programming to EPROM: The HD66704 character generator ROM can generate 432 5×8-dot character patterns. Table 12 shows the correspondence between the EPROM address, data, and the character pattern.

Table 12   Examples of Correspondence between EPROM Address, Data, and Character Pattern (5×8 Dots)

A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	O_4	O_3	O_2	O_1	O_0
0	0	1	0	1	1	0	0	1	0	0	0	0	1	0	0	0	1
									0	0	0	1	1	0	0	0	1
									0	0	1	0	1	0	0	0	1
									0	0	1	1	0	1	0	1	0
									0	1	0	0	0	0	1	0	0
									0	1	0	1	0	0	1	0	0
									0	1	1	0	0	0	1	0	0
									0	1	1	1	0	0	0	0	0

Column groups: EPROM Address (A12 to A0); Data with MSB at O4 and LSB at O0.

ROM bit: A12. Character code: A11 to A4. 0: A3. Line position: A2 to A0.

Notes: 1. EPROM address: Bit A12 corresponds to the CGROM memory bank switch bit ("ROM").
2. EPROM address: Bits A11 to A4 correspond to a character code.
3. EPROM address: Bits A2 to A0 specify the line position of the character pattern. EPROM address bit A3 must be set to 0.
4. EPROM data: Bits O4 to O0 correspond to character pattern data.
5. Areas which are darkened (indicated by shading) are stored as 1, and lightened areas as 0.
6. The eighth raster-row is also stored in the CGROM, and must also be programmed. If the eighth raster-row is used for a cursor, this data must all be set to zero.
7. EPROM data: Bits O7 to O5 are invalid. 0 must be written in all bits.

Handling Unused Character Patterns:

1. EPROM data outside the character pattern area: This is ignored by character generator ROM for display operation so any data is acceptable.
2. EPROM data in CGRAM area: Always fill with zeros.
3. Treatment of unused user patterns in the HD66704 EPROM: Depending on to the user application, these are handled in either of two ways:
   a. When unused character patterns are not programmed: If an unused character code is written into DDRAM, all its dots are darkened, because the EPROM is filled with 1s after it is erased.

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b.   When unused character patterns are programmed as 0s: Nothing is displayed even if unused character codes are written into DDRAM. (This is equivalent to a space.)

Instructions

Outline

Only the instruction register (IR) and the data register (DR) of the HD66704 can be controlled by the MPU. Before starting internal operation of the HD66704, control information is temporarily stored in these registers to allow interfacing with various peripheral control devices or MPUs which operate at different speeds. The internal operation of the HD66704 is determined by signals sent from the MPU. These signals, which include the register selection signal (RS) and the data bus signals (D7 to D0), make up the HD66704 instructions. There are four categories of instructions that:

- Control the display
- Control power management
- Set internal RAM addresses
- Write data to the internal RAM

Normally, instructions that perform data transfer with the internal RAM are used the most. However, auto-incrementation by 1 (or auto-decrementation by 1) of internal HD66704 RAM addresses after each data write can lighten the MPU program load.

Because instructions other than clear display instruction are executed in 0 cycle, instructions can be written in succession.

While the clear display instruction is being executed for internal operation, or during reset, no instruction other than the key scan read instruction can be executed.

Instruction Descriptions

Clear Display

The clear display instruction writes space code 20H (the character pattern for character code 20H must be a blank pattern) into all DDRAM addresses. It then sets DDRAM address 0 into the address counter. It also sets I/D to 1 (increment mode) in the entry mode set instruction. Since the execution of this instruction needs 85 clock cycles, do not send the next instruction during the execution time.

In segment mode, if 20H is explicitly written to the DDRAM after the display has been cleared, the result will be the activation (darkening) of a segment.

RS	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	1

Figure 3 Clear Display Instruction

Return Home

The return home instruction sets DDRAM address 0 into the address counter. The DDRAM contents do not change. The cursor or blinking goes to the top left of the display.

RS	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	1	0

Figure 4 Return Home Instruction

Start Oscillation

The start oscillation instruction restarts the oscillator from the halt state in the standby mode. After issuing this instruction, wait at least 10 ms for oscillation to stabilize before issuing the next instruction. (Refer to the Standby Mode section.)

RS	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	1	1

Figure 5 Start Oscillation Instruction

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Driver Output Control

CMS: Selects the output shift direction of a common driver. When CMS = 0, COM1/18 shifts to COM1, and COM18/1 to COM18. When CMS = 1, COM1/18 shifts to COM18, and COM18/1 to COM1. Output position of a common driver shifts depending on the CEN bit setting. For details, see the Display On/Off Control section.

SGS: Selects the output shift direction of a segment driver. When SGS = 0, SEG1/80 shifts to SEG1, and SEG80/1 to SEG80. When SGS = 1, SEG1/80 shifts SEG80, and SEG80/1 to SEG1.

RS	D7	D6	D5	D4	D3	D2	D1	D0	Initial value
0	0	0	0	0	0	1	CMS	SGS	CMS = "0" SGS = "0"

Figure 6 Driver Output Control Instruction

Power Control

AMP: When AMP = 1, each voltage follower for the V1 to V5 pins and the booster are turned on. When AMP = 0, current consumption can be reduced when the display is not being used.

SLP: When SLP = 1, the HD66704 enters the sleep mode, where the internal operations are halted except for the R-C oscillator, thus reducing current consumption. For details, refer to the Sleep Mode section. Only the power-control instructions (AMP, SLP, and STB bits) can be executed during the sleep mode.

During the sleep mode, the other RAM data and instructions cannot be updated although they are retained.

STB: When STB = 1, the HD66704 enters the standby mode, where all the internal operations including the internal R-C oscillator completely stop. For details, refer to the Standby Mode section. Only the following instructions can be executed during the standby mode.

  a. Standby mode cancel (STB = 0)
  b. Voltage follower circuit on/off (AMP = 1/0)
  c. Start oscillator

During the standby mode, the other RAM data and instructions may be lost. To prevent this, they must be set again after the standby mode is canceled.

RS	D7	D6	D5	D4	D3	D2	D1	D0	Initial value
0	0	0	0	0	1	AMP	SLP	STB	AMP = "0" SLP = "0" STB = "0"

Figure 7 Power Control Instruction

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Contrast Control 1/2

SW: Switches the bit configuration for the contrast control instruction. SW = 0 corresponds to CT2 to CT0. SW = 1 corresponds to BT and BS1 to BS0.

CT4–CT0: When SW = 0 controls the LCD drive voltage (potential difference between V1 and GND) to adjust contrast. A 25-step adjustment is possible. For details, refer to the Contrast Adjuster section.

BT1-0: When SW = 1, it selects the output factor for boosting. When BT = 0, it doubles boosting. When BT = 1, it triples boosting.

BS1-0: When SW = 1, it sets the crystal display drive bias value within the range of 1/2 to 1/5 bias. The liquid crystal display drive bias value can be selected according to its drive duty ratio and voltage. For details, see the Liquid Crystal Display Drive Bias Selector Circuit section.

RS	D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	1	0	SW	CT4	CT3	
0	0	0	0	1	1	CT2	CT1	CT0	(SW = "0")
						BT	BS1	BS0	(SW = "1")

Initial value
BT = "0"
BS1/0 = "00"
CT4–0 = "00000"

Figure 8 Contrast Control 1/2 Instruction
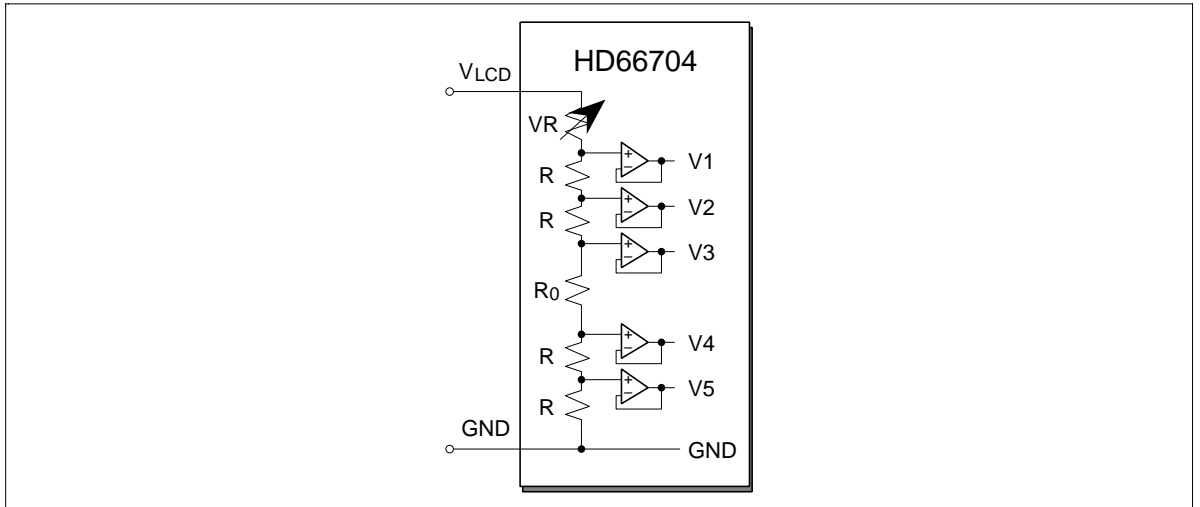
Figure 9 Contrast Adjuster

Table 13 CT Bits and Variable Resistor Value of Contrast Adjuster

CT Set Value					Variable	CT Set Value					Variable
CT4	CT3	CT2	CT1	CT0	Resistor (VR)	CT4	CT3	CT2	CT1	CT0	Resistor (VR)
0	0	0	0	0	2.5 x R (Initial value)	1	0	0	0	0	1.6 x R
0	0	0	0	1	2.5 x R	1	0	0	0	1	1.5 x R
0	0	0	1	0	2.5 x R	1	0	0	1	0	1.4 x R
0	0	0	1	1	2.5 x R	1	0	0	1	1	1.3 x R
0	0	1	0	0	2.5 x R	1	0	1	0	0	1.2 x R
0	0	1	0	1	2.5 x R	1	0	1	0	1	1.1 x R
0	0	1	1	0	2.5 x R	1	0	1	1	0	1.0 x R
0	0	1	1	1	2.5 x R	1	0	1	1	1	0.9 x R
0	1	0	0	0	2.4 x R	1	1	0	0	0	0.8 x R
0	1	0	0	1	2.3 x R	1	1	0	0	1	0.7 x R
0	1	0	1	0	2.2 x R	1	1	0	1	0	0.6 x R
0	1	0	1	1	2.1 x R	1	1	0	1	1	0.5 x R
0	1	1	0	0	2.0 x R	1	1	1	0	0	0.4 x R
0	1	1	0	1	1.9 x R	1	1	1	0	1	0.3 x R
0	1	1	1	0	1.8 x R	1	1	1	1	0	0.2 x R
0	1	1	1	1	1.7 x R	1	1	1	1	1	0.1 x R

Table 14 BS Bits and LCD Drive Bias Value

BS1	BS0	Liquid Crystal Display Drive Bias Value	
0	0	1/5 bias drive	(Initial value)
0	1	1/4 bias drive	
1	0	1/3 bias drive	
1	1	1/2 bias drive	

Entry Mode Set

ROM: Switches the CGROM memory bank in the character mode (NL2 = 1). Uses bank 0 for display when ROM = 0 and bank 1 for display when ROM = 1. For details, see the CGROM Bank Switching Function section.

I/D: Increments (I/D = 1) or decrements (I/D = 0) the DDRAM address by 1 when a character code is written into DDRAM. The cursor or blinking moves to the right when incremented by 1 and to the left when decremented by 1. The same applies to the writing of CGRAM.

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SB: Switches blinking of the segment display on and off. When SB = 0, the segments do not blink, and the data for display is more efficiently written by only using the upper four bits (D7 to D4) of the DDRAM. When SB = 1, blinking is enabled for any segment, and two bits of display data is used for each segment by using all eight bits of each byte in the DDRAM. In character mode (NL2 = 1), be sure to set SB to 1. For details, see the Segment Display Function section.

RS	D7	D6	D5	D4	D3	D2	D1	D0	Initial value
0	0	0	1	0	0	ROM	I/D	SB	ROM = "0" I/D = "1" SB = "0"

Figure 10 Entry Mode Set Instruction

Cursor Control

B/W: When B/W = 1 and LC = 0, the character at the cursor position is cyclically blink-displayed with black-white inversion. The blinking cycle is selected by the BL bit in the display on/off control register.

When B/W = 1 and LC = 1, all characters including the cursor on the display line appear with black-white inversion. The characters do not blink. For details, refer to the Line-Cursor Display section.

C: The cursor is displayed on the 8th raster-row when C = 1. The 5-dot cursor is ORed with the character pattern and displayed on the 8th raster-row.

B: The character indicated by the cursor blinks when B = 1 in the character mode (NL2 = 1). The blinking is displayed as switching between all black dots and displayed characters when B/W = 0. When B/W = 1, cursor blinking switches between all white dots and the display of the character at the cursor position. The cursor in the 8th raster-row and blinking can be set for simultaneous display. The blinking cycle is selected by the BL bit in the display on/off control register.

RS	D7	D6	D5	D4	D3	D2	D1	D0	Initial value
0	0	0	1	0	1	B/W	C	B	B/W = "0" C = "0" B = "0"

Figure 11 Cursor Control Instruction
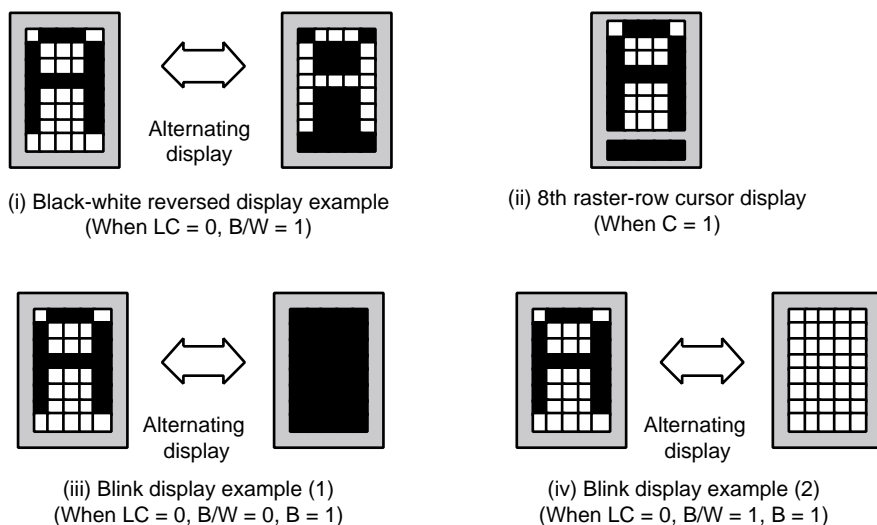
Figure 12 Cursor Control Examples

Display On/Off Control

D: Display is on when D = 1 and off when D = 0. When off, the display data remains in DDRAM, and can be displayed instantly by setting D to 1. When D is 0, the display is off with the SEG1 to SEG72 (96) outputs, COM1 to COM24 outputs, and COMS1/2 output set to the GND level and off. Because of this, the HD66704 can control charging current for the LCD with AC driving.

BL: Sets the blinking cycle in the character and segment modes. The display is switched every 32 frames when BL = 0. It is also switched every 64 frames when BL = 1.

LC: When LC = 1, a cursor attribute is assigned to the line that contains the address counter (AC) value. Cursor mode can be selected with the B/W, C, and B bits. Refer to the Line-Cursor Display section.

RS	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	1	0	D	BL	LC

Initial value
D = "0"
BL = "0"
LC = "0"

Figure 13 Display On/Off Control Instruction

Display Line Control

NL2-0: Specifies the display lines. Display lines change the liquid crystal display drive duty ratio. DDRAM address mapping does not depend on the number of display lines. When NL = 110, the character fonts from the CGROM/CGRAM are mirror-inverted for display on the second line alone. Wiring on the LCD glass is used to display one 32-character line. For details, see the LCD Panel Interface section.

RS	D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	1	1	1	NL2	NL1	NL0	Initial value NL2–0 = "101"

Figure 14 Display Line Control Instruction

Table 15 NL Bits and Display Lines

NL2	NL1	NL0	Display Lines	Liquid Crystal Display Drive Duty Ratio	Common Driver Used
0	0	0	1/2-duty segment	1/2 duty	COM1 to COM2
0	0	1	1/3-duty segment	1/3 duty	COM1 to COM3
0	1	0	1/4-duty segment	1/4 duty	COM1 to COM4
0	1	1	Setting inhibited	-	-
1	0	0	One character line + segment display	1/11 duty	COM1 to COM11
1	0	1	Two character lines + segment display	1/18 duty	COM1 to COM18 (Initial value)
1	1	0	Two character lines + segment display (fonts in the second line are horizontally inverted)	1/18 duty	COM1 to COM18

Double-Height Display Control

DL: When DL = 1, the first line is displayed at double height. Do not insert a space between the first and second lines when the double-height display function is used. For details, see the Double-Height Display section.

RS	D7	D6	D5	D4	D3	D2	D1	D0	
0	0	1	0	0	0	0	0	DL	Initial value DL = "0"

Figure 15 Double-Height Display Control Instruction

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Blink Synchronization

Initializes the blink counter to control the blinking cycle of the cursor or segment. After initialization, be sure to lighten the display. When this instruction is issued every second, the blinking cycle will be one second, in dependent of the LCD frame frequency. When the blinking is synchronized every second and the frame frequency is near 100 Hz, make the display blink for 64 frames by setting BL to 1.

RS	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	1	0	0	0	0

Figure 16 Blink Synchronization Instruction

RAM Address Set

RM: Selects DDRAM and CGRAM. The selected RAM is accessed with this setting.

AD6-0: Initially sets RAM addresses to the address counter (AC). Once RAM data is accessed, the AC is automatically updated according to the I/D bit. This allows consecutive accesses without resetting addresses. RAM address setting is not allowed in the sleep mode or standby mode.

RS	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	RM	0	0	0	0	AD6
0	1	1	AD5	AD4	AD3	AD2	AD1	AD0

Figure 17 RAM Address Set Instruction

Table 16 AD Bits and DDRAM Setting

RM	AD6-AD0	DDRAM Setting
0	"00"H-"13"H	Display data on the 1st line
0	"20"H-"33"H	Display data on the 2nd line
0	"40"H-"53"H	Display data on the 3rd line
0	"60"H-"73"H	Display data on the 4th line

Table 17   AD Bits and CGRAM Setting

RM	AD3-AD0	CGRAM Setting
1	"0"H-"7"H	Font data of CGRAM (1)
1	"8"H-"F"H	Font data of CGRAM (2)

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Write Data to RAM

WD7-0 : Writes 8-bit data to DDRAM and CGRAM. DDRAM or CGRAM is selected by the previous specification of the RM bit. After a write, the address is automatically incremented or decremented by 1 according to the I/D bit setting in the entry mode set instruction. During the sleep and standby modes, DDRAM or CGRAM cannot be accessed.

RS	D7	D6	D5	D4	D3	D2	D1	D0
1	WD7	WD6	WD5	WD4	WD3	WD2	WD1	WD0
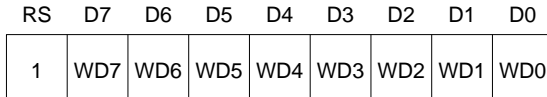
Figure 18 Write Data to RAM Instruction

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Table 18 Instruction List

Register Name	Code									Description	Execution Cycle*
	RS	D7	D6	D5	D4	D3	D2	D1	D0		
NOP	0	0	0	0	0	0	0	0	0	No operation. No processing is executed.	0
Clear display	0	0	0	0	0	0	0	0	1	Clears entire display and sets address 0 into the address counter (AC).	85
Return home	0	0	0	0	0	0	0	1	0	Sets DDRAM address 0 into the address counter (AC).	0
Start oscillator	0	0	0	0	0	0	0	1	1	Starts the oscillation standby mode.	—
Driver output control	0	0	0	0	0	0	1	CMS	SGS	Selects the common driver shift direction (CMS) and segment driver shift direction (SGS).	0
Power control	0	0	0	0	0	1	AMP	SLP	STB	Turns on LCD power supply (AMP), and sets the sleep mode (SLP) and standby mode (STB).	0
Contrast control 1	0	0	0	0	1	0	SW	CT4	CT3	Sets the register selection (SW) or upper contrast adjustment bits (CT4-3).	0
Contrast control 2	0	0	0	0	1	1	CT2	CT1	CT0	Sets the lower contrast adjustment bits (CT2-0), step-up factor (BT), or LCD bias value (BS1-0).	0
							BT	BS1	BS0		
Entry mode set	0	0	0	1	0	0	ROM	I/D	SB	Sets the CGROM memory bank switching (ROM), address update direction (I/D), and segment blink control (SB).	0
Cursor control	0	0	0	1	0	1	B/W	C	B	Sets black-white inverting cursor (B/W), 8th raster-row cursor (C), and blink cursor (B).	0
Display on/off control	0	0	0	1	1	0	D	BL	LC	Sets display on (D), blinking cycle (BL), and line cursor display (LC).	0
Display line control	0	0	0	1	1	1	NL2	NL1	NL0	Sets the number of display lines (drive duty).	0
Double-height display control	0	0	1	0	0	0	0	0	DL	Specifies double-height display lines (DL).	0
Blink synchronization	0	0	1	1	1	0	0	0	0	Synchronizes the blink counter.	0
RAM address set (upper bits)	0	1	0	RM	0	0	0	0	AD6 (upper bit)	Sets the RAM selection (RM) and most upper RAM address (AD6) to the DDRAM.	0

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Table 18 Instruction List (cont)

Register Name		Code								Description	Exe-cution Cycle*
	RS	D7	D6	D5	D4	D3	D2	D1	D0		
RAM address set (lower bits)	0	1	1			AD5-0 (lower bits)				Sets the initial lower RAM addresses (AD5-0) to the address counter (AC).	0
Write data to RAM	1				Write data					Writes data to DDRAM or CGRAM.	0

Note: Represented by the number of operating clock pulses; the execution time depends on the supplied clock frequency or the internal oscillation frequency.

Bit definition:

CMS = 0: COM1/18 => COM1

SGS = 0: SEG1/80 => SEG1

AMP = 1: Operational amplifier and booster circuit on

SLP = 1: Sleep mode

STB = 1: Standby mode

SW = 0: CT4-0 access/SW = 1: BS2-0 access

CT4-0: Contrast adjustment

BT = 0: Boost level selection (0: double, 1: triple)

BS1-0: LCD drive bias selection (00: 1/5, 01: 1/4, 10: 1/3, 11: 1/2)

ROM = 0: CGROM bank 0 selection/ROM = 1: CGROM bank 1 selection

ID = 1: Address increment

ID = 0: Address decrement

SB = 0: No segment blink

SB = 1: Segment blink

B/W = 1: Black-white inverting cursor on

C = 1: 8th raster-row cursor on

B = 1: Blink cursor on

D = 1: Display on

BL = 0: Blink every 32 frames

BL = 1: Blink every 64 frames

LC = 1: Cursor display for the all display lines including AC

NL2-0: Drive duty setting (000: 1/2 duty ratio, 001: 1/3 duty ratio, 010: 1/4 duty ratio, 100: 1/11 duty ratio, 101/110: 1/18 duty ratio)

DL = 1: Double-height display for the first line

RM: RAM selection (0: DDRAM, 1: CGRAM)

ADD6-0: DDRAM/CGRAM address set (DDRAM: 00H-73FH, CGRAM: 0H-FH)

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Reset Function

The HD66704 is internally initialized by RESET input. During initialization, the system executes a clear display instruction after reset is canceled. The system executes the other instructions during the reset period. Because the busy flag (BF) indicates a busy state (BF = 1) during the reset period and execution of the clear display instruction following reset cancellation, no instruction or RAM data access from the MPU is accepted. Here, reset input must be held back for at least 1 ms, and an issuing instruction must wait for 500 clock cycles after reset is canceled because the display clearing continues after reset cancellation.

When this function is used in the character mode (NL2 = 1) and the DDRAM contains character code data, set SB = 1.

Instruction Set Initialization:

1. Clear display executed (Writes 20H to DDRAM)
2. Return home executed (Sets the address counter (AC) to 00H to select DDRAM)
3. Start oscillator executed
4. Driver output control (SGS = 0, CMS = 0)
5. Power control (AMP = 0: LCD power off, SLP = 0: Sleep mode off, STB = 0: Standby mode off)
6. Double boost (BT = 0), 1/5 bias drive (BS1/0 = 00), Weak contrast (CT4-0 = 00000)
7. Entry mode set (ROM = 0: CGROM bank 0, I/D = 1: Increment by 1, SB = 0: No segment blinking)
8. Cursor display off (B/W = 0, C = 0, B = 0)
9. Display on/off control (D = 0: Display off, BL = 0: 32-frame blinking, LC = 0: Line-cursor off)
10. Display control (NL2/1/0 = 101: 1/18 duty ratio)
11. Double-height display off (DL = 0)

RAM Data Initialization:

1. DDRAM

   All addresses are initialized to 20H by the clear display instruction after the reset is canceled.
2. CGRAM

   This is not automatically initialized by reset input but must be initialized by software while display is off (D = 0)

Output Pin Initialization:

1. LCD driver output pins (SEG/COM): Outputs GND level
2. Booster output pins (VLOUT): Outputs V_{CC} level
3. Oscillator output pin (OSC2): Outputs oscillation signal

Clock-Synchronized Serial Interface

Setting the IM1 and IM2 pins (interface mode pins) to the GND level allows standard clock-synchronized serial data transfer, using the chip select line (CS*), serial data line (SDA), and serial transfer clock line (SCL). For a serial interface, the DB0/ID pin function uses an ID pin.

The HD66704 initiates serial data transfer by transferring the start byte at the falling edge of CS* input. They end serial data transfer at the rising edge of CS* input.

The HD66704 is selected when the 6-bit chip address in the start byte transferred from the transmitting device matches the 6-bit device identification code assigned to the HD66704. The HD66704, when selected, receives the subsequent data string. The least significant bit of the identification code can be determined by the ID pin. The five upper bits must be 01110. Two different chip addresses must be assigned to a single HD66704 because the seventh bit of the start byte is used as a register select bit (RS): that is, when RS = 0, an instruction can be issued, and when RS = 1, the data can be written to RAM. Therefore, assign two chip addresses to one HD66704. Be sure to set 0 to the eighth bit of the start byte (R/W bit) as shown in table 19.

After receiving the start byte, the HD66704 receives or transmits the subsequent data byte-by-byte. The data is transferred in the MSB-first format. To transfer the data consecutively, note that only the display-clear instruction requires a longer execution time than the others (see table 18).

Table 19 Start Byte Format

Transfer Bit	S	1	2	3	4	5	6	7	8
Start byte format	Transfer start	Device ID code						RS	0
		0	1	1	1	0	ID		

Note: The ID bit is selected by the DB0/ID pin.

Table 20 RS Bit Function of Clock-Synchronized Serial Interface Data

RS	Function
0	Writes instruction
1	Writes RAM data

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a) Basic Data-Transfer Timing through Clock-Synchronized Serial Bus Interface
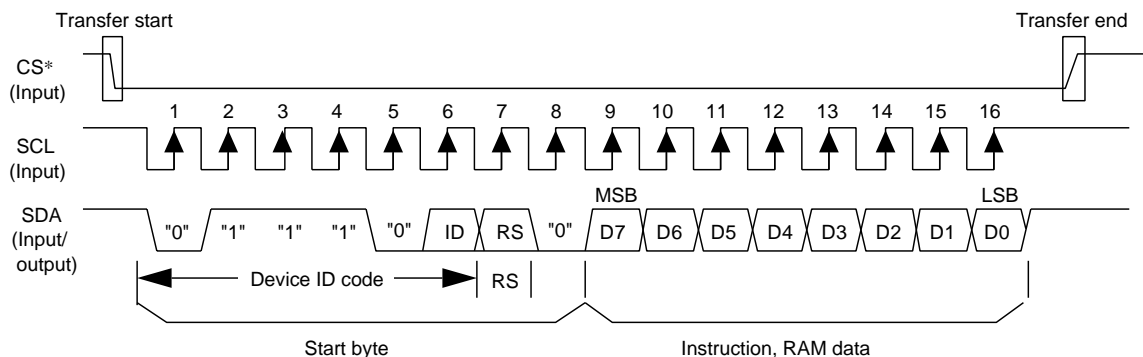
b) Consecutive Data-Transfer Timing Through Clock-Synchronized Serial Bus interface
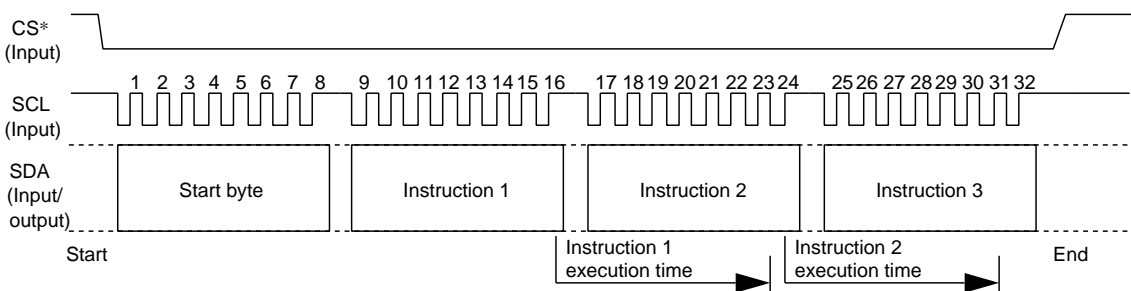
Note: When instruction 1 is a clear display instruction, adjust the transfer rate so that the 8th bit of instruction 2 is transferred after execution of the clear display instruction.

Figure 19 Clock-Synchronized Serial Interface Timing Sequence

4-Bit Bus Interface

Setting the IM2-1 (interface mode) to the GND/V_{CC} level allows 68-system 4-bit bus interface (DB3 to DB0). A direct interface using the 4-bit E-clock-synchronized bus or an interface via the I/O bus can be established. 8-bit instructions and RAM data are divided into four upper bits (D7 to D4) and lower bits (D3 to D0) and transfer starts.
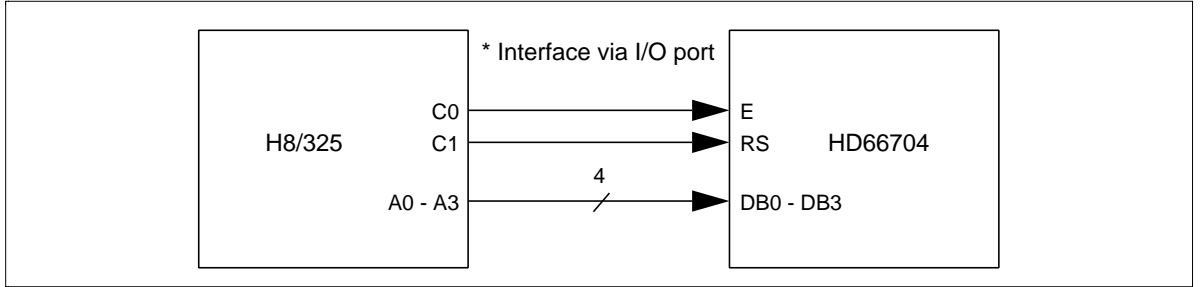
Figure 20 Interface to 4-Bit Microcomputer

The HD66704 supports transfer synchronization function which resets the upper/lower counter to count upper/lower four-bit data transfer in the 4-bit bus interface. Noise causing transfer mismatch between the four upper and lower bits can be corrected by a reset triggered by consecutively writing a 0000 instruction (NOP) four times.   The next transfer starts from the upper four bits. Executing synchronization function periodically can recover any runaway in the display system.
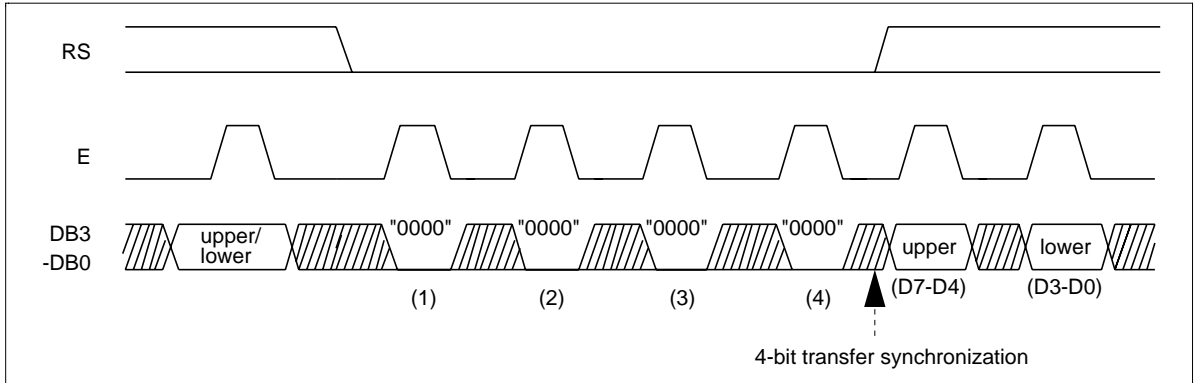
Figure 21 4-Bit Transfer Synchronization

Oscillator Circuit

The HD66704 can either be supplied with operating pulses externally (external clock mode), oscillate using an internal CR oscillator with an external oscillator-resistor (external resistor oscillation mode), or oscillate using an internal oscillator-resistor (internal resistor oscillation mode). Internal oscillator-resistors fluctuate by ±30% depending on products. Avoid frame frequency fluctuations as these affect video quality. To prevent these, use an external resistor.

1) External clock mode

Clock (32 kHz) → OSC1

HD66704

2) External resistor oscillation mode

OSC1
OSC2
Rf

HD66704

The oscillator frequency can be adjusted by oscillator resistor (Rf). If Rf is increased or power supply voltage is decreased, the oscillator frequency decreases. For the relationship between Rf resistor value and oscillation frequency, see the Electric Characteristics Footnote section.

3) Internal resistor oscillation mode

OSC1
R1   Rf 0 (=650 kΩ/typ.)
R2   Rf 1 (=150 kΩ/typ.)
R3   Rf 2 (=100 kΩ/typ.)
OSC2

HD66704

Note that the internal resistors RF0, RF1, and RF2 fluctuate by ±30% depending on products.
i) R1 - OSC2 short-circuiting
   $Rf = Rf_0 = 650$ kΩ (typ.)
ii) R1 - R2 short-circuiting, R3-OSC2 short-circuiting
   $Rf = Rf_0 + Rf_2 = 750$ kΩ (typ.)
iii) R2 - OSC2 short-circuiting
   $Rf = Rf_0 + Rf_1 = 800$ kΩ (typ.)
iv) R3 - OSC2 short-circuiting
   $Rf = Rf_0 + Rf_1 + Rf_2 = 900$ kΩ (typ.)

Figure 22 Oscillator Circuits

Table 21 Multiplexing Duty Ratio and LCD Frame Frequency (fosc = 32 kHz)

	Segment Display			One character line	Two character lines
	NL = 000	NL = 001	NL = 010	NL = 100	NL = 101/110
Drive duty	1/2	1/3	1/4	1/11	1/18
Total clocks/frame	360	360	360	352	360
Frame frequency	88 Hz	88 Hz	88 Hz	91 Hz	88 Hz
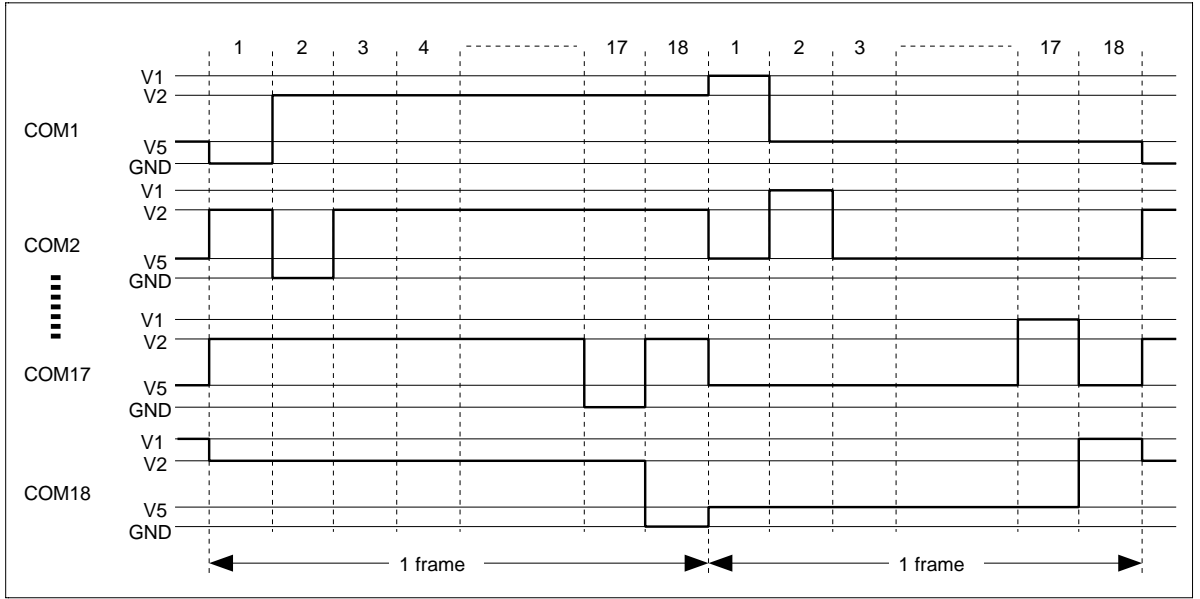
Figure 23 LCD Drive Output Waveform (2-Line Character Display with 1/18 Multiplexing Duty Ratio)

Power Supply for Liquid Crystal Display Drive

When External Power Supply is Used

To supply LCD drive voltage directly from the external power supply without using the internal booster, circuits should be connected as shown in figure 24. Here, contrast can be adjusted through the CT bits of the contrast control instruction.

When the operational amplifier is used (AMP = 1), be sure to boost the external power supply VLCD to double V_{CC} and set the BT bit to 0. When an operational amplifier is not used (AMP = 0), VLCD must be equal to or higher than V_{CC}.

The HD66704 incorporates a voltage-follower operational amplifier for each V1 to V5 to reduce current flowing through the internal bleeder-resistors, which generate different levels of LCD drive voltages. Thus, potential differences between VLCD and V1 and between V5 and GND must be 0.1 V or higher. If the display quality is poor, place a capacitor of about 0.1 μF to 0.47 μF between each internal operational amplifier output V1OUT to V5OUT and GND and stabilize the output level of the operational amplifier. Adjust the value of the capacitor if necessary after visually checking the display quality on the LCD panel.
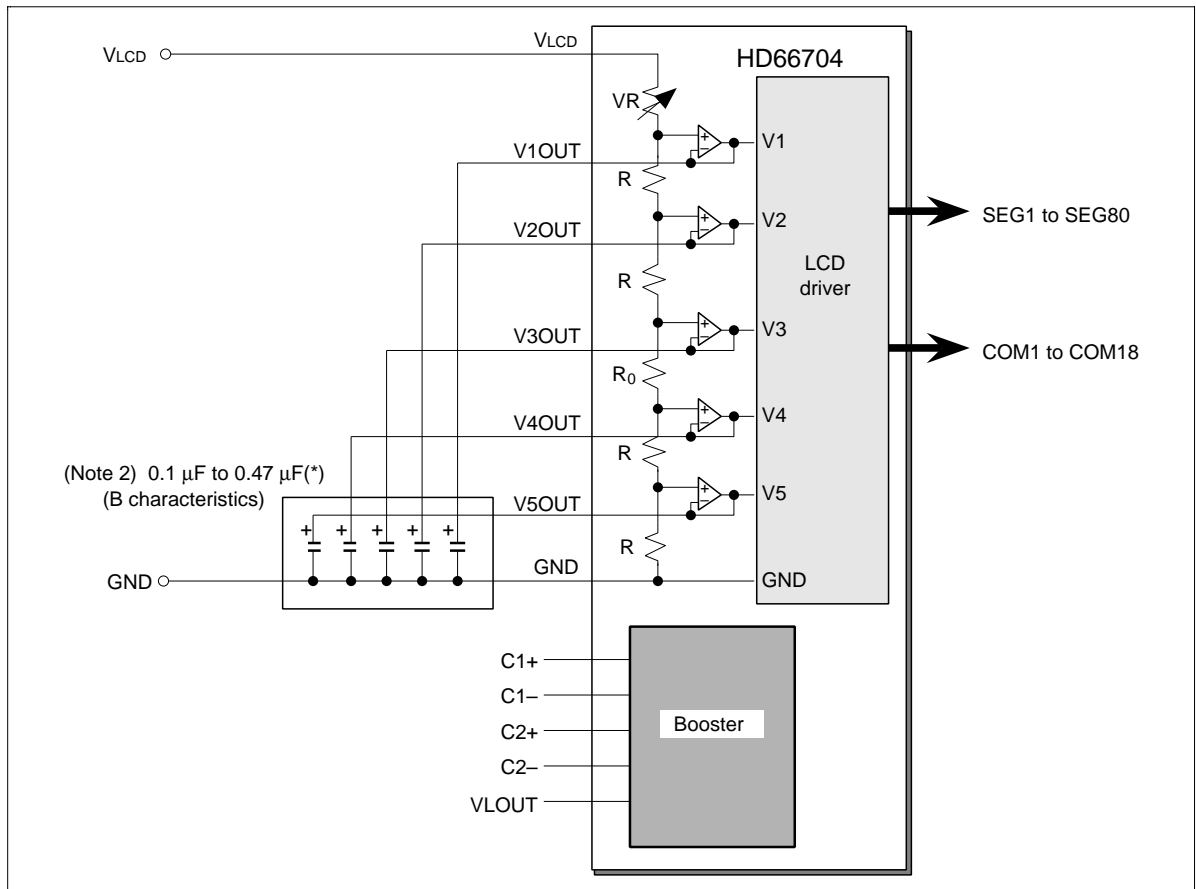
Figure 24 External Power Supply Circuit for LCD Drive Voltage Generation

Notes: 1. Adjust the value of the capacitor (*) after it is mounted on the LCD panel.

2. The capacitor to be connected to V1OUT to V5OUT must be able to withstand the VLCD voltage. Consider changes in the VLCD voltage and the breakdown voltage of the capacitor.

When an Internal Booster is Used

To supply LCD drive voltage using the internal booster, circuits should be connected as shown in figure 25. Here, contrast can be adjusted through the CT bits of the contrast adjustment register.

The reference power-supply voltage in the booster is between V_{CC} and GND. Be careful when lowering the V_{CC} voltage since the LCD drive current flows on the V_{CC} and GND pins.

The HD66704 incorporates a voltage-follower operational amplifier for each of V1 to V5 to reduce current flowing through the internal bleeder-resistors, which generate different LCD drive voltages. Thus, the potential differences between VLCD and V1 and between V5 and GND must be 0.1 V or higher. If the display quality is poor, place a capacitor of about 0.1 µF to 0.47 µF between each internal operational amplifier output V1OUT to V5OUT and GND and stabilize the output level of the operational amplifier. Adjust the value of the capacitor if necessary after visually checking the display quality on the LCD panel.
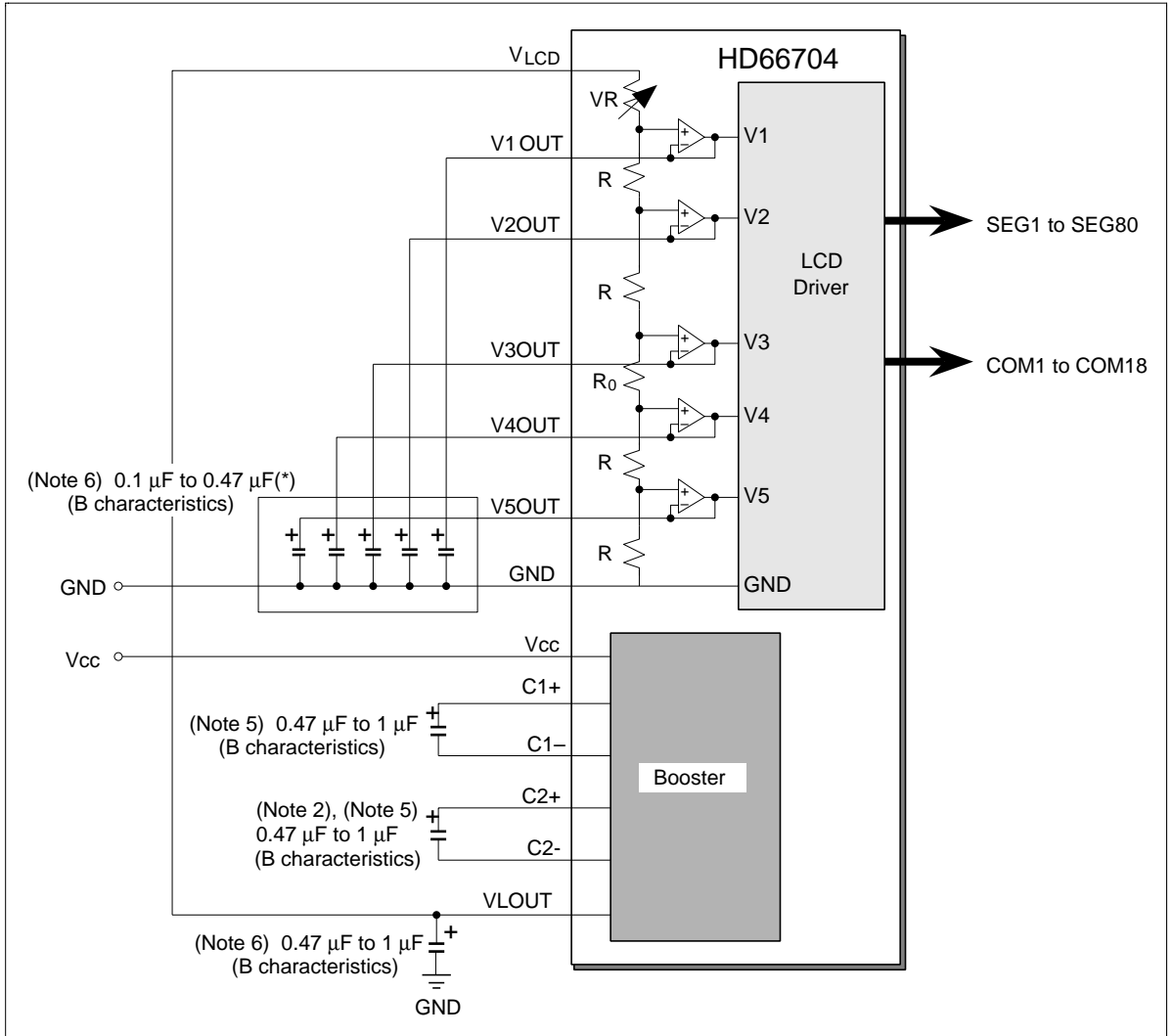
Figure 25 Internal Booster Circuit for LCD Drive Voltage Generation

Notes: 1. The reference voltage input (V_{CC}) must be adjusted so that the output voltage after boosting will not exceed the absolute maximum rating for the LCD power-supply voltage (6.5 V). Particularly, cares must be needed for triple boosting.

2. When using up to the double booster, no capacitors are required between C2+ and C2-.

3. If polarized capacitors are used, connect them correctly.

4. Adjust the value of the capacitor (*) after it is mounted on the LCD panel.

5. The capacitor to be connected to C1+/C1- and C2+/C2- must be resistant to the V_{CC} voltage.

6. The capacitor to be connected to VLOUT and V1OUT to V5OUT must be resistant to n-times or more of the V_{CC} voltage (n: boosting factor). Consider the change of the V_{CC} voltage and the resistant voltage of the capacitor.

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Liquid Crystal Display Drive Bias Selector Circuit

An optimum liquid crystal display bias value can be selected using BS1-0 bits, according to the liquid crystal drive duty ratio setting (NL2-0 bits). Liquid crystal display drive duty ratio and bias value can be displayed while switching software applications to match the LCD panel display status. The optimum bias value calculated using the following expression is an ideal value where the optimum contrast is obtained. Driving by using a lower value than the optimum bias value provides lower contrast and lower liquid crystal display voltage (potential difference between V1 and GND). When the liquid crystal display voltage is insufficient even if a triple booster is used or output voltage is lowered because the battery life has been reached, the display can be made easier to see by lowering the liquid crystal bias.

The liquid crystal display can be adjusted by using the contrast adjustment register (CT4-0 bits) and selecting the booster output level (BT bit).

$$\text{Optimum bias value for 1/N duty ratio drive voltage} = \frac{1}{\sqrt{N} + 1}$$

Table 22 LCD Drive Duty Ratio and Optimum Drive Bias Values

LCD drive duty ratio (NL2-0 set value)	1/18 (NL2-0 = 101/110)	1/11 (NL2-0 = 100)	1/4 (NL2-0 = 010)	1/3 (NL2-0 = 010)	1/2 (NL2-0 = 000)
Optimum drive bias value (BS1-0 set value)	1/5 or 1/4 (BS1-0 = 00, 01)	1/4 (BS1-0 = 01)	1/3 (BS1-0 = 10)	1/3 or 1/2 (BS1-0 = 10, 11)	

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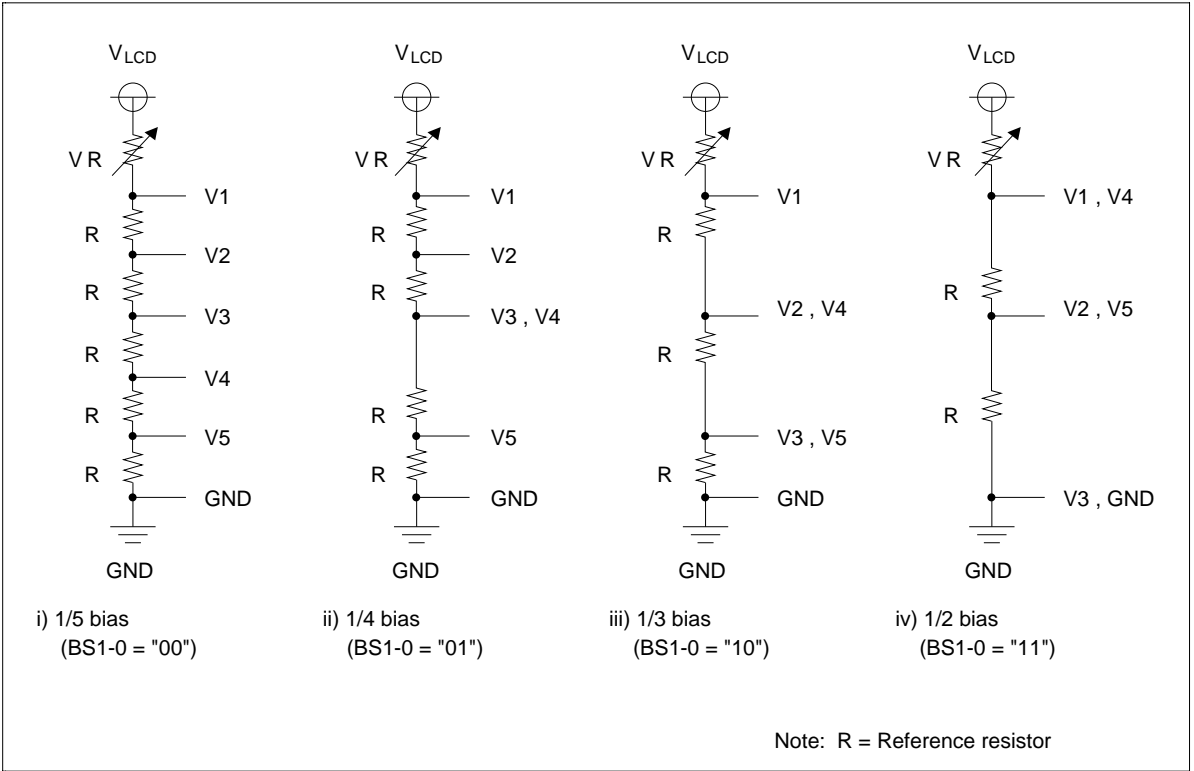
Figure 26 Liquid Crystal Display Drive Bias Circuit

Contrast Adjuster

Contrast for an LCD can be adjusted by varying the liquid-crystal drive voltage (potential difference between VLCD and V1) through the CT bits of the contrast control instruction (electron volume function). See figure 27 and table 23. The value of a variable resistor (VR) can be adjusted within a range from $0.1 \times R$ through $2.5 \times R$, where R is a reference resistance obtained by dividing the total resistance between VLCD and V1.

The HD66704 incorporates a voltage-follower operational amplifier for each of V1 to V5 to reduce current flowing through the internal bleeder-resistors, which generate different liquid-crystal drive voltages. Thus, CT4-0 bits must be adjusted so that the potential differences between VLCD and V1 and between V5 and GND are 0.1 V or higher when the LCD is driven.
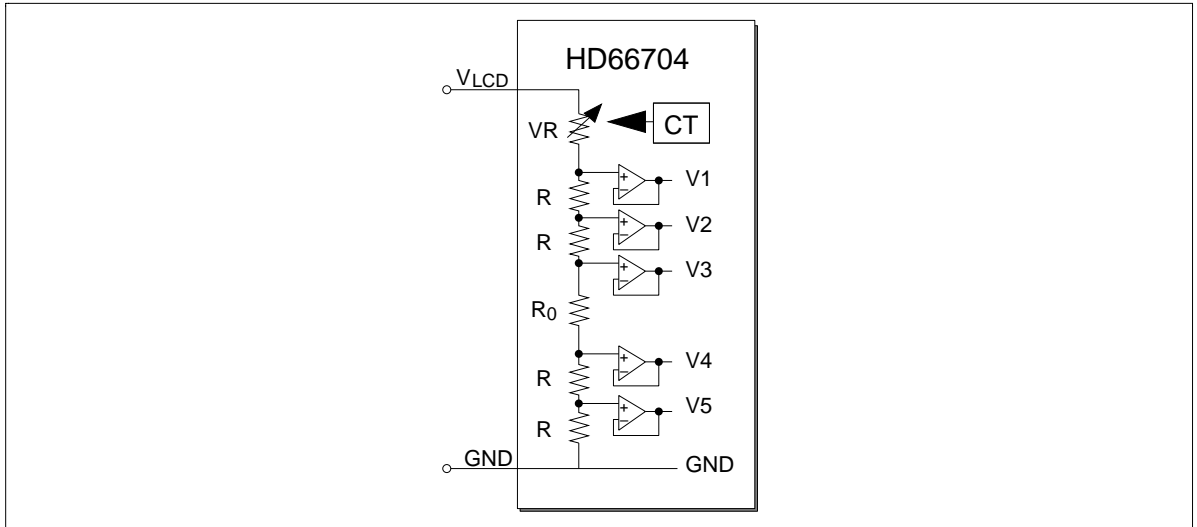
Figure 27 Contrast Adjuster

Table 23 Contrast-Adjust Bits (CT) and Variable Resistor Values

CT Set Value					Variable Resistor Value (VR)	Potential difference between V1 and GND	Display Color
CT4	CT3	CT2	CT1	CT0			
0	0	0	0	0	2.5 x R	(Small) ▲	(Light) ▲
0	0	0	0	1			
0	0	0	1	0			
0	0	0	1	1			
0	0	1	0	0			
0	0	1	0	1			
0	0	1	1	0			
0	0	1	1	1			
0	1	0	0	0	2.4 x R		
0	1	0	0	1	2.3 x R		
0	1	0	1	0	2.2 x R		
0	1	0	1	1	2.1 x R		
0	1	1	0	0	2.0 x R		
0	1	1	0	1	1.9 x R		
0	1	1	1	0	1.8 x R		
0	1	1	1	1	1.7 x R		
1	0	0	0	0	1.6 x R		
1	0	0	0	1	1.5 x R		
1	0	0	1	0	1.4 x R		
1	0	0	1	1	1.3 x R		
1	0	1	0	0	1.2 x R		
1	0	1	0	1	1.1 x R		
1	0	1	1	0	1.0 x R		
1	0	1	1	1	0.9 x R		
1	1	0	0	0	0.8 x R		
1	1	0	0	1	0.7 x R		
1	1	0	1	0	0.6 x R		
1	1	0	1	1	0.5 x R		
1	1	1	0	0	0.4 x R		
1	1	1	0	1	0.3 x R	▼	▼
1	1	1	1	0	0.2 x R	(Large)	(Deep)
1	1	1	1	1	0.1 x R		

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Table 24 Contrast Adjustment per Bias Drive Voltage

Bias	LCD drive voltage: VDR	Contrast adjustment range	
1/5 bias driver	$\dfrac{5 \times R}{5 \times R + VR} \times (V_{LCD} - GND)$	- LCD drive voltage adjustment range - Limit of potential difference between V5 and GND - Limit if potential difference between VLCD and V1	: $0.667 \times (V_{LCD}-GND) \leq V_{DR} \leq 0.980 \times (V_{LCD}-GND)$ $\dfrac{R}{5 \times R + VR} \times (V_{LCD}-GND) \geq 0.4$ [V] $\dfrac{VR}{5 \times R + VR} \times (V_{LCD}-GND) \geq 0.4$ [V]
1/4 bias driver	$\dfrac{4 \times R}{4 \times R + VR} \times (V_{LCD} - GND)$	- LCD drive voltage adjustment range - Limit of potential difference between V5 and GND - Limit if potential difference between VLCD and V1	: $0.615 \times (V_{LCD}-GND) \leq V_{DR} \leq 0.976 \times (V_{LCD}-GND)$ $\dfrac{R}{4 \times R + VR} \times (V_{LCD}-GND) \geq 0.4$ [V] $\dfrac{VR}{4 \times R + VR} \times (V_{LCD}-GND) \geq 0.4$ [V]
1/3 bias driver	$\dfrac{3 \times R}{3 \times R + VR} \times (V_{LCD} - GND)$	- LCD drive voltage adjustment range - Limit of potential difference between V5 and GND - Limit if potential difference between VLCD and V1	: $0.545 \times (V_{LCD}-GND) \leq V_{DR} \leq 0.968 \times (V_{LCD}-GND)$ $\dfrac{R}{3 \times R + VR} \times (V_{LCD}-GND) \geq 0.4$ [V] $\dfrac{VR}{3 \times R + VR} \times (V_{LCD}-GND) \geq 0.4$ [V]
1/2 bias driver	$\dfrac{2 \times R}{2 \times R + VR} \times (V_{LCD} - GND)$	- LCD drive voltage adjustment range - Limit of potential difference between V5 and GND - Limit if potential difference between VLCD and V1	: $0.444 \times (V_{LCD}-GND) \leq V_{DR} \leq 0.952 \times (V_{LCD}-GND)$ $\dfrac{R}{2 \times R + VR} \times (V_{LCD}-GND) \geq 0.4$ [V] $\dfrac{VR}{2 \times R + VR} \times (V_{LCD}-GND) \geq 0.4$ [V]

Note: The values in table 24 are ideal. Actual values will vary from product to product. Mount the adjuster on the LCD panel, and select the bias and contrast.

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LCD Panel Interface

The HD66704 has a function for changing the common driver/segment driver output shift direction using the CMS bit and SGS bit to meet the chip mounting positions of the HD66704. This is to facilitate the interface wiring to the LCD panel with COG installed.
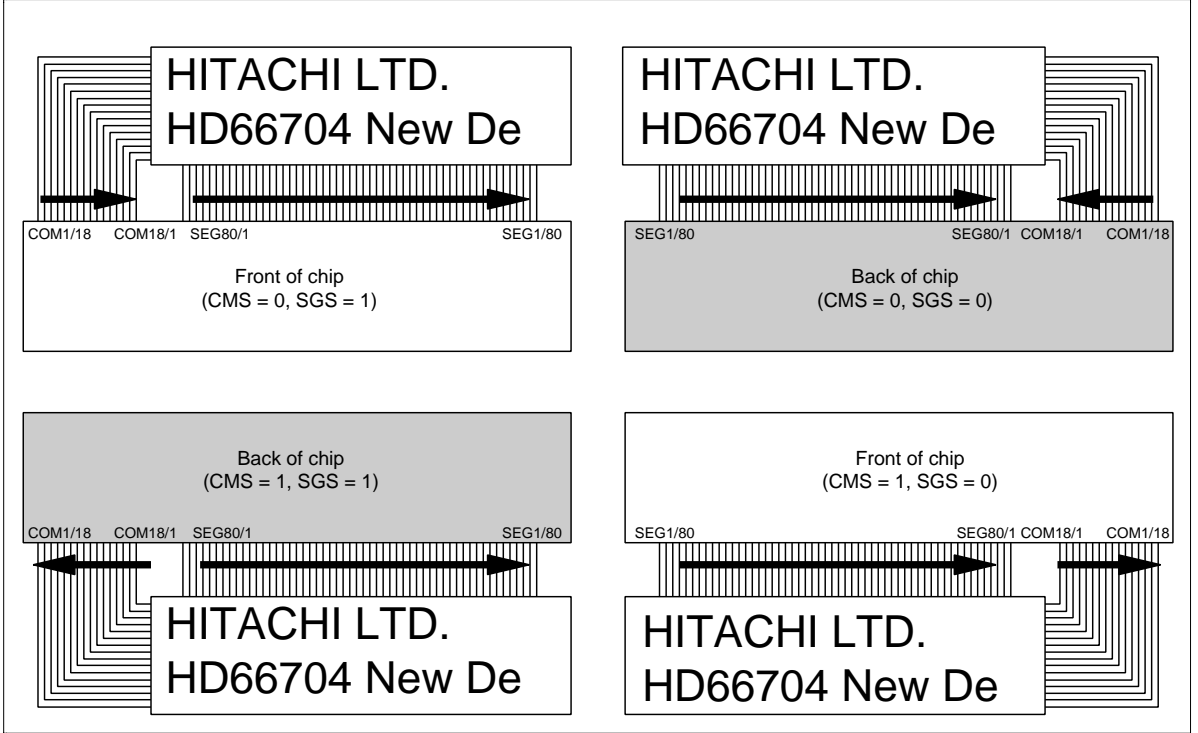
Figure 28 Pattern Wiring for 2-Line Character Display
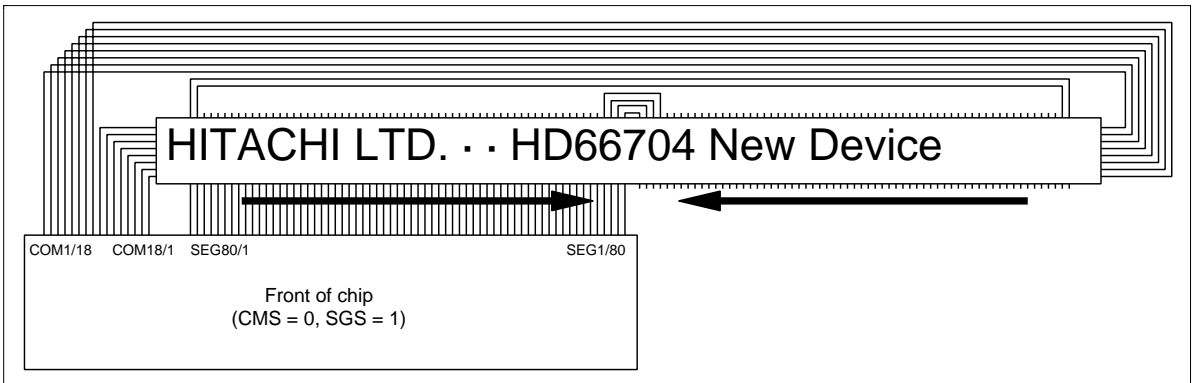
Figure 29 Pattern Wiring for 1-Line 32-Character Display at 1/18-Duty Ratio

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CGROM Bank Switching Function

The HD66704 incorporates two pages of CGROM. Switching the memory bank using the CGROM bank-switching bit (ROM) can display a total of 432 font patterns. Multinational fonts, special symbols, and icons can be displayed. Note that the number of fonts simultaneously displayed is CGROM: 240 + CGRAM: 2 when memory bank 0 is selected, and CGROM: 192 + CGRAM: 2 when memory bank 1 is selected. Font displays for CGRAM (1) to (2) are used in common with memory bank 0 and memory bank 1.

Table 25 CGROM Bank Switching

Character Code	Memory Bank 0 (ROM = 0)	Memory Bank 1 (ROM = 1)
"00"H to "0F"H	*CGRAM (1) to (2)*	*CGRAM (1) to (2)*
"10"H to "1F"H	CGROM (1) to (16)	*CGRAM (1) to (2)*
"20"H to "2F"H	CGROM (17) to (32)	CGROM (241) to (256)
"30"H to "3F"H	CGROM (33) to (48)	CGROM (257) to (272)
"40"H to "4F"H	CGROM (49) to (64)	CGROM (273) to (288)
"50"H to "5F"H	CGROM (65) to (80)	CGROM (289) to (304)
"60"H to "6F"H	CGROM (81) to (96)	CGROM (305) to (320)
"70"H to "7F"H	CGROM (97) to (112)	CGROM (321) to (336)
"80"H to "8F"H	CGROM (113) to (128)	*CGRAM (1) to (2)*
"90"H to "9F"H	CGROM (129) to (144)	*CGRAM (1) to (2)*
"A0"H to "AF"H	CGROM (145) to (160)	CGROM (337) to (352)
"B0"H to "BF"H	CGROM (161) to (176)	CGROM (353) to (368)
"C0"H to "CF"H	CGROM (177) to (192)	CGROM (369) to (384)
"D0"H to "DF"H	CGROM (193) to (208)	CGROM (385) to (400)
"E0"H to "EF"H	CGROM (209) to (224)	CGROM (401) to (416)
"F0"H to "FF"H	CGROM (225) to (240)	CGROM (417) to (432)

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Double-Height Display

The HD66704 can generate a double-height display of the characters on the first line when the DL bit is set to 1. All the incorporated font characters set in the CGROM and CGRAM can be doubled in height, allowing easy recognition. Note that there should be no space between the lines for double-height display (figure 30).

DL = 1 (1st line: double-height display)
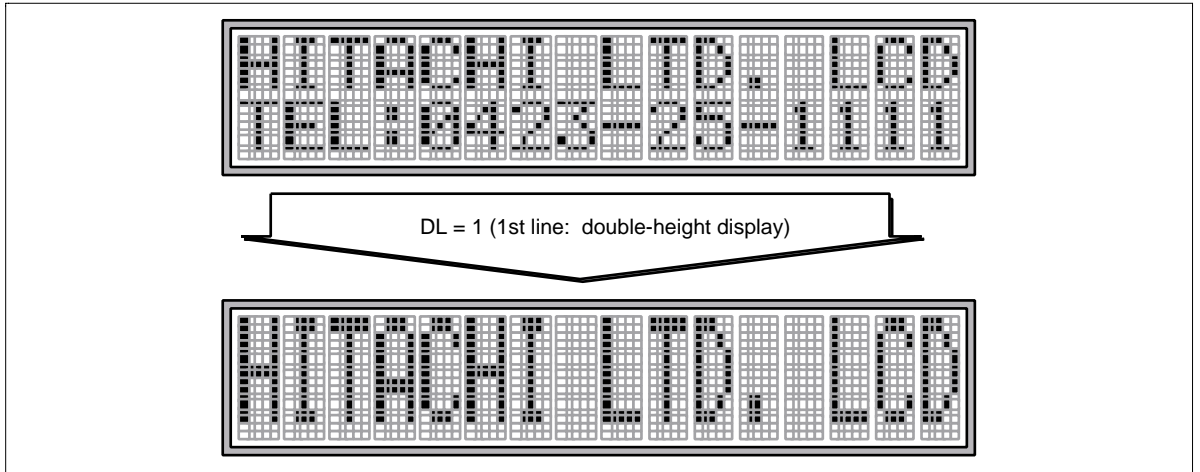
Figure 30 Double-Height Display

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Line-Cursor Display

In the character mode, the HD66704 can assign a cursor attribute to an entire line corresponding to the address counter value by setting the LC bit to 1. One of three line-cursor modes can be selected: a black-white reversed cursor (B/W = 1), an underline cursor (C = 1), and a blinking cursor (B = 1). The cycle for a blinking cursor is 32 or 64 frames according to the BL bit setting. These line cursors are suitable for highlighting an index and/or marker, or for indicating an item in a menu with a cursor or an underline.

Table 26 Address Counter Value and Line-Cursor Display

Address Counter Value (AC)	Selected Line for Line-Cursor Display
00H to 13H	Entire 1st line (16 characters)
20H to 33H	Entire 2nd line (16 characters)

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i) Normal Display (LC = 0)
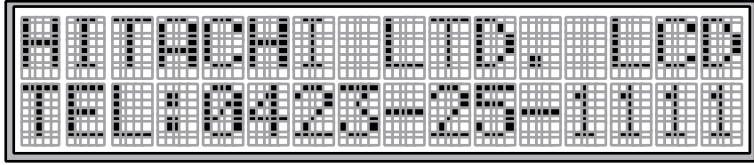
ii) Black-White Reversed Cursor Display (LC = 1, B/W = 1)
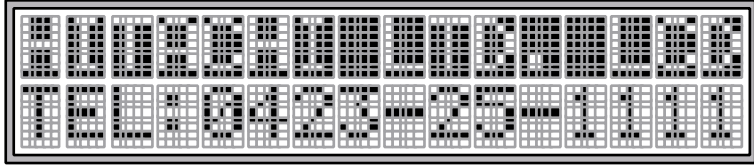
iii) Underline Cursor Display (LC = 1, C = 1)
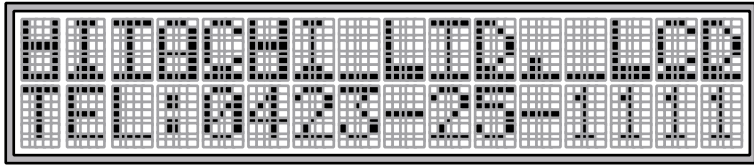
iv) Blinking Cursor Display (LC = 1, B = 1)

Alternates every 32 or 64 frames
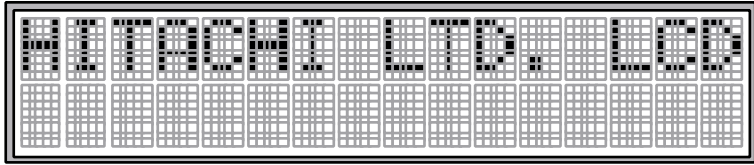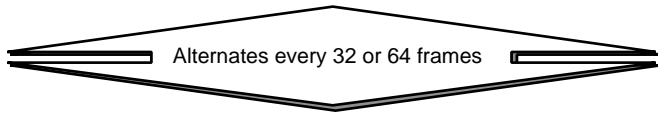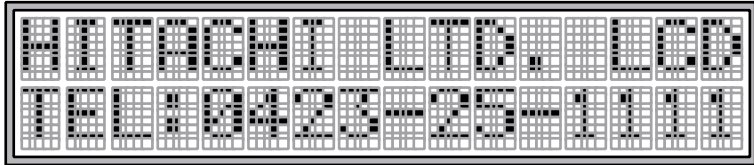
Figure 31 Examples of Cursor Display

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Segment Display Function

Using some of the DDRAM area allows the display of 160 segments in two-row character mode, 240 segments in one-row character mode, and 320 segments in segment mode.

These segments are displayed without blink control by setting the SB bit to 0. Data for the segment display is one bit/segment and only the upper four bits (D7-D4) of locations in the DDRAM are used. After display data has been written to the upper four bits of a given byte, the address counter (AC) is automatically incremented or decremented. In this case (SB = 0), the lower four bits (D3-D0) are ignored (see table 27).

When the SB bit is set to 1, segments are displayed with blink control. Data for the segment display is now two bits/segment. The two bits control whether segments are light or dark, and the blinking of segments (see table 28). During blinking, the segment goes dark or light for 32 or 64 frames. The BL bit selects the number of frames. In normal display mode, the blink activates the segment. In inverse display mode, the blink deactivates the segment. A combination of normal and inverse display modes with blinking can display motion in sets of segments.

When the device is in character display mode (NL2 = 1) and a character code is written to the DDRAM, the SB bit must be 1 when data is written to the DDRAM.

Table 27   Relationship between Data in the DDRAM and Segment Display, in Segment Mode without Blinking (SB = 0)

DDRAM data setting				Segment
D7	D6	D5	D4	LCD-display control
0	0	0	0	0 (Always light)
1	1	1	1	1 (Always dark)
SEG1, 5, 9, 13, 17, 21, 25, 29, 33, 37, 41, 45, 49, 53, 57, 61, 65, 69, 73, 77	SEG2, 6, 10, 14, 18, 22, 26, 30, 34, 38, 42, 46, 50, 54, 58, 62, 66, 70, 74, 78	SEG3, 7, 11, 15, 19, 23, 27, 31, 35, 39, 43, 47, 51, 55, 59, 63, 67, 71, 75, 79	SEG4, 8, 12, 16, 20, 24, 28, 32, 36, 40, 44, 48, 52, 56, 60, 64, 68, 72, 76, 80	Segment driver

Note: Only the upper four bits of data in the DDRAM are used to display segments. Settings in the lower four bits are invalid and are ignored.

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Table 28   Relationship between Data in the DDRAM and Segment Display, in Segment Mode with Blinking (SB = 1)

DDRAM data setting								Segment
D7	D6	D5	D4	D3	D2	D1	D0	LCD-display control
0	0	0	0	0	0	0	0	0 (Always light)
0	1	0	1	0	1	0	1	Blinking display
1	0	1	0	1	0	1	0	Blinking display in inverse mode
1	1	1	1	1	1	1	1	1 (Always dark)
SEG1, 5, 9, 13, 17, 21, 25, 29, 33, 37, 41, 45, 49, 53, 57, 61, 65, 69, 73, 77		SEG2, 6, 10, 14, 18, 22, 26, 30, 34, 38, 42, 46, 50, 54, 58, 62, 66, 70, 74, 78		SEG3, 7, 11, 15, 19, 23, 27, 31, 35, 39, 43, 47, 51, 55, 59, 63, 67, 71, 75, 79		SEG4, 8, 12, 16, 20, 24, 28, 32, 36, 40, 44, 48, 52, 56, 60, 64, 68, 72, 76, 80		Segment driver

Note: The BL bit selects the blink cycle and the cycle is each 32 (BL = 0) or 64 frames (BL = 1).

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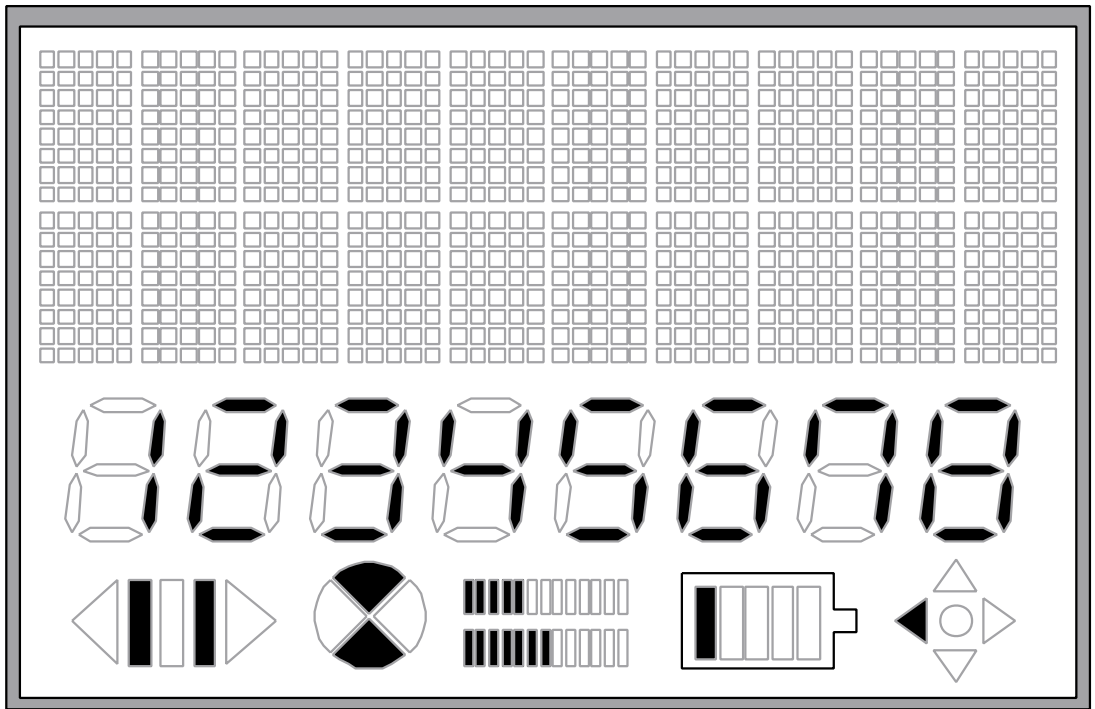
Indicates alternation every 32 or 64 frames
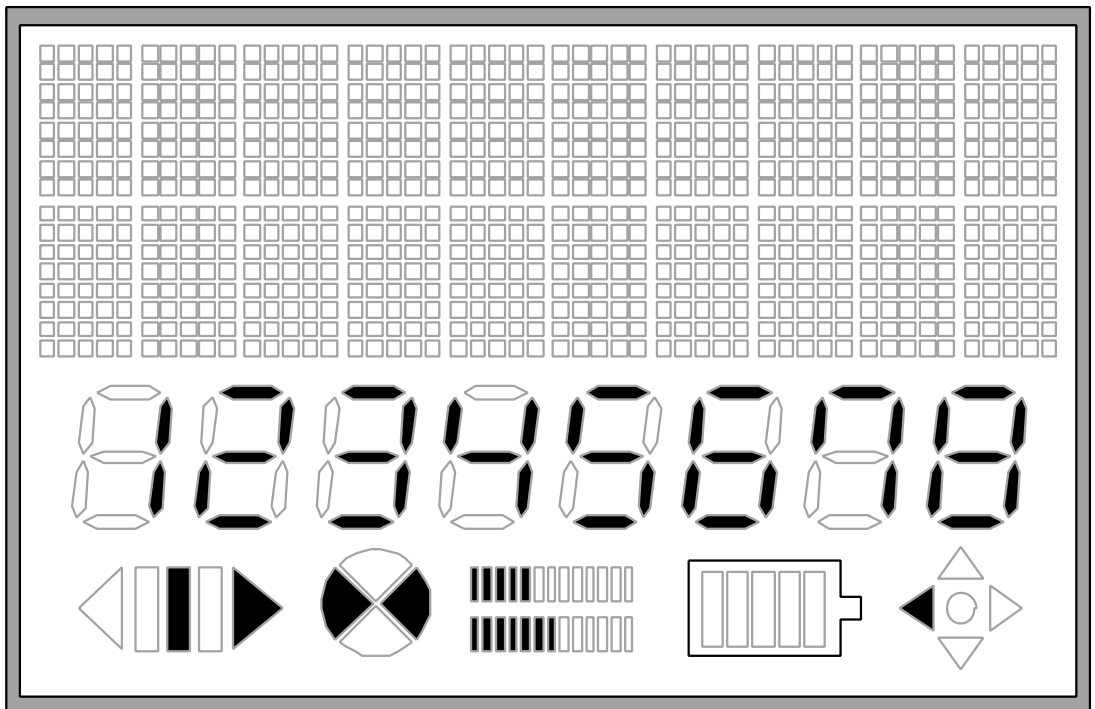
Figure 32 Example of a Segment-Based Display

Blink Synchronization Function

Issuing a blink synchronization instruction (70H) resets the blink cycle counter and starts a blink by activating the segment. It can be, for example, issued every second to make the colon on a clock display indicate the passage of seconds. When a blink cycle is started by blink synchronization in inverse display mode, the segment will be de-activated. When the frame frequency exceeds 96 Hz, make the blink take 64 frames, by setting the BL bit to 1. When using the built-in R-C oscillator circuit, the dispersion of the frame frequency will match that of the R-C oscillation frequency. Note that the oscillation frequency is dispersed by ±30 % at least when an R-C oscillator is configured with the built-in Rf resistance.
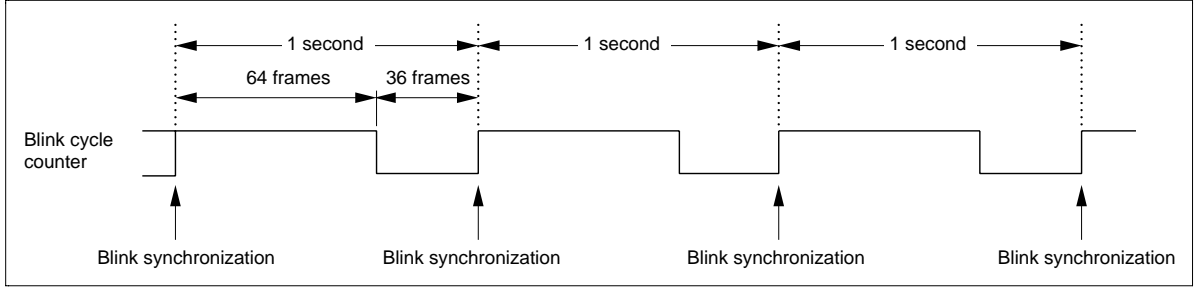
Figure 33 Blink Synchronization Function
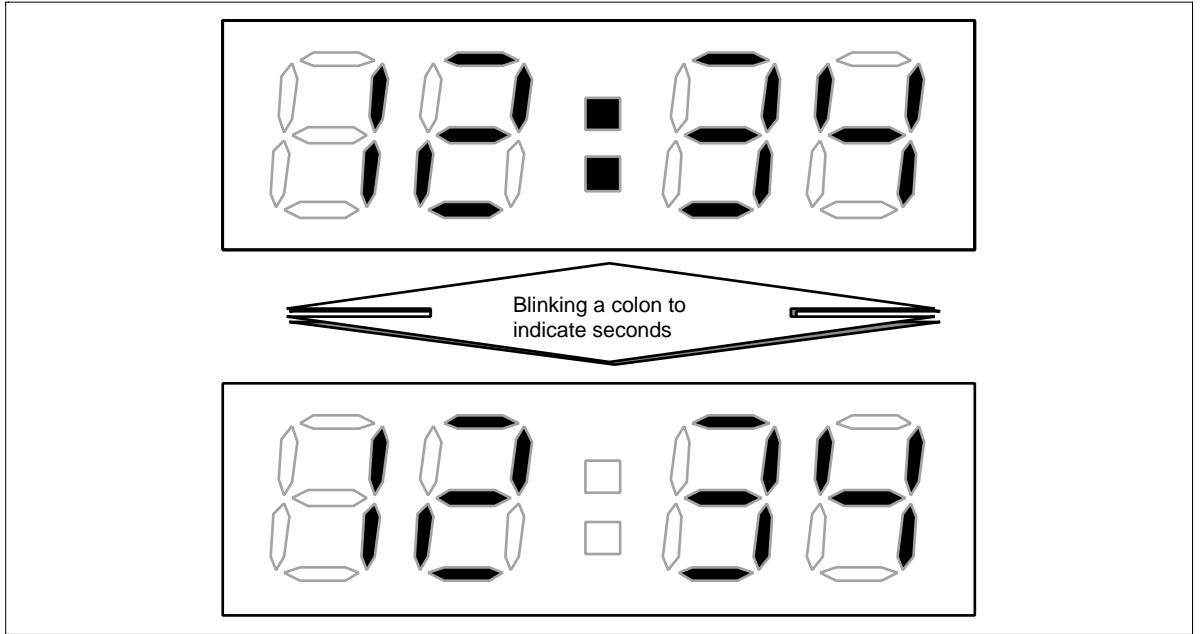
Figure 34 Usage Example of Blink Synchronization

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Sleep Mode

Setting the sleep mode bit (SLP) to 1 puts the HD66704 in the sleep mode, where the device stops all internal display operations except for the R-C oscillator, thus reducing current consumption. Specifically, LCD drive is completely halted. Here, all the SEG (SEG1 to SEG80) and COM (COM1 to COM18) pins output the GND level, resulting in no drive voltage being applied to any LCD cell. If the AMP bit is set to 0 in the sleep mode, the LCD drive power supply can be turned off, reducing the total current consumption of the LCD module.

Standby Mode

Setting the standby mode bit (STB) to 1 puts the HD66704 in the standby mode, where the device stops completely, halting all internal operations including the R-C oscillator, thus further reducing current consumption compared to that in the sleep mode. Here, all the SEG (SEG1 to SEG80) and COM (COM1 to COM18) pins output the GND level, resulting that no drive voltage is applied to each LCD cell. If the AMP bit is set to 0 in the standby mode, the LCD drive power supply can be turned off.

During the standby mode, no instructions can be accepted other than the start-oscillator instruction. To cancel the standby mode, issue the start oscillator instruction to stabilize R-C oscillation before setting the STB bit to 0.
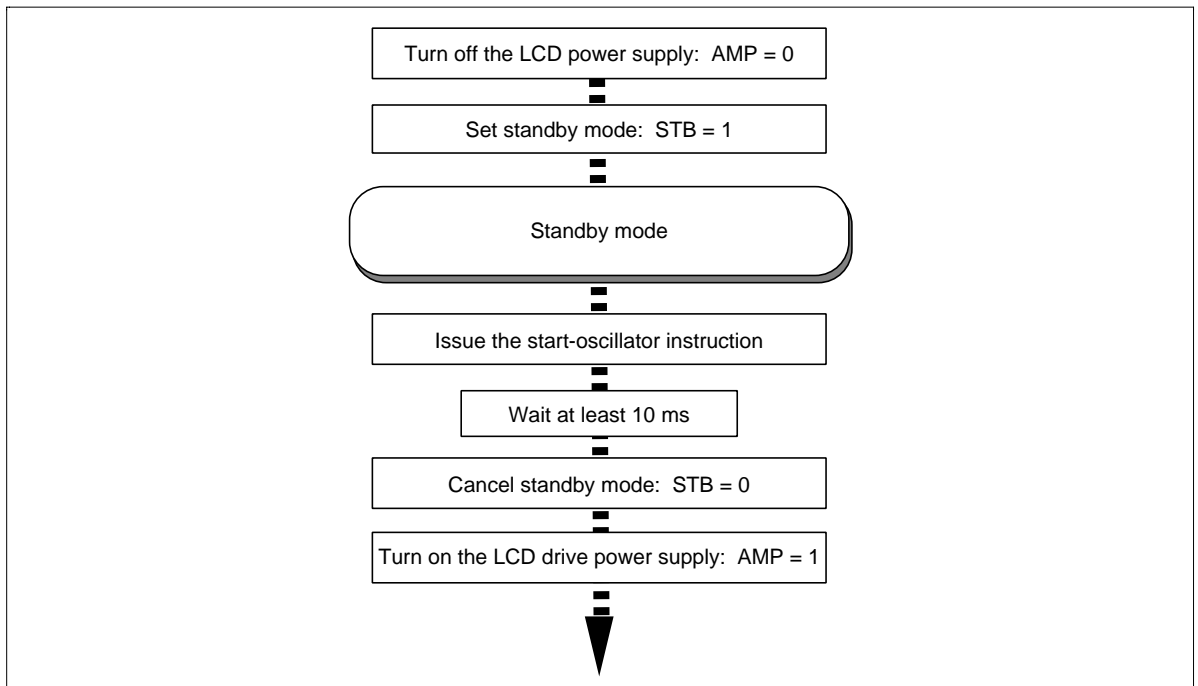
Figure 35 Procedure for Setting and Canceling Standby Mode

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Absolute Maximum Ratings

Item	Symbol	Unit	Value	Notes*
Power supply voltage (1)	V_{CC}	V	−0.3 to +7.0	1, 2
Power supply voltage (2)	V_{LCD} − GND	V	−0.3 to +7.0	1, 3
Input voltage	Vt	V	−0.3 to V_{CC} + 0.3	1
Operating temperature	Topr	°C	−40 to +85	1, 4

Notes: 1. If the LSI is used above these absolute maximum ratings, it may become permanently damaged. Using the LSI within the following electrical characteristics limits is strongly recommended for normal operation. If these electrical characteristic conditions are also exceeded, the LSI will malfunction and cause poor reliability.
2. $V_{CC} \geq$ GND must be maintained.
3. $V_{LCD} \geq V_{CC}$ must be maintained.
4. For the DC/AC characteristics for bare die products, specified up to 85°C.

DC Characteristics (V_{CC} = 1.8 to 5.5 V, Ta = −40 to +85°C*1)

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	V_{IH}	0.7 V_{CC}	—	V_{CC}	V		2, 3
Input low voltage	V_{IL}	−0.3	—	0.15 V_{CC}	V	V_{CC} = 1.8 to 2.7 V	2, 3
		−0.3	—	0.15 V_{CC}	V	V_{CC} = 2.7 to 5.5 V	2, 3
Driver ON resistance (COM pins)	R_{COM}	—	3	20	kΩ	±Id = 0.05 mA, V_{LCD} = 5 V	4
Driver ON resistance (SEG pins)	R_{SEG}	—	3	30	kΩ	±Id = 0.05 mA, V_{LCD} = 5 V	4
Input leakage current	I_{Li}	−1	—	1	μA	Vin = 0 to V_{CC}	
Current consumption during normal operation (V_{CC}–GND)	I_{OP}	—	20	35	μA	R-C oscillation, V_{CC} = 3 V, Ta = 25°C, f_{OSC} = 32 kHz (1/17 duty)	5, 6
Current consumption during sleep mode (V_{CC}–GND)	I_{SL}	—	(11)	—	μA	R-C oscillation, V_{CC} = 3 V, Ta = 25°C, f_{OSC} = 32 kHz (1/17 duty)	5, 6
Current consumption during standby mode (V_{CC}–GND)	I_{ST}	—	0.1	5	μA	V_{CC} = 3 V, Ta = 25°C	5, 6
LCD drive power supply current (V_{LCD}–GND)	I_{LCD}	—	17	35	μA	V_{LCD} − GND = 5.5 V, Ta = 25°C, f_{OSC} = 32 kHz, 1/5 bias	6
LCD drive voltage (V_{LCD} − GND)	V_{LCD}	3.0	—	6.5	V	$V_{LCD} \geq V_{CC}$, AMP = 0 ($V_{LCD} \geq$ VLOUT, AMP = 1)	7

Note: For the numbered notes, refer to the Electrical Characteristics Notes section following these tables.

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Booster Characteristics

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes
Double-boost output voltage (VLOUT–GND)	V_{UP2}	5.5	5.9	6.0	V	V_{CC} = 3.0 V, I_O = 30 µA, C = 1 µF, f_{OSC} = 32 kHz, Ta = 25°C	11
Triple-boost output voltage (VLOUT–GND)	V_{UP3}	6.1	6.5	6.6	V	V_{CC} = 2.2 V, I_O = 30 µA, C = 1 µF, f_{OSC} = 32 kHz, Ta = 25°C	11
Range of boosting output voltage (VLOUT–GND)	V_{UP2}	V_{CC}	—	6.5	V	Double boost	11
	V_{UP3}	V_{CC}	—	6.5	V	Triple boost	11

Note: For the numbered notes, refer to the Electrical Characteristics Notes section following these tables.

AC Characteristics (V_{CC} = 1.8 to 5.5 V, Ta = –40 to +85°C*[1])

Clock Characteristics (V_{CC} = 1.8 to 5.5 V)

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes
External clock frequency	fcp	15	32	100	kHz		8
External clock duty ratio	Duty	45	50	55	%		8
External clock rise time	t_{rcp}	—	—	0.2	µs		8
External clock fall time	t_{fcp}	—	—	0.2	µs		8
External Rf oscillation frequency	t_{OSC1}	25	32	40	kHz	Rf = 620 kΩ, V_{CC} = 3 V	9
Internal Rf oscillation frequency	t_{OSC2}	19	32	45	kHz	R1-OSC2: short-circuiting, V_{CC} = 3 V	10

Note: For the numbered notes, refer to the Electrical Characteristics Notes section following these tables.

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4-Bit Bus Interface Timing Characteristics

$(V_{CC} = 1.8$ to 2.7 V$)$

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	t_{CYCE}	800	—	—	ns	Figure 41
Enable high-level pulse width	PW_{EH}	150	—	—	ns	Figure 41
Enable low-level pulse width	PW_{EL}	300	—	—	ns	Figure 41
Enable rise/fall time	t_{Er}, t_{Ef}	—	—	25	ns	Figure 41
Setup time (RS to E, CS*)	t_{ASE}	60	—	—	ns	Figure 41
Address hold time	t_{AHE}	20	—	—	ns	Figure 41
Write data set-up time	t_{DSWE}	60	—	—	ns	Figure 41
Write data hold time	t_{HE}	20	—	—	ns	Figure 41

$(V_{CC} = 2.7$ to 5.5 V$)$

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	t_{CYCE}	500	—	—	ns	Figure 41
Enable high-level pulse width	PW_{EH}	80	—	—	ns	Figure 41
Enable low-level pulse width	PW_{EL}	250	—	—	ns	Figure 41
Enable rise/fall time	t_{Er}, t_{Ef}	—	—	25	ns	Figure 41
Setup time (RS to E, CS*)	t_{ASE}	60	—	—	ns	Figure 41
Address hold time	t_{AHE}	20	—	—	ns	Figure 41
Write data set-up time	t_{DSWE}	60	—	—	ns	Figure 41
Write data hold time	t_{HE}	20	—	—	ns	Figure 41

Clock-Synchronized Serial Interface Timing Characteristics (V_{CC} = 1.8 to 5.5 V)

(V_{CC} = 1.8 to 2.7 V)

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Serial clock cycle time	t_{SCYC}	0.5	—	20	µs	Figure 42
Serial clock high-level width	t_{SCH}	230	—	—	ns	Figure 42
Serial clock low-level width	t_{SCL}	230	—	—	ns	Figure 42
Serial clock rise/fall time	t_{scf}, t_{scr}	—	—	20	ns	Figure 42
Chip select set-up time	t_{CSU}	60	—	—	ns	Figure 42
Chip select hold time	t_{CH}	200	—	—	ns	Figure 42
Serial input data set-up time	t_{SISU}	100	—	—	ns	Figure 42
Serial input data hold time	t_{SIH}	100	—	—	ns	Figure 42

(V_{CC} = 2.7 to 5.5 V)

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Serial clock cycle time	t_{SCYC}	0.2	—	20	µs	Figure 42
Serial clock high-level width	t_{SCH}	80	—	—	ns	Figure 42
Serial clock low-level width	t_{SCL}	80	—	—	ns	Figure 42
Serial clock rise/fall time	t_{scf}, t_{scr}	—	—	20	ns	Figure 42
Chip select set-up time	t_{CSU}	60	—	—	ns	Figure 42
Chip select hold time	t_{CH}	200	—	—	ns	Figure 42
Serial input data set-up time	t_{SISU}	40	—	—	ns	Figure 42
Serial input data hold time	t_{SIH}	40	—	—	ns	Figure 42

Reset Timing Characteristics (V_{CC} = 1.8 to 5.5 V)

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Reset low-level width	t_{RES}	1	—	—	ms	Figure 43

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Electrical Characteristics Notes

1. For bare die products, specified up to +85°C.

2. The following two circuits are I/O pin configurations (figure 36).
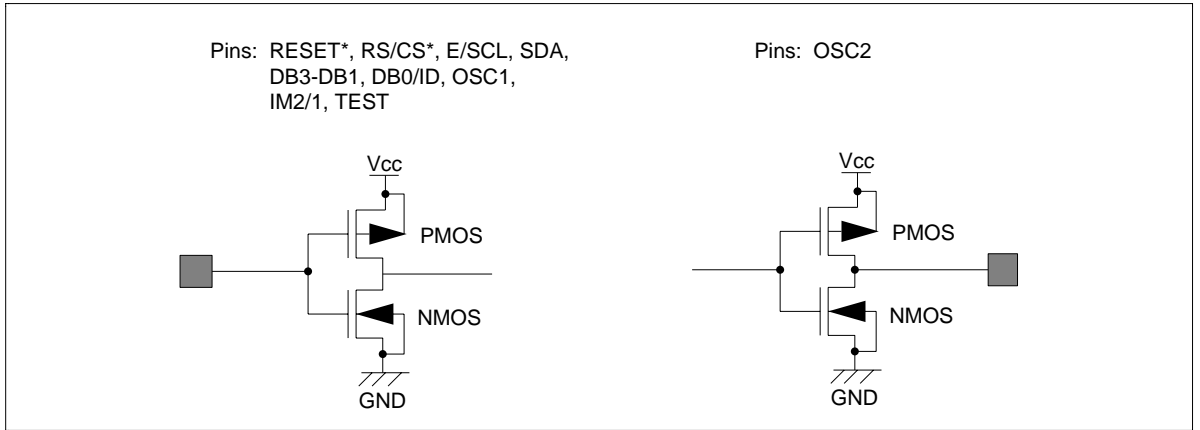
Figure 36 I/O Pin Configuration

3. The TEST pin must be grounded and the IM2/1 pin must be grounded or connected to V_{CC}. When using the clock-synchronized serial interface, DB3-1 and DB0/ID must be grounded or connected to V_{CC}.

4. Applies to the resistor value (RCOM) between power supply pins V1OUT, V2OUT, V5OUT, GND and common signal pins, and resistor value (RSEG) between power supply pins V1OUT, V3OUT, V4OUT, GND and segment signal pins, when current Id is flown through all driver output pins.

5. This excludes the current flowing through the input/output units. The input level must be fixed to V_{CC} or GND because through current increases if the CMOS input is left floating.

6. The following shows the relationship between the operation frequency and current consumption (figure 37).
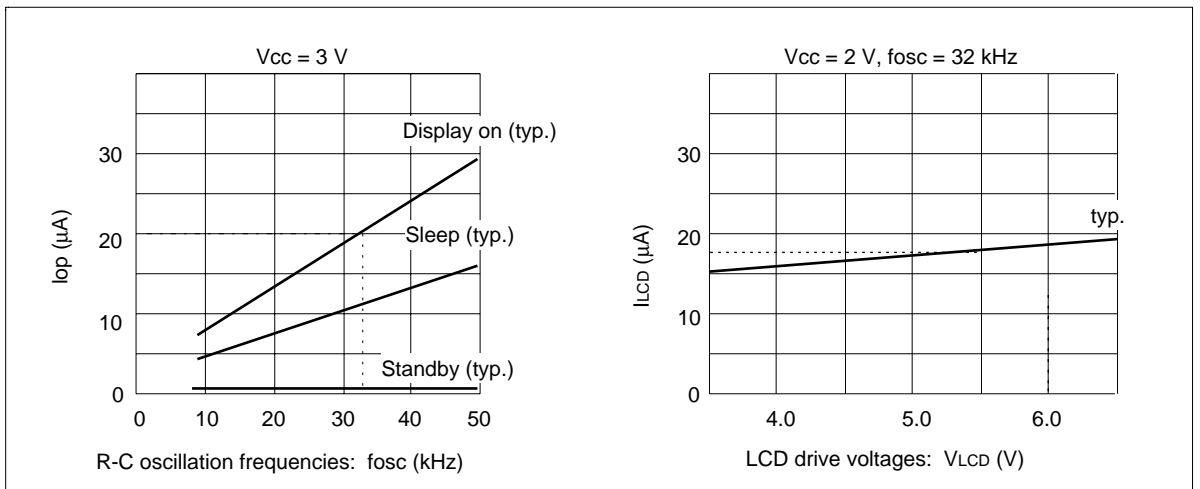
Figure 37   Relationship between the Operation Frequency and Current Consumption

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7. Each COM and SEG output voltage is within ±0.15 V of the LCD voltages (V_{CC}, V1, V2, V3, V4, and V5) when there is no load.

8. Applies to the external clock input (figure 38).
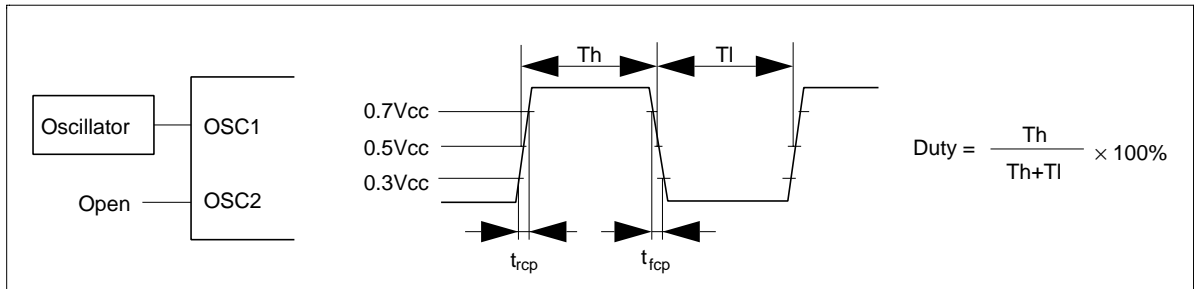
Figure 38 External Clock Supply

9. Applies to the internal oscillator operations using external oscillation resistor Rf (figure 39).

Since the oscillation trequency varies depending on the OSC1 and ISC2 pin capacitance, the wiring length to these pins should be minimized.
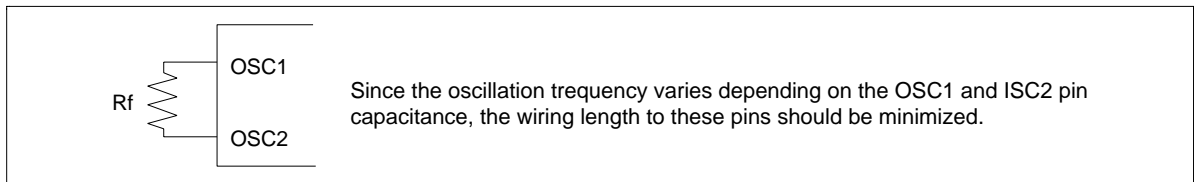
Figure 39 Internal Oscillation

Table 29 External Resistance Value and R-C Oscillation Frequency (Referential Data)

External Resistance (Rf)	R-C Oscillation Frequency: fosc				
	Vcc = 1.8 V	Vcc = 2.2 V	Vcc = 3.0 V	Vcc = 4.0 V	Vcc = 5.0 V
390 kΩ	40 kHz	45 kHz	48 kHz	50 kHz	51 kHz
510 kΩ	33 kHz	36 kHz	38 kHz	40 kHz	41 kHz
560 kΩ	30 kHz	33 kHz	35 kHz	36 kHz	37 kHz
620 kΩ	28 kHz	30 kHz	32 kHz	33 kHz	33 kHz
680 kΩ	26 kHz	29 kHz	30 kHz	31 kHz	31 kHz
750 kΩ	24 kHz	27 kHz	28 kHz	29 kHz	29 kHz

10. Note that the oscillation and frame frequencies are changed by ±30% or more when the internal oscillation resistance is used.

11. Booster characteristics test circuits are shown in figure 40.
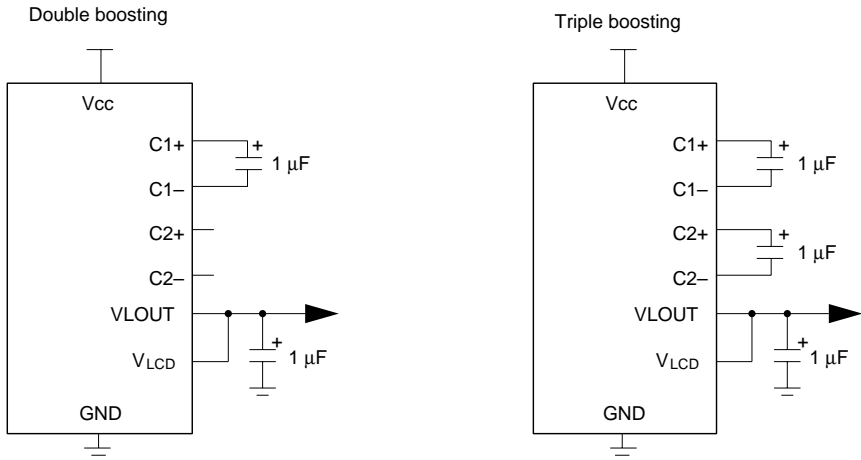
Figure 40 Booster

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(iii) Relation between the obtained voltage and capacitance
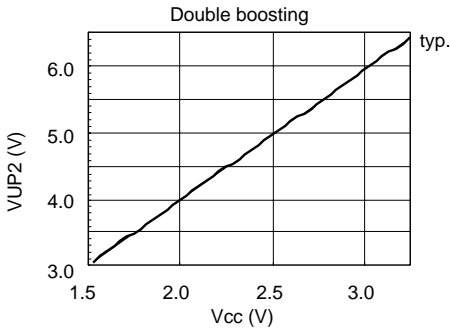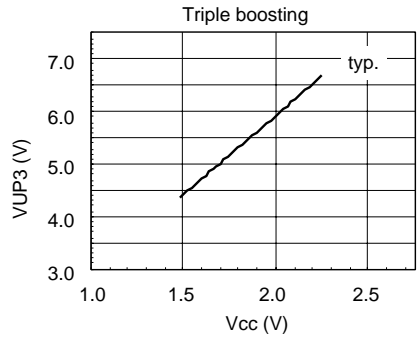
Double boosting
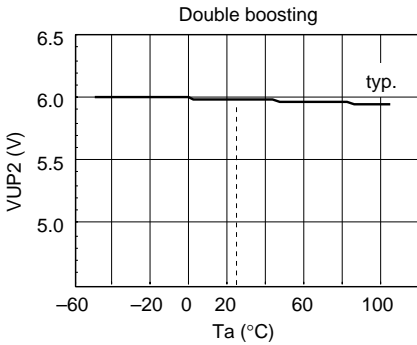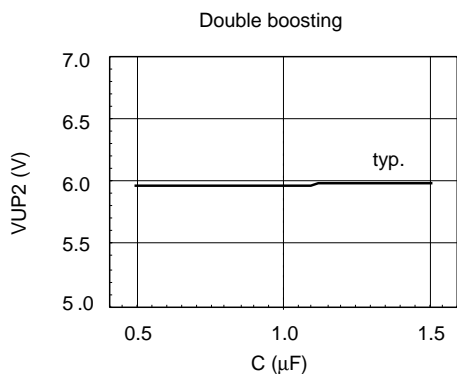
Test condition: Vcc = 3.0 V, fosc = 32 kHz, Io = 30 μA

Triple boosting
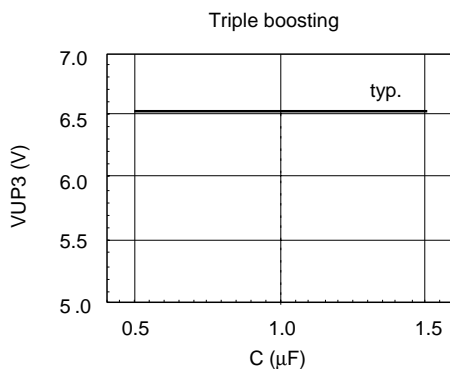
Test condition: Vcc = 2.2 V, fosc = 32 kHz, Io = 30 μA

(iv) Relation between the obtained voltage and current

Double boosting
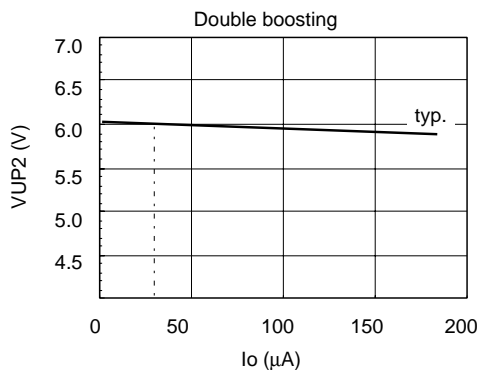
Test condition: Vcc = 3.0 V, fosc = 32 kHz, Ta = 25°C

Triple boosting
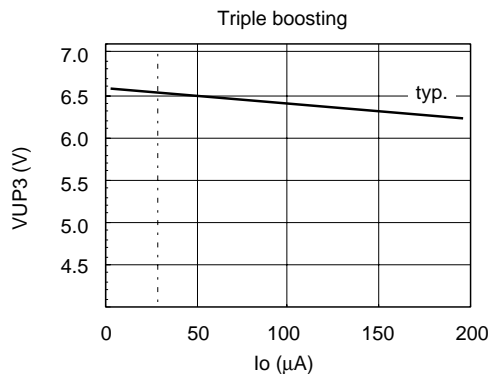
Test condition: Vcc = 2.2 V, fosc = 32 kHz, Ta = 25°C

Figure 40 Booster (cont)

Timing Characteristics

4-Bit Bus Operation
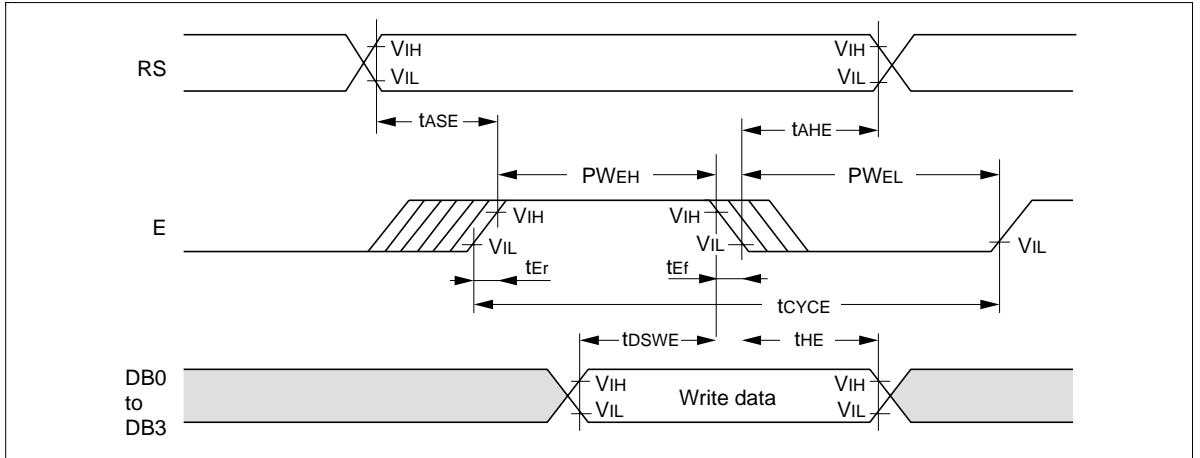
Figure 41 4-Bit Bus Timing

Clock-Synchronized Serial Operation
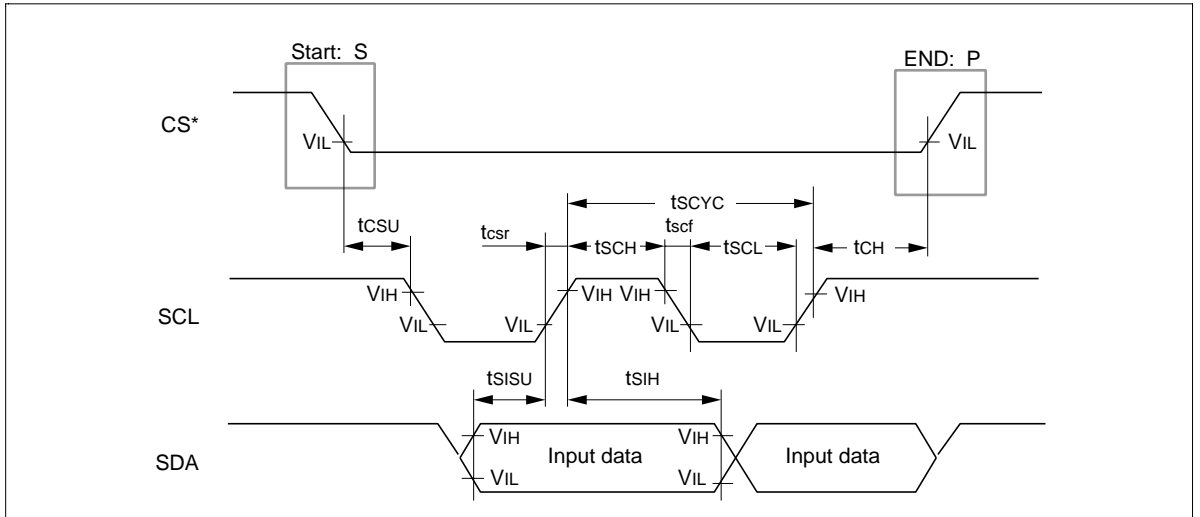
Figure 42 Clock-Synchronized Serial Interface Timing

Reset Operation
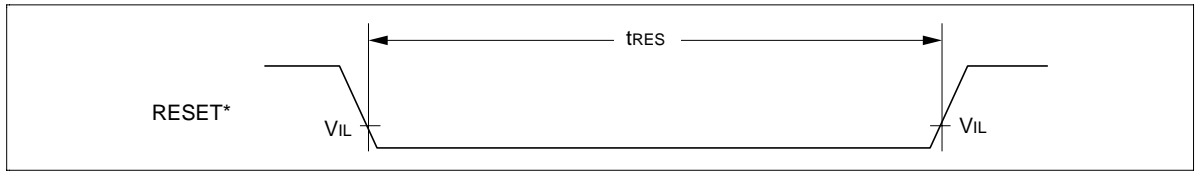
Figure 43 Reset Timing

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