

# NSTB60ADW1T1

## PNP General Purpose and NPN Bias Resistor Transistor Combination

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- Available in 8 mm, 7 inch/3000 Unit Tape and Reel
- ESD Rating – Human Body Model: Class 1B  
– Machine Model: Class B

### MAXIMUM RATINGS

(T<sub>A</sub> = 25°C unless otherwise noted, common for Q<sub>1</sub> and Q<sub>2</sub>)

Rating	Symbol	Q <sub>1</sub>	Q <sub>2</sub>	Unit
Collector-Emitter Voltage	V <sub>CEO</sub>	-50	50	Vdc
Collector-Base Voltage	V <sub>CBO</sub>	-50	50	Vdc
Emitter-Base Voltage	V <sub>EBO</sub>	-6.0	5.0	Vdc
Collector Current – Continuous	I <sub>C</sub>	-150	150	mAdc

### THERMAL CHARACTERISTICS

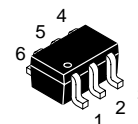
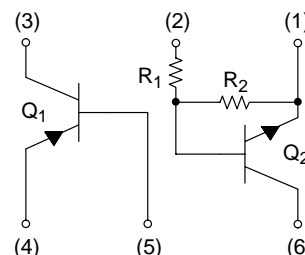
Characteristic (One Junction Heated)	Symbol	Max	Unit
Total Device Dissipation T <sub>A</sub> = 25°C Derate above 25°C	P <sub>D</sub>	187 (Note 1) 256 (Note 2) 1.5 (Note 1) 2.0 (Note 2)	mW mW/°C
Thermal Resistance – Junction-to-Ambient	R <sub>θJA</sub>	670 (Note 1) 490 (Note 2)	°C/W
Characteristic (Both Junctions Heated)	Symbol	Max	Unit
Total Device Dissipation T <sub>A</sub> = 25°C Derate above 25°C	P <sub>D</sub>	250 (Note 1) 385 (Note 2) 2.0 (Note 1) 3.0 (Note 2)	mW mW/°C
Thermal Resistance – Junction-to-Ambient	R <sub>θJA</sub>	493 (Note 1) 325 (Note 2)	°C/W
Thermal Resistance – Junction-to-Lead	R <sub>θJL</sub>	188 (Note 1) 208 (Note 2)	°C/W
Junction and Storage Temperature	T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	°C

1. FR-4 @ Minimum Pad
2. FR-4 @ 1.0 x 1.0 inch Pad



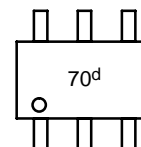
ON Semiconductor®

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SOT-363  
CASE 419B  
STYLE 1

### MARKING DIAGRAM



70 = Specific Device Code  
d = Date Code

### ORDERING INFORMATION

Device	Package	Shipping
NSTB60ADW1T1	SOT-363	3000/Tape & Reel

# NSTB60ADW1T1

## ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>Q<sub>1</sub></b>					
Collector-Base Breakdown Voltage (I <sub>C</sub> = -50 μAdc, I <sub>E</sub> = 0)	V <sub>(BR)CBO</sub>	-50	-	-	Vdc
Collector-Emitter Breakdown Voltage (I <sub>C</sub> = -1.0 mAdc, I <sub>B</sub> = 0)	V <sub>(BR)CEO</sub>	-50	-	-	Vdc
Emitter-Base Breakdown Voltage (I <sub>E</sub> = -50 μAdc, I <sub>E</sub> = 0)	V <sub>(BR)EBO</sub>	-6.0	-	-	Vdc
Collector-Base Cutoff Current (V <sub>CB</sub> = -50 Vdc, I <sub>E</sub> = 0)	I <sub>CBO</sub>	-	-	-0.1	μA
Emitter-Base Cutoff Current (V <sub>EB</sub> = -6.0 Vdc, I <sub>B</sub> = 0)	I <sub>EBO</sub>	-	-	-0.1	μA
Collector-Emitter Saturation Voltage (I <sub>C</sub> = -50 mAdc, I <sub>B</sub> = -5.0 mAdc) (Note 3)	V <sub>CE(sat)</sub>	-	-	-0.5	Vdc
DC Current Gain (V <sub>CE</sub> = -10 V, I <sub>C</sub> = -5.0 mA) (Note 3)	h <sub>FE</sub>	120	-	560	-
Transition Frequency (V <sub>CE</sub> = -12 Vdc, I <sub>C</sub> = -2.0 mAdc, f = 100 MHz)	f <sub>T</sub>	-	140	-	MHz
Output Capacitance (V <sub>CB</sub> = -12 Vdc, I <sub>E</sub> = 0 Adc, f = 1.0 MHz)	C <sub>OB</sub>	-	3.5	-	pF

## Q<sub>2</sub>

Collector-Base Breakdown Voltage (I <sub>C</sub> = 50 μA, I <sub>E</sub> = 0)	V <sub>(BR)CBO</sub>	50	-	-	Vdc
Collector-Emitter Breakdown Voltage (I <sub>C</sub> = 1.0 mA, I <sub>B</sub> = 0) (Note 3)	V <sub>(BR)CEO</sub>	50	-	-	Vdc
Collector-Base Cutoff Current (V <sub>CB</sub> = 50 V, I <sub>E</sub> = 0)	I <sub>CBO</sub>	-	-	100	nAdc
Collector-Emitter Cutoff Current (V <sub>CE</sub> = 50 V, I <sub>B</sub> = 0)	I <sub>CEO</sub>	-	-	500	nAdc
Emitter-Base Cutoff Current (V <sub>EB</sub> = 6.0 V, I <sub>C</sub> = 0)	I <sub>EBO</sub>	-	-	0.15	mAdc
Collector-Emitter Saturation Voltage (I <sub>C</sub> = 10 mA, I <sub>B</sub> = 5.0 mA) (Note 3)	V <sub>CE(sat)</sub>	-	-	0.25	Vdc
DC Current Gain (V <sub>CE</sub> = 10 V, I <sub>C</sub> = 5.0 mA) (Note 3)	h <sub>FE</sub>	40	-	-	
Output Voltage (on) (V <sub>CC</sub> = 5.0 V, V <sub>B</sub> = 4.0 V, R <sub>L</sub> = 1.0 kΩ) (Note 3)	V <sub>OL</sub>	-	-	0.2	Vdc
Output Voltage (off) (V <sub>CC</sub> = 5.0 V, V <sub>B</sub> = 0.25 V, R <sub>L</sub> = 1.0 kΩ) (Note 3)	V <sub>OH</sub>	4.9	-	-	Vdc
Input Resistor (Note 3)	R1	32.9	47	61.1	kΩ
Resistor Ratio (Note 3)	R1/R2	3.76	4.7	5.64	

3. Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0%

# NSTB60ADW1T1

## Typical Electrical Characteristics – PNP Transistor

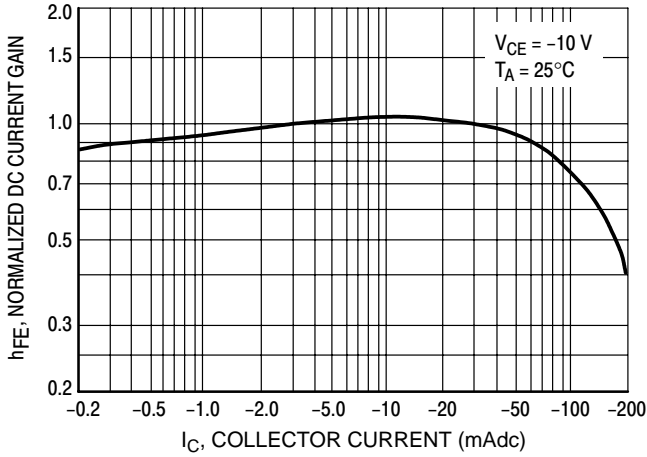


Figure 1. Normalized DC Current Gain

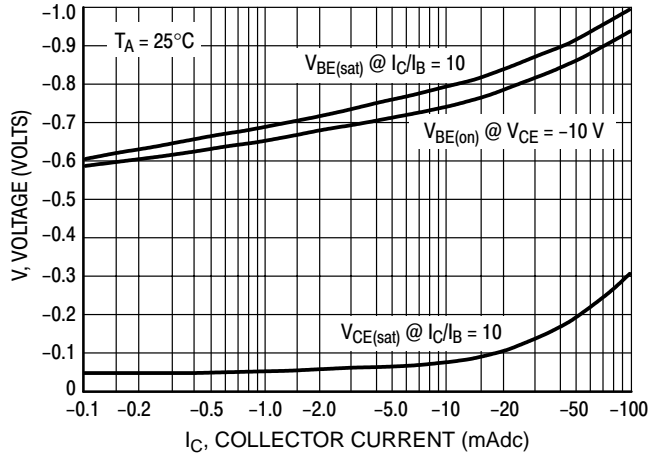


Figure 2. "Saturation" and "On" Voltages

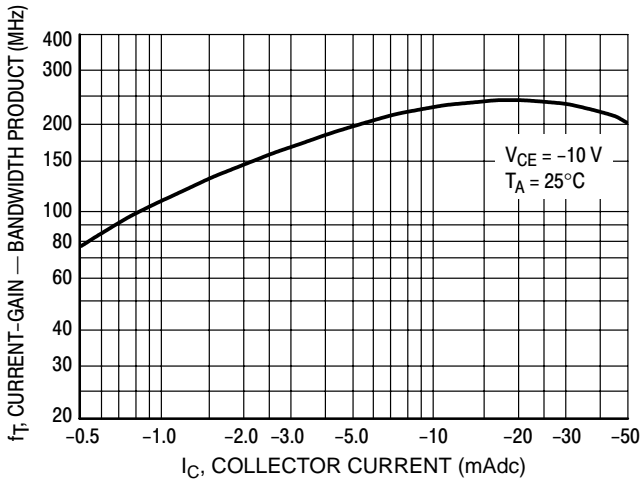


Figure 3. Current-Gain – Bandwidth Product

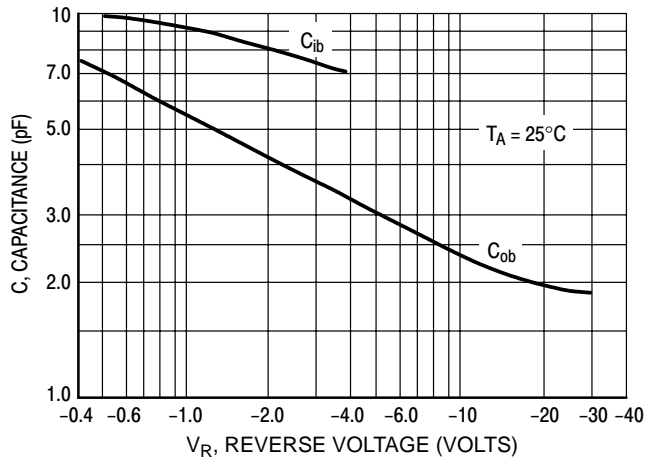


Figure 4. Capacitances

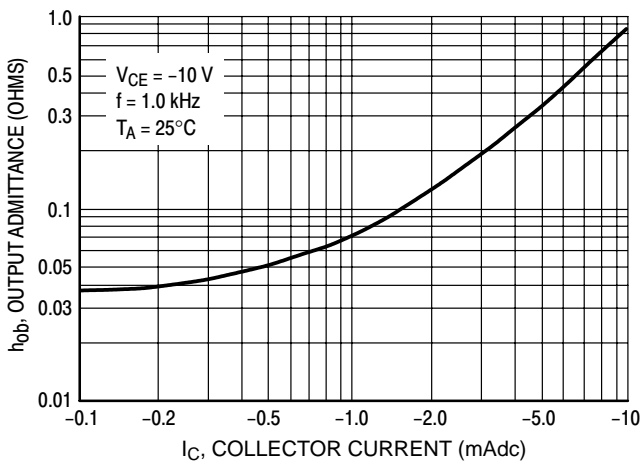


Figure 5. Output Admittance

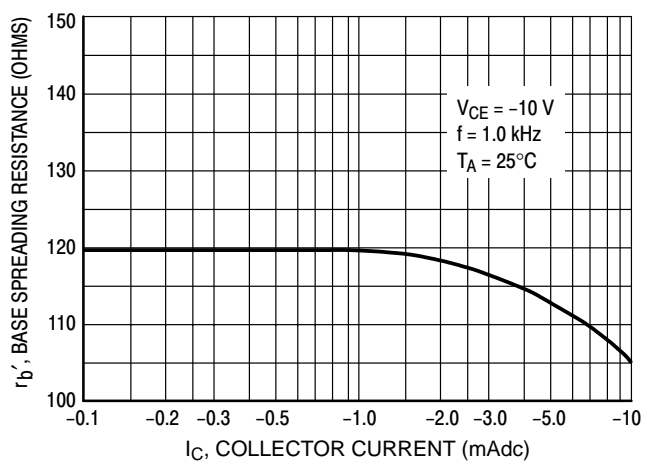


Figure 6. Base Spreading Resistance

# NSTB60ADW1T1

## Typical Electrical Characteristics – NPN BRT

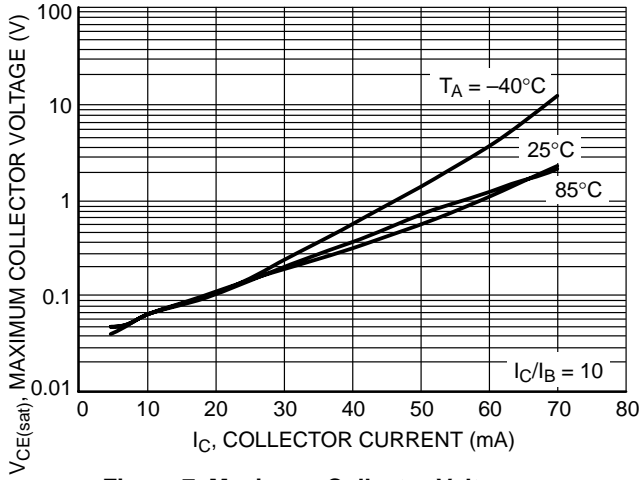


Figure 7. Maximum Collector Voltage versus Collector Current

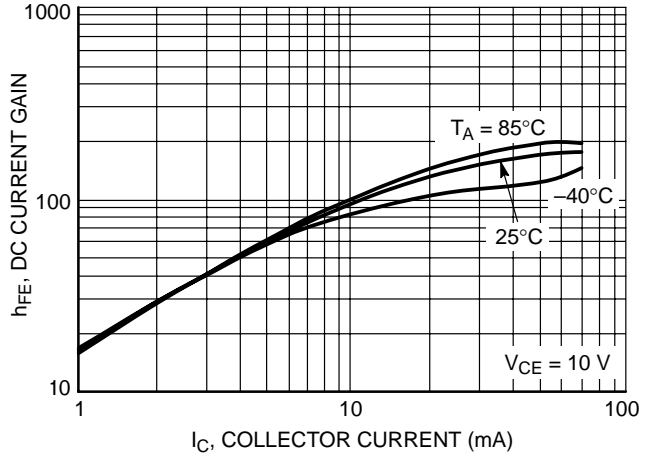


Figure 8. DC Current Gain

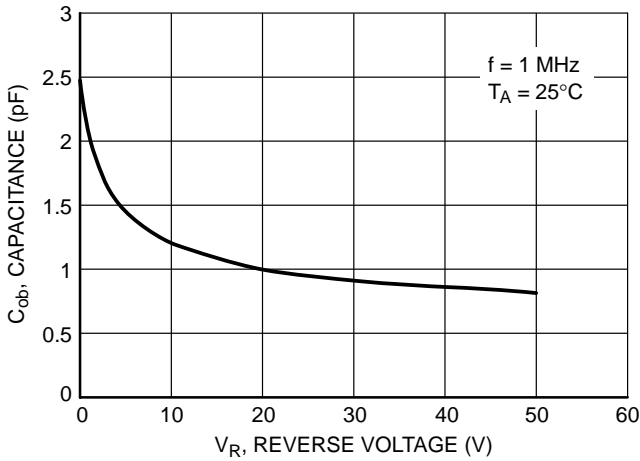


Figure 9. Output Capacitance

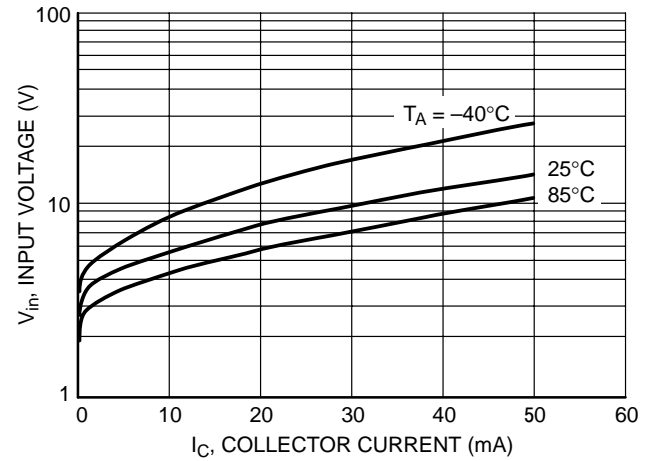


Figure 10. Input Voltage versus Output Voltage

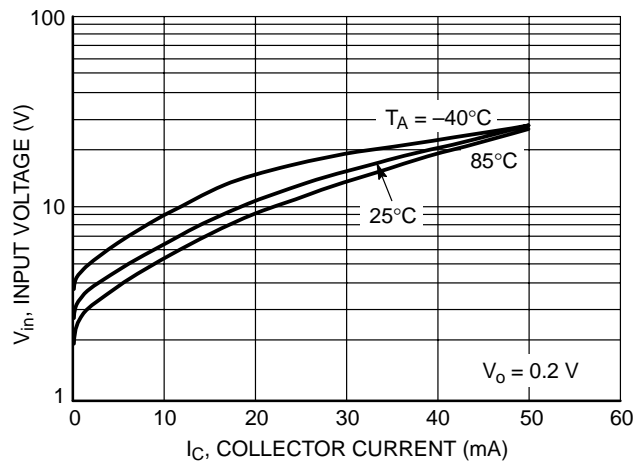


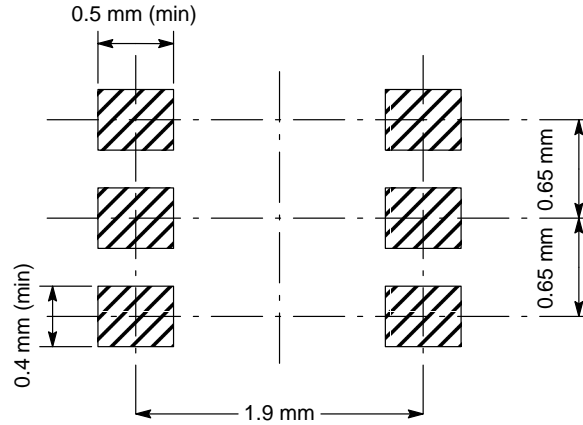
Figure 11. Input Voltage versus Output Current

**INFORMATION FOR USING THE SOT-363 SURFACE MOUNT PACKAGE**

**MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS**

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection

interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.



**SOT-363**

**SOT-363 POWER DISSIPATION**

The power dissipation of the SOT-363 is a function of the pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by  $T_{J(max)}$ , the maximum rated junction temperature of the die,  $R_{\theta JA}$ , the thermal resistance from the device junction to ambient, and the operating temperature,  $T_A$ . Using the values provided on the data sheet for the SOT-363 package,  $P_D$  can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature  $T_A$  of 25°C, one can calculate the power dissipation of the device which in this case is 256 milliwatts.

$$P_D = \frac{150^\circ\text{C} - 25^\circ\text{C}}{490^\circ\text{C/W}} = 256 \text{ milliwatts}$$

The 490°C/W for the SOT-363 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 256 milliwatts. There are other alternatives to achieving higher power dissipation from the SOT-363 package. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad®. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

**SOLDERING PRECAUTIONS**

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.\*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

\* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

**SOLDER STENCIL GUIDELINES**

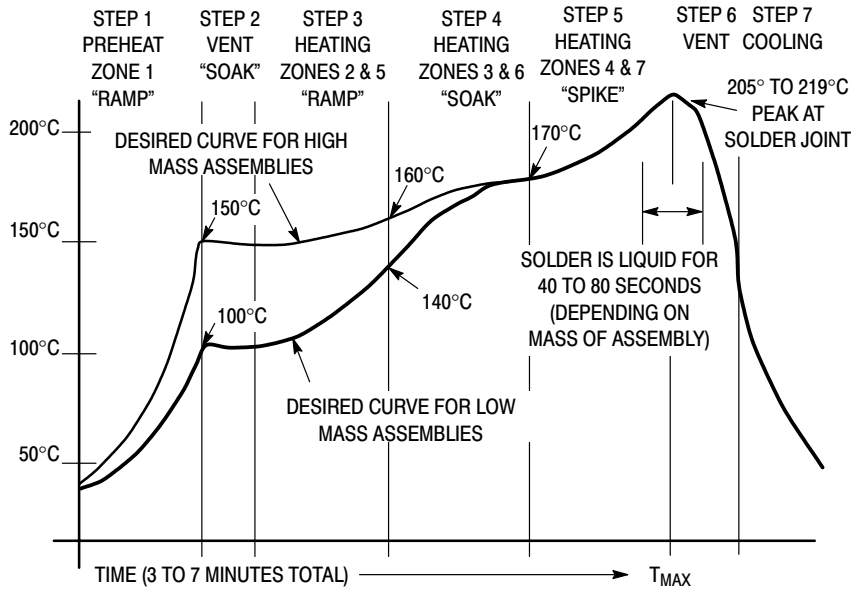
Prior to placing surface mount components onto a printed circuit board, solder paste must be applied to the pads. A solder stencil is required to screen the optimum amount of solder paste onto the footprint. The stencil is made of brass or stainless steel with a typical thickness of 0.008 inches.

The stencil opening size for the surface mounted package should be the same as the pad size on the printed circuit board, i.e., a 1:1 registration.

**TYPICAL SOLDER HEATING PROFILE**

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones, and a figure for belt speed. Taken together, these control settings make up a heating “profile” for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 12 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time.

The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

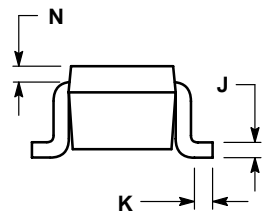
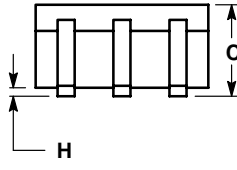
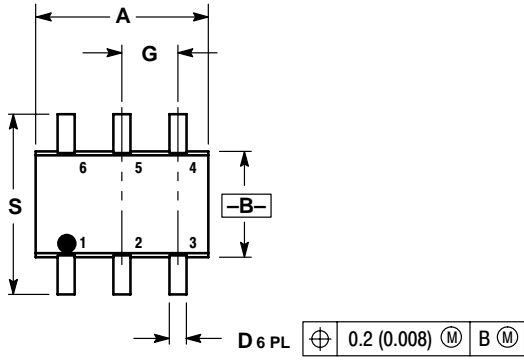


**Figure 12. Typical Solder Heating Profile**

# NSTB60ADW1T1

## PACKAGE DIMENSIONS

SOT-363  
CASE 419B-02  
ISSUE J




- NOTES:  
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.  
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20

- STYLE 1:  
PIN 1. EMITTER 2  
2. BASE 2  
3. COLLECTOR 1  
4. EMITTER 1  
5. BASE 1  
6. COLLECTOR 2

# NSTB60ADW1T1

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