EP7211

Preliminary Product Bulletin

FEATURES

- **Dynamically programmable clock speeds of 18, 36, 49, and 74 MHz at 2.5 V**
- **Performance matching 100-MHz Intel® Pentium-based PC**
- **Socket and register compatible with CL-PS7111**
- **Ultra low power**
  - — Designed for applications that require long battery life while using standard AA/AAA batteries or rechargeable cells
  - — 170 mW at 74 MHz in the Operating State
  - — 50 mW at 18 MHz in the Operating State
  - — 15 mW in the Idle State (clock to the CPU stopped, everything else running)
  - — 10 µW in the Standby State (realtime clock 'on', everything else stopped)
- **LCD controller**
  - — Interfaces directly to a single-scan panel monochrome LCD
  - — Panel width size is programmable from 32 to 1024 pixels in 16-pixel increments

(cont.)

High-Performance Ultra-Low-Power System-on-Chip with LCD Controller

OVERVIEW

The EP7211 is designed for ultra-low-power applications such as organizers/PDAs, two-way pagers, smart cellular phones, and industrial hand-held information appliances. The core-logic functionality of the device is built around an ARM720T processor with 8 K-bytes of four-way set-associative unified cache and a write buffer. Incorporated into the ARM720T is an enhanced memory management unit (MMU) which allows for Microsoft Windows CE support.

The EP7211 also includes a 32-bit Y2K-compliant Real-Time Clock (RTC) and comparator.

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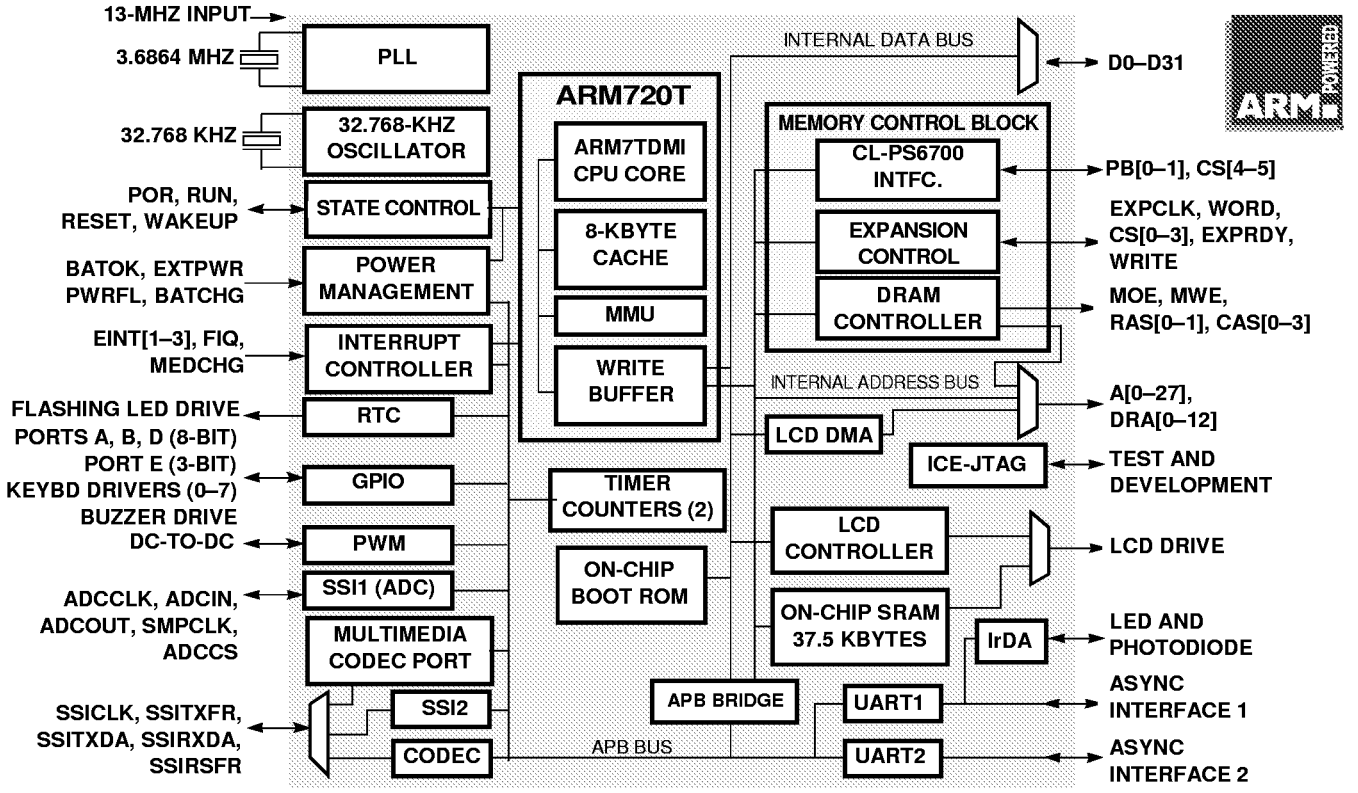
Functional Block Diagram



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FEATURES (cont.)

- — Video frame buffer size programmable up to 128 K-bytes
- — Bits per pixel programmable from 1, 2, or 4

- **ARM720T processor**
  - — ARM7TDMI CPU
  - — 8 K-bytes of four-way set-associative cache
  - — MMU with 64-entry TLB (transition look-aside buffer)
  - — Write Buffer
  - — Windows® CE enabled
  - — Thumb code support enabled
- **DRAM controller**
  - — Supports both 16- and 32-bit-wide DRAMs
  - — EDO support (Fast Page Mode support for 13 MHz and 18 MHz operation only)
- **ROM/SRAM/FLASH memory control**
  - — Decodes 4, 5, or 6 separate memory segments of up to 256 Mbytes each
  - — Each segment can be configured as 8, 16, or 32 bits wide and supports page-mode access
  - — Programmable access time for conventional ROM/SRAM/FLASH memory
- **37.5 K-bytes of on-chip SRAM for fast program execution and/or as a frame buffer**
- **On-chip ROM; for manufacturing boot-up support**
- **Four synchronous serial interfaces**
  - — ADC (SSI1) Interface: Master mode only; SPI®[1] and Microwire1®[2]-compatible (128 kbps operation)
  - — SSI2 Interface: Master/Slave mode; SPI/Microwire2 compatible (512 kbps operation)
  - — Audio Codec Interface: (64 kbps operation); for 18 Mhz operation only
  - — Multimedia Codec Port (Interfaces to Philips' UCB1100 and UCB1200 codecs) (9.216 Mbps operation)
- **27-bits of general-purpose I/O**
  - — Three 8-bit and one 3-bit GPIO port
  - — Supports scanning keyboard matrix
- **Two UARTs (16550 type)**
  - — Supports bit rates up to 115.2 kbps
  - — Contains two 16-byte FIFOs for TX and RX
  - — UART1 supports modem control signals
- **SIR (up to 115.2 kbps) infrared encoder**
  - — IrDA (Infrared Data Association) SIR protocol encoder can be optionally switched into TX and RX signals of UART1
- **DC-to-DC converter interface (PWM)**
  - — Provides two 96-kHz clock outputs with programmable duty ratio (from 1-in-16 to 15-in-16) that can be used to drive a DC to DC converter
- **Two timer counters**
- **208-pin LQFP and 256-ball PBGA packages**
- **Evaluation kit available with BOM, schematics, sample code, and design database**
- **Support for up to two ultra-low-power CL-PS6700 PC Card controllers**
- **Dedicated LED flasher pin from RTC**
- **Full JTAG boundary scan and Embedded ICE support**

[1] SPI is a registered trademark of Motorola®.
[2] Microwire is a registered trademark of National Semiconductor.

OVERVIEW (cont.)

Power Management

The EP7211 is designed for ultra-low-power operation. Its core operates at only 2.5 V, while its I/O has an operation range of 2.5 V–3.3 V. The device has three basic power states:

Operating — This state is the full performance state. All the clocks and peripheral logic are enabled.

Idle — This state is the same as the Operating State, except the CPU clock is halted while waiting for an event such as a key press.

Standby — This state is equivalent to the computer being switched off (no display), and the main oscillator shut down. An event such as a key press can wake-up the processor.

Memory Interfaces

There are two main external memory interfaces.

The first one is the ROM/SRAM/FLASH-style interface that has programmable wait-state timings and includes burst-mode capability, with eight chip selects decoding six 256-Mbyte sections of addressable space. For maximum flexibility, each bank can be specified to be 8, 16, or 32 bits wide. This allows the use of 8-bit-wide boot ROM options to minimize overall system cost. The on-chip boot ROM can be used in product manufacturing to serially download system code into system FLASH memory. To further minimize system memory requirements and cost, the ARM Thumb® instruction set is supported, providing for the

OVERVIEW (cont.)

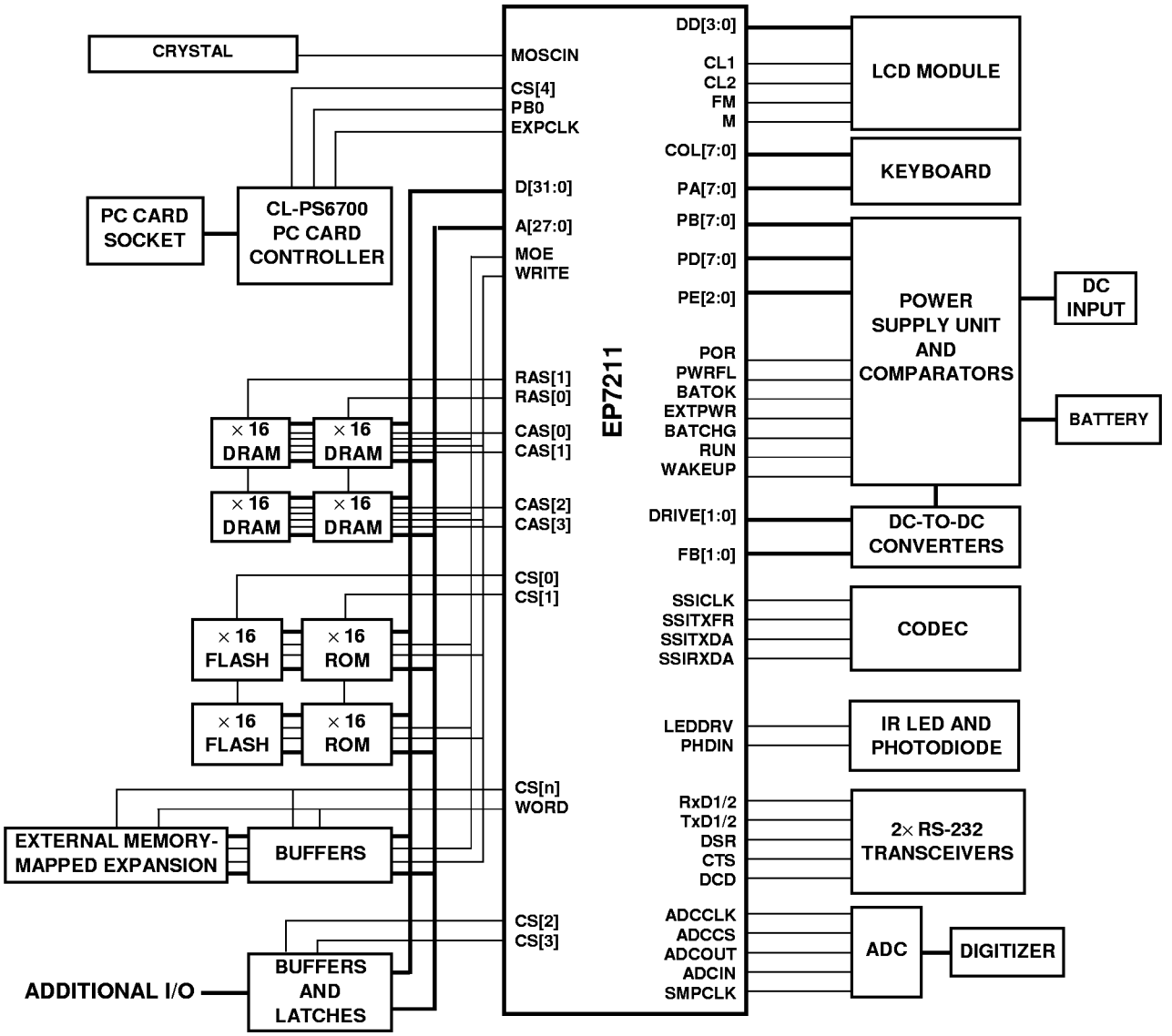
use of high-speed 32-bit operations in 16-bit op-codes and yielding industry-leading code density.

The second is the programmable 16- or 32-bit-wide DRAM interface that allows direct connection of up to two banks of DRAM, each bank containing up to 256 Mbytes. To assure the lowest possible power consumption, the EP7211 supports self-refresh DRAMs, which are placed in a low-power state by the device when it enters the low-power Standby State. EDO and Fast Page DRAM are supported.

A DMA address generator is also provided that fetches video display data for the LCD controller from main DRAM memory. The display frame buffer start address is programmable. In addition, the built-in LCD controller can utilize external or internal SRAM for memory, thus eliminating the need for DRAMs.

Serial Interfaces

The EP7211 includes two 16550-type UARTs for RS-232 serial communications, both of which have two 16-byte FIFOs for receiving and transmitting data. The UARTs support bit rates up to 115.2 kbps. An IrDA SIR protocol encoder/decoder can be optionally switched into the RX/TX signals to/from one of the UARTs to



A EP7211–Based System

OVERVIEW *(cont.)*

enable these signals to drive an infrared communication interface directly.

Four synchronous serial interfaces (codec, SSI1, SSI2, and MCP) are provided. Three of them (codec, SSI2, and MCP) are multiplexed onto a single set of interface pins. The full-duplex codec interface allows direct connection of a standard audio codec chip to the EP7211, allowing storage and playback of sound. SSI2 supports both master and slave mode. SSI1 supports master mode only. Both SSI1 and SSI2 support two industry-standard protocols (SPI® and Microwire®) for interfacing standard devices (e.g. Max148/9 or AD7811/12 ADC) and for allowing peripheral expansion (e.g. a digitizer pen). A Multimedia CODEC Port (MCP) can be used to communicate with a multi-functional codec device like the Philips® UCB1100.

Packaging

The EP7211 is available in a 208-pin LQFP package and a 256-ball PBGA package.

System Design

As shown in system block diagram, simply adding desired memory and peripherals to the highly integrated EP7211 completes a low-power system solution. All necessary interface logic is integrated on-chip.

Development Boards

Cirrus Logic offers an evaluation and development environment for the EP7211 in the form of the EDB7211-2 Development Kit.

The EDB7211-2 developmnet kit is a complete development platform with access to the features and capabilities of the EP7211. The kit provides the tools required for developing and testing the design of a highly integrated EP7211 system.

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