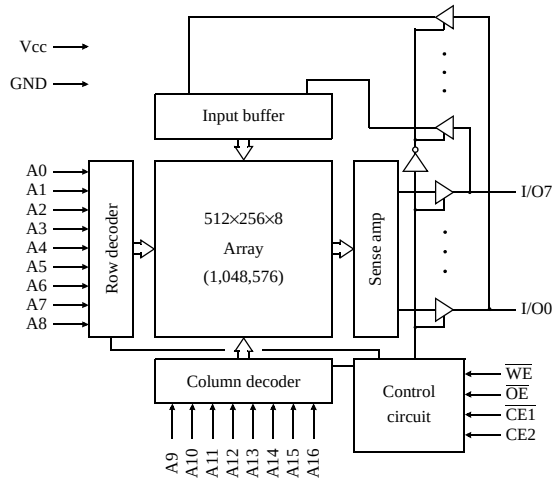
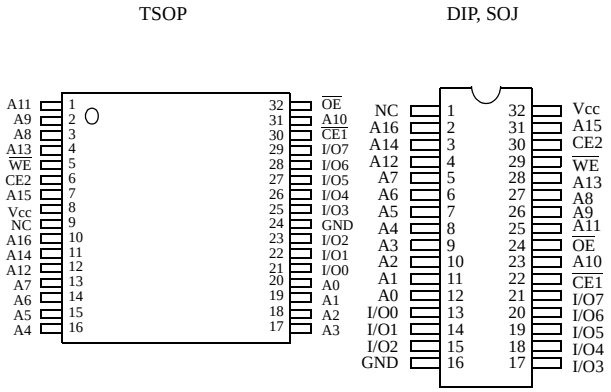
Features

- Organization: 131,072 words × 8 bits
- High speed
  - 10/12/15/20 ns address access time
  - 3/3/4/5 ns output enable access time
- Low power consumption available
  - Active: 180 mW max (3V, 15 ns)
  - Standby: 1.8 mW max, CMOS I/O
  - Very low DC component in active power
- 2.0V data retention
- Equal access and cycle times
- Easy memory expansion with $\overline{CE1}$, CE2, $\overline{OE}$ inputs
- TTL/LVTTL-compatible, three-state I/O
- 32-pin JEDEC standard packages
  - 300 mil PDIP and SOJ
    Socket compatible with 7C512 (64K×8)
  - 400 mil SOJ
  - 8mm × 20mm TSOP
- ESD protection ≥ 2000 volts
- Latch-up current ≥ 200 mA
- 3.3V and 5.0V versions available
- Industrial and commercial temperature available
- Intelliwatt[tm] low power and CPG versions available

Logic block diagram



Pin arrangement



Selection guide

		-10	-12	-15	-20	Unit
Maximum address access time		10	12	15	20	ns
Maximum output enable access time		3	3	4	5	ns
Maximum operating current	AS7C1024	175	160	120	110	mA
	AS7C1024L	–	120	95	80	mA
	AS7C31024	150	100	70	65	mA
	AS7C31024L	–	60	50	45	mA
Maximum static standby current (L)		0.1	0.1	0.1	0.1	mA

Shaded areas contain advance information.

Functional description

The AS7C1024 and AS7C31024 are high performance CMOS 1,048,576-bit Static Random Access Memories (SRAM) organized as 131,072 words × 8 bits. It is designed for memory applications where fast data access, low power, and simple interfacing are desired.

Equal address access and cycle times (t_{AA}, t_{RC}, t_{WC}) of 10/12/15/20 ns with output enable access times (t_{OE}) of 3/3/4/5 ns are ideal for high performance applications. Active high and low chip enables ($\overline{CE1}$, CE2) permit easy memory expansion with multiple-bank systems.

When $\overline{CE1}$ is HIGH or CE2 is LOW the device enters standby mode. If inputs are still toggling, the devices will consume I_{SB} power. If the bus is static, then full standby power is reached (I_{SB1} or I_{SB2}). The 31024L for example, is guaranteed not to exceed 0.33mW under nominal full standby conditions. All devices in this family will retain data when V_{CC} is reduced as low as 2.0V.

A write cycle is accomplished by asserting write enable ($\overline{WE}$) and both chip enables ($\overline{CE1}$, CE2). Data on the input pins I/O0-I/O7 is written on the rising edge of $\overline{WE}$ (write cycle 1) or the active-to-inactive edge of $\overline{CE1}$ or CE2 (write cycle 2). To avoid bus contention, external devices should drive I/O pins only after outputs have been disabled with output enable ($\overline{OE}$) or write enable ($\overline{WE}$).

A read cycle is accomplished by asserting output enable ($\overline{OE}$) and both chip enables ($\overline{CE1}$, CE2), with write enable ($\overline{WE}$) HIGH. The chip drives I/O pins with the data word referenced by the input address. When either chip enable is inactive, output enable is inactive, or write enable is active, output drivers stay in high-impedance mode.

All chip inputs and outputs are TTL/LVTTL-compatible, and operation is from a single 5V supply or 3.3V supply. 128Kx8 and 64Kx16 SRAMs are also available in ultra-low power Intelliwatt^{tm} versions. For Intelliwatt specifications, please see the AS7C31024LL and AS7C31026LL datasheets respectively. The revolutionary pinout (CPG) version of the 128Kx8 may be found as AS7C1025, AS7C31025.

Absolute maximum ratings

Parameter	Symbol	Min	Max	Unit
Voltage on any pin relative to GND	V_t	–0.5	+7.0	V
Power dissipation	P_D	–	1.0	W
Storage temperature (plastic)	T_{stg}	–55	+150	°C
Temperature under bias	T_{bias}	–10	+85	°C
DC output current	I_{out}	–	20	mA

Stresses greater than those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Truth table

$\overline{CE1}$	CE2	$\overline{WE}$	$\overline{OE}$	Data	Mode
H	X	X	X	High Z	Standby (I_{SB}, I_{SB1})
X	L	X	X	High Z	Standby (I_{SB}, I_{SB1})
L	H	H	H	High Z	Output disable
L	H	H	L	D_{out}	Read
L	H	L	X	D_{in}	Write

Key: X = Don't Care, L = LOW, H = HIGH

Recommended operating conditions

Parameter		Symbol	Min	Nominal	Max	Unit
Supply voltage	5V devices	V_{CC}	4.5	5.0	5.5	V
	3.3V devices	V_{CC}	3.0	3.3	3.6	V
		GND	0.0	0.0	0.0	V
Input voltage	AS7C1024	V_{IH}	2.2	–	V_{CC} + 0.5	V
	AS7C31024	V_{IH}	2.0	–	V_{CC} + 0.5	V
		V_{IL}†	–0.5	–	0.8	V

†V_{IL} min = –3.0V for pulse width less than $t_{RC}/2$.

DC input/output characteristics, AS7C1024 family[1]

Parameter	Symbol	Test conditions	-10 Min	-10 Max	-12 Min	-12 Max	-15 Min	-15 Max	-20 Min	-20 Max	Unit
Input leakage current	$\lvert I_{LI} \rvert$	V_{CC} = Max, V_{in} = GND to V_{CC}	–	1	–	1	–	1	–	1	µA
Output leakage current	$\lvert I_{LO} \rvert$	$\overline{CE1}$ = V_{IH} *or* CE2 = V_{IL}, V_{CC} = Max, V_{out} = GND to V_{CC}	–	1	–	1	–	1	–	1	µA
Output voltage	V_{OL}	I_{OL} = 8 mA, V_{CC} = Min	–	0.4	–	0.4	–	0.4	–	0.4	V
	V_{OH}	I_{OH} = –4 mA, V_{CC} = Min	2.4	–	2.4	–	2.4	–	2.4	–	V

Shaded areas contain advance information.

Power supply characteristics, AS7C1024 and AS7C1024L[1]

Parameter	Symbol	Test conditions		-10 Min	-10 Max	-12 Min	-12 Max	-15 Min	-15 Max	-20 Min	-20 Max	Unit
Operating power supply current	I_{CC}	$\overline{CE1}$ = V_{IL}, CE2 = V_{IH}, $f = f_{max}$, I_{out} = 0 mA		–	175	–	160	–	120	–	110	mA
			L	–	–	–	120	–	95	–	80	mA
Standby power supply current	I_{SB}	$\overline{CE1}$ = V_{IH} *or* CE2 = V_{IL}, $f = f_{max}$, all inputs toggling		–	55	–	50	–	40	–	40	mA
			L	–	–	–	35	–	25	–	25	mA
	I_{SB1}	Chip disabled, f = 0, $V_{in} \le 0.2V$ *or* $V_{in} \ge V_{CC}–0.2V$		–	5	–	5	–	5	–	5	mA
			L	–	–	–	0.5	–	0.5	–	0.5	mA
	I_{SB2}	Chip disabled, f = 0, t_A = 25°C $V_{in} \le 0.2V$ *or* $V_{in} \ge V_{CC}–0.2V$,	L	–	–	–	0.1	–	0.1	–	0.1	mA

Shaded areas contain advance information.

Power supply characteristics, AS7C31024 and AS7C31024L[1]

Parameter	Symbol	Test conditions		-10 Min	-10 Max	-12 Min	-12 Max	-15 Min	-15 Max	-20 Min	-20 Max	Unit
Operating power supply current	I_{CC}	$\overline{CE1}$ = V_{IL}, CE2 = V_{IH}, $f = f_{max}$, I_{out} = 0 mA		–	150	–	100	–	70	–	65	mA
			L	–	–	–	60	–	50	–	45	mA
Standby power supply current	I_{SB}	$\overline{CE1}$ = V_{IH} *or* CE2 = V_{IL}, $f = f_{max}$		–	55	–	50	–	40	–	40	mA
			L	–	–	–	35	–	25	–	25	mA
	I_{SB1}	Chip disabled, f = 0, $V_{in} \le 0.2V$ *or* $V_{in} \ge V_{CC}-0.2V$		–	5	–	5	–	5	–	5	mA
			L	–	–	–	0.5	–	0.5	–	0.5	mA
	I_{SB2}	Chip disabled, f = 0,t_A = 25C $V_{in} \le 0.2V$ *or* $V_{in} \ge V_{CC}-0.2V$,	L	–	–	–	0.1	–	0.1	–	0.1	mA

Shaded areas contain advance information.

Capacitance [2]

(f = 1 MHz, T_a = Room temperature, V_{CC} = 5V)

Parameter	Symbol	Signals	Test conditions	Max	Unit
Input capacitance	C_{IN}	A, $\overline{CE1}$, CE2, $\overline{WE}$, $\overline{OE}$	V_{in} = 0V	5	pF
I/O capacitance	$C_{I/O}$	I/O	V_{in} = V_{out} = 0V	7	pF

Read cycle [3,9,12]

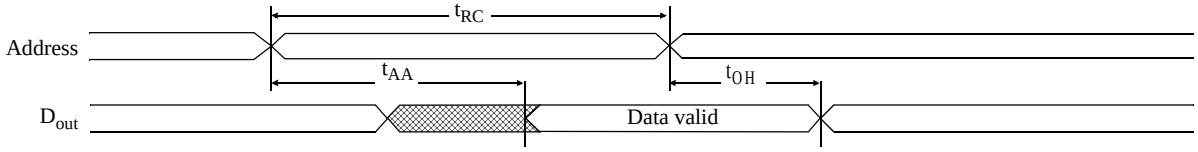
Parameter	Symbol	-10 Min	-10 Max	-12 Min	-12 Max	-15 Min	-15 Max	-20 Min	-20 Max	Unit	Notes
Read cycle time	t_{RC}	10	–	12	–	15	–	20	–	ns	
Address access time	t_{AA}	–	10	–	12	–	15	–	20	ns	3
Chip enable ($\overline{CE1}$) access time	t_{ACE1}	–	10	–	12	–	15	–	20	ns	3, 12
Chip enable (CE2) access time	t_{ACE2}	–	10	–	12	–	15	–	20	ns	3, 12
Output enable ($\overline{OE}$) access time	t_{OE}	–	3	–	3	–	4	–	5	ns	
Output hold from address change	t_{OH}	2	–	3	–	3	–	3	–	ns	5
$\overline{CE1}$ LOW to output in Low Z	t_{CLZ1}	3	–	3	–	3	–	3	–	ns	4, 5, 12
CE2 HIGH to output in Low Z	t_{CLZ2}	3	–	3	–	3	–	3	–	ns	4, 5, 12
$\overline{CE1}$ HIGH to output in High Z	t_{CHZ1}	–	3	–	3	–	4	–	5	ns	4, 5, 12
CE2 LOW to output in High Z	t_{CHZ2}	–	3	–	3	–	4	–	5	ns	4, 5, 12
$\overline{OE}$ LOW to output in Low Z	t_{OLZ}	0	–	0	–	0	–	0	–	ns	4, 5
$\overline{OE}$ HIGH to output in High Z	t_{OHZ}	–	3	–	3	–	4	–	5	ns	4, 5
Power up time	t_{PU}	0	–	0	–	0	–	0	–	ns	4, 5, 12
Power down time	t_{PD}	–	10	–	12	–	15	–	20	ns	4, 5, 12

Key to switching waveforms

Rising input Falling input Undefined output/don't care

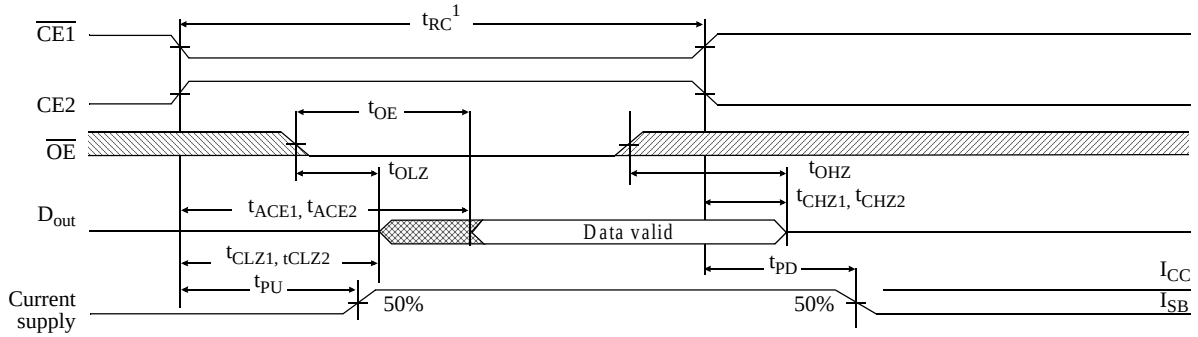
Read waveform 1 *3,6,7,9,12*

Address controlled



Read waveform 2 *3,6,8,9,12*

$\overline{CE1}$ and CE2 controlled



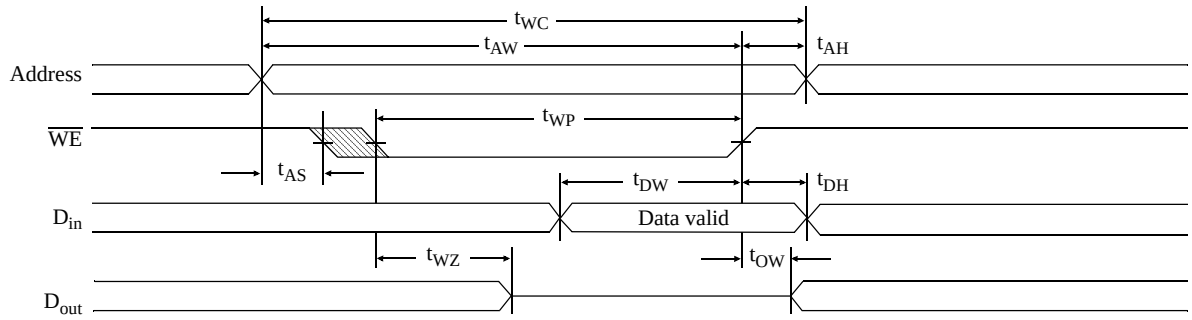
Write cycle *11, 12*

		-10		-12		-15		-20			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
Write cycle time	t_{WC}	10	–	12	–	15	–	20	–	ns	
Chip enable ($\overline{CE1}$) to write end	t_{CW1}	9	–	10	–	12	–	12	–	ns	12
Chip enable (CE2) to write end	t_{CW2}	9	–	10	–	12	–	12	–	ns	12
Address setup to write end	t_{AW}	9	–	10	–	12	–	12	–	ns	
Address setup time	t_{AS}	0	–	0	–	0	–	0	–	ns	12
Write pulse width	t_{WP}	7	–	8	–	9	–	12	–	ns	
Address hold from end of write	t_{AH}	0	–	0	–	0	–	0	–	ns	
Data valid to write end	t_{DW}	6	–	6	–	9	–	10	–	ns	
Data hold time	t_{DH}	0	–	0	–	0	–	0	–	ns	4, 5
Write enable to output in High Z	t_{WZ}	–	5	–	5	–	5	–	5	ns	4, 5
Output active from write end	t_{OW}	3	–	3	–	3	–	3	–	ns	4, 5

Shaded areas contain advance information.

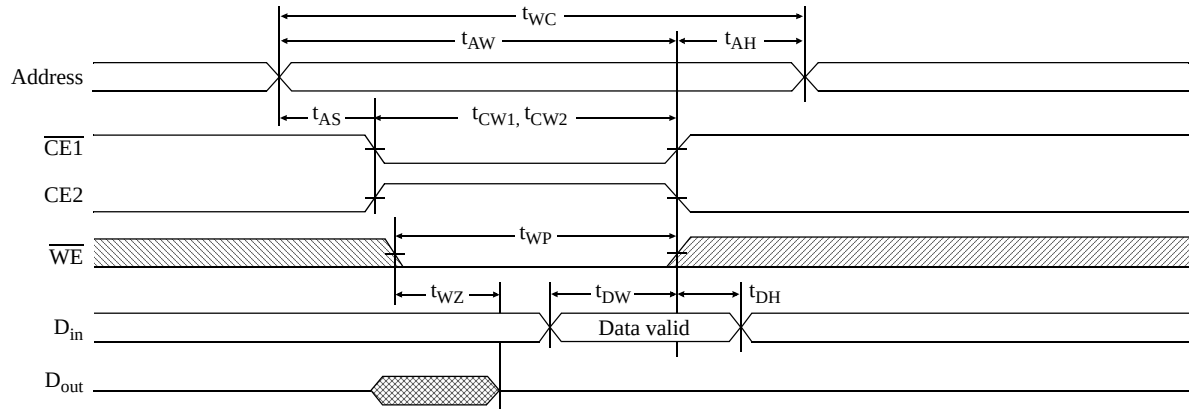
Write waveform 1 *10,11,12*

$\overline{WE}$ controlled



Write waveform 2 *10,11,12*

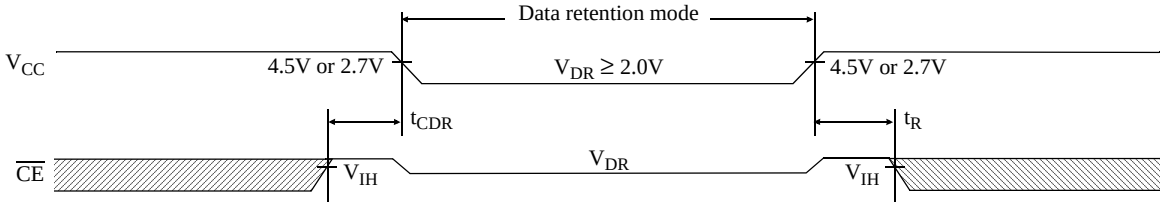
$\overline{CE1}$ and CE2 controlled



Data retention characteristics [14]

Parameter	Symbol	Test conditions	Min	Max	Unit
V_{CC} for data retention	V_{DR}	V_{CC} = 2.0V	2.0	–	V
Data retention current	I_{CCDR}	$\overline{CE1} \geq V_{CC}-0.2V$ *or* $CE2 \leq 0.2V$	–	500 (100 L)	µA
Chip deselect to data retention time	t_{CDR}		0	–	ns
Operation recovery time	t_R	$V_{in} \geq V_{CC}-0.2V$ *or* $V_{in} \leq 0.2V$	t_{RC}	–	ns
Input leakage current	$\lvert I_{LI} \rvert$		–	1	µA

Data retention waveform



AC test conditions

- 5V output load: see Figure B, except as noted see Figure C.
- 3.3V output load: see Figure D, except as noted see Figure E.
- Input pulse level: GND to 3.0V. See Figure A.
- Input rise and fall times: 5 ns. See Figure A.
- Input and output timing reference levels: 1.5V.

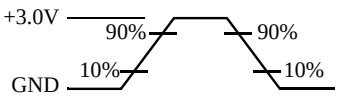


Figure A: Input waveform

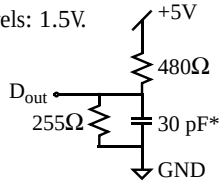
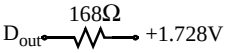


Figure B: Output load

Thevenin equivalent:



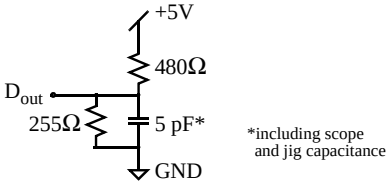


Figure C: Output load for t_{CLZ}, t_{CHZ}, t_{OLZ}, t_{OHZ}, t_{OW}

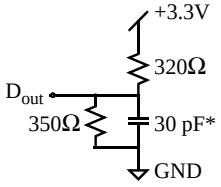


Figure D: Output load

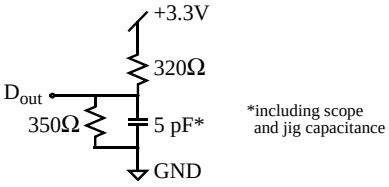
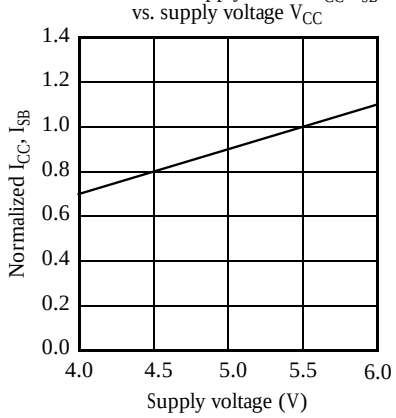


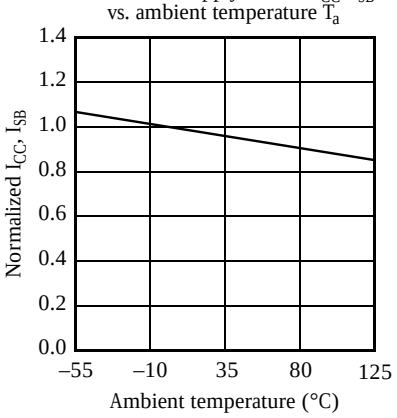
Figure C: Output load for t_{CLZ}, t_{CHZ}, t_{OLZ}, t_{OHZ}, t_{OW}

Typical DC and AC characteristics

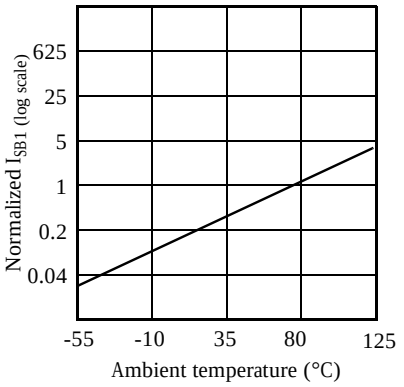
Normalized supply current I_{CC}, I_{SB} vs. supply voltage V_{CC}



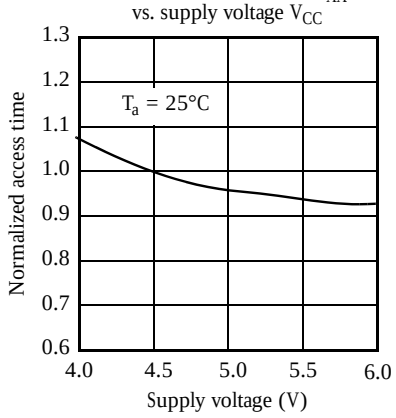
Normalized supply current I_{CC}, I_{SB} vs. ambient temperature T_a



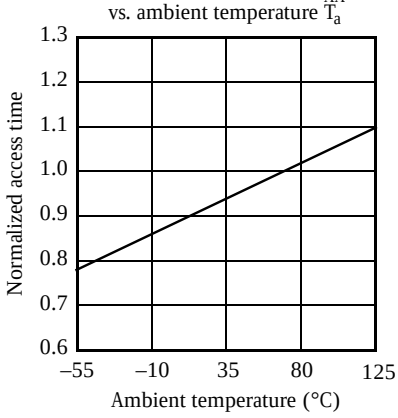
Normalized supply current I_{SB1} vs. ambient temperature T_a



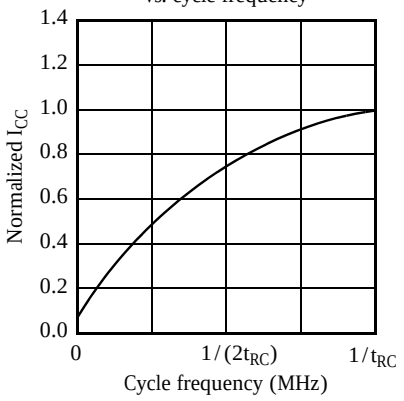
Normalized access time t_{AA} vs. supply voltage V_{CC}



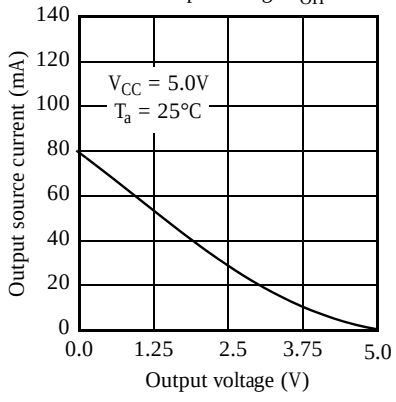
Normalized access time t_{AA} vs. ambient temperature T_a



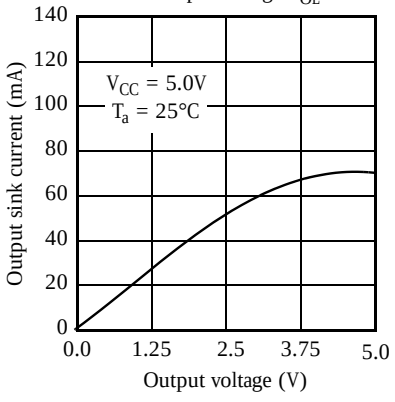
Normalized supply current I_{CC} vs. cycle frequency



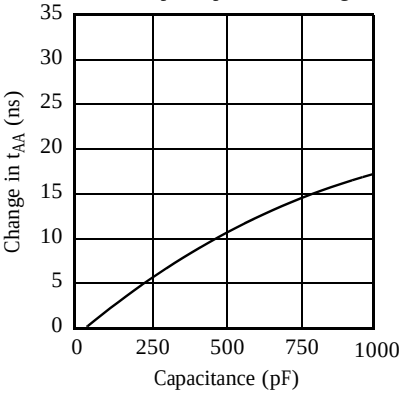
Output source current I_{OH} vs. output voltage V_{OH}



Output sink current I_{OL} vs. output voltage V_{OL}



Typical access time change Δt_{AA} vs. output capacitive loading



Notes

1 During V_{CC} power-up, a pull-up resistor to V_{CC} on $\overline{CE1}$ is required to meet I_{SB} specification.
2 This parameter is sampled and not 100% tested.
3 For test conditions, see *AC Test Conditions*, Figures A, B, C.
4 t_{CLZ} and t_{CHZ} are specified with CL = 5pF as in Figure C. Transition is measured ±500mV from steady-state voltage.
5 This parameter is guaranteed but not tested.
6 $\overline{WE}$ is HIGH for read cycle.
7 $\overline{CE1}$ and $\overline{OE}$ are LOW and CE2 is HIGH for read cycle.
8 Address valid prior to or coincident with $\overline{CE}$ transition LOW.
9 All read cycle timings are referenced from the last valid address to the first transitioning address.
10 $\overline{CE1}$ or $\overline{WE}$ must be HIGH or CE2 LOW during address transitions.
11 All write cycle timings are referenced from the last valid address to the first transitioning address.
12 $\overline{CE1}$ and CE2 have identical timing.
13 This data applicable to the AS7C1024. The AS7C31024 functions similarly.
14 2V data retention applies to commercial temperature operating range only.

AS7C1024 family ordering codes

Package \ Access time	10 ns	12 ns	15 ns	20 ns
Plastic DIP, 300 mil	New designs using PDIP are discouraged. Contact Alliance Sales for PDIP availability of limited production.			
Plastic SOJ, 300 mil	AS7C1024-10TJC	AS7C1024-12TJC	AS7C1024-15TJC	AS7C1024-20TJC
		AS7C1024L-12TJC	AS7C1024L-15TJC	AS7C1024L-20TJC
	AS7C31024-10TJC	AS7C31024-12TJC	AS7C31024-15TJC AS7C31024-15TJI	AS7C31024-20TJC AS7C31024-20TJI
		AS7C31024L-12TJC	AS7C31024L-15TJC	AS7C31024L-20TJC
Plastic SOJ, 400 mil	AS7C1024-10JC	AS7C1024-12JC	AS7C1024-15JC AS7C1024-15JI	AS7C1024-20JC AS7C1024-20JI
		AS7C1024L-12JC	AS7C1024L-15JC	AS7C1024L-20JC
	AS7C31024-10JC	AS7C31024-12JC	AS7C31024-15JC AS7C31024-15JI	AS7C31024-20JC AS7C31024-20JI
		AS7C31024L-12JC	AS7C31024L-15JC	AS7C31024L-20JC
TSOP 8×20		AS7C1024-12TC	AS7C1024-15TC	AS7C1024-20TC
		AS7C1024L-12TC	AS7C1024L-15TC	AS7C1024L-20TC
		AS7C31024-12TC	AS7C31024-15TC	AS7C31024-20TC
		AS7C31024L-12TC	AS7C31024L-15TC	AS7C31024L-20TC

Shaded areas contain advance information.

AS7C1024 family part numbering system

AS7C	X	1024	X	–XX	X	X
SRAM prefix	Blank=5V CMOS 3=3.3V CMOS	Device number	L = low power	Access time	Package:TP =PDIP 300 mil T =TSOP 8×20 J =SOJ 400 mil TJ =SOJ 300 mil	Temperature range C = Commercial, 0°C to 70°C I = Industrial, -40°C to 85°C