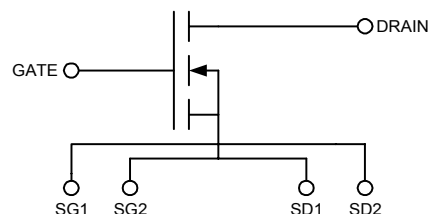


- ◆ N-Channel Enhancement Mode
- ◆ Low Q_g and R_g
- ◆ High dv/dt
- ◆ Nanosecond Switching
- ◆ 30MHz Maximum Frequency

$V_{DSS} = 1000 \text{ V}$
 $I_{D25} = 21 \text{ A}$
 $R_{DS(on)} = 0.52 \Omega$
 $P_{DHS} = 600 \text{ W}$

| Symbol | Test Conditions | Maximum Ratings | |
|---------------|---|-----------------|------------------|
| V_{DSS} | $T_J = 25^\circ\text{C}$ to 150°C | 1000 | V |
| V_{DGR} | $T_J = 25^\circ\text{C}$ to 150°C ; $R_{GS} = 1 \text{ M}\Omega$ | 1000 | V |
| V_{GS} | Continuous | ± 20 | V |
| V_{GSM} | Transient | ± 30 | V |
| I_{D25} | $T_c = 25^\circ\text{C}$ | 21 | A |
| I_{DM} | $T_c = 25^\circ\text{C}$, pulse width limited by T_{JM} | 126 | A |
| I_{AR} | $T_c = 25^\circ\text{C}$ | 21 | A |
| E_{AR} | $T_c = 25^\circ\text{C}$ | 30 | mJ |
| dv/dt | $I_s \leq I_{DM}$, $di/dt \leq 100 \text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DSS}$, $T_J \leq 150^\circ\text{C}$, $R_G = 0.2 \Omega$ | 5 | V/ns |
| | $I_s = 0$ | >200 | V/ns |
| P_{DHS} | $T_c = 25^\circ\text{C}$ Derate $4.4 \text{ W}/^\circ\text{C}$ above 25°C | 600 | W |
| P_{DAMB} | $T_c = 25^\circ\text{C}$ | 4.5 | W |
| T_J | | -55...+150 | $^\circ\text{C}$ |
| T_{JM} | | 150 | $^\circ\text{C}$ |
| T_{stg} | | -55...+150 | $^\circ\text{C}$ |
| T_L | 1.6mm (0.063 in) from case for 10 s | 300 | $^\circ\text{C}$ |
| Weight | | 3 | g |



Features

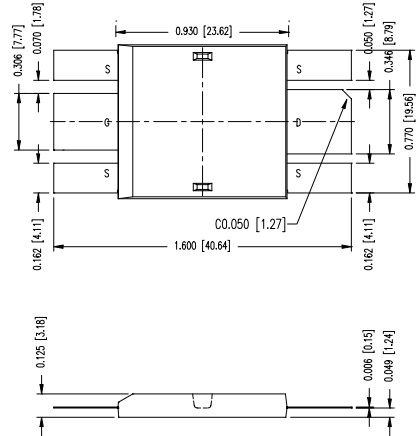
- Isolated Substrate
 - high isolation voltage (>2500V)
 - excellent thermal transfer
 - Increased temperature and power cycling capability
- IXYS advanced low Q_g process
- Low gate charge and capacitances
 - easier to drive
 - faster switching
- Low $R_{DS(on)}$
- Very low insertion inductance (<2nH)
- No beryllium oxide (BeO) or other hazardous materials

Advantages

- Optimized for RF and high speed switching at frequencies to 30MHz
- Easy to mount—no insulators needed
- High power density

| Symbol | Test Conditions | Characteristic Values | | |
|--------------|---|---|------|--------------------------|
| | | $T_J = 25^\circ\text{C}$ unless otherwise specified | | |
| | | min. | typ. | max. |
| V_{DSS} | $V_{GS} = 0 \text{ V}$, $I_D = 3 \text{ ma}$ | 1000 | | V |
| $V_{GS(th)}$ | $V_{DS} = V_{GS}$, $I_D = 4 \text{ ma}$ | 2.5 | | 5.5 V |
| I_{GSS} | $V_{GS} = \pm 20 \text{ V}_{DC}$, $V_{DS} = 0$ | | | $\pm 100 \text{ nA}$ |
| I_{DSS} | $V_{DS} = 0.8 V_{DSS}$, $T_J = 25^\circ\text{C}$ $V_{GS} = 0$, $T_J = 125^\circ\text{C}$ | | | 50 μA 1 mA |
| $R_{DS(on)}$ | $V_{GS} = 15 \text{ V}$, $I_D = 0.5 I_{D25}$ Pulse test, $t \leq 300 \mu\text{s}$, duty cycle $d \leq 2\%$ | | | 0.52 Ω |
| g_{fs} | $V_{DS} = 15 \text{ V}$, $I_D = 0.5 I_{D25}$, pulse test | | 22 | S |

| Symbol | Test Conditions | Characteristic Values ($T_J = 25^\circ\text{C}$ unless otherwise specified) | | |
|--------------|---|---|------|----------|
| | | min. | typ. | max. |
| R_G | | | 0.3 | Ω |
| C_{iss} | | | 5500 | pF |
| C_{oss} | $V_{GS} = 0\text{ V}, V_{DS} = 0.8 V_{DSS(max)},$ $f = 1\text{ MHz}$ | | 640 | pF |
| C_{rss} | | | 190 | pF |
| $T_{d(on)}$ | | | 5 | ns |
| T_{on} | $V_{GS} = 15\text{ V}, V_{DS} = 0.8 V_{DSS}$ $I_D = 0.5 I_{DM}$ | | 5 | ns |
| $T_{d(off)}$ | $R_G = 0.2\ \Omega$ (External) | | 5 | ns |
| T_{off} | | | 8 | ns |
| $Q_{g(on)}$ | | | 160 | nC |
| Q_{gs} | $V_{GS} = 10\text{ V}, V_{DS} = 0.5 V_{DSS}$ $I_D = 0.5 I_{D25}$ | | 35 | nC |
| Q_{gd} | | | 77 | nC |
| R_{thJHS} | | | 0.20 | K/W |



| Symbol | Test Conditions | Characteristic Values ($T_J = 25^\circ\text{C}$ unless otherwise specified) | | |
|----------|--|---|------|---------------|
| | | min. | typ. | max. |
| I_S | $V_{GS} = 0\text{ V}$ | | | 21 A |
| I_{SM} | Repetitive; pulse width limited by T_{JM} | | | 126 A |
| V_{SD} | $I_F = I_S, V_{GS} = 0\text{ V},$ Pulse test, $t \leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$ | | | 1.5 V |
| T_{rr} | | | 200 | ns |
| Q_{RM} | $I_F = I_S, -di/dt = 100\text{ A}/\mu\text{s},$ $V_R = 100\text{ V}$ | | 0.6 | μC |
| I_{RM} | | | 8 | A |

For detailed device mounting and installation instructions, see the “*DE-Series MOSFET Mounting Instructions*” technical note on DEI’s web site at www.directedenergy.com/apptech.htm

Directed Energy, Inc. reserves the right to change limits, test conditions and dimensions.
DEI MOSFETS are covered by one or more of the following U.S. patents:

- | | | | | | |
|-----------|-----------|-----------|-----------|-----------|-----------|
| 4,835,592 | 4,850,072 | 4,881,106 | 4,891,686 | 4,931,844 | 5,017,508 |
| 5,034,796 | 5,049,961 | 5,063,307 | 5,187,117 | 5,237,481 | 5,486,715 |
| 5,381,025 | 5,640,045 | | | | |

102N21A DE-SERIES SPICE Model (Preliminary)

The DE-SERIES SPICE Model is illustrated in Figure 1. The model is an expansion of the SPICE level 3 MOSFET model. It includes the stray inductive terms L_G , L_S and L_D . R_d is the $R_{DS(ON)}$ of the device, R_{ds} is the resistive leakage term. The output capacitance, C_{OSS} , and reverse transfer capacitance, C_{RSS} are modeled with reversed biased diodes. This provides a varactor type response necessary for a high power device model. The turn on delay and the turn off delay are adjusted via R_{on} and R_{off} .

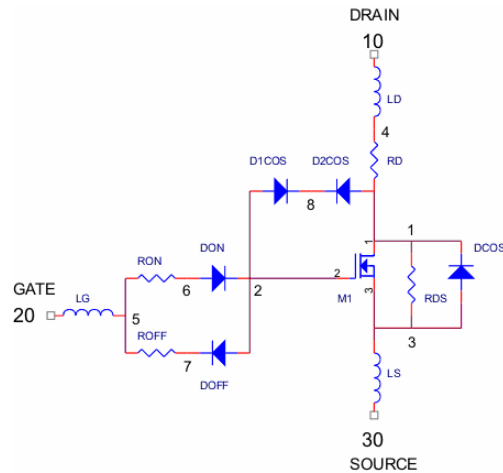


Figure 1 DE-SERIES SPICE Model

This SPICE model may be downloaded as a text file from the DEI web site at www.directedenergy.com/spice.htm

Net List:

```
.SUBCKT 102N21A 10 20 30
* TERMINALS: D G S
* 1000 Volt 21 Amp 0.52 ohm N-Channel Power MOSFET
* REV.A 01-09-02
M1 1 2 3 3 DMOS L=1U W=1U
RON 5 6 0.3
DON 6 2 D1
ROF 5 7 .1
DOF 2 7 D1
D1CRS 2 8 D2
D2CRS 1 8 D2
CGS 2 3 5.5N
RD 4 1 0.5
DCOS 3 1 D3
RDS 1 3 5.0MEG
LS 3 30 .5N
LD 10 4 1N
LG 20 5 1N
.MODEL DMOS NMOS (LEVEL=3 VTO=3.0 KP=3.8)
.MODEL D1 D (IS=.5F CJO=1P BV=100 M=.5 VJ=.6 TT=1N)
.MODEL D2 D (IS=.5F CJO=400P BV=1000 M=.4 VJ=.6 TT=400N RS=10M)
.MODEL D3 D (IS=.5F CJO=900P BV=1000 M=.3 VJ=.4 TT=400N RS=10M)
.ENDS
```

Doc #9200-0247 Rev 1
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