



STD6N95K5, STF6N95K5 STP6N95K5, STW6N95K5

N-channel 950 V, 1 Ω , 5 A TO-220, TO-220FP, TO-247, DPAK
Zener-protected SuperMESH 5™ Power MOSFET

Preliminary data

Features

Type	V _{DSS}	R _{DS(on)} max	I _D	P _W
STD6N95K5	950 V	< 1.25 Ω	5 A	90 W
STF6N95K5				25 W
STP6N95K5				90 W
STW6N95K5				

- DPAK worldwide best R_{DS(on)}
- Worldwide best FOM (figure of merit)
- Ultra low gate charge
- 100% avalanche tested
- Zener-protected

Application

- Switching applications

Description

SuperMESH 5™ is a revolutionary avalanche-rugged very high voltage Power MOSFET technology based on an innovative proprietary vertical structure. The result is a drastic reduction in on-resistance and ultra low gate charge for applications which require superior power density and high efficiency.

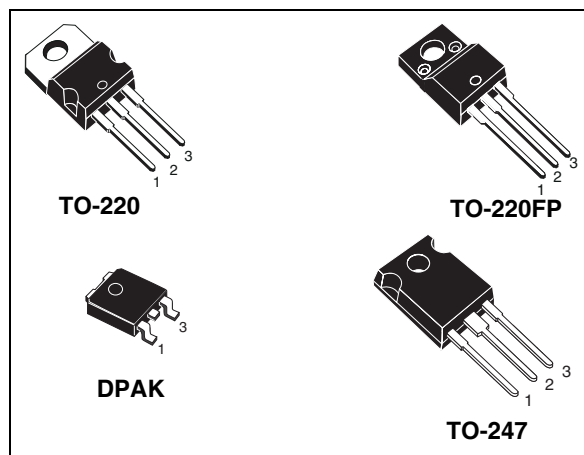
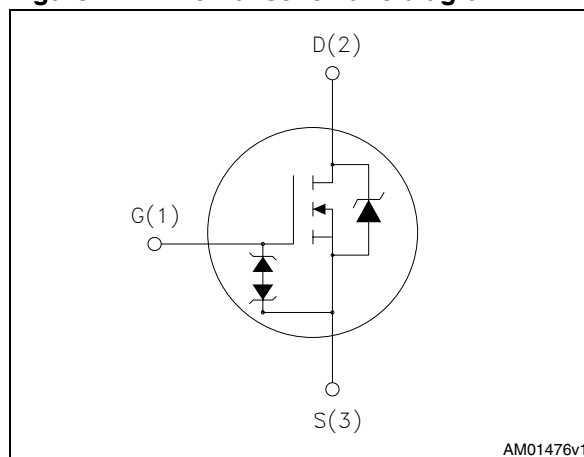


Figure 1. Internal schematic diagram



AM01476v1

Table 1. Device summary

Order codes	Marking	Package	Packaging
STD6N95K5	6N95K5	DPAK	Tape and reel
STF6N95K5		TO-220FP	Tube
STP6N95K5		TO-220	
STW6N95K5		TO-247	

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220, DPAK TO-247	TO-220FP	
V _{GS}	Gate- source voltage	± 30		V
I _D	Drain current (continuous) at T _C = 25 °C	5		A
I _D	Drain current (continuous) at T _C = 100 °C	3.1		A
I _{DM} ⁽¹⁾	Drain current (pulsed)	20		A
P _{TOT}	Total dissipation at T _C = 25 °C	90	25	W
I _{AR}	Max current during repetitive or single pulse avalanche (pulse width limited by T _{jmax})	TBD		A
E _{AS}	Single pulse avalanche energy (starting T _J = 25 °C, I _D =I _{AS} , V _{DD} = 50 V)	TBD		mJ
V _{ESD(G-S)}	Gate source ESD (HBM-C = 100 pF, R = 1.5 kΩ)	TBD		V
V _{iso}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1 s; T _C =25 °C)		2500	V
dv/dt ⁽²⁾	Peak diode recovery voltage slope	TBD		V/ns
T _j T _{stg}	Operating junction temperature Storage temperature	-55 to 150		°C

1. Pulse width limited by safe operating area.
2. I_{SD} ≤ 5 A, di/dt ≤ 100 A/μs, V_{Peak} ≤ V_{(BR)DSS}

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Table 3. Thermal data

Symbol	Parameter	Value				Unit
		TO-220	DPAK	TO-247	TO-220FP	
R _{thj-case}	Thermal resistance junction-case max	1.38			5	°C/W
R _{thj-amb}	Thermal resistance junction-amb max	62.5		50	62.5	°C/W
R _{thj-pcb} ⁽¹⁾	Thermal resistance junction-pcb max		50			°C/W
T _l	Maximum lead temperature for soldering purpose	300		300		°C

1. When mounted on 1inch² FR-4 board, 2 oz Cu

2 Electrical characteristics

($T_{CASE} = 25\text{ °C}$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0$	950			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{max rating}$, $V_{DS} = \text{Max rating}$, $T_c = 125\text{ °C}$			1 50	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{ V}$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 100\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$, $I_D = 2.5\text{ A}$		1	1.25	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance			450		pF
C_{oss}	Output capacitance	$V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$	-	30	-	pF
C_{rss}	Reverse transfer capacitance			1		
$C_{o(tr)}^{(1)}$	Equivalent capacitance time related	$V_{GS} = 0$, $V_{DS} = 0\text{ to }720\text{ V}$	-	TBD	-	pF
$C_{o(er)}^{(2)}$	Equivalent capacitance energy related			TBD		
R_G	Intrinsic gate resistance	$f = 1\text{ MHz}$ open drain	-	10.5	-	Ω
Q_g	Total gate charge	$V_{DD} = 760\text{ V}$, $I_D = 5\text{ A}$ $V_{GS} = 10\text{ V}$ (see Figure 3)	-	11	-	nC
Q_{gs}	Gate-source charge			TBD		
Q_{gd}	Gate-drain charge			TBD		

1. Time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}
2. energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 475 \text{ V}$, $I_D = 2.5 \text{ A}$, $R_G = 4.7 \text{ } \Omega$, $V_{GS} = 10 \text{ V}$ (see Figure 5)	-	TBD	-	ns
t_r	Rise time			TBD		ns
$t_{d(off)}$	Turn-off delay time			TBD		ns
t_f	Fall time			TBD		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		5	mA
I_{SDM}	Source-drain current (pulsed)				20	A
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 5 \text{ A}$, $V_{GS} = 0$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 5 \text{ A}$, $V_{DD} = 60 \text{ V}$ $di/dt = 100 \text{ A}/\mu\text{s}$, (see Figure 4)	-	TBD		ns
Q_{rr}	Reverse recovery charge			TBD		μC
I_{RRM}	Reverse recovery current			TBD		A
t_{rr}	Reverse recovery time	$I_{SD} = 5 \text{ A}$, $V_{DD} = 60 \text{ V}$ $di/dt = 100 \text{ A}/\mu\text{s}$, $T_j = 150 \text{ }^\circ\text{C}$ (see Figure 4)	-	TBD		ns
Q_{rr}	Reverse recovery charge			TBD		μC
I_{RRM}	Reverse recovery current			TBD		A

1. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min	Typ.	Max.	Unit
BV_{GSO}	Gate-source breakdown voltage	$I_{gs} \pm 1 \text{ mA}$, (open drain)	30	-		V

The built-in-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

3 Test circuits

Figure 2. Switching times test circuit for resistive load

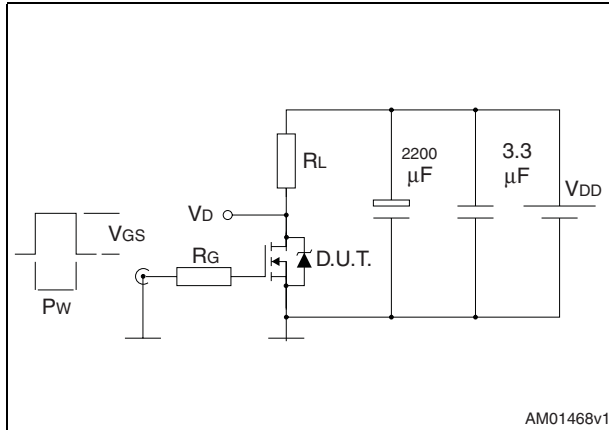


Figure 3. Gate charge test circuit

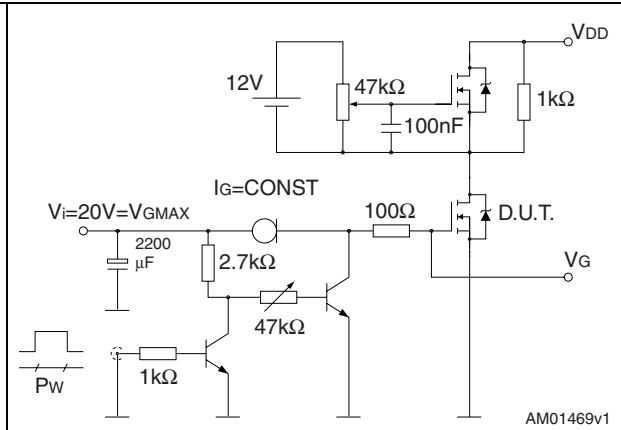


Figure 4. Test circuit for inductive load switching and diode recovery times

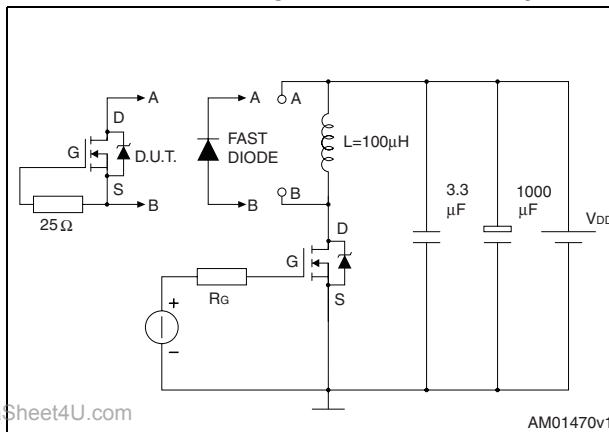


Figure 5. Unclamped inductive load test circuit

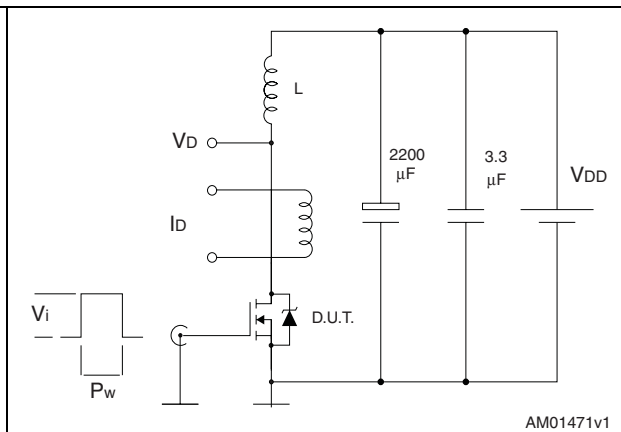


Figure 6. Unclamped inductive waveform

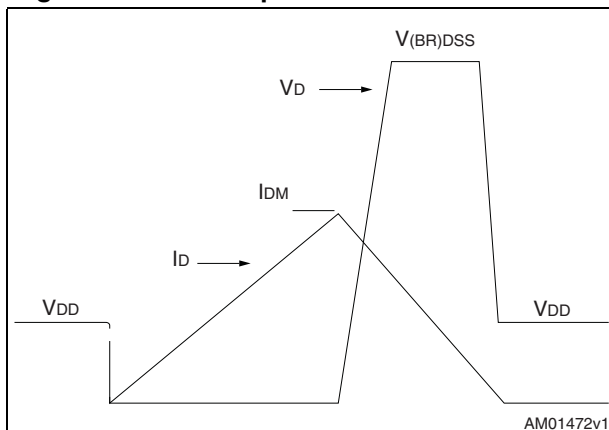
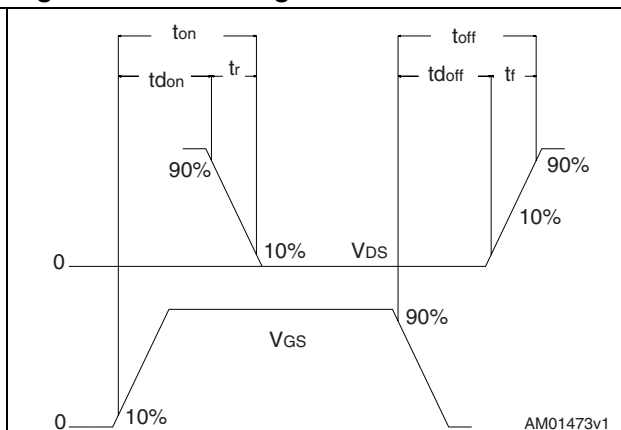


Figure 7. Switching time waveform



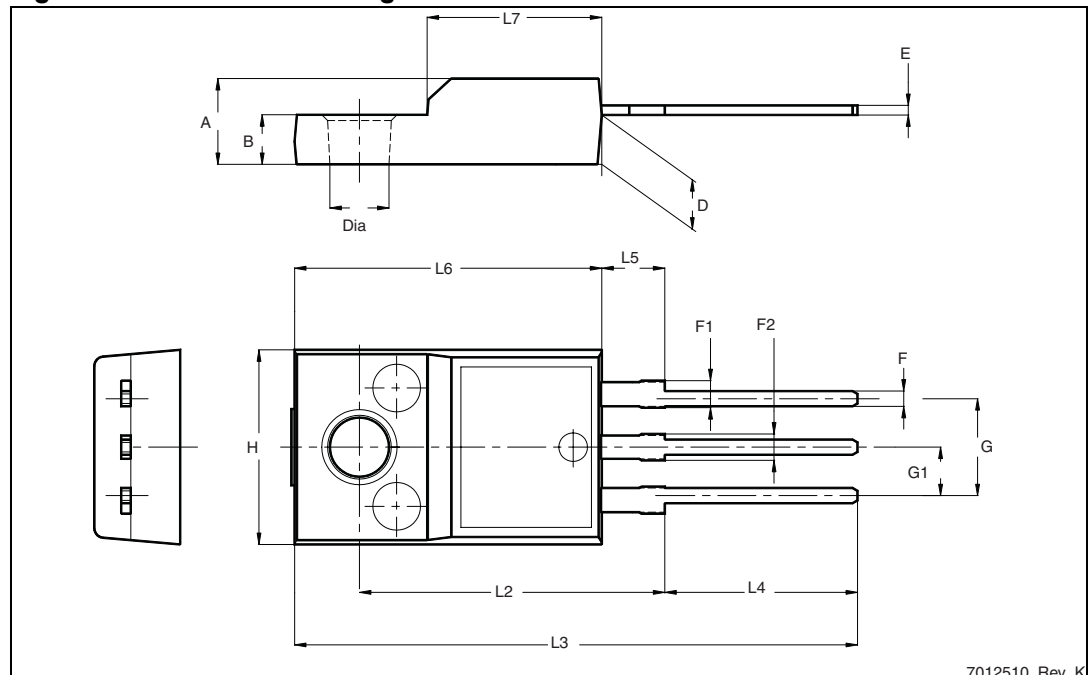
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

Table 9. TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

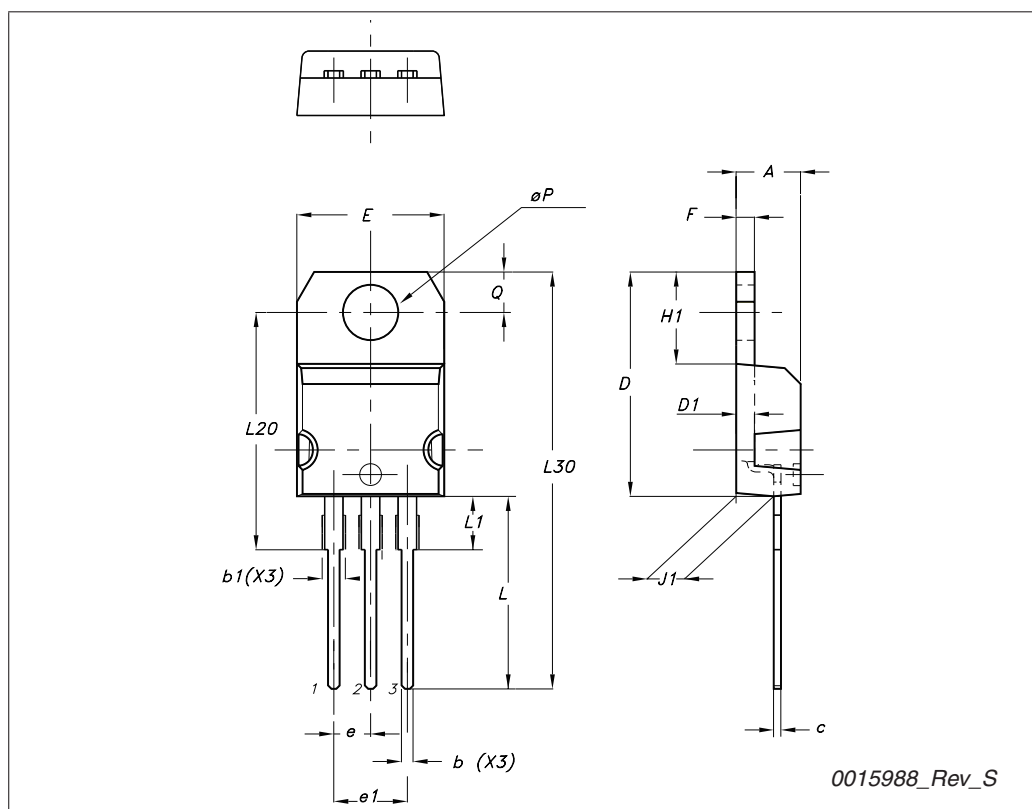
Figure 8. TO-220FP drawing



7012510 Rev K

TO-220 type A mechanical data

Dim	mm		
	Min	Typ	Max
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
∅P	3.75		3.85
Q	2.65		2.95

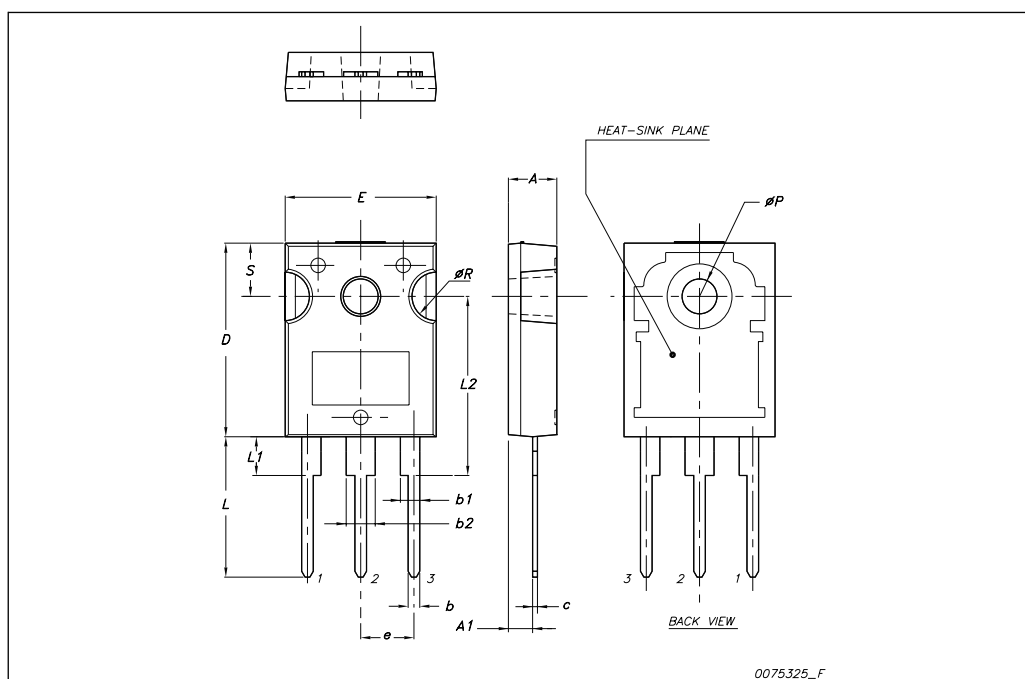


Package mechanical data

STD/F/P/W6N95K5

TO-247 mechanical data

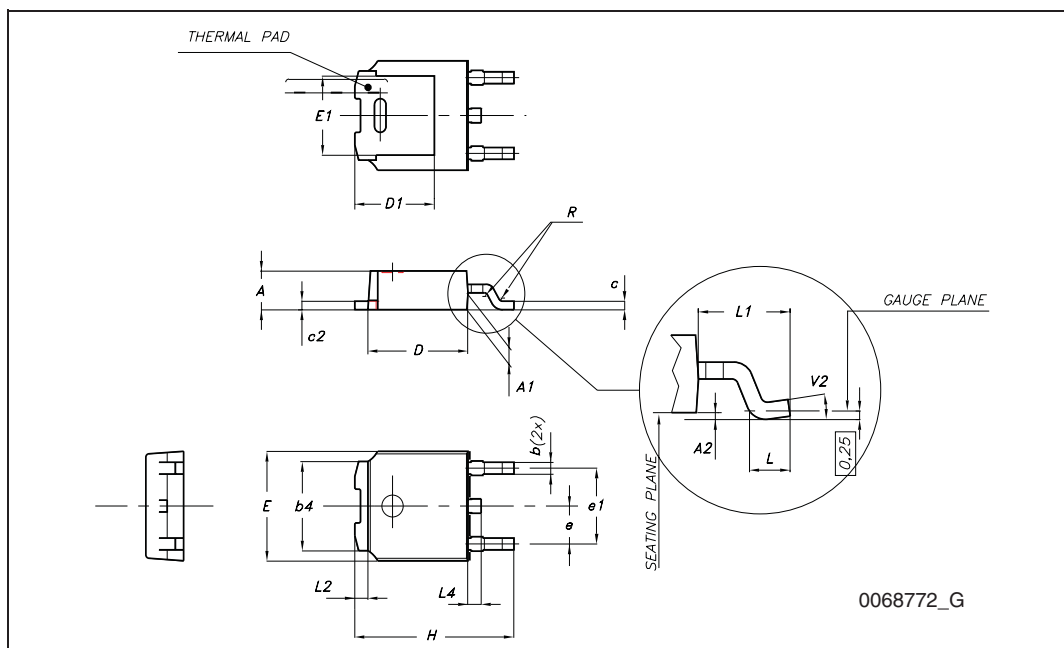
Dim.	mm.		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e		5.45	
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
øP	3.55		3.65
øR	4.50		5.50
S		5.50	



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TO-252 (DPAK) mechanical data

DIM.	mm.		
	min.	typ	max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1		
L1		2.80	
L2		0.80	
L4	0.60		1
R		0.20	
V2	0°		8°



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5 Revision history

Table 10. Document revision history

Date	Revision	Changes
12-Jan-2010	1	First release.

STD/F/P/W6N95K5

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