N-Channel 200-V (D-S) MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
200	0.130 @ V_{GS} = 10 V	4.1
	0.142 @ V_{GS} = 6.0 V	3.9

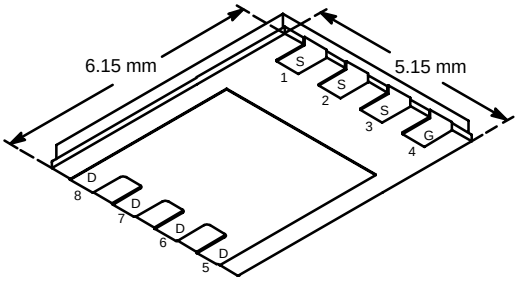
FEATURES

- TrenchFET® Power MOSFETS
- New Low Thermal Resistance PowerPAK™ Package with Low 1.07-mm Profile
- PWM Optimized For Fast Switching

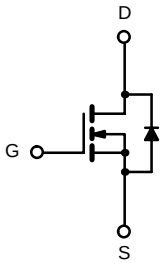
APPLICATIONS

- Primary Side Switch

PowerPAK™ SO-8



Bottom View
Ordering Information: Si7462DP-T1



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C UNLESS OTHERWISE NOTED)					
Parameter		Symbol	10 secs	Steady State	Unit
Drain-Source Voltage		V_{DS}	200		V
Gate-Source Voltage		V_{GS}	±20		
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	4.1	2.6	A
	T_A = 85°C		3.0	1.9	
Pulsed Drain Current		I_{DM}	12		
Avalanche Current	L = 0.1 mH	I_{AS}	6		
Single Avalanche Energy (Duty Cycle ≤ 1%)		E_{AS}	1.8		mJ
Continuous Source Current (Diode Conduction)[a]		I_S	4.0	1.6	A
Maximum Power Dissipation[a]	T_A = 25°C	P_D	4.8	1.9	W
	T_A = 85°C		2.6	1.0	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient[a]	t ≤ 10 sec	R_{thJA}	21	26	°C/W
	Steady State		55	65	
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	1.7	2.1	

Notes
a. Surface Mounted on 1" x 1" FR4 Board.

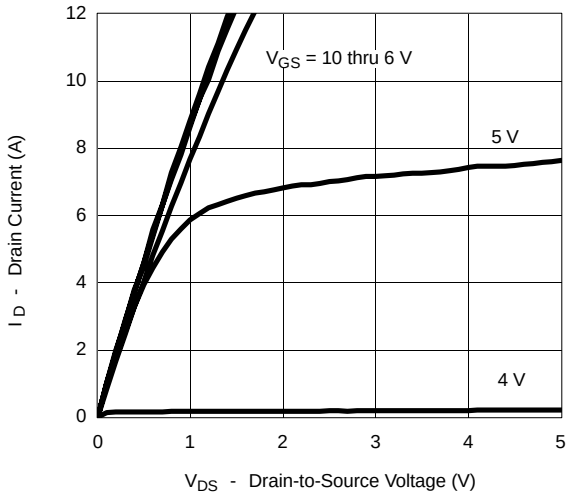
SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	2		4	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 160 V, V_{GS} = 0 V			1	μA
		V_{DS} = 160 V, V_{GS} = 0 V, T_J = 85°C			20	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} ≥ 5 V, V_{GS} = 10 V	12			A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 4.1 A		0.110	0.130	Ω
		V_{GS} = 6.0 V, I_D = 3.9 A		0.120	0.142	
Forward Transconductance[a]	g_{fs}	V_{DS} = 15 V, I_D = 4.1 A		13		S
Diode Forward Voltage[a]	V_{SD}	I_S = 4 A, V_{GS} = 0 V		0.8	1.2	V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = 100 V, V_{GS} = 10 V, I_D = 4.1 A		20	30	nC
Gate-Source Charge	Q_{gs}			4.5		
Gate-Drain Charge	Q_{gd}			6.5		
Gate Resistance	R_G			2		Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 100 V, R_L = 100 Ω I_D ≅ 1 A, V_{GEN} = 10 V, R_G = 6 Ω		15	25	ns
Rise Time	t_r			15	25	
Turn-Off Delay Time	$t_{d(off)}$			40	60	
Fall Time	t_f			20	30	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 4 A, di/dt = 100 A/μs		70	110	

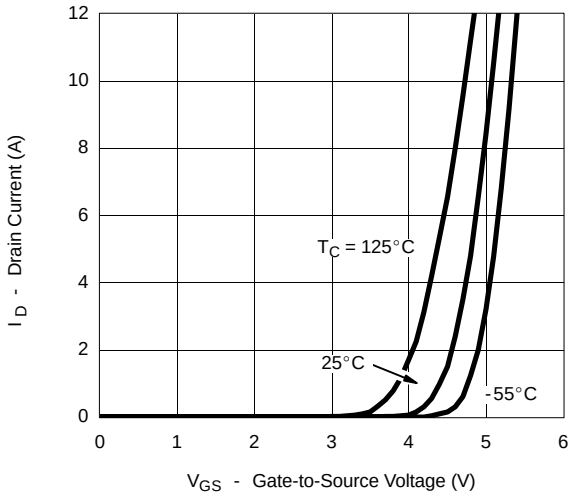
Notes
a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

Output Characteristics

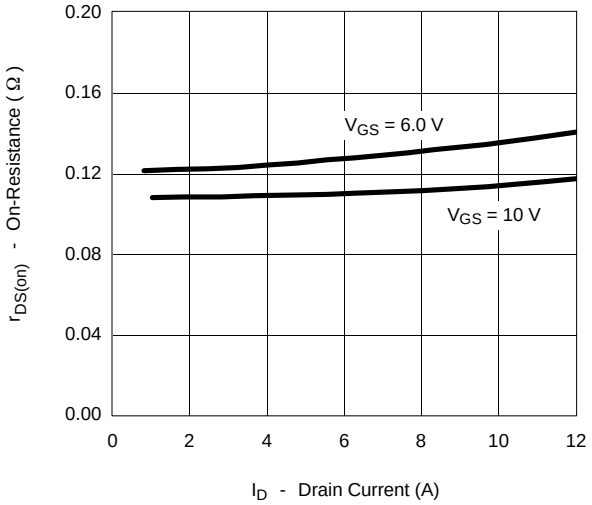


Transfer Characteristics

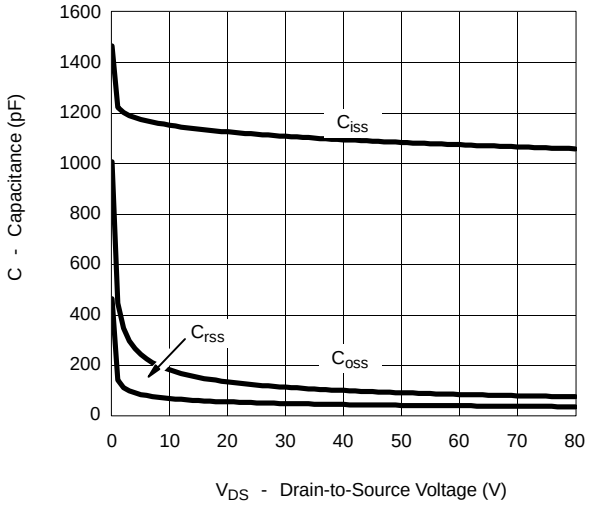


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

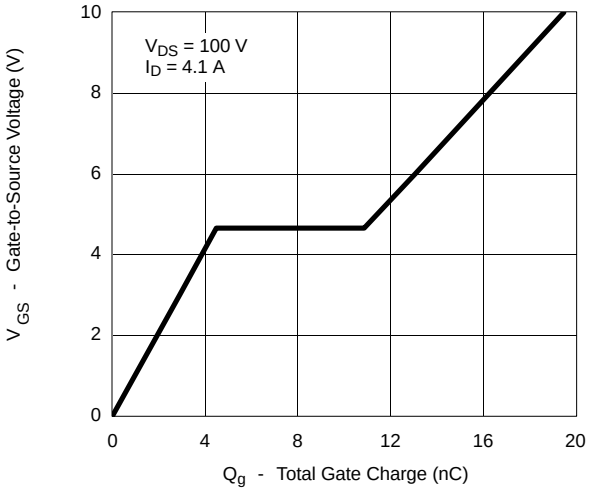
On-Resistance vs. Drain Current



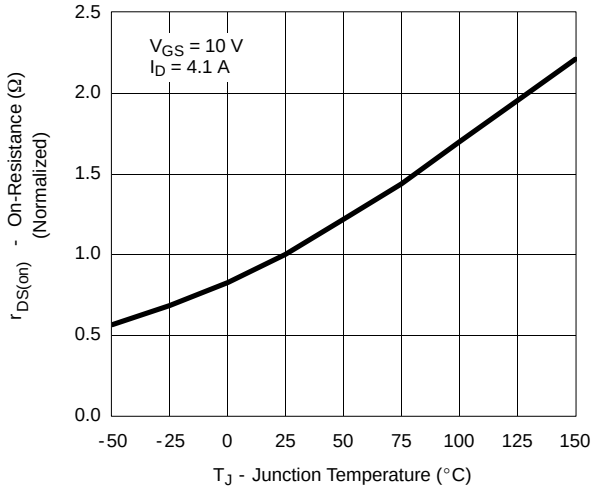
Capacitance



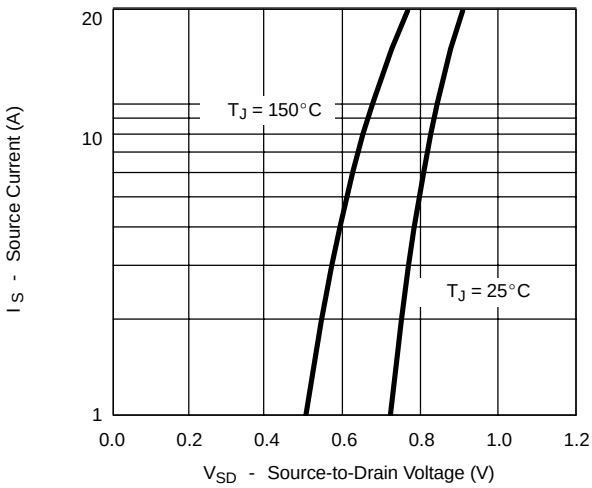
Gate Charge



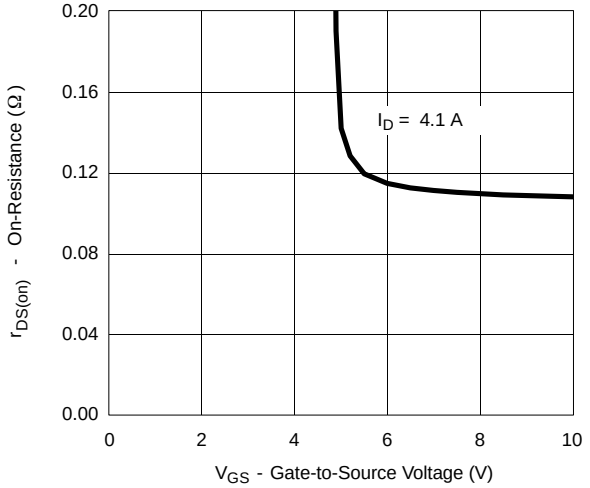
On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage

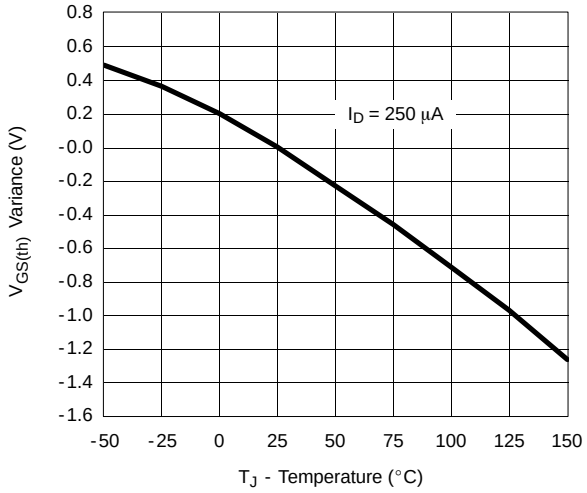


On-Resistance vs. Gate-to-Source Voltage

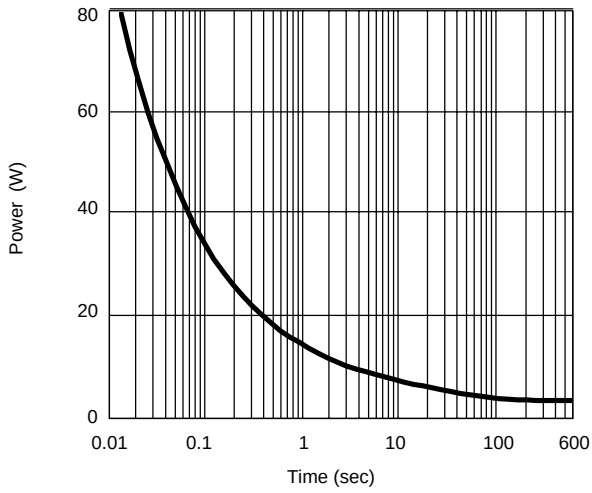


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

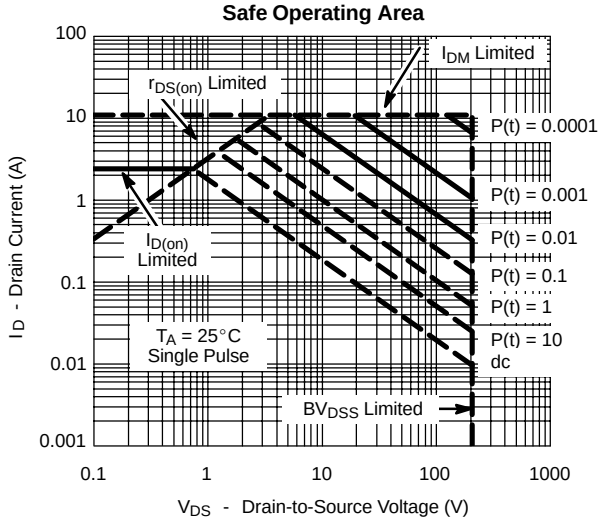
Threshold Voltage



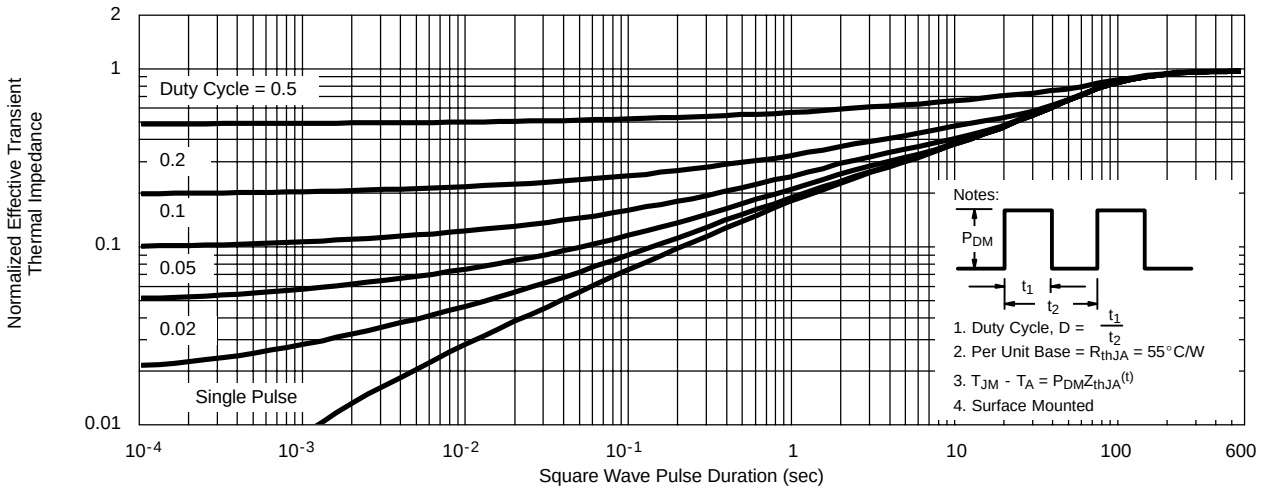
Single Pulse Power



Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient



TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

Normalized Thermal Transient Impedance, Junction-to-Case