FAIRCHILD SEMICONDUCTOR®

October 2007

UniFET™

# FDP20N50F / FDPF20N50FT

## N-Channel MOSFET, FRFET

### 500V, 20A, 0.26Ω

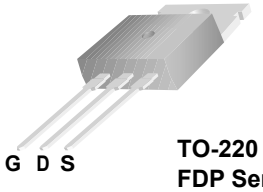
## Features

- $R_{DS(on)}$ = 0.22Ω ( Typ.)@ $V_{GS}$ = 10V, $I_D$ = 10A
- Low gate charge ( Typ. 50nC)
- Low $C_{rss}$ ( Typ. 27pF)
- Fast reverse recovery switching of built-in diode
- Fast switching
- 100% avalanche tested
- Improve dv/dt capability
- RoHS compliant

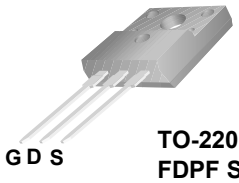
## Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

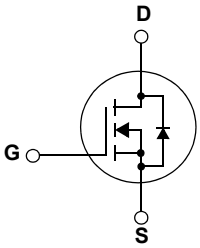
This advance technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficient switching mode power supplies and active power factor correction.




TO-220
FDP Series




TO-220F
FDPF Series




## MOSFET Maximum Ratings $T_C$ = 25°C unless otherwise noted

| Symbol | Parameter | | | FDP20N50F | FDPF20N50FT | Units |
|---|---|---|---|---|---|---|
| $V_{DSS}$ | Drain to Source Voltage | | | 500 | | V |
| $V_{GSS}$ | Gate to Source Voltage | | | ±30 | | V |
| $I_D$ | Drain Current | -Continuous ($T_C$ = 25°C) | | 20 | 20* | A |
| | | -Continuous ($T_C$ = 100°C) | | 12.9 | 12.9* | |
| $I_{DM}$ | Drain Current | - Pulsed | (Note 1) | 80 | 80* | A |
| $E_{AS}$ | Single Pulsed Avalanche Energy | | (Note 2) | 1110 | | mJ |
| $I_{AR}$ | Avalanche Current | | (Note 1) | 20 | | A |
| $E_{AR}$ | Repetitive Avalanche Energy | | (Note 1) | 25 | | mJ |
| dv/dt | Peak Diode Recovery dv/dt | | (Note 3) | 4.5 | | V/ns |
| $P_D$ | Power Dissipation | ($T_C$ = 25°C) | | 250 | 38.5 | W |
| | | - Derate above 25°C | | 2.0 | 0.3 | W/°C |
| $T_J$, $T_{STG}$ | Operating and Storage Temperature Range | | | -55 to +150 | | °C |
| $T_L$ | Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds | | | 300 | | °C |

*Drain current limited by maximum junction temperature

## Thermal Characteristics

| Symbol | Parameter | FDP20N50F | FDPF20N50FT | Units |
|---|---|---|---|---|
| $R_{\theta JC}$ | Thermal Resistance, Junction to Case | 0.5 | 3.3 | °C/W |
| $R_{\theta CS}$ | Thermal Resistance, Case to Sink Typ. | 0.5 | - | |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient | 62.5 | 62.5 | |

## Package Marking and Ordering Information $T_C = 25^oC$ unless otherwise noted

| Device Marking | Device | Package | Reel Size | Tape Width | Quantity |
|---|---|---|---|---|---|
| FDP20N50F | FDP20N50F | TO-220 | - | - | 50 |
| FDPF20N50FT | FDPF20N50FT | TO-220F | - | - | 50 |

## Electrical Characteristics

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | |
| $BV_{DSS}$ | Drain to Source Breakdown Voltage | $I_D$ = 250μA, $V_{GS}$ = 0V, $T_J$ = 25°C | 500 | - | - | V |
| $\Delta BV_{DSS}$ / $\Delta T_J$ | Breakdown Voltage Temperature Coefficient | $I_D$ = 250μA, Referenced to 25°C | - | 0.7 | - | V/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 500V, $V_{GS}$ = 0V | - | - | 10 | μA |
| | | $V_{DS}$ = 400V, $T_C$ = 125°C | - | - | 100 | |
| $I_{GSS}$ | Gate to Body Leakage Current | $V_{GS}$ = ±30V, $V_{DS}$ = 0V | - | - | ±100 | nA |
| **On Characteristics** | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{GS}$ = $V_{DS}$, $I_D$ = 250μA | 3.0 | - | 5.0 | V |
| $R_{DS(on)}$ | Static Drain to Source On Resistance | $V_{GS}$ = 10V, $I_D$ = 10A | - | 0.22 | 0.26 | Ω |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = 20V, $I_D$ = 10A (Note 4) | - | 25 | - | S |
| **Dynamic Characteristics** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 25V, $V_{GS}$ = 0V, f = 1MHz | - | 2550 | 3390 | pF |
| $C_{oss}$ | Output Capacitance | | - | 350 | 465 | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | - | 27 | 40 | pF |
| $Q_{g(tot)}$ | Total Gate Charge at 10V | $V_{DS}$ = 400V, $I_D$ = 20A, $V_{GS}$ = 10V (Note 4, 5) | - | 50 | 65 | nC |
| $Q_{gs}$ | Gate to Source Gate Charge | | - | 14 | - | nC |
| $Q_{gd}$ | Gate to Drain “Miller” Charge | | - | 20 | - | nC |
| **Switching Characteristics** | | | | | | |
| $t_{d(on)}$ | Turn-On Delay Time | $V_{DD}$ = 250V, $I_D$ = 20A, $R_G$ = 25Ω (Note 4, 5) | - | 45 | 100 | ns |
| $t_r$ | Turn-On Rise Time | | - | 120 | 250 | ns |
| $t_{d(off)}$ | Turn-Off Delay Time | | - | 100 | 210 | ns |
| $t_f$ | Turn-Off Fall Time | | - | 60 | 130 | ns |
| **Drain-Source Diode Characteristics** | | | | | | |
| $I_S$ | Maximum Continuous Drain to Source Diode Forward Current | | - | - | 20 | A |
| $I_{SM}$ | Maximum Pulsed Drain to Source Diode Forward Current | | - | - | 80 | A |
| $V_{SD}$ | Drain to Source Diode Forward Voltage | $V_{GS}$ = 0V, $I_{SD}$ = 20A | - | - | 1.5 | V |
| $t_{rr}$ | Reverse Recovery Time | $V_{GS}$ = 0V, $I_{SD}$ = 20A, $dI_F/dt$ = 100A/μs (Note 4) | - | 154 | - | ns |
| $Q_{rr}$ | Reverse Recovery Charge | | - | 0.5 | - | μC |

**Notes:**

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. L = 5mH, $I_{AS}$ = 20A, $V_{DD}$ = 50V, $R_G$ = 25Ω, Starting $T_J$ = 25°C
3. $I_{SD}$ ≤ 20A, di/dt ≤ 200A/μs, $V_{DD}$ ≤ $BV_{DSS}$, Starting $T_J$ = 25°C
4. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
5. Essentially Independent of Operating Temperature Typical Characteristics

## Typical Performance Characteristics

**Figure 1. On-Region Characteristics**

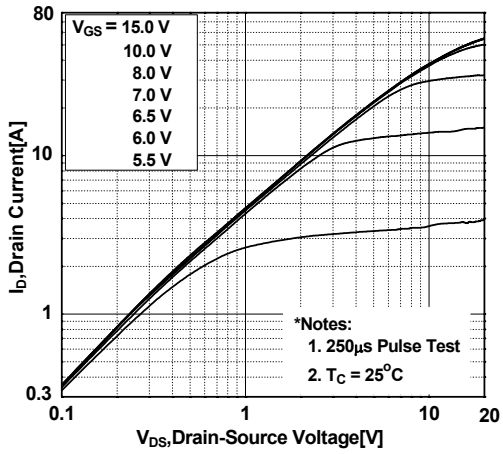



**Figure 2. Transfer Characteristics**

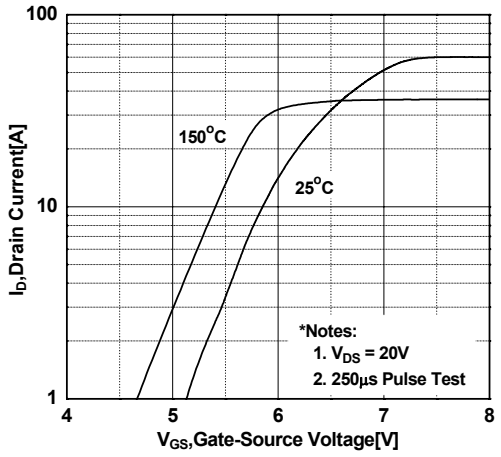



**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**

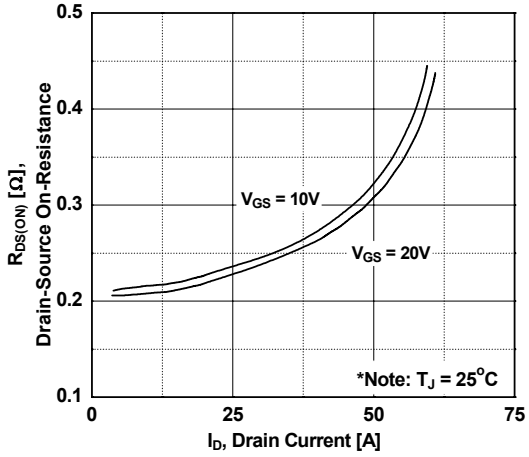



**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**

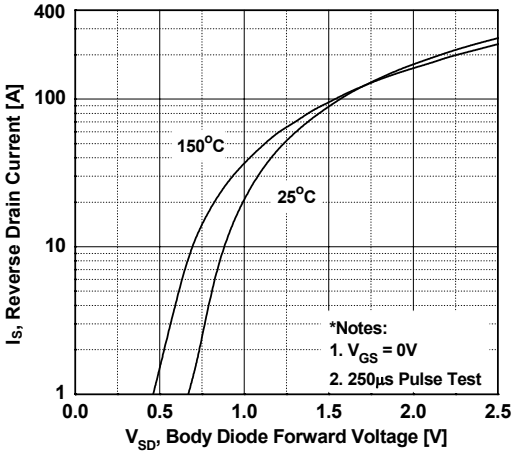



**Figure 5. Capacitance Characteristics**

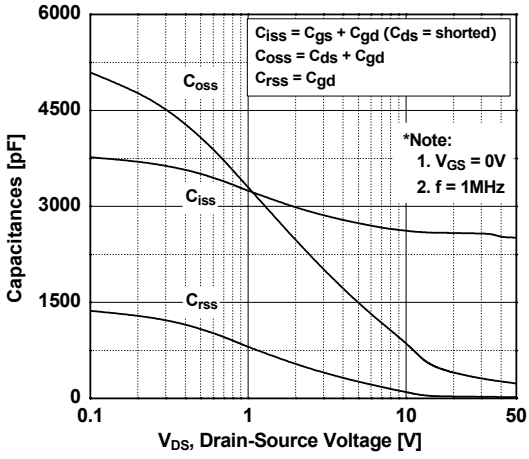
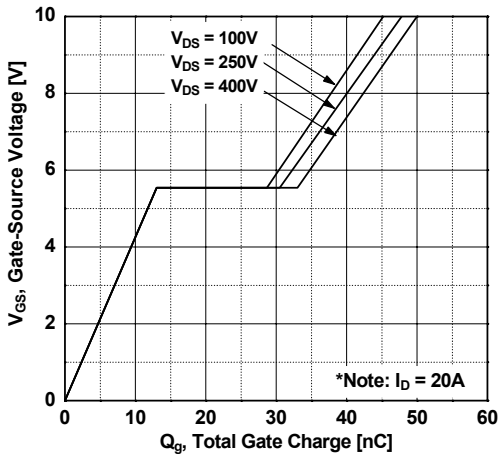



**Figure 6. Gate Charge Characteristics**



## Typical Performance Characteristics (Continued)

**Figure 7. Breakdown Voltage Variation vs. Temperature**

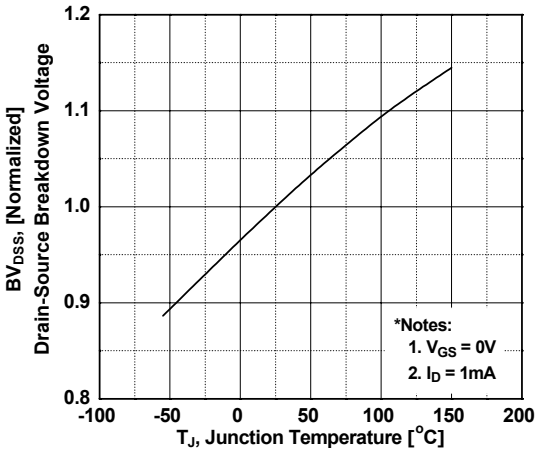



**Figure 8. Maximum Safe Operating Area - FDP20N50F**

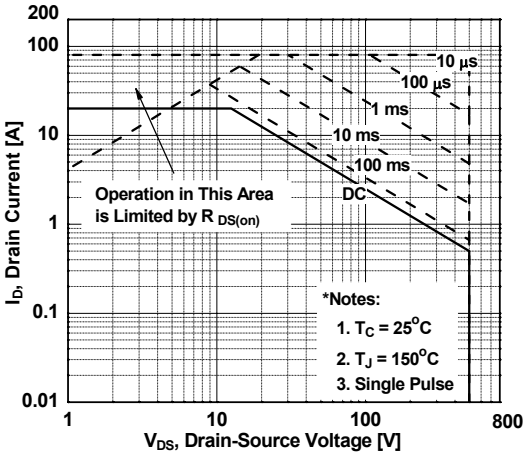



**Figure 9. Maximum Safe Operating Area - FDPF20N50FT**

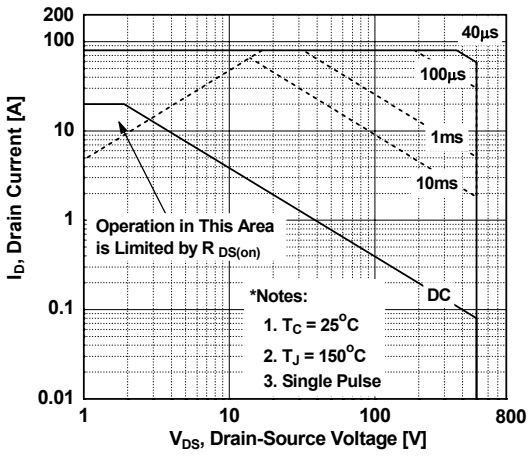



**Figure 10. Maximum Drain Current vs. Case Temperature**

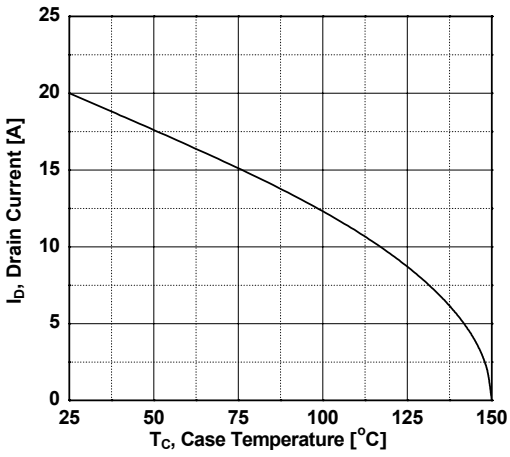
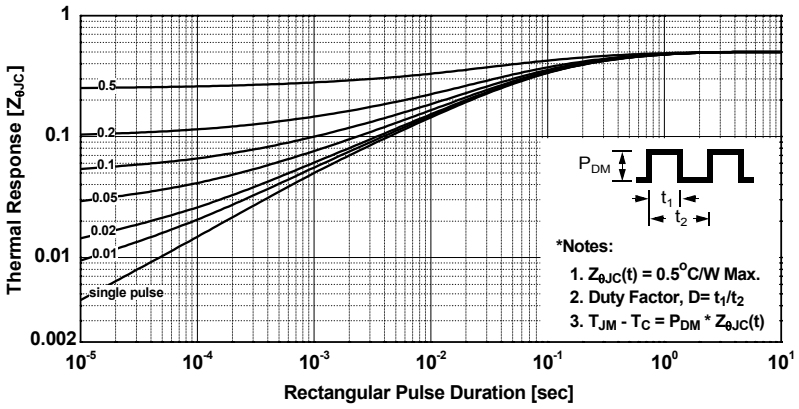
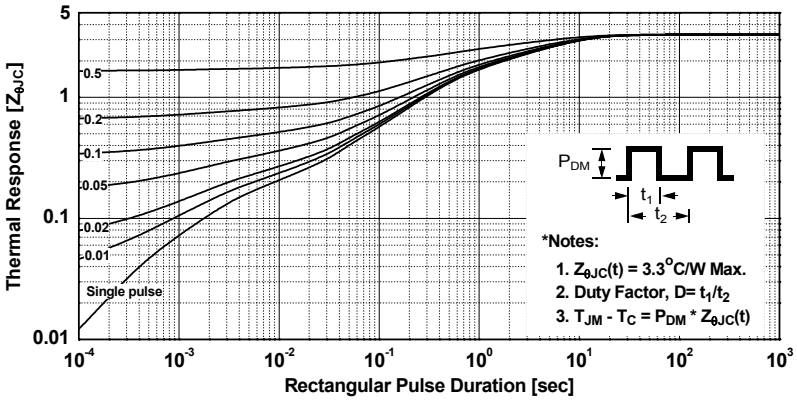



**Figure 11. Transient Thermal Response Curve - FDP20N50F**

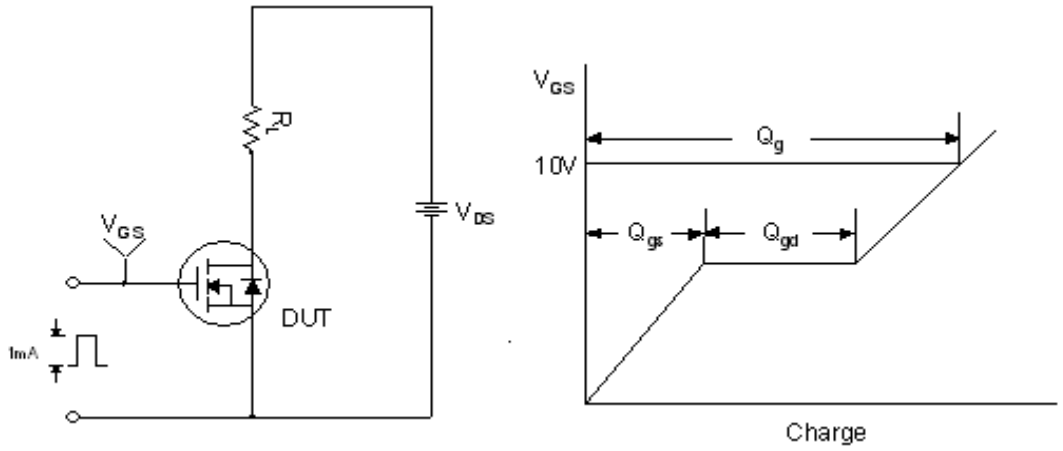


## Typical Performance Characteristics (Continued)

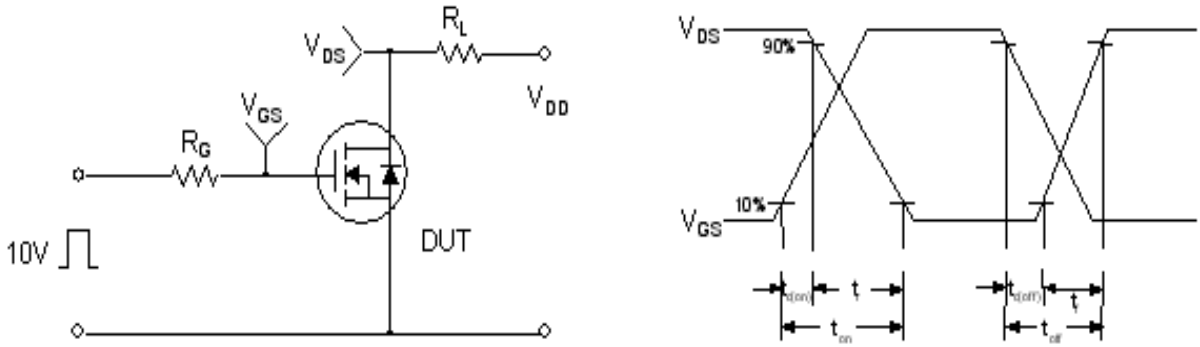
**Figure 12. Transient Thermal Response Curve - FDPF20N50FT**



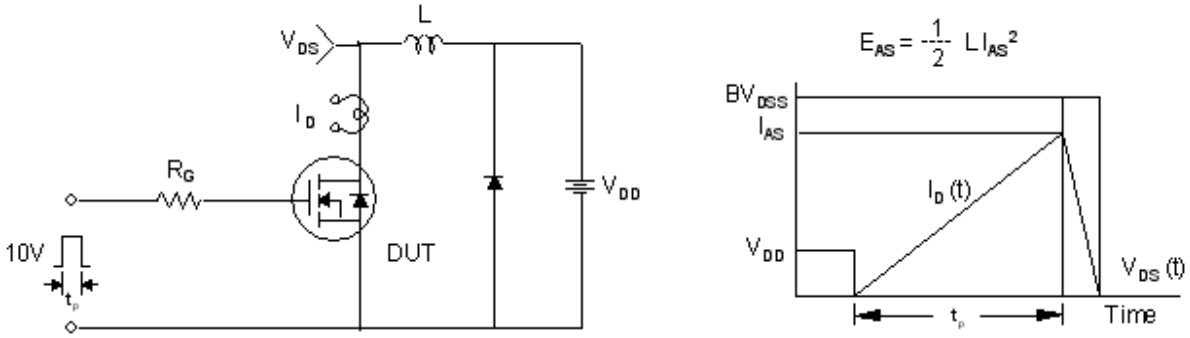
**Gate Charge Test Circuit & Waveform**



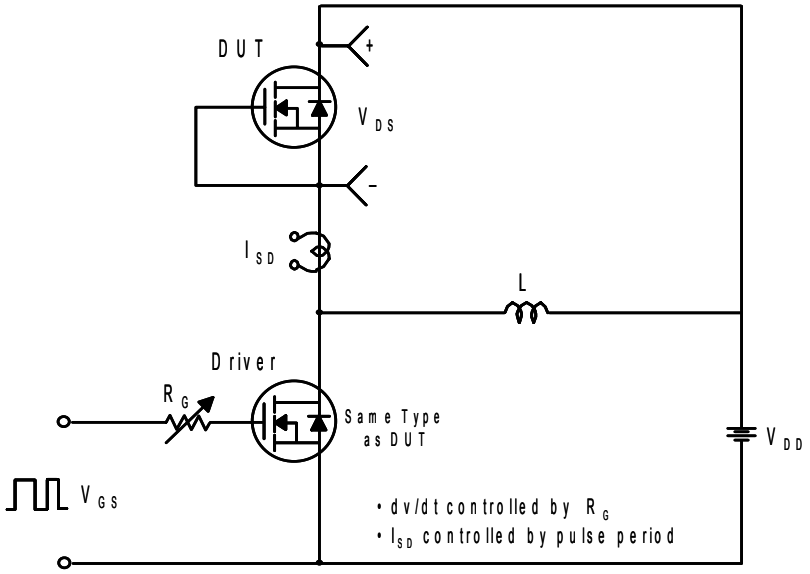

**Resistive Switching Test Circuit & Waveforms**

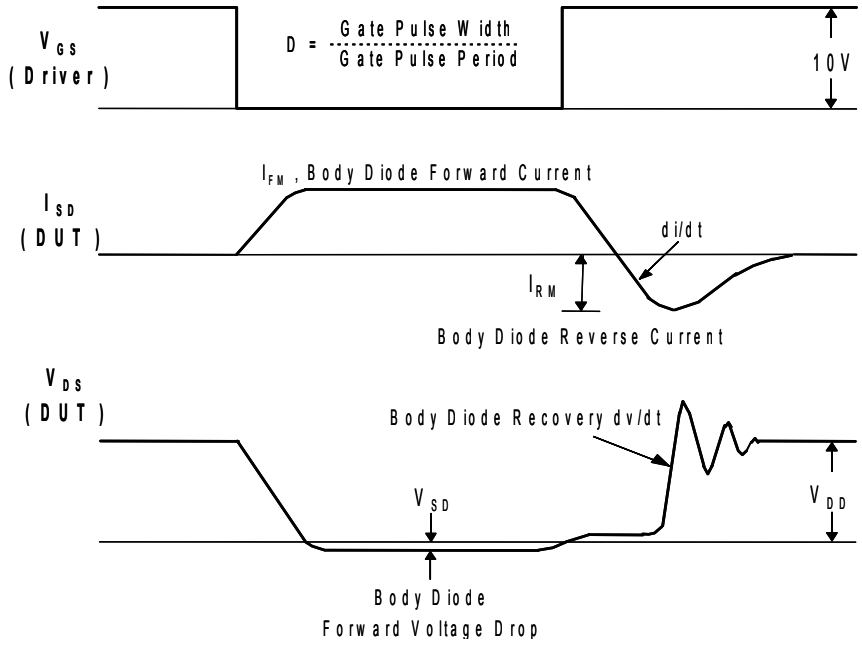



**Unclamped Inductive Switching Test Circuit & Waveforms**



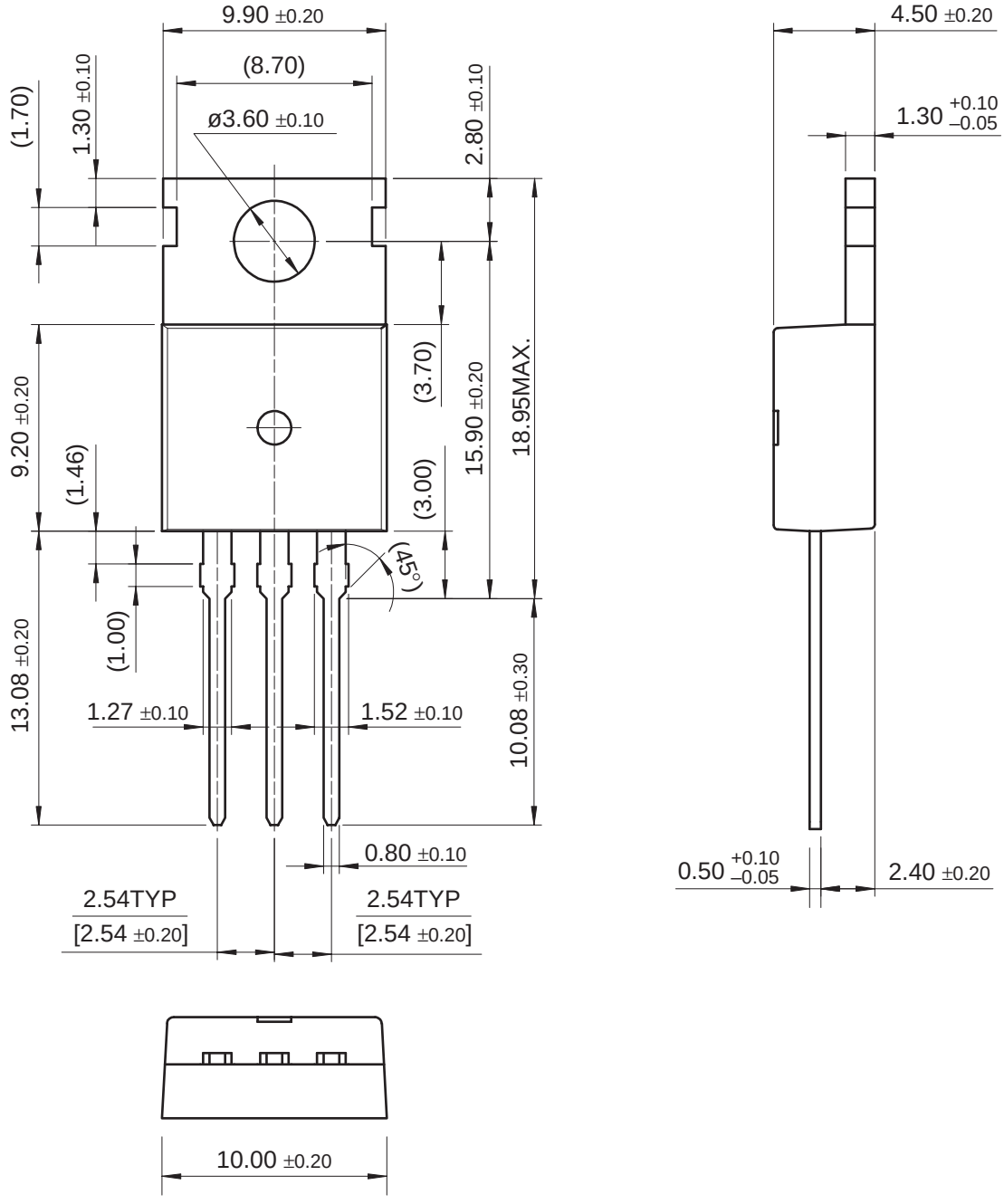
**Peak Diode Recovery dv/dt Test Circuit & Waveforms**



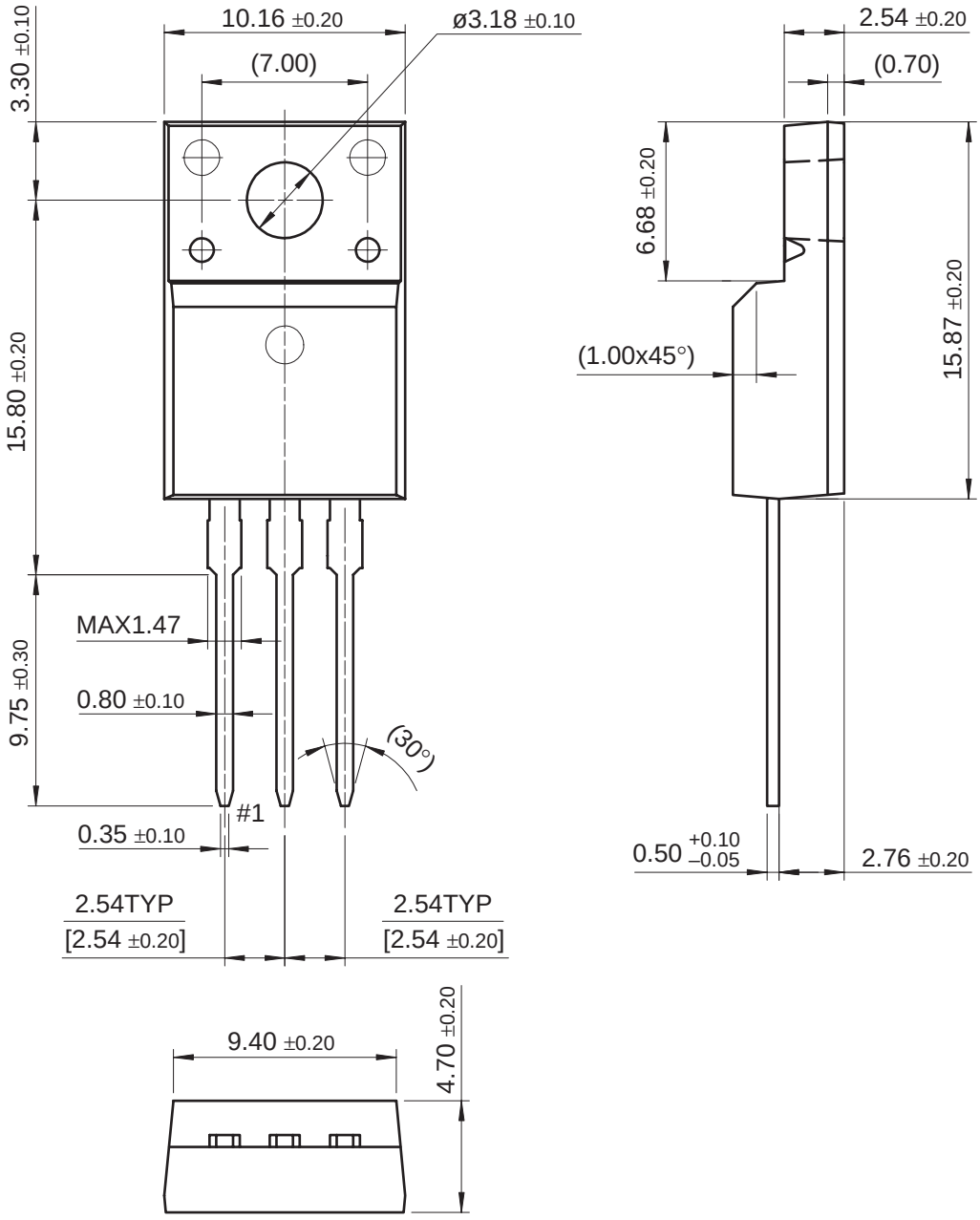
## Mechanical Dimensions

TO-220



## Mechanical Dimensions

TO-220F




Dimensions in Millimeters

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