



# STD8N65M5, STF8N65M5, STI8N65M5 STP8N65M5, STU8N65M5

N-channel 650 V, 0.56  $\Omega$ , 7 A MDmesh™ V Power MOSFET  
in I<sup>2</sup>PAK, TO-220, TO-220FP, DPAK and IPAK

Preliminary data

## Features

Type	V <sub>DSS</sub> @ T <sub>Jmax</sub>	R <sub>DS(on)</sub> max	I <sub>D</sub>
STD8N65M5	710 V	< 0.6 $\Omega$	7 A
STF8N65M5	710 V	< 0.6 $\Omega$	7 A <sup>(1)</sup>
STI8N65M5	710 V	< 0.6 $\Omega$	7 A
STP8N65M5	710 V	< 0.6 $\Omega$	7 A
STU8N65M5	710 V	< 0.6 $\Omega$	7 A

1. Limited only by maximum temperature allowed

- Worldwide best R<sub>DS(on)</sub> \* area
- Higher V<sub>DSS</sub> rating
- High dv/dt capability
- Excellent switching performance
- Easy to drive
- 100% avalanche tested

## Application

- Switching applications

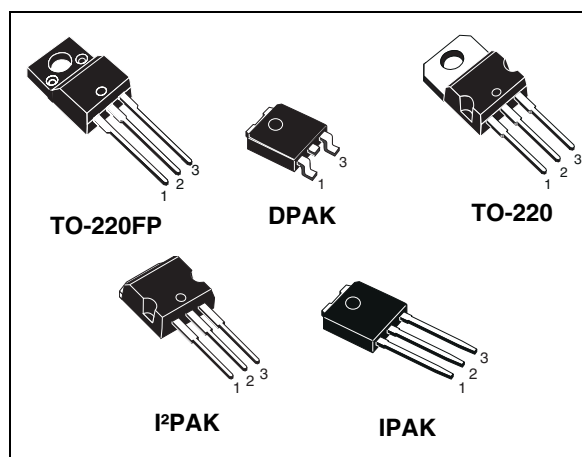
## Description

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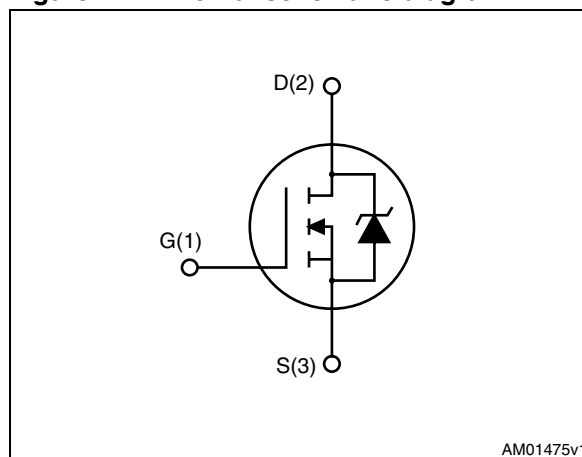
MDmesh™ V is a revolutionary Power MOSFET technology based on an innovative proprietary vertical process, which is combined with STMicroelectronics' well-known PowerMESH™ horizontal layout structure. The resulting product has extremely low on-resistance, which is unmatched among silicon-based Power MOSFETs, making it especially suitable for applications which require superior power density and outstanding efficiency.

**Table 1. Device summary**

Order codes	Marking	Package	Packaging
STD8N65M5	8N65M5	DPAK	Tape and reel
STF8N65M5	8N65M5	TO-220FP	Tube
STI8N65M5	8N65M5	I <sup>2</sup> PAK	Tube
STP8N65M5	8N65M5	TO-220	Tube
STU8N65M5	8N65M5	IPAK	Tube



**Figure 1. Internal schematic diagram**



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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value		Unit
		TO-220, IPAK DPAK, I <sup>2</sup> PAK	TO-220FP	
V <sub>GS</sub>	Gate- source voltage	± 25		V
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 25 °C	7	7 <sup>(1)</sup>	A
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 100 °C	4.4	4.4 <sup>(1)</sup>	A
I <sub>DM</sub> <sup>(2)</sup>	Drain current (pulsed)	28	28 <sup>(1)</sup>	A
P <sub>TOT</sub>	Total dissipation at T <sub>C</sub> = 25 °C	70	25	W
I <sub>AR</sub>	Max current during repetitive or single pulse avalanche (pulse width limited by T <sub>JMAX</sub> )	TBD		A
E <sub>AS</sub>	Single pulse avalanche energy (starting T <sub>j</sub> = 25°C, I <sub>D</sub> = I <sub>AR</sub> , V <sub>DD</sub> = 50V)	TBD		mJ
dv/dt <sup>(3)</sup>	Peak diode recovery voltage slope	TBD		V/ns
V <sub>ISO</sub>	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; T <sub>C</sub> = 25 °C)		2500	V
T <sub>stg</sub>	Storage temperature	-55 to 150		°C
T <sub>j</sub>	Max. operating junction temperature	150		°C

- Limited only by maximum temperature allowed
- Pulse width limited by safe operating area
- $I_{SD} \leq 33 \text{ A}$ ,  $di/dt \leq 400 \text{ A}/\mu\text{s}$ ,  $V_{Peak} < V_{(BR)DSS}$

**Table 3. Thermal data**

Symbol	Parameter	Value					Unit
		DPAK	IPAK	TO-220	I <sup>2</sup> PAK	TO-220FP	
R <sub>thj-case</sub>	Thermal resistance junction-case max	1.79			5	°C/W	
R <sub>thj-amb</sub>	Thermal resistance junction-ambient max		100	62.5		°C/W	
R <sub>thj-pcb</sub>	Thermal resistance junction-pcb max	50				°C/W	
T <sub>l</sub>	Maximum lead temperature for soldering purpose	300					°C

## 2 Electrical characteristics

( $T_C = 25\text{ }^\circ\text{C}$  unless otherwise specified)

**Table 4. On /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$ , $V_{GS} = 0$	650			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max rating}$ $V_{DS} = \text{Max rating}$ , $T_C = 125\text{ }^\circ\text{C}$			1 100	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate-body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 25\text{ V}$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$ , $I_D = 3.5\text{ A}$		0.56	0.6	$\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$ $C_{oss}$ $C_{rss}$	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 100\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0$	-	TBD TBD TBD	-	pF pF pF
$C_{o(er)}^{(1)}$	Equivalent output capacitance energy related	$V_{GS} = 0$ , $V_{DS} = 0\text{ to }520\text{ V}$	-	TBD	-	pF
$C_{o(tr)}^{(2)}$	Equivalent output capacitance time related	$V_{GS} = 0$ , $V_{DS} = 0\text{ to }520\text{ V}$	-	TBD	-	pF
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz}$ open drain	-	TBD	-	$\Omega$
$Q_g$ $Q_{gs}$ $Q_{gd}$	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 520\text{ V}$ , $I_D = 3.5\text{ A}$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 3</a> )	-	190 TBD TBD	-	nC nC nC

- $C_{o(er)}^{(1)}$  is a constant capacitance value that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$
- $C_{o(tr)}^{(2)}$  is a constant capacitance value that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-off delay time	$V_{DD} = 400\text{ V}$ , $I_D = 4\text{ A}$ , $R_G = 4.7\ \Omega$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 4</a> ) (see <a href="#">Figure 7</a> )		TBD		ns
$t_r$	Rise time		-	TBD	-	ns
$t_c$	Cross time		TBD			ns
$t_f$	Fall time		TBD			ns

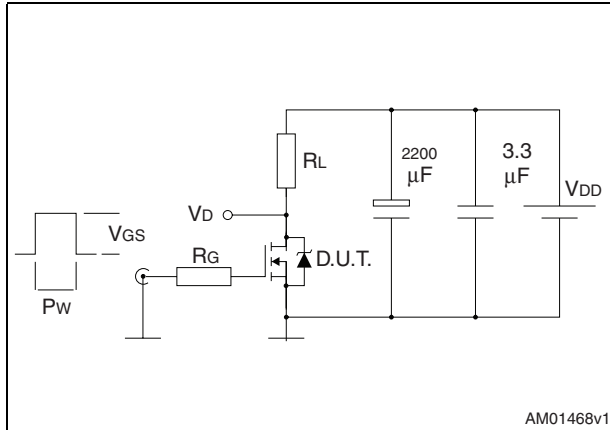
Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		7	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				28	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 7\text{ A}$ , $V_{GS} = 0$	-		1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 7\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 100\text{ V}$ (see <a href="#">Figure 4</a> )	-	TBD		ns
$Q_{rr}$	Reverse recovery charge			TBD		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current			TBD		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 7\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 100\text{ V}$ , $T_j = 150\text{ }^\circ\text{C}$ (see <a href="#">Figure 4</a> )	-	TBD		ns
$Q_{rr}$	Reverse recovery charge			TBD		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current			TBD		A

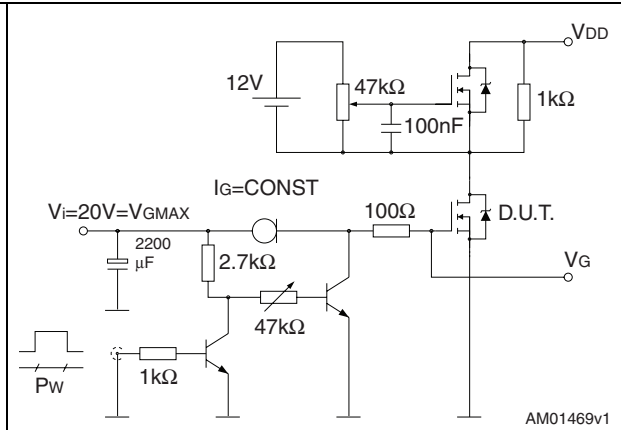
1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

### 3 Test circuits

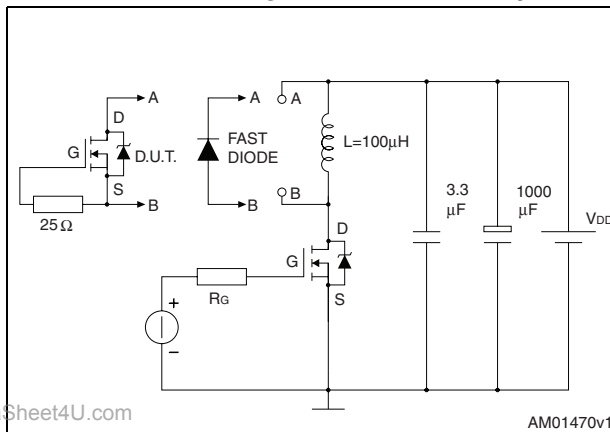
**Figure 2. Switching times test circuit for resistive load**



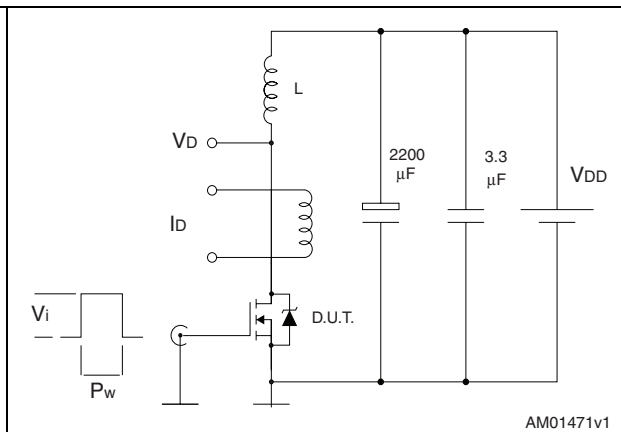
**Figure 3. Gate charge test circuit**



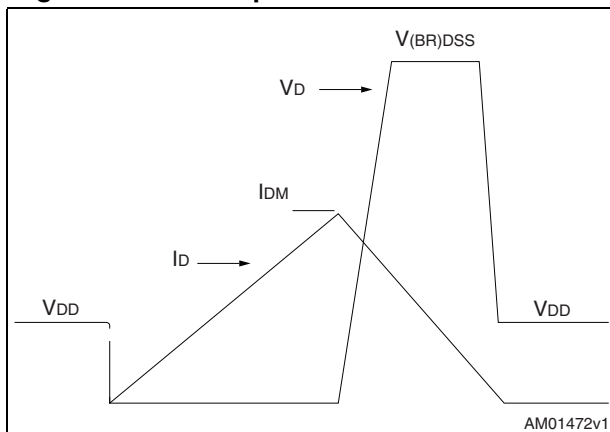
**Figure 4. Test circuit for inductive load switching and diode recovery times**



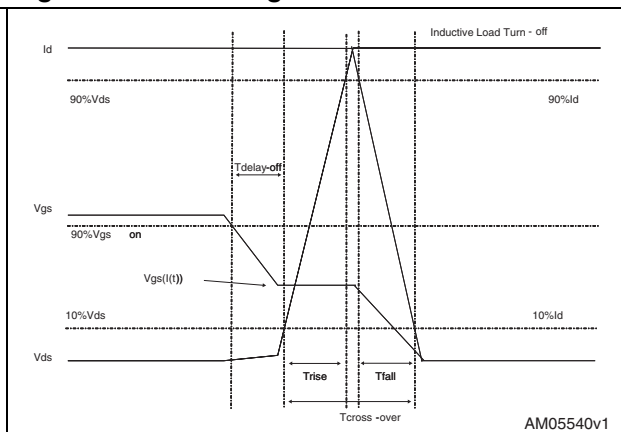
**Figure 5. Unclamped inductive load test circuit**



**Figure 6. Unclamped inductive waveform**



**Figure 7. Switching time waveform**



## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

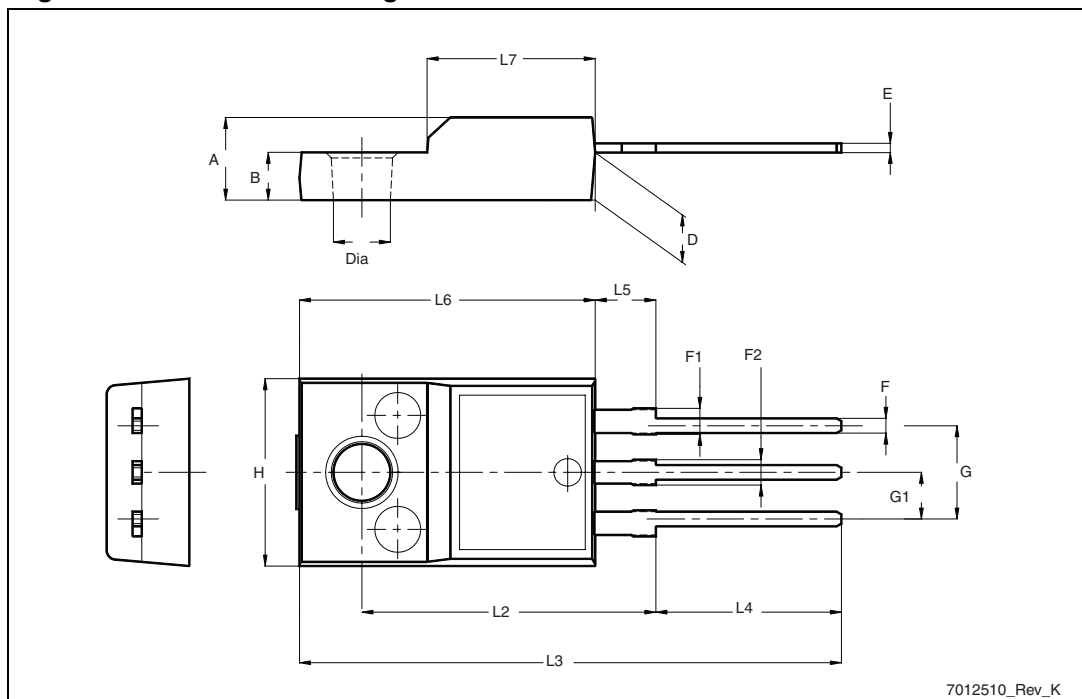
## Package mechanical data

STD/F//P/U8N65M5

Table 8. TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

Figure 8. TO-220FP drawing mechanical data

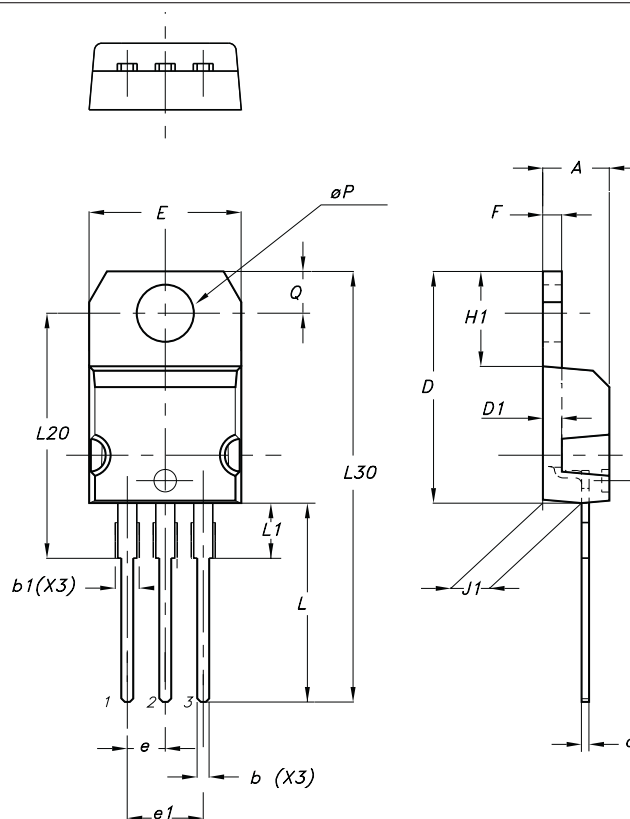


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## TO-220 type A mechanical data

Dim	mm		
	Min	Typ	Max
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
∅P	3.75		3.85
Q	2.65		2.95



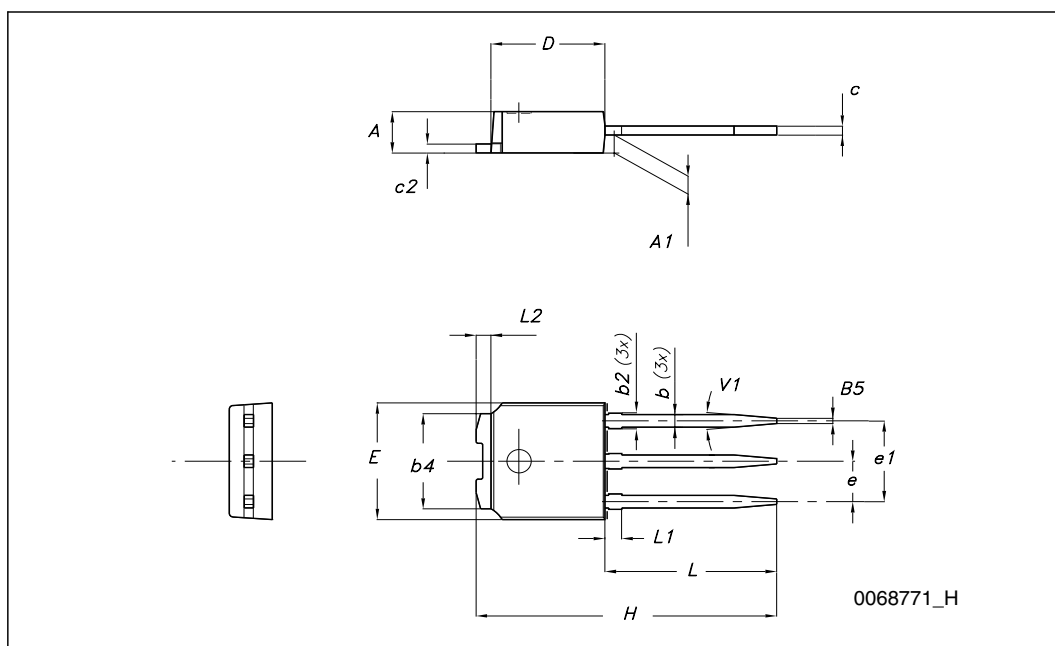
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## Package mechanical data

STD/F//P/U8N65M5

## TO-251 (IPAK) mechanical data

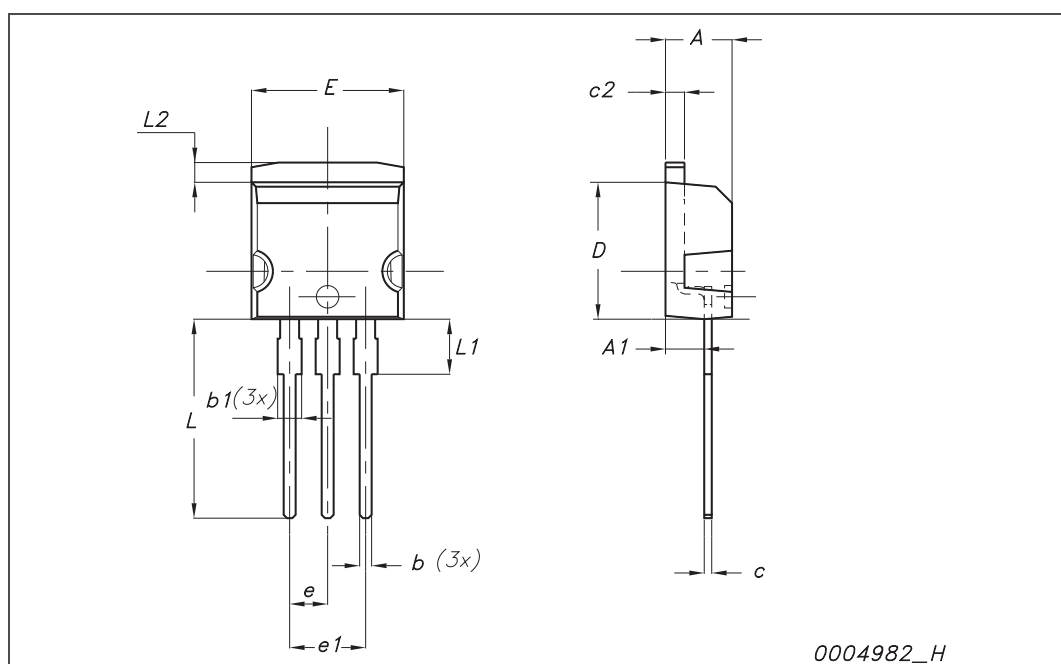
DIM.	mm.		
	min.	typ	max.
A	2.20		2.40
A1	0.90		1.10
b	0.64		0.90
b2			0.95
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
E	6.40		6.60
e		2.28	
e1	4.40		4.60
H		16.10	
L	9.00		9.40
(L1)	0.80		1.20
L2		0.80	
V1		10°	



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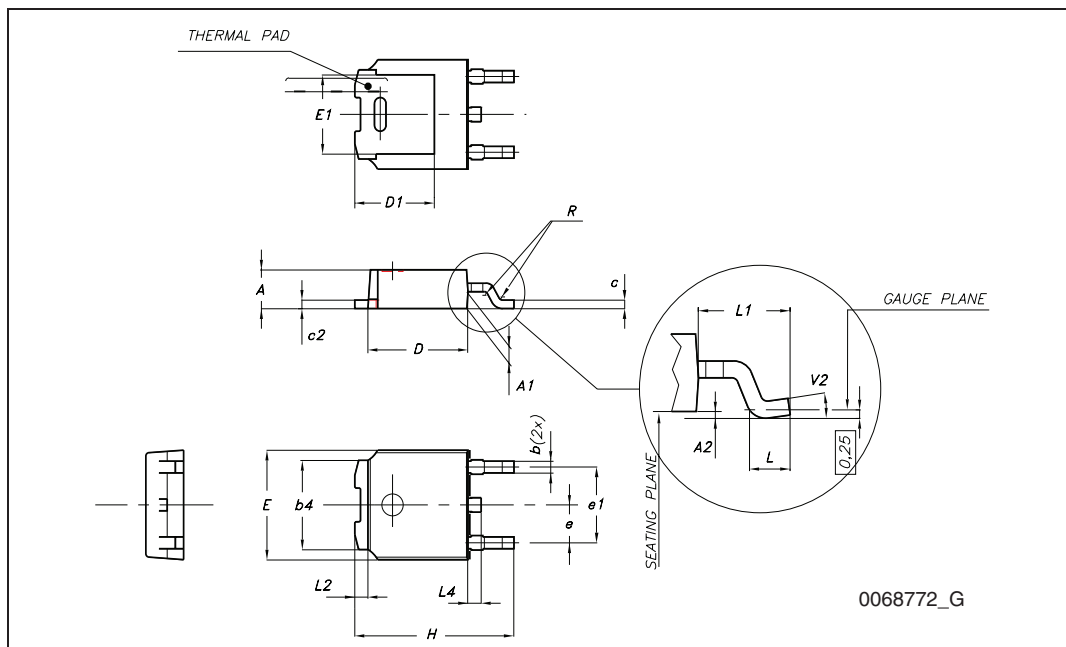
I<sup>2</sup>PAK (TO-262) mechanical data

Dim	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A	4.40		4.60	0.173		0.181
A1	2.40		2.72	0.094		0.107
b	0.61		0.88	0.024		0.034
b1	1.14		1.70	0.044		0.066
c	0.49		0.70	0.019		0.027
c2	1.23		1.32	0.048		0.052
D	8.95		9.35	0.352		0.368
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
E	10		10.40	0.393		0.410
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L2	1.27		1.40	0.050		0.055



TO-252 (DPAK) mechanical data

DIM.	mm.		
	min.	typ	max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1		
L1		2.80	
L2		0.80	
L4	0.60		1
R		0.20	
V2	0°		8°

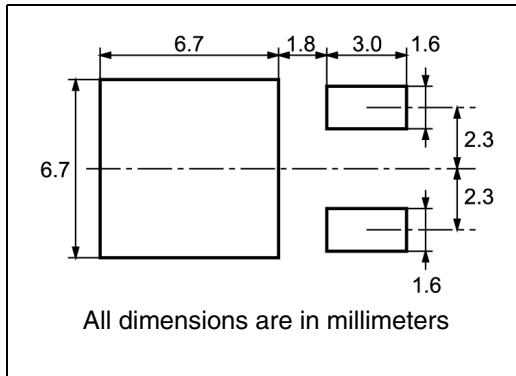


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# 5 Packaging mechanical data

## DPAK FOOTPRINT



## TAPE AND REEL SHIPMENT

40 mm min. Access hole at slot location

Full radius

Tape slot in core for tape start 2.5mm min. width

G measured at hub

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	16.4	18.4	0.645	0.724
N	50		1.968	
T		22.4		0.881

BASE QTY	BULK QTY
2500	2500

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	6.8	7	0.267	0.275
B0	10.4	10.6	0.409	0.417
B1		12.1		0.476
D	1.5	1.6	0.059	0.063
D1	1.5		0.059	
E	1.65	1.85	0.065	0.073
F	7.4	7.6	0.291	0.299
K0	2.55	2.75	0.100	0.108
P0	3.9	4.1	0.153	0.161
P1	7.9	8.1	0.311	0.319
P2	1.9	2.1	0.075	0.082
R	40		1.574	
W	15.7	16.3	0.618	0.641

TOP COVER TAPE

10 pitches cumulative tolerance on tape +/- 0.2 mm

User Direction of Feed

Center line of cavity

For machine ref. only including draft and radii concentric around B0

TRL

FEED DIRECTION

Bending radius R min.

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## 6 Revision history

**Table 9. Document revision history**

Date	Revision	Changes
23-Oct-2009	1	First release

**STD/F//P/U8N65M5**

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