19-5867; Rev 0; 6/11

EVALUATION KIT AVAILABLE

MAX7049

High-Performance, 288MHz to 945MHz ASK/FSK ISM Transmitter

General Description

The MAX7049 high-performance, single-chip, ultra-low-power ASK/FSK UHF transmitter operates in the industrial, scientific, medical (ISM) band at 288MHz to 945MHz carrier frequencies. The IC also includes a low phase noise fractional-N synthesizer for precise tuning, fast frequency agility, and low out-of-band power. To support narrow-band applications, the IC has both amplitude-shaping and frequency-shaping functions that enable the user to optimize spectral efficiency. The IC offers Tx power up to +15dBm. These features make the transmitter ideally suited for long-range applications.

Additional system-level features of the IC include a digital temperature sensor and a number of flexible GPOs for monitoring radio status and for the control of external functions. A complete transmitter system can be built using a low-end microprocessor control unit (MCU), the IC, a crystal, and a small number of passive components.

The IC is available in a small, 5mm x 5mm, 28-pin TQFN package with an exposed pad. It is specified to operate in the -40°C to +125°C automotive temperature range.

Applications

Automatic Meter Reading (AMR)

RF Modules

Long-Range, One-Way Remote Keyless Entry (RKE)

Wireless Sensor Networks

TPMS

Home Security

Home Automation

RFID

Remote Controls

Benefits and Features

- **Transmitter (Tx)**
  - **Provides Long Transmit Range Up to +15dBm**
  - **21mA Tx Current for +10dBm Tx Power***
  - **41mA Tx Current for +15dBm Tx Power***
  - **Modulation Shaping, ASK, FSK**
- **General**
  - **Delivers Long Battery Life**
    < 50nA Shutdown Current
    < 350nA Sleep Current
  - **Minimizes the Number of I/Os Required Between the IC and the MCU Serial Peripheral Interface (SPI™)**
  - **Regulatory Compliant**
    FCC Part 15 Frequency Hopping
    ETSI EN300-220 Compatible
  - **On-Chip Temperature Sensor**
  - **Fast Fractional-N Synthesizer with a User-Defined External Loop Filter**

**V_{DD} = 3.0V. Includes losses for the matching network and regulatory-compliant harmonic filter.*

***Ordering Information* appears at end of data sheet.**

*For related parts and recommended products to use with this part, refer to **www.maxim-ic.com/MAX7049.related**.*

SPI is a trademark of Motorola, Inc.

High-Performance, 288MHz to 945MHz ASK/FSK ISM Transmitter

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ABSOLUTE MAXIMUM RATINGS

PAVDD, LOVDD, VCOVDD, CPVDD, PLLVDD, XOVDD, DVDD, and AVDD to EP .....-0.3V to +3.6V
ENABLE, DATAIN, SDI, SDO, $\overline{CS}$, SCLK, GPO1, GPO2, HOP, and SHDN to EP . -0.3V to (V_{DD} + 0.3V)
All Other Pins to EP..... -0.3V to (V_{DD} + 0.3V)

Continuous Power Dissipation (T_A = +70°C)
TQFN (single-layer board)
(derate 21.3mW/°C above +70°C).....1702.1mW
Operating Temperature Range ..... -40°C to +125°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION! ESD SENSITIVE DEVICE

DC ELECTRICAL CHARACTERISTICS

(Figure 2, 50Ω system impedance, V_{DD} = +2.1V to +3.6V, f_{RF} = 868MHz, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DD} = +3.0V, T_A = +25°C, unless otherwise noted. All min and max values are 100% tested at T_A = +125°C and are guaranteed by design and characterization over temperature, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD}	PAVDD, LOVDD, VCOVDD, CPVDD, PLLVDD, XOVDD, DVDD, and AVDD connected to power supply		2.1	3.0	3.6	V
Operating Current	I_{DD}	PA off	f_{RF} = 315MHz		11.2		mA
			f_{RF} = 434MHz		10.4		
			f_{RF} = 863MHz to 945MHz		10.2		
		PA off, PA predriver at high current setting	f_{RF} = 315MHz		13.2		
			f_{RF} = 434MHz		12.4		
			f_{RF} = 863MHz to 945MHz		12.2		
		P_{OUT} = +15dBm	868MHz +15dBm matching network with harmonic filter		41		
		P_{OUT} = +10dBm	868MHz +10dBm matching network with harmonic filter		21		
Shutdown Current		T_A = +25°C, Sleep mode			350		nA
		T_A = +85°C, Sleep mode			600		
		T_A = +125°C, Sleep mode			1700	4000	
		T_A = +25°C, Shutdown mode (registers reset)			50		
		T_A = +85°C, Shutdown mode (registers reset)			200		
		T_A = +125°C, Shutdown mode (registers reset)			1300	3500	
Input Low Voltage	V_{IL}					0.2 x V_{DD}	V
Input High Voltage	V_{IH}			0.8 x V_{DD}			

DC ELECTRICAL CHARACTERISTICS (continued)

(Figure 2, 50Ω system impedance, V_{DD} = +2.1V to +3.6V, f_{RF} = 868MHz, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DD} = +3.0V, T_A = +25°C, unless otherwise noted. All min and max values are 100% tested at T_A = +125°C and are guaranteed by design and characterization over temperature, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Pulldown Sink Current				12.5		µA
Pullup Source Current				12.5		
Output Low Voltage	V_{OL}	In buffer mode, GPO1 250µA sink current, SDO 1mA sink current, and GPO2 4mA sink current		0.225		V
Output High Voltage	V_{OH}	In buffer mode, GPO1 250µA source current, SDO 1mA source current, and GPO2 4mA source current		V_{DD} - 0.225		

AC ELECTRICAL CHARACTERISTICS

(Figure 2, 50Ω system impedance, V_{DD} = +2.1V to +3.6V, f_{RF} = 868MHz, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DD} = +3.0V, T_A = +25°C, unless otherwise noted. All min and max values are 100% tested at T_A = +125°C and are guaranteed by design and characterization over temperature, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GENERAL CHARACTERISTICS						
Operating Frequency		Divide-by-1 LO divider setting	863		945	MHz
		Divide-by-2 LO divider setting	431.5		472.5	
		Divide-by-3 LO divider setting	287.7		315	
Maximum Data Rate		Manchester encoded		100		kbps
		NRZ encoded		200		
Maximum Frequency Deviation		100kHz synthesizer loop bandwidth		±150		kHz
Frequency Settling Time	t_{ON}	From Enable low-to-high transition to LO within 5kHz of final value, 100kHz synthesizer loop bandwidth		330		µs
		From Enable low-to-high transition to LO within 1kHz of final value, 100kHz synthesizer loop bandwidth		400		
POWER AMPLIFIER						
Maximum Output Power	P_{MAX}	Match to 50Ω, including harmonic filter		+15		dBm
Programmable PA Bias Current Step		With ±1% 56.2kΩ external PA reference current setting resistor		0.5		mA
Programmable PA Power Dynamic Range		Power range from decimal 1 to decimal 63 on digital PA bias current		36		dB
Modulation Depth		With respect to +10dBm output power		57		dB
Maximum Carrier Harmonics		With output matching network		-50		dBc

AC ELECTRICAL CHARACTERISTICS (continued)

(Figure 2, 50Ω system impedance, V_{DD} = +2.1V to +3.6V, f_{RF} = 868MHz, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DD} = +3.0V, T_A = +25°C, unless otherwise noted. All min and max values are 100% tested at T_A = +125°C and are guaranteed by design and characterization over temperature, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
FRACTIONAL-N SYNTHESIZER						
VCO Gain	K_{VCO}	Referenced to 863MHz to 945MHz LO		108		MHz/V
Close-In Phase Noise		10kHz offset, 100kHz loop BW		-101		dBc/Hz
VCO Phase Noise		1MHz offset, 863MHz to 945MHz		-126		dBc/Hz
Charge-Pump Current	I_{CP}	V_{OUT} = V_{CPVDD}/2, low setting (icont bit = 0)		204		µA
		V_{OUT} = V_{CPVDD}/2, high setting (icont bit = 1)		407		µA
LO Divider Settings				1		
				2		
				3		
Minimum Synthesizer Frequency Step		Referenced to 863MHz to 945MHz LO or carrier frequency band		$f_{XTAL}/2^{16}$		Hz
Reference Spur				-71		dBc
Frequency Switching Time		26MHz frequency step, 902MHz to 928MHz band, 100kHz synthesizer loop bandwidth		48		µs
Reference Frequency Input Level				1		V_{P-P}
ADC						
Resolution				7		Bits
LSB Bit Width				7.25		mV
CRYSTAL OSCILLATOR						
Crystal Frequency	f_{XTAL}			16 to 22.4		MHz
Frequency Pulling by V_{DD}				0.5		ppm/V
Recommended Crystal Load Capacitance				10		pF
Maximum Crystal Load Capacitance				20		
TEMPERATURE SENSOR						
Range				-40 to +125		°C
Digital Code Slope				2		°C/LSB
SPI TIMING CHARACTERISTICS (Figure 1)						
Minimum SCLK Low to Falling Edge of $\overline{CS}$ Setup Time	t_{SC}			20		ns
Minimum $\overline{CS}$ Low to Rising Edge of SCLK Setup Time	t_{CSS}			30		ns

AC ELECTRICAL CHARACTERISTICS (continued)

(Figure 2, 50Ω system impedance, V_{DD} = +2.1V to +3.6V, f_{RF} = 868MHz, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DD} = +3.0V, T_A = +25°C, unless otherwise noted. All min and max values are 100% tested at T_A = +125°C and are guaranteed by design and characterization over temperature, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Minimum SCLK Low to Rising Edge of $\overline{CS}$ Setup Time	t_{HCS}			30		ns
Minimum SCLK Low after Rising Edge of $\overline{CS}$ Hold Time	t_{HS}			20		ns
Minimum Data Valid to SCLK Rising-Edge Setup Time	t_{DS}			15		ns
Minimum Data Valid to SCLK Rising-Edge Hold Time	t_{DH}			10		ns
Minimum SCLK High Pulse Width	t_{CH}			30		ns
Minimum SCLK Low Pulse Width	t_{CL}			30		ns
Minimum $\overline{CS}$ High Pulse Width	t_{CSH}			30		ns
Maximum Transition Time from Falling Edge of $\overline{CS}$ to Valid SDO	t_{CSG}	C_L = 10pF load capacitance from SDO to GND		20		ns
Maximum Transition Time from Falling Edge of SCLK to Valid SDO	t_{CG}	C_L = 10pF load capacitance from SDO to GND		20		ns

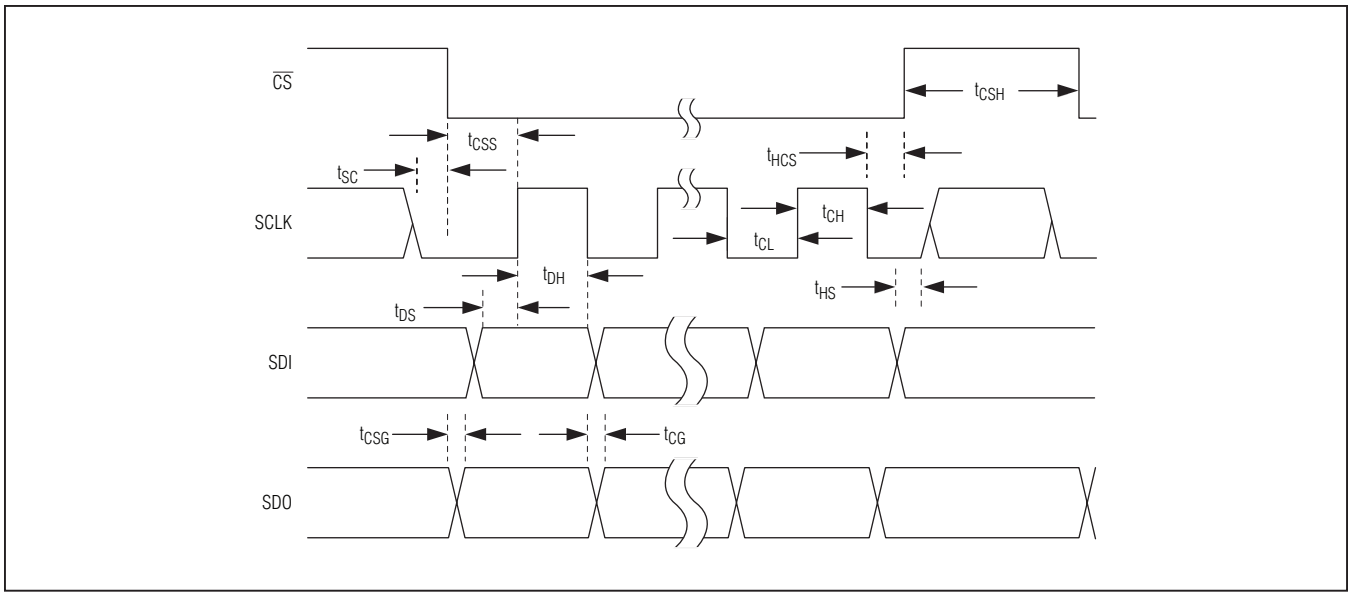


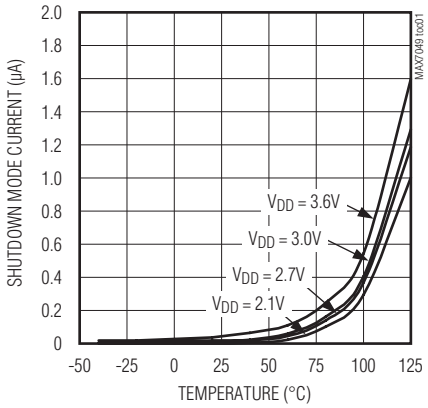
Figure 1. SPI Timing Diagram

High-Performance, 288MHz to 945MHz ASK/FSK ISM Transmitter

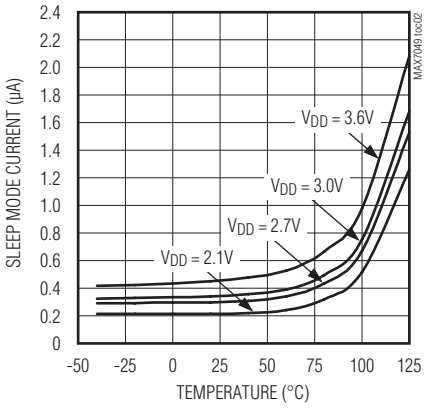
Typical Operating Characteristics

(Figure 2, 50Ω system impedance, V_{DD} = +2.1V to +3.6V, f_{RF} = 288MHz to 945MHz, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DD} = +3.0V, T_A = +25°C, unless otherwise noted.)

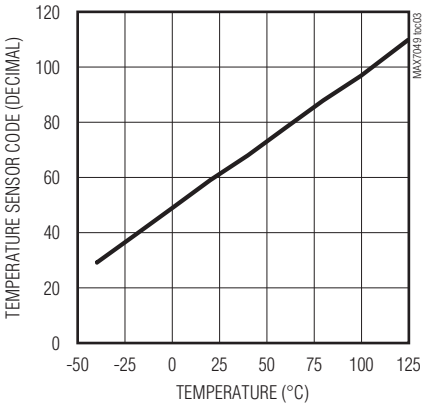
SHUTDOWN MODE CURRENT vs. TEMPERATURE



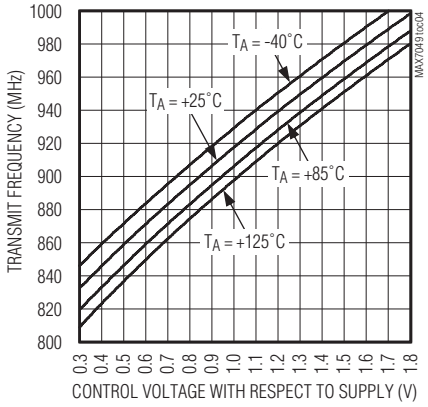
SLEEP MODE CURRENT vs. TEMPERATURE



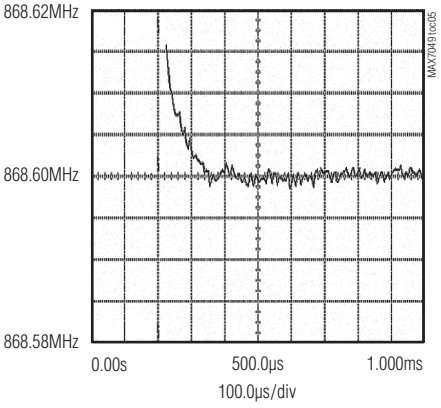
TEMPERATURE SENSOR CODE vs. TEMPERATURE



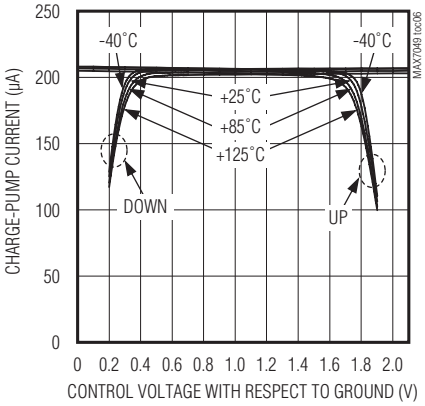
VCO TUNING CHARACTERISTIC (IN 900MHz BAND) vs. CONTROL VOLTAGE



FREQUENCY SETTLING AFTER POWER-UP



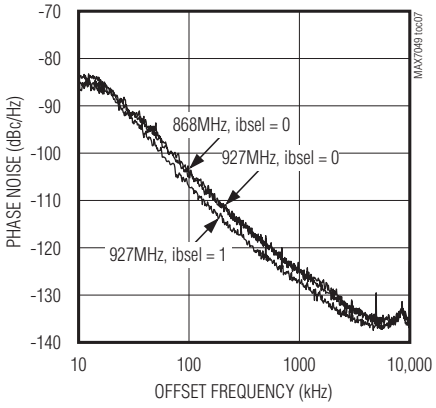
CHARGE-PUMP CURRENT vs. CONTROL VOLTAGE (LOW CURRENT SETTING, 2.1V SUPPLY)



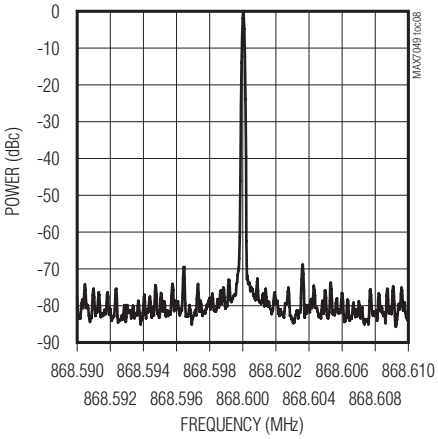
Typical Operating Characteristics (continued)

(Figure 2, 50Ω system impedance, V_{DD} = +2.1V to +3.6V, f_{RF} = 288MHz to 945MHz, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DD} = +3.0V, T_A = +25°C, unless otherwise noted.)

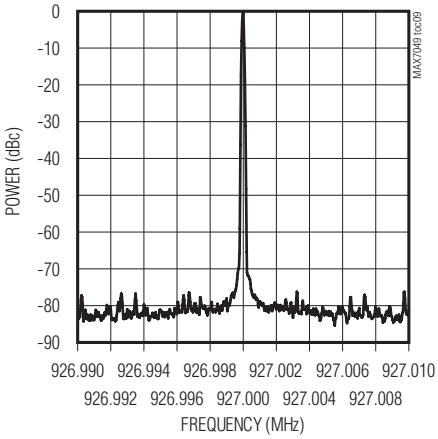
PHASE NOISE (VCO DOMINATED) vs. OFFSET FREQUENCY (C_L = 0.1µF, CS = 0.01µF, R = 200Ω, RP = CP = 0)



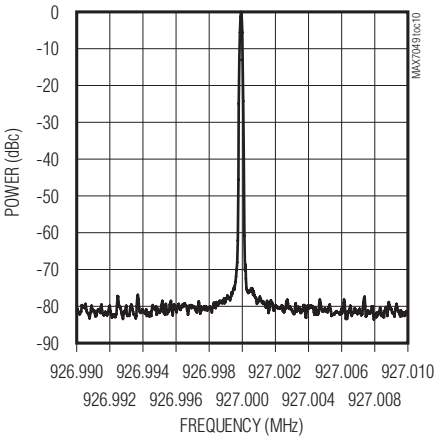
UNMODULATED CLOSE-IN SPECTRUM (100Hz RBW, 100 SAMPLE AVERAGE, 22.4MHz CRYSTAL, ibsel = 0, icont = 0)



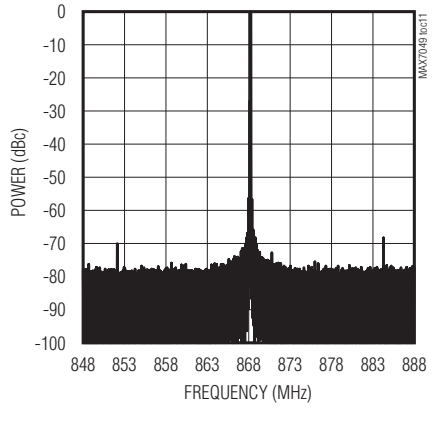
UNMODULATED CLOSE-IN SPECTRUM (100Hz RBW, 100 SAMPLE AVERAGE, 22.4MHz CRYSTAL, ibsel = 0, icont = 0)



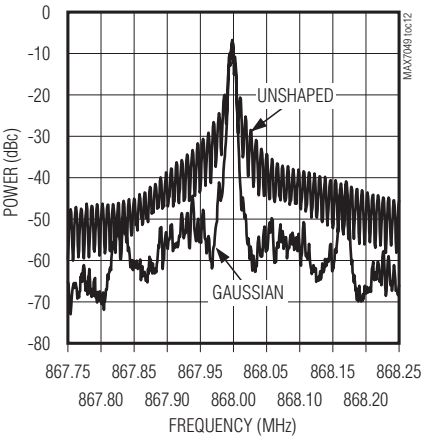
UNMODULATED CLOSE-IN SPECTRUM (100Hz RBW, 100 SAMPLE AVERAGE, 16MHz CRYSTAL, ibsel = 0, icont = 0)



UNMODULATED SPECTRUM (palopwr = 0, 100% DUTY CYCLE, +10dBm, 868MHz, WITH +10dBm AT 3V MATCH)



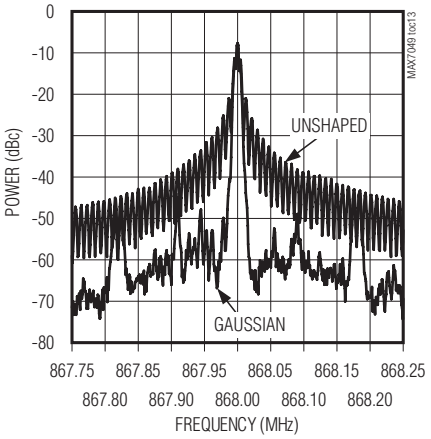
ASK MODULATION SPECTRUM (3kHz RBW, 4kHz SQUARE-WAVE MODULATION, +10dBm OUTPUT POWER, WITH +10dBm AT 3V MATCH)



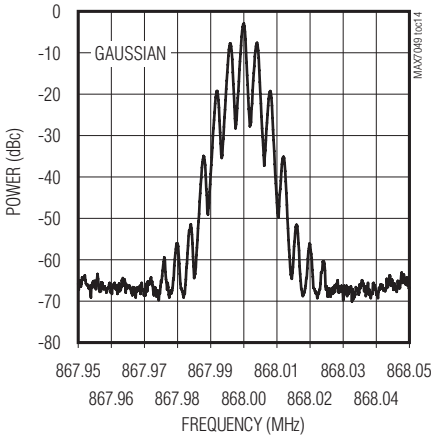
Typical Operating Characteristics (continued)

(Figure 2, 50Ω system impedance, V_{DD} = +2.1V to +3.6V, f_{RF} = 288MHz to 945MHz, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DD} = +3.0V, T_A = +25°C, unless otherwise noted.)

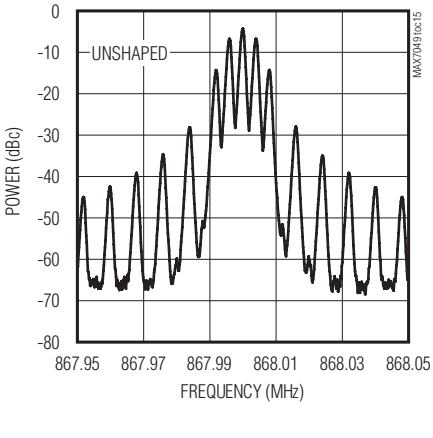
ASK MODULATION SPECTRUM (3kHz RBW, 4kHz SQUARE-WAVE MODULATION, +9dBm OUTPUT POWER, WITH +10dBm AT 3V MATCH)



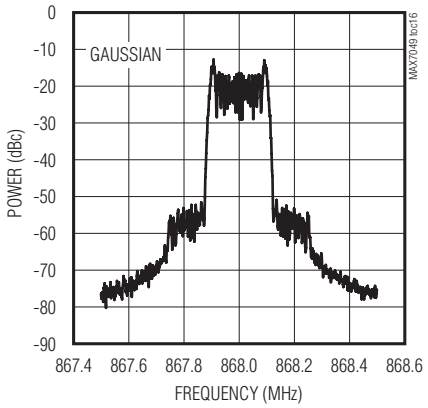
FSK MODULATION SPECTRUM (1kHz RBW, 4kHz SQUARE-WAVE MODULATION, ±4kHz DEVIATION, +10dBm OUTPUT POWER, WITH +10dBm AT 3V MATCH)



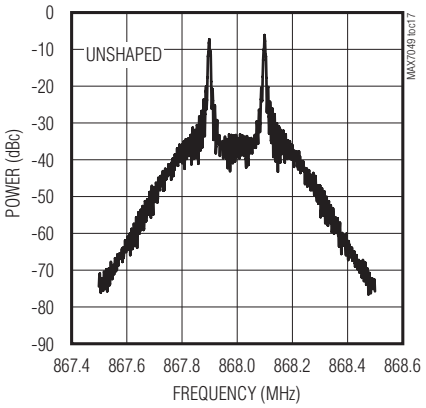
FSK MODULATION SPECTRUM (1kHz RBW, 4kHz SQUARE-WAVEMODULATION, ±4kHz DEVIATION, +10dBm OUTPUT POWER, WITH +10dBm AT 3V MATCH)



FSK MODULATION SPECTRUM (3kHz RBW, 4kHz SQUARE-WAVE MODULATION, ±100kHz DEVIATION, +10dBm OUTPUT POWER, WITH +10dBm AT 3V MATCH)



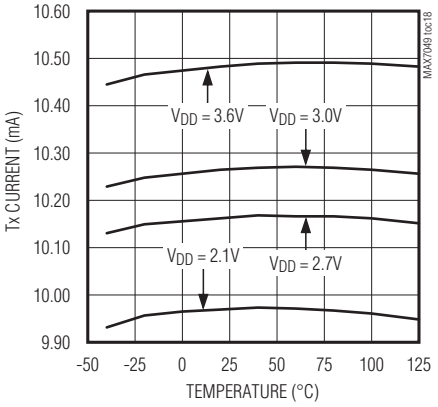
FSK MODULATION SPECTRUM (3kHz RBW, 4kHz SQUARE-WAVE MODULATION, ±100kHz DEVIATION, +10dBm OUTPUT POWER, WITH +10dBm AT 3V MATCH)



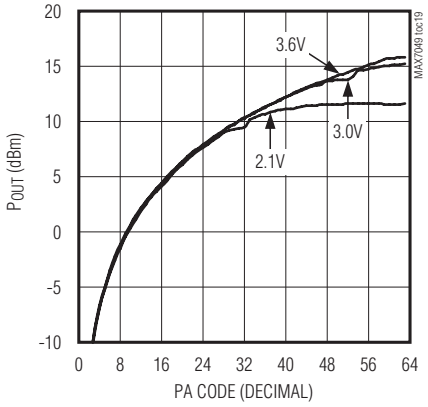
Typical Operating Characteristics (continued)

(Figure 2, 50Ω system impedance, V_{DD} = +2.1V to +3.6V, f_{RF} = 288MHz to 945MHz, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DD} = +3.0V, T_A = +25°C, unless otherwise noted.)

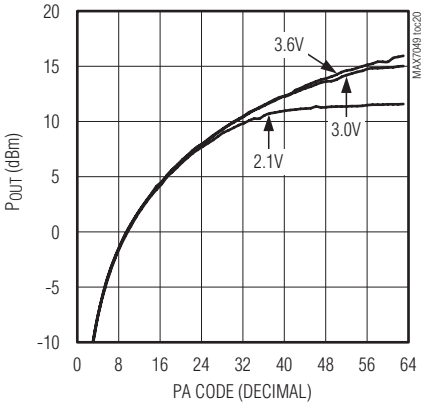
Tx CURRENT vs. TEMPERATURE (PA OFF, 900MHz BAND, palopwr = 1)



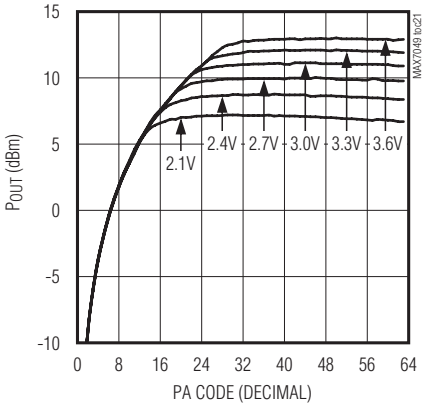
PA POWER vs. PA CODE (palopwr = 0, 100% DUTY CYCLE, 915MHz, WITH +15dBm AT 3V MATCH)



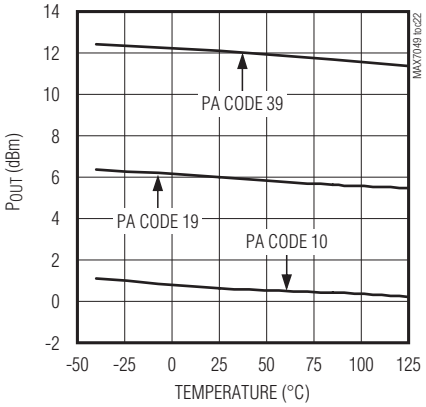
PA POWER vs. PA CODE (palopwr = 0, 100% DUTY CYCLE, 868MHz, WITH +15dBm AT 3V MATCH)



PA POWER vs. PA CODE (palopwr = 1, 100% DUTY CYCLE, 868MHz, WITH +10dBm AT 3V MATCH)

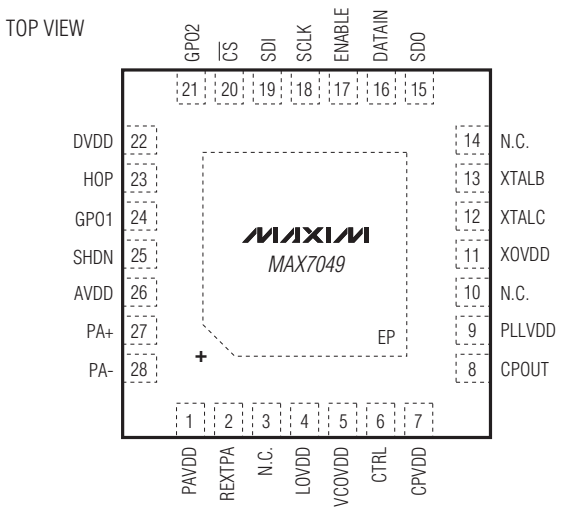


PA POWER vs. PA CODE (palopwr = 0, 100% DUTY CYCLE, 868MHz, WITH +15dBm AT 3V MATCH)



High-Performance, 288MHz to 945MHz ASK/FSK ISM Transmitter

Pin Configuration



TQFN
(5mm x 5mm)

Pin Description

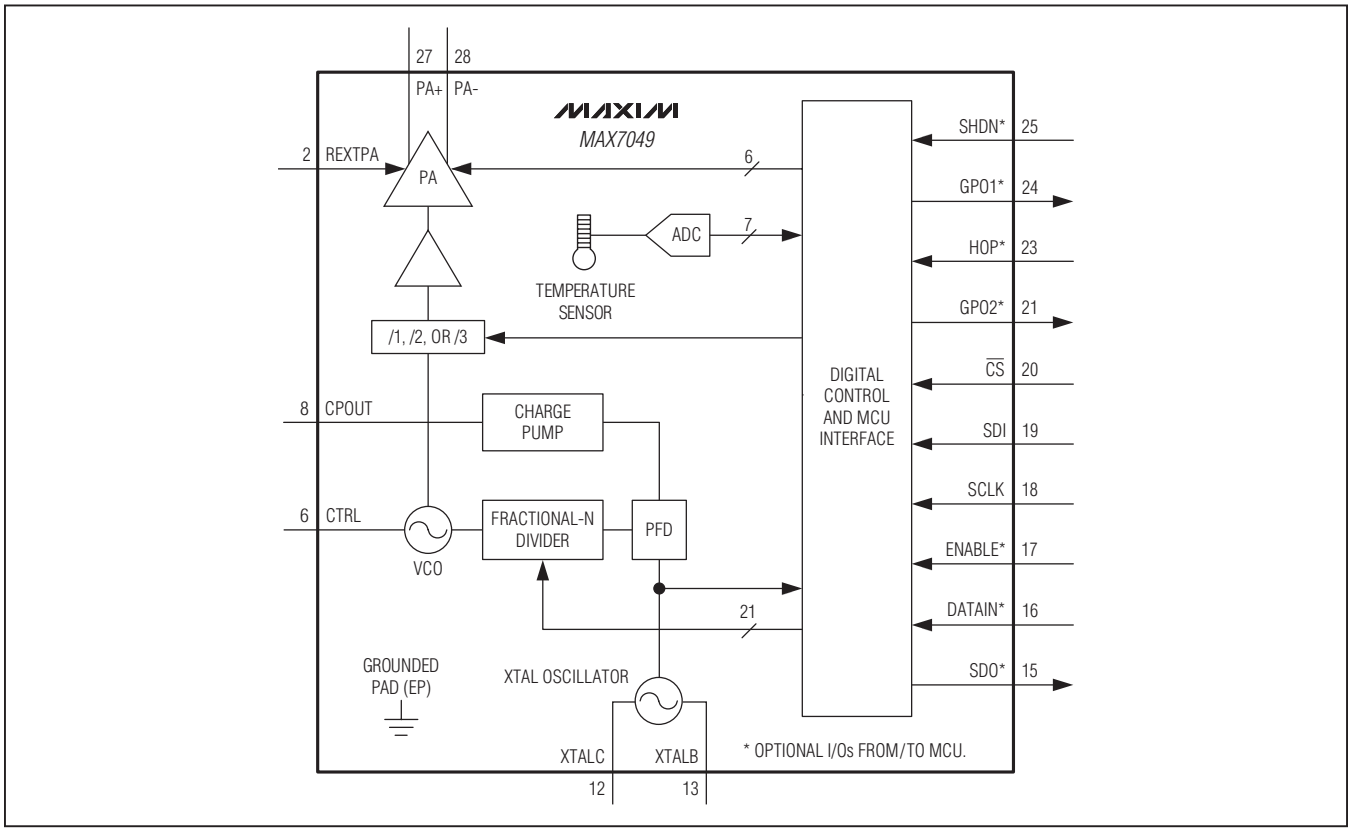
PIN	NAME	FUNCTION
1	PAVDD	Power Amplifier Supply Voltage Input. Bypass to ground with 33pF capacitor as close as possible to the pin.
2	REXTPA	External PA Bias Current Setting Resistor Connection. Couple to ground through a ±1% tolerance low-temperature coefficient resistor. A resistor of 56.2kΩ is recommended for a 0.5mA nominal PA bias current DAC LSB value.
3, 10, 14	N.C.	No Connection. Leave unconnected.
4	LOVDD	Local Oscillator (LO) Supply Voltage Input. Bypass to ground with 33pF capacitor as close as possible to the pin.
5	VCOVDD	Voltage-Controlled Oscillator (VCO) Supply Voltage. Bypass to ground with 1µF capacitor as close as possible to the pin.
6	CTRL	Control (Tuning) Voltage for VCO Input. Referenced to VCOVDD pin. Connect through passive loop filter to CPOUT.
7	CPVDD	Charge-Pump Supply Voltage Input. Bypass to ground with 0.01µF capacitor as close as possible to the pin.
8	CPOUT	Charge-Pump Output. Connect through passive loop filter to CTRL.
9	PLLVDD	Synthesizer Supply Voltage Input. Bypass to ground with 33pF capacitor as close as possible to the pin.
11	XOVDD	Crystal Oscillator Supply Voltage Input. Bypass to ground with 0.1µF capacitor as close as possible to the pin.

Pin Description (continued)

PIN	NAME	FUNCTION
12	XTALC	Collector Crystal Input. Connect to crystal either directly or through an AC-coupling capacitor. A shunt capacitance to ground might be needed depending on the specified load capacitance of the crystal and PCB stray capacitances. Can be driven by an AC-coupled external reference with a signal swing of $0.8V_{P-P}$ to $1.2V_{P-P}$.
13	XTALB	Base Crystal Input. Connect to crystal either directly or through an AC-coupling capacitor. A shunt capacitance to ground might be needed depending on the specified load capacitance of the crystal and PCB stray capacitances. Must be DC shorted to ground if XTALC is driven by external reference.
15	SDO	Serial Peripheral Interface (SPI) Data Output. It can also be configured as a general-purpose digital output.
16	DATAIN	Transmitter Data Input. The Datain function can also be controlled by SPI. Internally pulled to ground.
17	ENABLE	Enable. Drive high for active operation. Drive low or leave unconnected to put the device into Sleep mode. The enable function can also be controlled by SPI. Internally pulled to ground.
18	SCLK	SPI Clock. Internally pulled to ground.
19	SDI	SPI Data Input. Internally pulled to ground.
20	$\overline{CS}$	SPI Active-Low Chip Select. Internally pulled to supply.
21	GPO2	General-Purpose Output 2. High drive strength digital general-purpose output.
22	DVDD	Digital Supply Voltage Input. Bypass to ground with 0.1µF capacitor as close as possible to the pin.
23	HOP	Frequency Hop Pin. Transfers the base[20:0] bits to the fractional-N divider. See the *Fractional-N Synthesizer* section. The hop function can also be controlled by SPI. Internally pulled to ground.
24	GPO1	General-Purpose Output 1. Low drive strength digital general-purpose output.
25	SHDN	Shutdown Digital Input. Turns off internal power-on-reset (POR) circuit when driven high. Register contents are set to the initial state when driven high. Must be driven low for normal operation. Not internally pulled to supply or ground.
26	AVDD	Analog Supply Voltage Input. Bypass to ground with a 1µF capacitor as close as possible to the pin.
27	PA+	Power Amplifier (PA) Positive Output. Requires DC current path to supply voltage through an inductive path. The DC current path can be part of the output impedance matching and harmonic filter network.
28	PA-	Power Amplifier (PA) Negative Output. Requires DC current path to supply voltage through an inductive path. The DC current path can be part of the output impedance matching and harmonic filter network.
—	EP	Exposed Pad. This is the only ground connection. Solder evenly to the PCB ground plane for proper operation. Multiple vias from the solder pad to the PCB ground plane are recommended.

High-Performance, 288MHz to 945MHz ASK/FSK ISM Transmitter

Functional Diagram



Detailed Description

Architectural Overview and Applications Circuit

The MAX7049 includes a single precision local oscillator fractional-N synthesizer with an integrated VCO, fractional-N divider, phase/frequency detector, charge pump, LO divider, and lock detector. The loop filter is located off-chip to allow the user to optimize the synthesizer noise and transient characteristics for a particular application. In FSK transmit mode, the synthesizer transitions between the mark and the space frequency based on the state of the DATAIN pin or datain bit (Datain register, 0x3D, bit 6). A user-programmable frequency-shaping function enables the user to precisely define the transition from the mark frequency to the space frequency and vice versa to minimize spectral width of the modulated Tx waveform.

The IC utilizes a differential emitter-coupled, dual-open-collector power amplifier for the transmitter output. The bias current of the output stage is set with a combination of an external resistor and an internal amplitude-shaping function. The programmable shaping function enables the user to precisely define the transition between carrier on and carrier off and vice versa based on the state of the DATAIN pin or datain bit so as to minimize the spectral width of the modulated Tx signal. Linear amplitude ramping is used in FSK mode as the PA is enabled at the beginning of a data burst and disabled at the end of a data burst for spectral control.

A complete transmitter system can be built using a low-end MCU, the IC, a crystal, and a small number of passive components for power-supply bypassing and for RF matching, as illustrated in Figure 2.

Communication between the MCU and the IC is accomplished through a 4-pin SPI bus and a number of optional digital inputs and outputs.

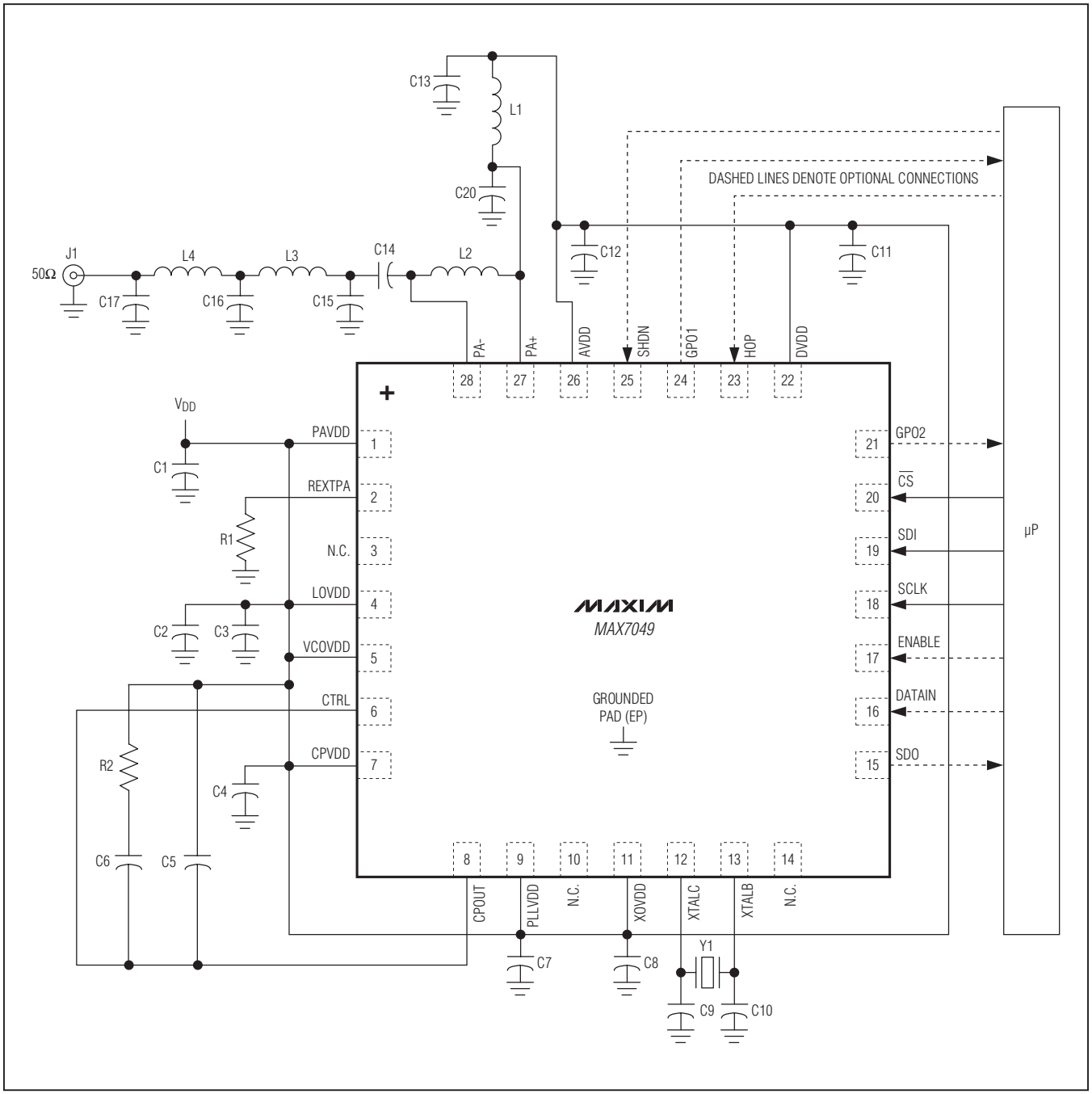


Figure 2. Typical Operating Circuit

Digital Inputs and Outputs

Digital Inputs

The IC's SPI inputs are the $\overline{CS}$, SCLK, and SDI pins. The $\overline{CS}$ pin is active low, so this pin has an internal pullup. The SCLK and SDI pins have internal pulldowns. In addition to the SPI inputs, there are also a number of optional digital inputs to the IC. These inputs are DATAIN, ENABLE, and HOP. These optional inputs, which have internal pulldowns, give the user the option to control an internal signal by either driving the pin to the appropriate logic level or by setting a control bit to the appropriate state. This is illustrated in Figure 3.

SPI control minimizes the number of I/Os required between the IC and the MCU, whereas the pin control eliminates the configuration overhead associated with SPI communication.

Digital Outputs

The IC has two dedicated general-purpose outputs (GPO1 and GPO2), one SPI output (SDO) that can also serve as a general-purpose output when $\overline{CS}$ is high. The GPO1, GPO2, and SDO pins can be configured to output various internal status signals and clocks, as illustrated in Figure 4.

The outputs (GPO1 and GPO2) offer a feature where the pin can operate either as a digital buffer or as a current-limited source/sink output, as illustrated in Figure 5.

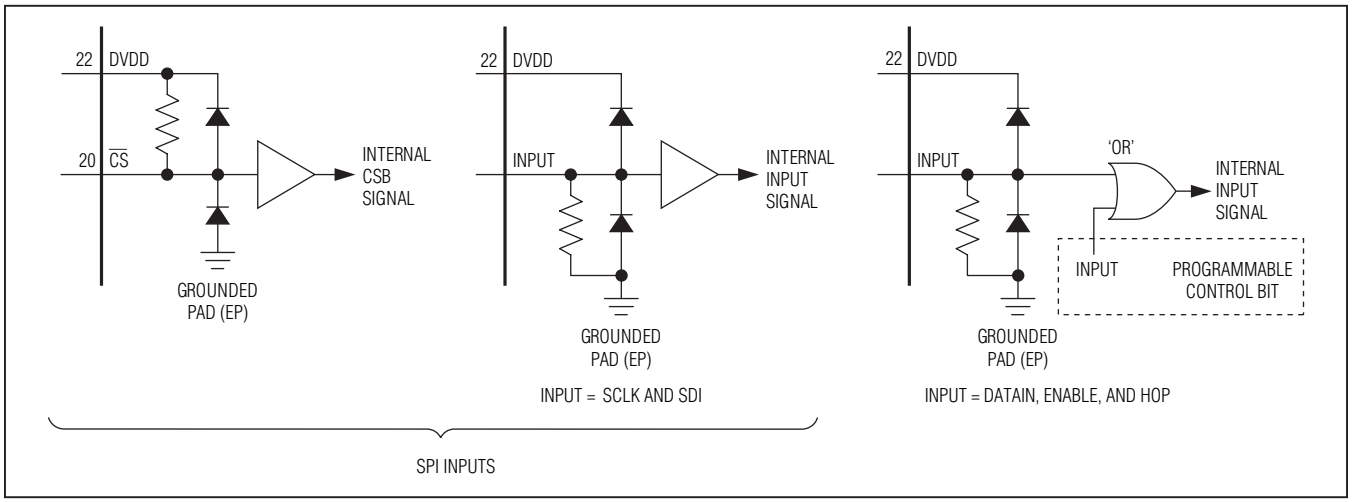


Figure 3. Digital Inputs

Table 1. Optional Digital Input Controls

PIN	BIT NAME	REGISTER NAME	REGISTER ADDRESS (hex)	BIT LOCATION (7:0)	FUNCTION
DATAIN	datain	Datain	0x3D	6	Data input to transmitter.
ENABLE	enable	EnableReg	0x3E	0	Enable input for transmitter.
HOP	hop	FLoad	0x0B	0	Initiates the transition to the next frequency as defined by base[20:0].

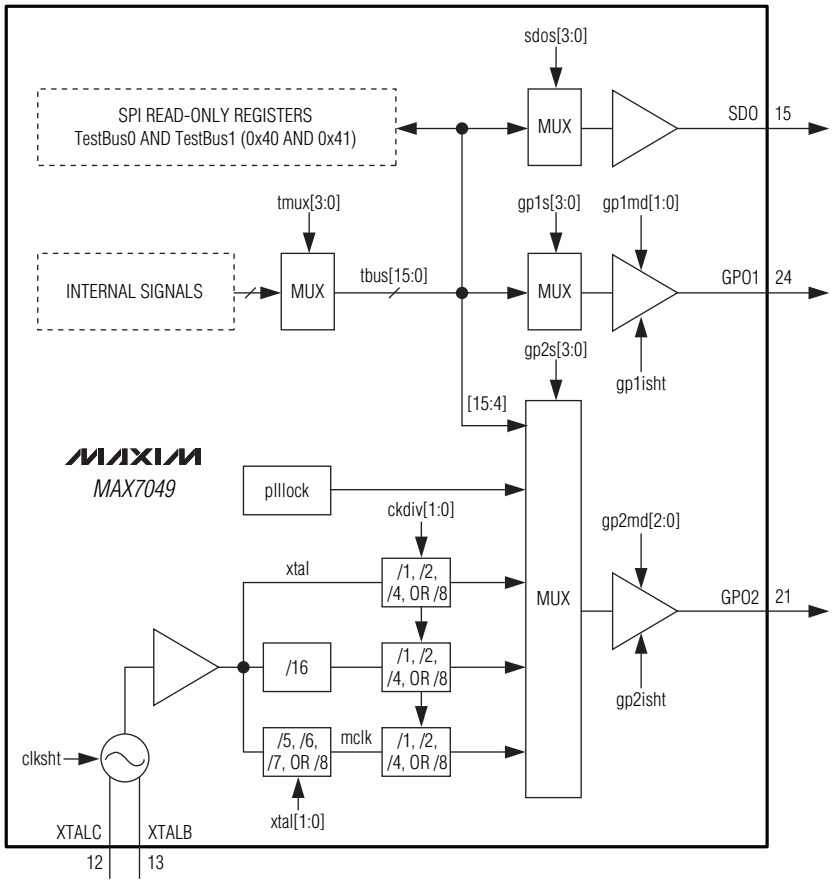


Figure 4. Digital Outputs

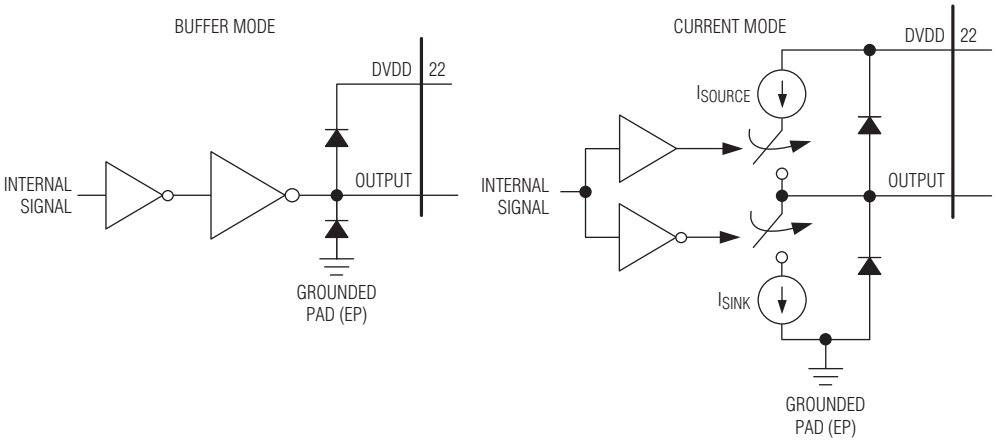


Figure 5. Digital Output Options

The current mode of operation can reduce digital noise associated with large supply current spikes. The GPO1 pin has a relatively small current drive capability (80µA or 160µA). The IOConf2 register (0x05) (gp1md[1:0] bits) control the current settings:

gp1md[1:0]	Mode
0x	Buffer mode
10	80µA sink/source capability
11	160µA sink/source capability

GPO2 has a much larger current drive capability (up to 4mA), as this GPO can be the source of output clock signals. The IOConf2 register (0x05) (gp2md[2:0] bits) control the current settings:

gp2md[2:0]	Mode
0xx	Buffer mode
100	1.0mA sink/source capability
101	2.0mA sink/source capability
110	3.0mA sink/source capability
111	4.0mA sink/source capability

Two other bits also control the operation of GPO1 and GPO2. The IOConf0 register (0x03) (gp1isht and gp2isht bits) allows the current mode operation to continue even if the IC is disabled (Sleep mode).

The GPO2 pin is designated as the primary output for driving a clock, as it has the strongest buffer and highest current output capabilities.

The GPO2 clock signal can be selected by the gp2s[3:0] and ckdiv[1:0] bits (IOConf0 register, 0x03).

gp2s[3:0]	GPO2 Output
0000	plllock
0001	mclk/(ckdiv divider)
0010	xtal/(ckdiv divider)
0011	xtal/16/(ckdiv divider)

where the ckdiv divider is given by:

ckdiv[1:0]	Divide by
00	1
01	2
10	4
11	8

and xtal is the crystal frequency, and mclk is the master digital clock. The master digital clock is the divided crystal frequency given by the xtal[1:0] bits (Conf0 register, 0x01), according to:

xtal[1:0]	Divide by
00	5
01	6
10	7
11	8

If a clock output on GPO2 is required even when the IC is in Sleep mode (ENABLE pin and enable bit reset to 0), the SHDN pin is reset to 0, and the clksht bit (IOConf2 register, 0x05, bit 3) must be set to 1.

A very useful function of the GPOs is to output status signals that reflect the state of the transmitter at any particular instance in time. See the *Register Details* section for an in-depth description of the status signals available for the TestBus0 and TestBus1 registers.

Serial Peripheral Interface (SPI)

The IC utilizes a 4-wire SPI protocol for programming its registers, configuring and controlling the operation of the whole transmitter.

The following digital pins control the operation of the SPI:

$\overline{CS}$: Active-low SPI chip select

SDI: SPI data input

SCLK: SPI serial clock

SDO: SPI data output

The SPI operates on a byte format, as shown in Figure 6.

Any number of 8-bit data bursts (Data 1, Data 2, … Data N) can be sent within one low cycle of $\overline{CS}$, to allow for burst-write or burst-read operations. The SDO pin acts as another general-purpose output (GPO) when the $\overline{CS}$ pin is high.

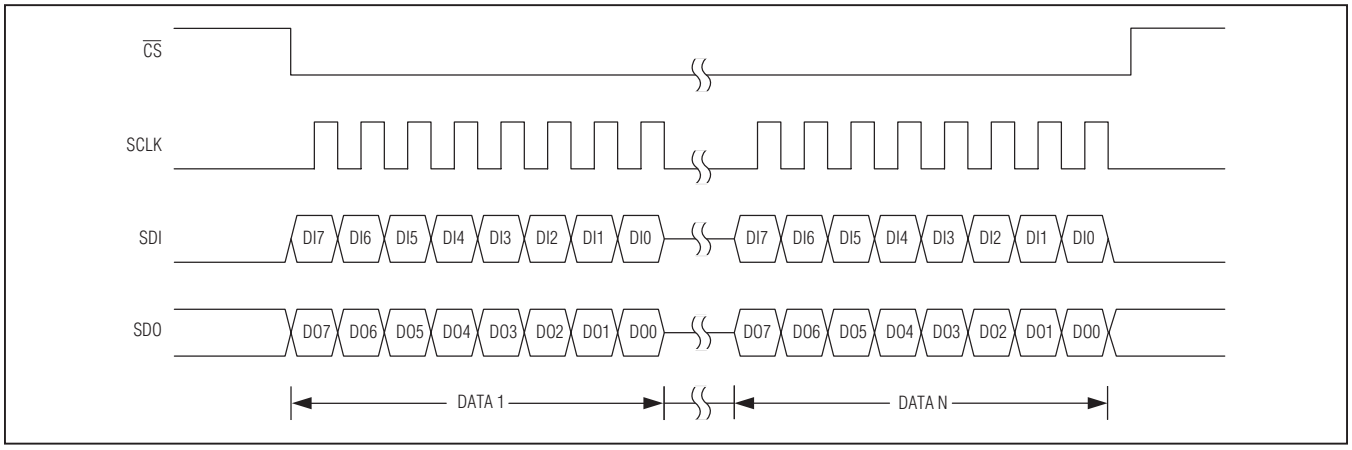


Figure 6. SPI Format

SPI Commands

The following commands are implemented in the IC:

Write: Within the same $\overline{CS}$ cycle, a write command is implemented as follows:

SDI: <0x01> <Initial Address> <Data 1> <Data 2> … <Data N>

With this command, Data 1 is written to the address given by <Initial Address>, Data 2 is written to <Initial Address + 1>, and so on.

Read: Within the same $\overline{CS}$ cycle, a read command is implemented as follows:

SDI: <0x02> <Address 1> <Address 2> <Address 3> … <Address N> <0x00>

SDO: <0xXX> <0xXX> <Data 1> <Data 2> … <Data N - 1> <Data N>

With this command, all the registers can be read within the same cycle of $\overline{CS}$. The addresses can be given in any order.

Read All: With two $\overline{CS}$ cycles, the Read All command is implemented as follows:

	$\overline{CS}$ Cycle 1	**$\overline{CS}$ Cycle 2**
SDI:	<0x03> <Address N>	<0x00> <0x00> <0x00> … <0x00>
SDO:		<Data N> <Data N + 1> <Data N + 2> … <Data N + n>

Reset: A SPI reset command is implemented as follows:

SDI: <0x04>

An internal active-low master resetb signal is generated, from the falling edge of the last SCLK signal to the falling edge of the following $\overline{CS}$ signal (t_{HCS} + t_{CSH}).

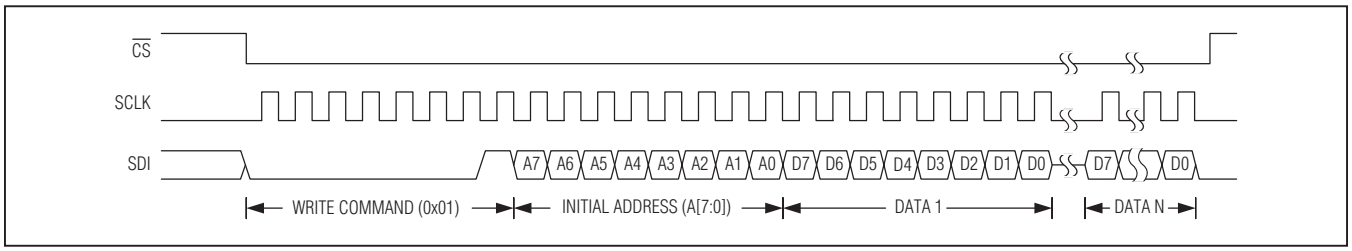


Figure 7. SPI Write Command Format

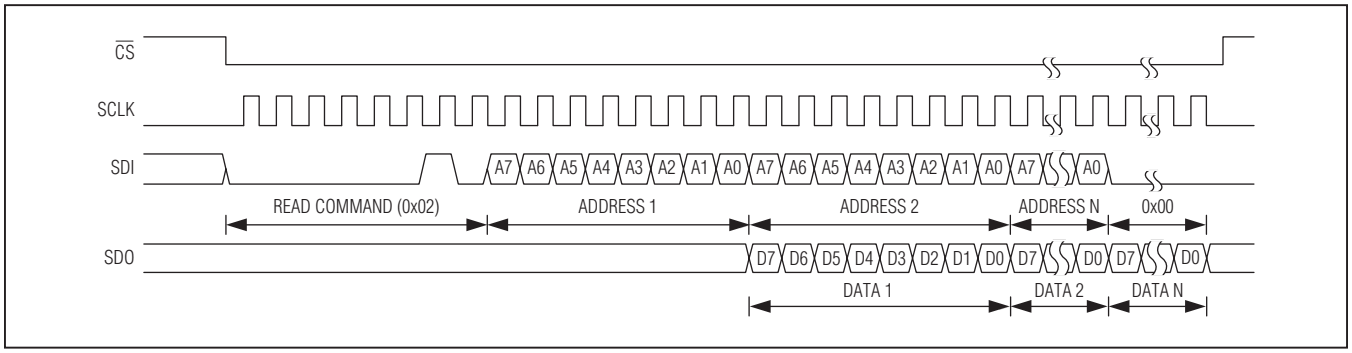


Figure 8. SPI Read Command Format

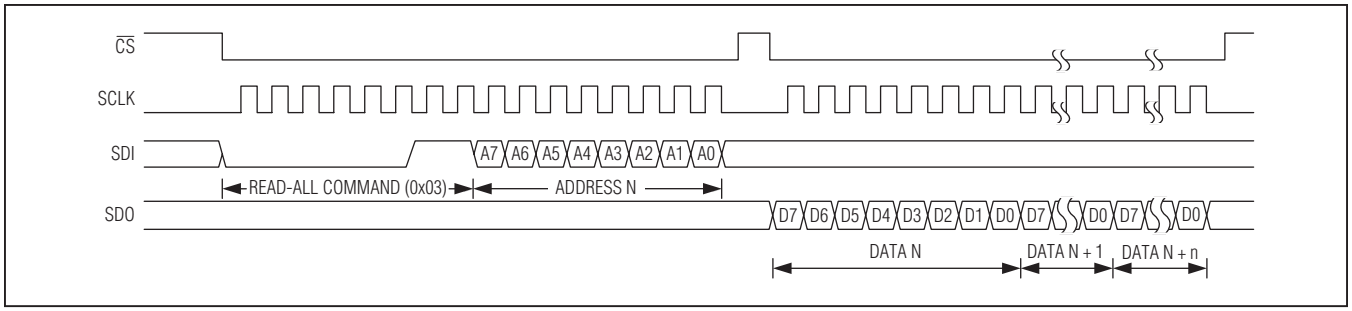


Figure 9. SPI Read-All Command Format

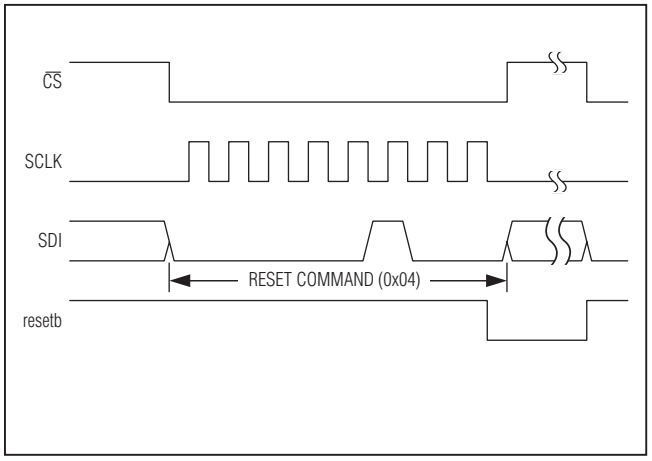


Figure 10. SPI Reset Command Format

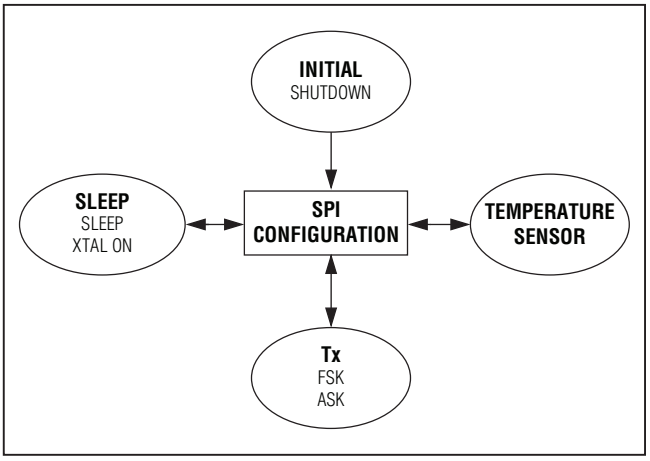


Figure 11. Operating Modes

Operating Mode Overview

The IC offers several modes of operation that allow the user to optimize the transmitter's power consumption for a particular application. The primary operating modes are Initial, Sleep, Temperature Sensor, and Tx, as illustrated in Figure 11.

When the SHDN pin is high, the IC is in Shutdown mode. In Shutdown mode, the POR circuit internal to the IC is disabled and draws virtually no current. In Shutdown mode, all internal data registers are reset to the initial states and must be rewritten for desired transmitter operation after the SHDN pin is driven low.

When the SHDN pin is low, the POR circuit is active and holds the internal data registers in the initial state until the power supply is above 2.1V and the IC enters the Initial mode. From the Initial mode, the IC can be configured for operation in Sleep mode, Temperature Sensor mode, or Tx mode. In Sleep mode, there are two options available: Sleep and XTAL ON. In Sleep mode, the current drain is typically 350nA. All register states are retained in Sleep mode. In XTAL ON mode, controlled by the clksht bit (IOConf2 register, 0x05, bit 3), the crystal oscillator is enabled and the divided output of the crystal oscillator (/1, /2, /4, /8, as set by the ckdiv[1:0] bits (IOConf0 register, 0x03, bits [5:4]) can be directed to GPO2. The XTAL ON mode is designed so an accurate high-speed clock is always available to the MCU.

In Temperature Sensor mode, the internal temperature sensor function can be executed.

In Tx mode, the transmitter can be configured to transmit ASK data or FSK data.

The Tx mode is determined by the logic states of the SHDN pin, ENABLE pin, and the enable bit (EnableReg register, 0x3E, bit 0). The transmitter is enabled if the SHDN pin is driven low and the ENABLE pin is driven high, or the enable bit is set. This logic is summarized in Table 2.

The mode options are selected by the mode SPI bit (Conf0 register, 0x01, bit 4) and these options are summarized in Table 3.

Sleep Mode

From the Initial mode, the transmitter directly enters Sleep mode. In XTAL ON mode, the crystal oscillator is enabled and the divided output of the crystal oscillator can be directed to GPO2. This mode is enabled when the RF functions are disabled and the clksht bit is set. The current drain in this mode is highly dependent on the frequency of the output signal and the load capacitance on the GPO2 pin. The current drain is typically 750µA when the output signal is 3.2MHz and the load capacitance is 10pF. See the *Digital Outputs* section for more details. Table 4 summarizes the Sleep mode functions.

Table 2. Mode Control Logic

SHDN PIN	ENABLE PIN	enable BIT	TRANSMITTER MODE
0	0	0	Sleep
0	0	1	Tx
0	1	0	Tx
0	1	1	Tx
1	0	0	Shutdown
1	0	1	Shutdown
1	1	0	Shutdown
1	1	1	Shutdown

Table 3. Mode Option Logic

mode BIT	MODE OPTION
0	ASK
1	FSK

Table 4. Sleep Mode Summary

SLEEP MODE	SETTINGS	TYPICAL CURRENT DRAIN	COMMENTS
Sleep	Enable = 0	350nA	All register contents are retained.
XTAL ON	clksht = 1	750µA*	Divided XTAL oscillator signal can be directed to GPO2.

**Dependent on GPO2 load capacitance and output clock frequency.*

Temperature Sensor Mode

The user must initiate the temperature sensor from Sleep mode, and the transmitter automatically returns to sleep when the measurement sequence is completed.

The on-chip temperature sensor is enabled when the tsensor bit (EnableReg register, 0x3E, bit 3) is set. Once the internal analog temperature sensor circuit has settled, an A/D conversion is performed and the resultant ADC value is stored in the tsadc[6:0] bits that are accessed through the TestBus1 register (0x41, bits 6:0) when the digital test mux bits tmux[3:0] (TestMux register, 0x3C, bits 3:0) are set to 0. The tsensor bit is a self-reset bit, so it returns to a zero state once the temperature sensor measurement is completed. The tsdone status bit (Status1 register, 0x43, bit 4) is also set when the measurement is completed. The current drain in Temperature Sensor mode is less than 1mA and the sensor settling time plus the ADC conversion time is less than 2ms. The pertinent features of the Temperature Sensor mode are summarized in Table 5.

Tx Mode

There are two subsets of the Tx mode. These subsets include FSK and ASK.

The transmitter output signal is generated by the fractional-N synthesizer, then buffered, and amplified by the power amplifier (PA) to the programmed output power level. There is a finite warmup time for the transmitter. Upon entering Tx mode from Sleep mode, the following sequence occurs:

1) The crystal oscillator is enabled and settles to a steady state. The rising edge of the internal ckalive status signal indicates that the crystal oscillator has settled and an accurate time base is available. All other Tx modules are enabled except the PA. The synthesizer settles to the desired LO frequency at the same time the other modules settle to their desired operating points. A rising edge of the lockdet status signal indicates that the synthesizer has locked. In some narrowband applications, the lockdet signal can effectively be delayed with the plldl[2:0] bits (Conf1 register, 0x02, bits 5:3) to ensure that the synthesizer has settled to within the desired accuracy. This delayed signal is called plllock. The rising edge of the txready status signal is coincident with the rising edge of the plllock signal.
2) In ASK mode, the power amplifier ramp-up sequence begins on the rising edge of either the DATAIN pin or the datain bit after the internal txready signal transitions high. In FSK mode, the power amplifier linear ramp-up sequence begins on the rising edge of the txready signal.

Figure 12 illustrates this warmup sequence.

In an ASK application, the output of the synthesizer is fixed at the carrier frequency. The output power is alternated between fully off when both the DATAIN pin is logic 0 and the datain bit is cleared, and the programmed output power level when either the DATAIN

Table 5. Temperature Sensor Mode Summary

BIT	EXECUTION TIME (ms)	TYPICAL CURRENT DRAIN (mA)	COMMENTS
tsensor	< 2	< 1	The tsdone status bit is set when the measurement is completed. The results are stored in tsadc[6:0].

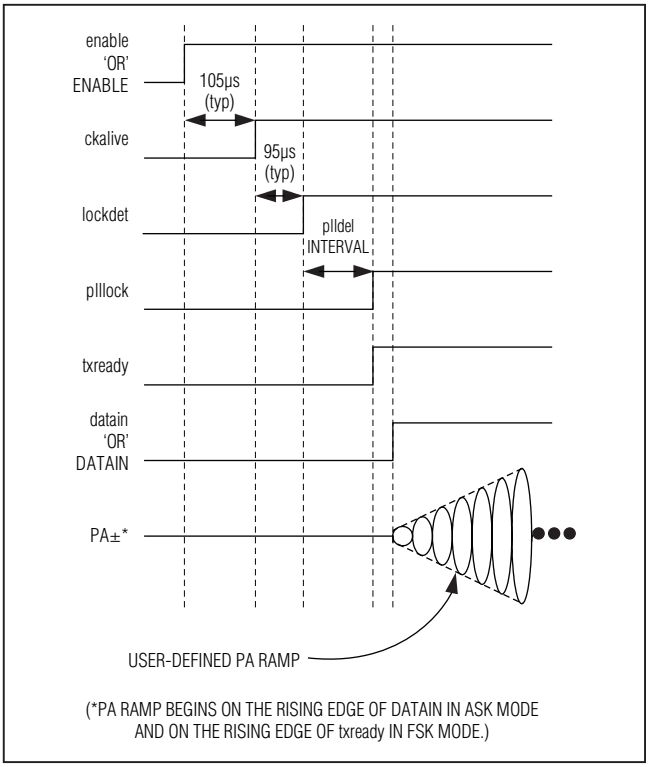


Figure 12. Tx Warmup Timing Diagram

pin is logic 1 or the datain bit is set. The output signal can be waveshaped in amplitude to reduce the spectral width of the transmission. See the *Power Amplifier* section for more information regarding amplitude waveshaping. The PA power is determined by the 6-bit amplitude word that linearly controls the PA output bias current. The LSB current amplitude is set by an off-chip resistor placed between the REXTPA pin and ground. The LSB current is nominally 0.5mA for a 56.2kΩ resistor and allows for very tight transmitter power control with a low-temperature coefficient ±1% tolerance resistor.

In an FSK application, the output of the synthesizer alternates between the space frequency when both the DATAIN pin is logic 0 and the datain bit is cleared, and the mark frequency when either the DATAIN pin is logic 1 or the datain bit is set. The output signal can be waveshaped in frequency to reduce the spectral width of the transmission. See the *Fractional-N Synthesizer* section for more information regarding frequency waveshaping. The PA power is determined by the 6-bit amplitude word. The PA output power linearly ramps between fully off and the programmed power when the transmitter is enabled or disabled. The ramp slope is also programmable. To transmit the entire message at the desired power level, the user should wait until the PA ramp is completed before initiating the data sequence.

The typical current drain in Tx mode is 10.2mA (low-power buffer mode) or 12.2mA (high-power buffer mode) plus the programmable PA output current. The buffer power mode is controlled by the palopwr bit (TxConf0 register, 0x0C, bit 7) and is in low-power mode when the bit is set.

Frequency-Hopping Spread-Spectrum (FHSS) Operation

The IC is fully capable of FHSS operation. The fast-settling fractional-N synthesizer and amplitude-shaping PA work in concert to allow clean, time efficient, and easy-to-implement frequency hopping under the control of a low-end MCU.

Figure 13 shows the recommended sequence during FHSS operation.

Use of the hop bit is preferred during initial configuration. Use of the HOP pin is preferred over the hop bit during active transmitter operation. This eliminates the possibility of SPI activity during active transmitter operation and allows for exact control of transmitter timing.

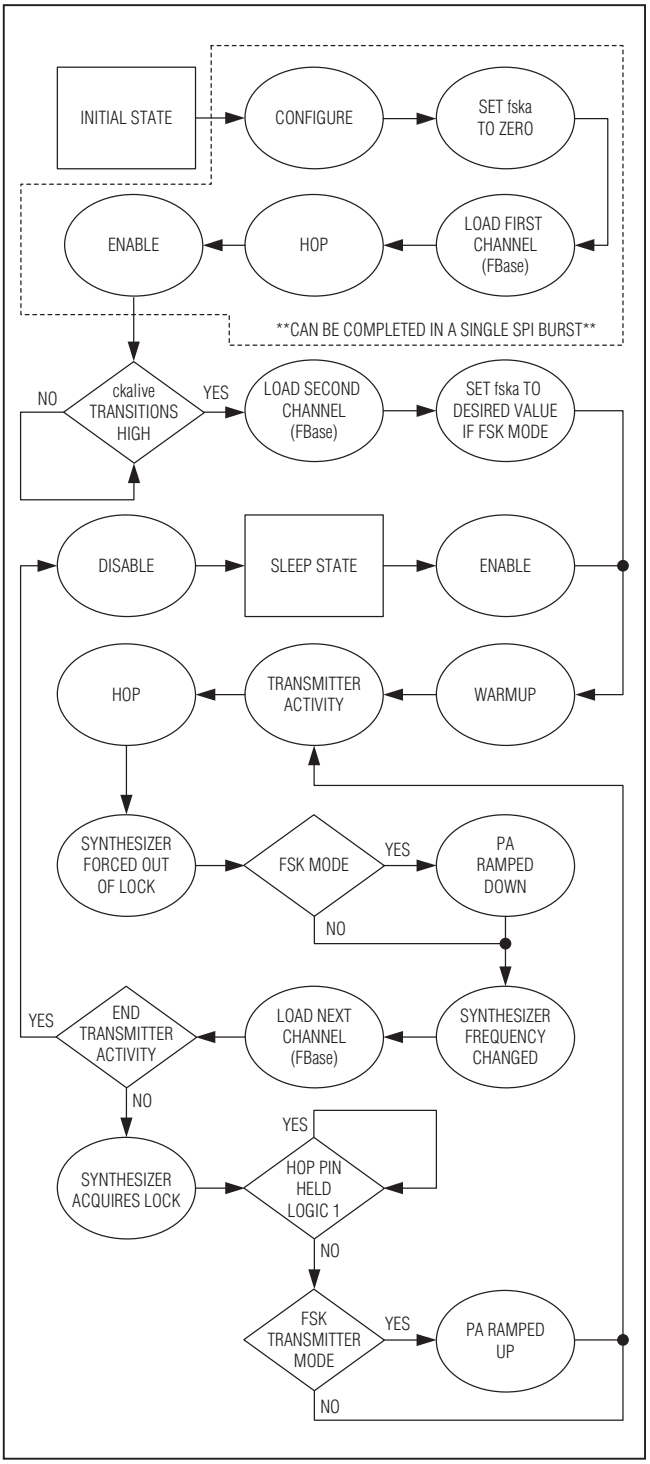


Figure 13. Frequency-Hopping Spread-Spectrum (FHSS) Flowchart

Functional Descriptions

Crystal Oscillator

The IC's crystal oscillator circuitry is designed to operate in conjunction with a parallel resonant crystal to generate the fractional-N synthesizer reference frequency and the clock signal for the digital control block. Only the crystal, attached between pins XTALB and XTALC, and two optional loading capacitors are typically required.

The oscillator typically presents a load capacitance of approximately 8pF between the pins of the crystal when PCB stray capacitance is considered. Capacitance must be added equally from pin XTALC to ground and pin XTALB to ground to operate the crystal at the specified crystal load capacitance. If the crystal is operated at a load capacitance different from the specified load capacitance, the oscillation frequency is pulled away from the specified operating frequency, introducing an error in the fractional-N synthesizer reference frequency. Crystals specified to operate with higher load capacitance than the applied load capacitance oscillate at a higher than specified frequency.

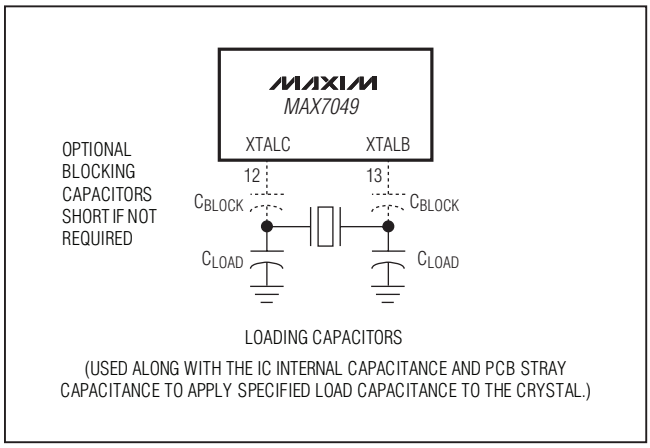


Figure 14. Recommended Crystal Connection to the IC

Frequency pulling from the specified operating frequency can be calculated if the electrical parameters of the crystal are known. The frequency pulling is given by:

$$f_P = \frac{C_M}{2}\left(\frac{1}{C_{CASE}+C_{LOAD}} - \frac{1}{C_{CASE}+C_{SPEC}}\right)\times 10^6$$

where:

f_P is the amount the crystal frequency is pulled in ppm.

C_M is the motional capacitance of the crystal.

C_{CASE} is the case capacitance (includes package capacitance and crystal blank capacitance).

C_{SPEC} is the specified load capacitance.

C_{LOAD} is the applied load capacitance.

When the crystal is loaded as specified (i.e., $C_{LOAD} = C_{SPEC}$), the frequency pulling equals zero.

The oscillator circuitry is designed to operate with crystal load capacitances between 8pF and 20pF. Operation at an applied load capacitance of 10pF is recommended for optimal startup times. Operation with applied load capacitances greater than 20pF can prevent oscillator startup.

The operating range of the crystal oscillator is 16.0MHz to 22.4MHz. To maintain an internal 3.2MHz time base mclk, the xtal[1:0] (Conf0 register, 0x01, bits 1:0), must be programmed as shown in Table 6. The 3.2MHz internal time base is recommended for all data rates below 80kbps (Manchester coded) or 160kbps (NRZ coded). For higher data rates (up to 100kbps (Manchester coded) or 200kbps (NRZ coded)), a 4MHz internal time base is needed, as shown in Table 6.

The crystal initial tolerance, temperature coefficient, and aging must be specified so that the cumulative error between the transmitter and companion receiver frequencies allows proper operation. The transmitted signal must be downconverted by the companion receiver so that all necessary modulation sidebands are within the

Table 6. Crystal Divider Programming

CRYSTAL FREQUENCY (MHz)	CRYSTAL DIVIDER RATIO	xtal[1:0] Conf0 REGISTER, ADDRESS 0x01, BITS 1:0	mclk (MHz)
16.0	5	00	3.2
19.2	6	01	3.2
22.4	7	10	3.2
20.0	5	00	4.0

Note: *The combinations of crystal frequency and divide ratio in this table are recommended, but not all inclusive.*

passband of the predemodulation filter to operate properly. For channelized operation, the transmitted signal, including modulation sidebands, must be contained within a given frequency range, placing limits on the crystal initial tolerance, temperature coefficient, and aging.

The IC provides a temperature sensor and a fine-step fractional-N synthesizer to ease crystal frequency stability requirements. This sensor can be used by the system MCU along with the crystal temperature coefficient to calculate the necessary frequency correction and adjust the fractional-N synthesizer in $f_{XTAL}/2^{16}$Hz steps.

The IC allows for an external reference signal to be applied in place of a crystal. The external reference signal should be applied to pin XTALC through an AC-coupling capacitor at an amplitude between $0.8V_{P-P}$ and $1.2V_{P-P}$ with pin XTALB DC grounded.

Fractional-N Synthesizer

The IC contains a fully integrated fractional-N synthesizer with the exception of a passive off-chip loop filter for generating the transmitted signal frequency. This includes an on-chip voltage-controlled oscillator (VCO), charge pump, phase-frequency detector (PFD), fractional-N frequency divider, LO frequency divider, and all necessary support circuitry. The on-chip crystal oscillator generates the reference frequency for the fractional-N synthesizer.

The operating range of the fractional-N synthesizer is 863MHz to 945MHz. The LO frequency divider has three modes: divide by 1, divide by 2, and divide by 3. This allows for operation at frequencies of 863MHz to 945MHz, 431.5MHz to 472.5MHz, and 287.7MHz to 315MHz, respectively. The frequency resolution is $f_{XTAL}/2^{16}$ in the 863MHz to 945MHz range, and is smaller at the LO frequency-divider output by the LO division ratio. The division ratio of the LO frequency divider is set by the fsel[1:0] bits (Conf0 register, 0x01, bits 3:2). These division ratios are shown in Table 7.

The VCO operates over the entire specified frequency range with no calibration required. The typical VCO gain is 108MHz/V and the typical phase noise is -126dBc/Hz at 1MHz offset. The phase noise improves by 20 x $\log_{10}(2)$ for divide-by-2 LO frequency-divider operation, and improves by 20 x $\log_{10}(3)$ for divide-by-3 LO frequency divider operation. The VCO control voltage is applied at the CTRL pin and is referenced to the VCOVDD pin. The ibsel bit (Conf1 register, 0x02, bit 6) sets the VCO bias current. The VCO current increases by 1mA with the ibsel bit set. The VCO phase noise improves to -128dBc/Hz at 1MHz offset with the additional current drain.

The charge pump operates within a typical compliance range of 0.4V to 0.4V below the supply voltage. The typical charge-pump current is 204µA with the icont bit (Conf1 register, 0x02, bit 7) reset. It nearly doubles to 407µA with icont set. The CPOUT pin is the charge-pump output.

Tx ASK Mode

The fractional-N frequency divider is programmed with a 21-bit divider word. The divider word consists of a 5-bit integer portion and a 16-bit fractional portion as illustrated in Figure 15.

The parameter D is the fractional-N divider ratio, where:

$$D = 32 + base[20:0]/2^{16}$$

and therefore, the synthesizer output frequency is given by:

$$f_{SYNTH} = D \times f_{XTAL}$$

where f_{XTAL} is the reference frequency generated by the crystal oscillator.

The 21-bit divider word as defined by the contents of the FBase0, FBase1, and FBase2 registers is latched into the fractional-N divider on the rising edge of the Hop signal, which is the logical OR of the HOP input pin and the hop bit (FLoad register, 0x0B, bit 0), when the IC is enabled.

Table 7. LO Frequency-Divider Modes

fsel[1:0] Conf0 REGISTER, ADDRESS 0x01, BITS 3:2	LO DIVISION RATIO	TRANSMITTER OPERATING FREQUENCIES (MHz)
00	3	287.7 to 315
01	2	431.5 to 472.5
10	Not used	N/A
11	1	863 to 945

Figure 15 illustrates the synthesizer operation in Tx ASK mode, where the Tx carrier frequency is static. For Tx FSK applications, where the frequency of the carrier alternates between the space frequency and the mark frequency based on the Datain input, the IC includes a frequency waveshaping function that allows the user to control the spectral width of the transmit signal.

Tx FSK Mode Using Frequency Waveshaping

The inputs to the waveshaping function are illustrated in Figure 16. In this mode, the wsoff bit (TxConf0 register, 0x0C, bit 6) is cleared and the wsmlt[1:0] bits (TxConf1 register, 0x0D, bits 7:6) are cleared. The base[20:0] bits set the divider ratio for the lowest (space) frequency and base1[20:0] corresponds to the divider ratio for the highest (mark) frequency. On the rising edge of the Datain signal, the input to the fractional-N divider transitions between base[20:0] and base1[20:0] in 20 discrete steps, as defined by the tstep[7:0] bits (TxTstep register, 0x0E, bits 7:0) and the shpnn[7:0] bits (Shape00–Shape18 registers, 0x0F–0x21, bits 7:0, where nn = 00 to 18), as shown in Figure 17.

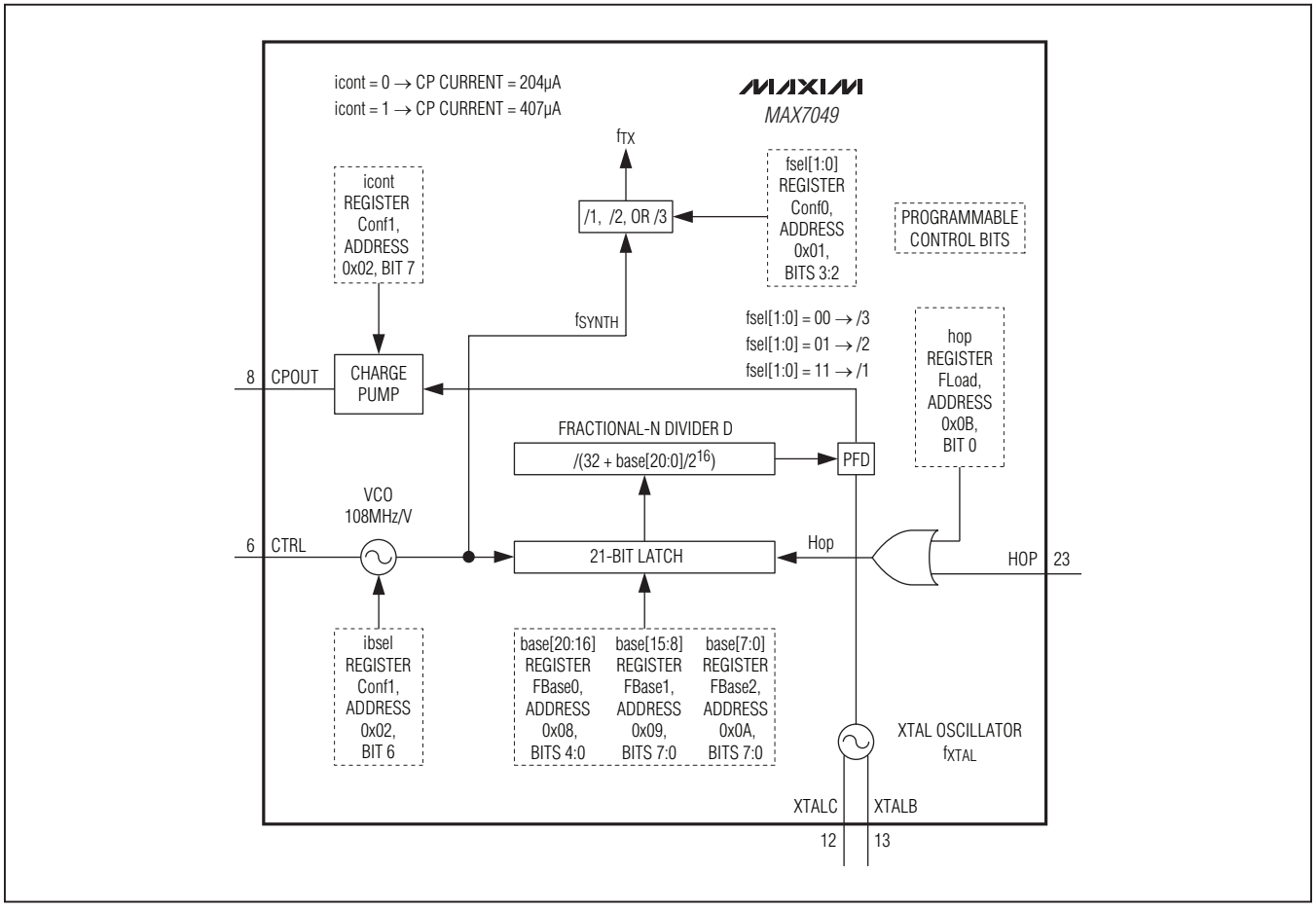


Figure 15. Fractional-N Synthesizer Configuration Tx ASK Mode

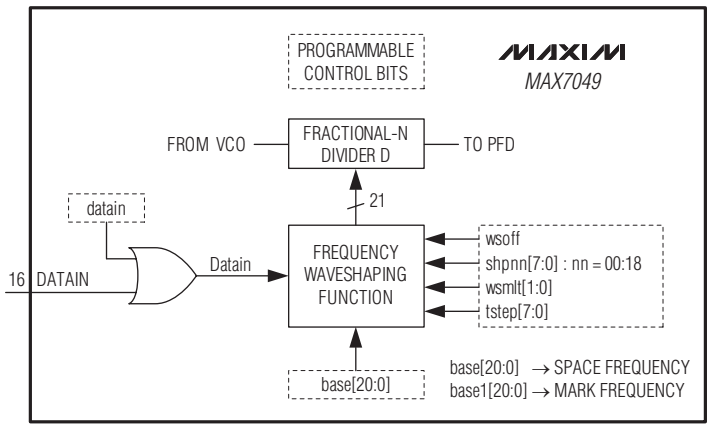


Figure 16. Tx FSK Mode Programming

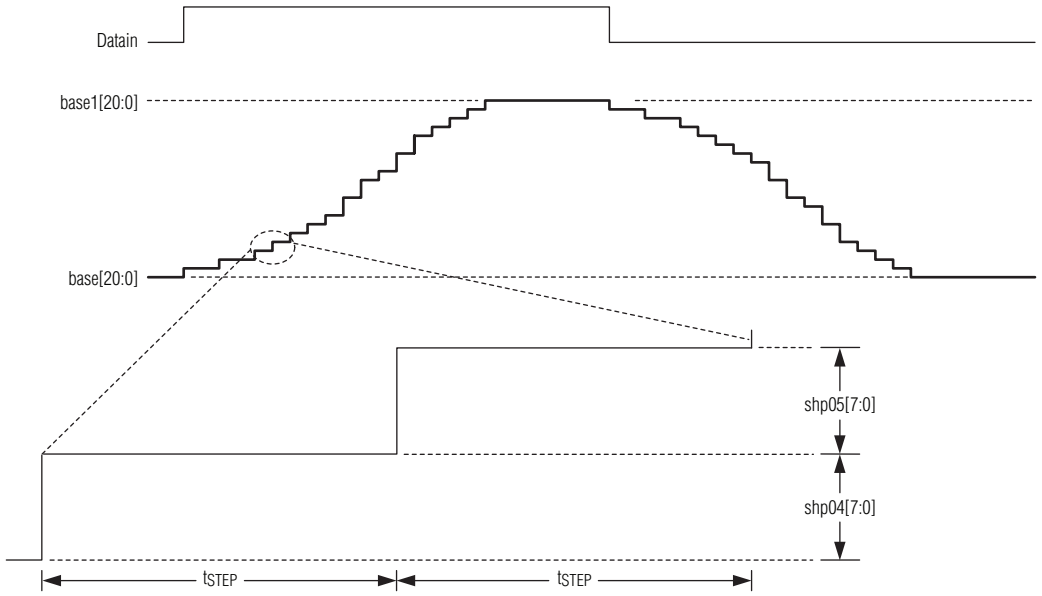


Figure 17. Tx FSK Frequency Waveshaping Timing Diagram

The 21-bit divider word is updated at a rate defined by the tstep[7:0] bits, and this update time step is given by:

$$t_{STEP} = tstep[7:0]/mclk$$

In terms of the shpnn[7:0] bits, the value of base1[20:0] is therefore:

$$base1[20:0] = base[20:0] + \sum_{nn=00}^{nn=18} shpnn[7:0]$$

As Figure 17 illustrates, the frequency ramp-down shape is the inverse, not the mirror image, of the frequency ramp-up shape. The frequency deviation, which is the difference between the mark frequency and the space frequency, can also be expressed in terms of the shpnn[7:0] bits:

$$\text{frequency deviation} = f_{XTAL}/2^{16} \times \sum_{nn=00}^{nn=18} shpnn[7:0]$$

The waveshaping function allows for the approximation of any monotonic-shape characteristic. An example of the waveshaping function is the approximation of a 2kbps NRZ with linear ramp shaping of duration at a 1/2 bit interval and deviation of 50kHz. The length of the ramp time is 250µs. With a 3.2MHz mclk, a decimal value of 40 (0x28) is required for the tstep[7:0] SPI bits because each of the time steps would need to be 12.5µs, and 40 x 0.3125µs yields 12.5µs. This requires a decimal value of 11 (0xB) for the shpnn[7:0] bits if used with a 16MHz crystal. In this case the deviation is 19 (# of frequency steps) x 11 (frequency change per step) x 16,000,000/2^{16} or 51.03kHz. To attain a value closer to 50kHz at the expense of linearity, four of the Shape00–Shape18 register values could have been set to decimal 10 (0xA). This results in a deviation of 205 x 16,000,000/2^{16} or 50.05kHz. The maximum programmable deviation (not typically used with companion receivers due to bandwidth limitations) in this mode with a 16.0MHz crystal is 19 x 255 x 16,000,000/2^{16} or 1.18MHz.

Tx Pulse FSK Mode

In this mode, the wsoff bit (TxConf0 register, 0x0C, bit 6) is set and the wsmlt[1:0] bits (TxConf1 register, 0x0D, bits 7:6) are used to transition directly from the space frequency to the mark frequency without the use of shaping. The value of base1[20:0] is expressed as:

$$base1[20:0] = base[20:0] + wsm \times shp00[7:0]$$

where wsm is a multiplier whose value is given in Table 8.

This mode of pulsed FSK might offer slightly better range when compared to shaped FSK at the expense of a higher occupied bandwidth. A waveshaping function is also available in Tx ASK mode. This feature is documented in the *Power Amplifier* section.

Loop Bandwidth

The required loop bandwidth of the fractional-N synthesizer is dependent on the required phase noise characteristics of the transmitted carrier signals, the required frequency settling times, the FSK modulation rates, and the current consumption.

Three components dominate the phase noise of the fractional-N synthesizer output: close-in phase noise, VCO phase noise, and fractional quantization phase noise. The loop bandwidth and filter order can be set to meet the requirements for a wide range of applications due to the low close-in phase noise (for excellent performance at wide-loop bandwidths) and low VCO phase noise (for excellent performance at narrow-loop bandwidths). The loop filter order can be increased to lessen the effect of fractional quantization phase noise for wide-loop bandwidths if necessary.

Table 8. Tx FSK Pulse Mode Frequency Multiplier Values

wsmlt[1:0] TxConf1 REGISTER, ADDRESS 0x0D, BITS 7:6	wsm
00	1
01	2
10	4
11	8

Generally, a 100kHz loop bandwidth works for most applications. This choice allows for fast settling times, within typically 48µs for less than 5kHz offset during a 26MHz step in the 902MHz to 928MHz ISM band. This loop bandwidth is near the optimum for minimizing the contributions of both close-in phase noise and VCO phase noise. In addition, this choice allows for FSK modulation rates up to 160kbps NRZ and 80kbps Manchester for most applications. If the phase noise at higher offset frequencies needs to be reduced, the loop bandwidth can be lowered to allow for the VCO noise to dominate the phase-noise profile completely.

The loop filter components can be calculated as follows:

$$R = (2 \times \pi \times D \times BW)/(I_{CP} \times K_{VCO})\Omega$$

where:

R is the loop filter resistor in Ω.

D is the frequency division ratio of the feedback divider of the fractional-N synthesizer.

BW is the desired fractional-N synthesizer loop bandwidth in Hz.

I_{CP} is the charge-pump current in A.

K_{VCO} is the VCO gain at the synthesizer output frequency (863MHz to 945MHz) in Hz/V.

$$C_L = (\sqrt{10})/(2 \times \pi \times R \times BW) \text{ in F}$$

where:

C_L is the large-loop filter capacitor in series with R.

R is the loop filter resistor in Ω.

BW is the desired fractional-N synthesizer loop bandwidth in Hz.

The value of 10 is approximate.

$$C_S = 1/(2 \times \pi \times R \times BW \times (\sqrt{10})) \text{ in F}$$

where:

C_S is the small-loop filter capacitor in parallel with the series combination of R and C_L.

R is the loop filter resistor in Ω.

BW is the desired fractional-N synthesizer loop bandwidth in Hz.

The value of 10 is approximate.

An additional RC pole can be added to the loop filter to remove more fractional quantization phase noise at wide-loop bandwidths. This pole is added between the CPOUT pin and the CTRL pin. The resistance of the RC pole should be 1.5x the value of the loop filter resistor to limit loading while minimizing thermal noise as a phase-noise contributor. The pole frequency should be greater than ten times the loop bandwidth. The loop filter configuration is shown in Figure 18.

Lock Detector

The primary support circuit for the fractional-N synthesizer is the lock detector. The internal lock-detect signal is a gate for transmitter operation as illustrated in the *Operating Mode Overview* section. The lock-detect signal itself is adequate for most operating conditions, but additional delay can be added if this signal is asserted too quickly, such that it does not allow the synthesizer to settle to within the desired frequency accuracy as illustrated in Figure 19.

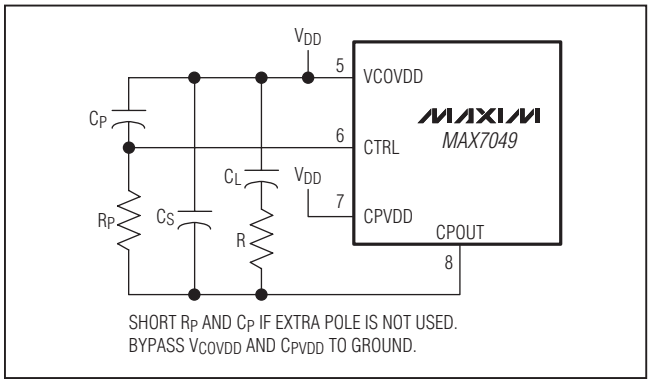


Figure 18. Synthesizer Loop Filter Topology

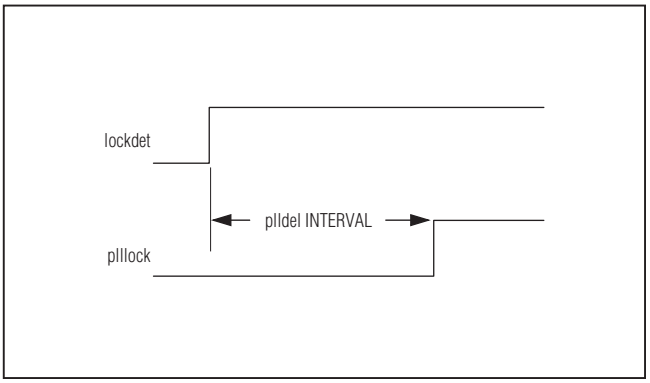


Figure 19. Lock Detector Delay Function

The additional delay interval is set by the plldl[2:0] bits (Conf1 register, 0x02, bits 5:3), and this delay is given by:

plldel interval = plldl[2:0] x (64/mclk)s

where plldl[2:0] is the decimal equivalent of the bits, yielding a norminal (3.2MHz mclk) plldel interval from 0 to 140µs. Both the lockdet and plllock status signals are available on SDO, GPO1, and GPO2, as described in the *Register Details* section for the TestBus0 and TestBus1 registers.

Power Amplifier

The IC contains a programmable current-drain, high-efficiency power amplifier (PA). The PA is a differential output stage capable of delivering more than +15dBm to a 50Ω load including the losses of the matching network and harmonic filter. The bias current for the PA (IPA) is configurable in 64 linear steps, as illustrated in Figure 20.

An external resistor (R_{EXT}) is placed between the REXTPA pin and ground. This resistor, along with an on-chip reference voltage of 1.13V, sets the reference current (IR). This resistor should be placed as close as possible to the IC to minimize the capacitance on this node. A temperature-stable, high-tolerance ±1% resistor is recommended to minimize variations in output power. An on-chip current multiplier of 25 x IR determines the LSB of the PA bias DAC. For example, a 56.2kΩ resistor sets the LSB to 0.5mA. The palopwr bit (TxConf0 register, 0x0C, bit 7) controls the bias current in the PA buffer amplifier. When this bit is set, it lowers the buffer bias current by 2mA for low-power applications. The buffer amplifier sets the pedestal voltage (V_P), which is required for sufficient PA bias DAC headroom.

The function of the matching network is to transform the load resistance (R_L) to the differential optimal PA load resistance (R_{OPT}). The value of R_{OPT} is determined by the desired output power (P_D), the loss of the matching network (Lm), the supply voltage (V_{DD}), and the pedestal voltage (V_P). Table 9 illustrates a design example for determining R_{OPT} and IPA_peak, where IPA_peak is the peak value of the DC current.

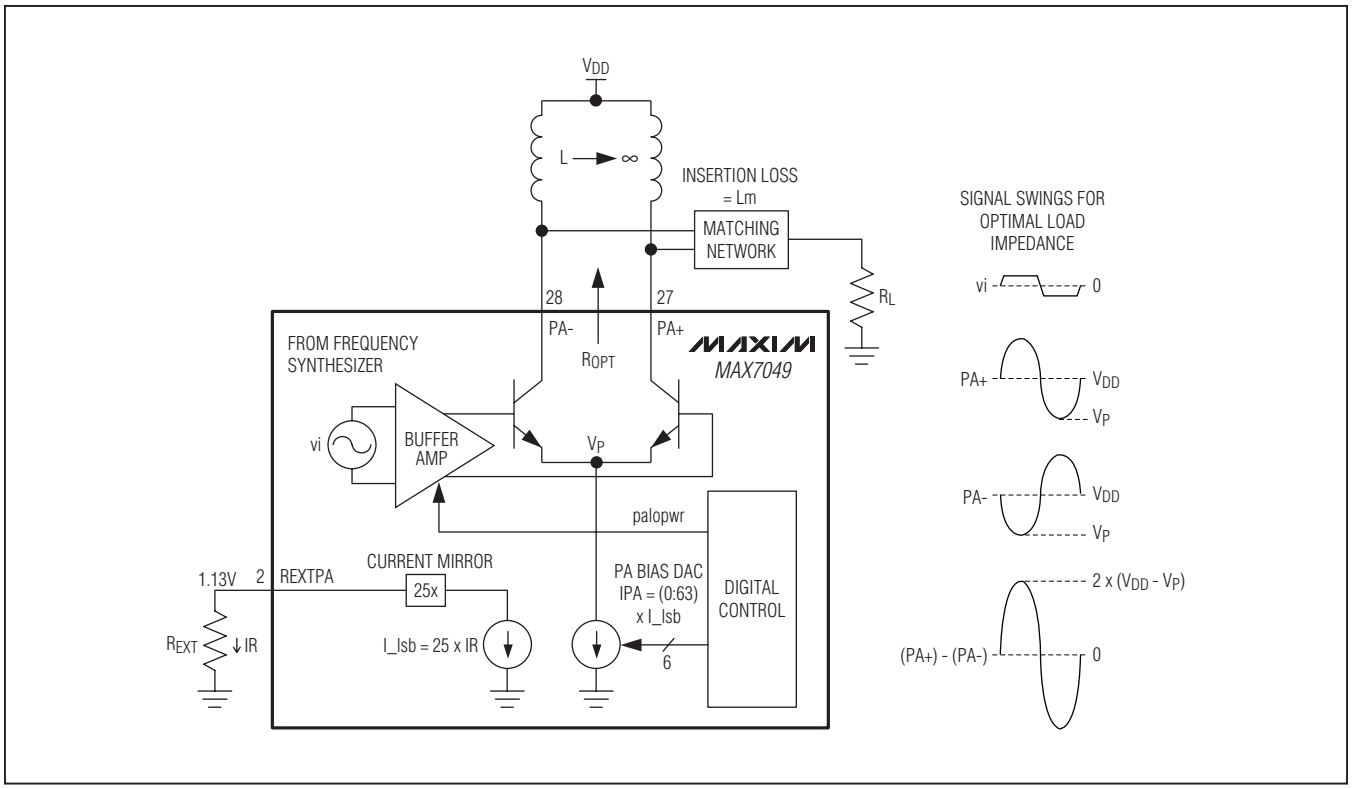


Figure 20. Power Amplifier Topology and Optimum Signal Swings

The maximum efficiency of an ideal differential output stage is $2/\pi$ and this must also be adjusted by the factor $(V_{DD} - V_P)/V_{DD}$ to account for the headroom required for the PA bias DAC current source. Note that an unbalanced differential impedance, as seen by the PA output pins, causes different clipping levels for the PA+ pin vs. the PA- pin. This degrades efficiency. In addition, if the matching network does not transform the load resistance to a differential impedance whose value is exactly R_{OPT} + j0, then this mismatch loss further degrades the efficiency. In this PA design example, if the PA bias current switched from zero to IPA_peak with the data input in ASK mode, the occupied bandwidth of the modulated signal would be significant. The IC includes an amplitude waveshaping function to reduce the occupied bandwidth of ASK modulation.

Table 9. PA Design Example

PARAMETER	SYMBOL AND/OR EQUATION	EXAMPLE VALUE
Supply Voltage	V_{DD}	3V
Pedestal Voltage	V_P	0.5V
External PA Bias Resistance	R_{EXT}	56.2kΩ
PA Bias DAC LSB	$I\_lsb = 25 \times 1.13/R_{EXT}$	0.5mA
Desired Peak RF Output Power	P_D	14dBm
Harmonic Filter and Composite Matching/Combiner Network Loss	Lm	2dB
Actual PA RF Output Power	$P_{PA} = P_L + Lm$	16dBm
Actual PA RF Output Power	$P_{PA\_mW} = 10^{(P_{PA}/10)}$	40mW
Required PA DC Power	$P_{DC} = P_{PA\_mW} \times \pi/2 \times V_{DD}/(V_{DD} - V_P)$	75mW
Maximum PA Efficiency	Maximum efficiency = $100 \times 2/\pi \times (V_{DD} - V_P)/V_{DD}$	53%
Composite PA Efficiency (includes Matching Network Loss)	Efficiency = $100 \times 10^{(P_D/10)}/P_{DC}$	33%
Required Peak DC Current	$IPA\_peak = P_{DC}/V_{DD}$	25mA
PA Code for Desired Power	idac_peak[5:0]	50 decimal (0x32)

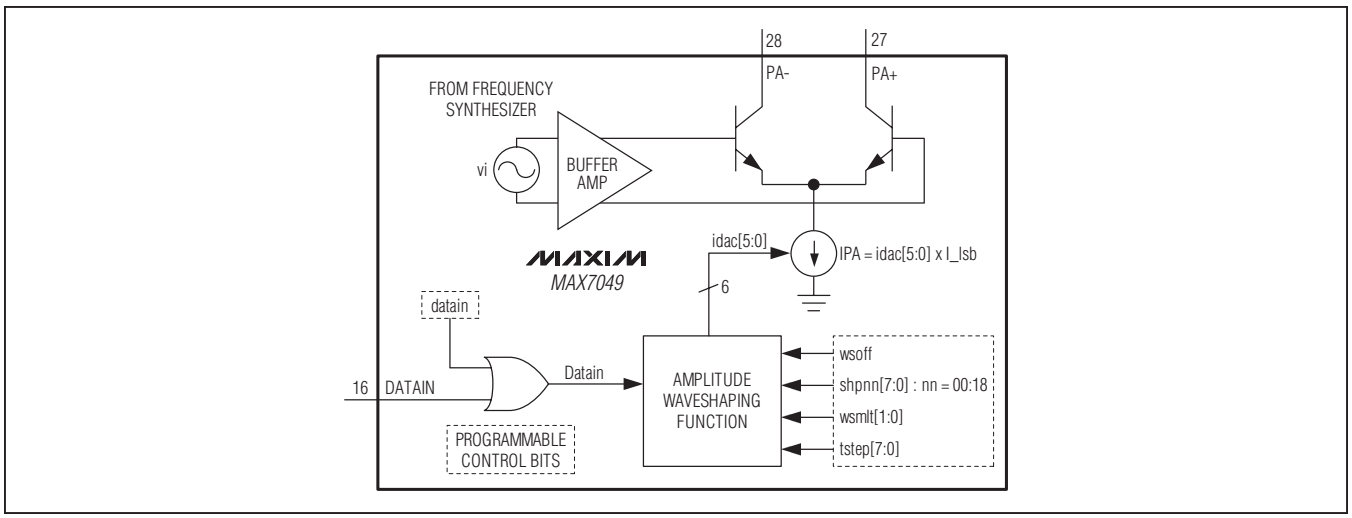


Figure 21. Tx ASK Mode Programming

Tx ASK Mode Using Amplitude Waveshaping

The ASK waveshaping function is illustrated in Figure 21.

In this mode, the wsoff bit (TxConf0 register, 0x0C, bit 6) is cleared and the wsmlt[1:0] bits (TxConf1 register, 0x0D, bits 7:6) are cleared. After txready is high, the PA transitions from zero bias current to IPA_peak, on the rising edge of the Datain signal. This transition occurs in 20 discrete steps, determined by the tstep[7:0] bits (TxTstep register, 0x0E, bits 7:0) and the shpnn[7:0] bits (Shape00–Shape18 registers, 0x0F–0x21, bits 7:0, where nn = 00 to 18), as shown in Figure 22.

The PA DAC word is updated at a rate defined by the tstep[7:0] bits, and this update time step is given by:

$$t_{STEP} = tstep[7:0]/mclk$$

In terms of the shpnn[7:0] bits, the value of idac_peak[5:0] is therefore:

$$idac\_peak[5:0] = \sum_{nn=00}^{nn=18} shpnn[7:0]$$

The two most-significant bits of shpnn[7:0] should always be zero in ASK mode. As Figure 22 illustrates, the ramp-down shape is the inverse of the ramp-up shape. The waveshaping function allows for the approximation of any monotonic shape characteristic. Since the shpnn registers are 8 bits wide, the PA can be pulsed from zero current to the maximum bias current in one time step if desired.

An example is the approximation of a 4kbps NRZ with linear ramp shaping of 1/2 bit interval duration and peak PA bias current of 10mA using R_{EXT} = 56.2kΩ. The length of the ramp time is 125µs. With a 3.2MHz mclk, this requires a decimal value of 20 (0x14) for the tstep[7:0] because each of the 20 time steps would need to be 6.25µs, and 20 x 0.3125µs yields 6.25µs. This requires a decimal value of 1 (0x1) for each Shape00–Shape18 register. In this case, the peak PA bias current is 19 x 25 x 1.13/56,200, or 9.55mA. To attain a value closer to 10mA at the expense of linearity, one of the Shape00–Shape18 register values could have been set to decimal 2 (0x2). This results in a peak PA bias current of 20 x 25 x 1.13/56,200, or 10.05mA.

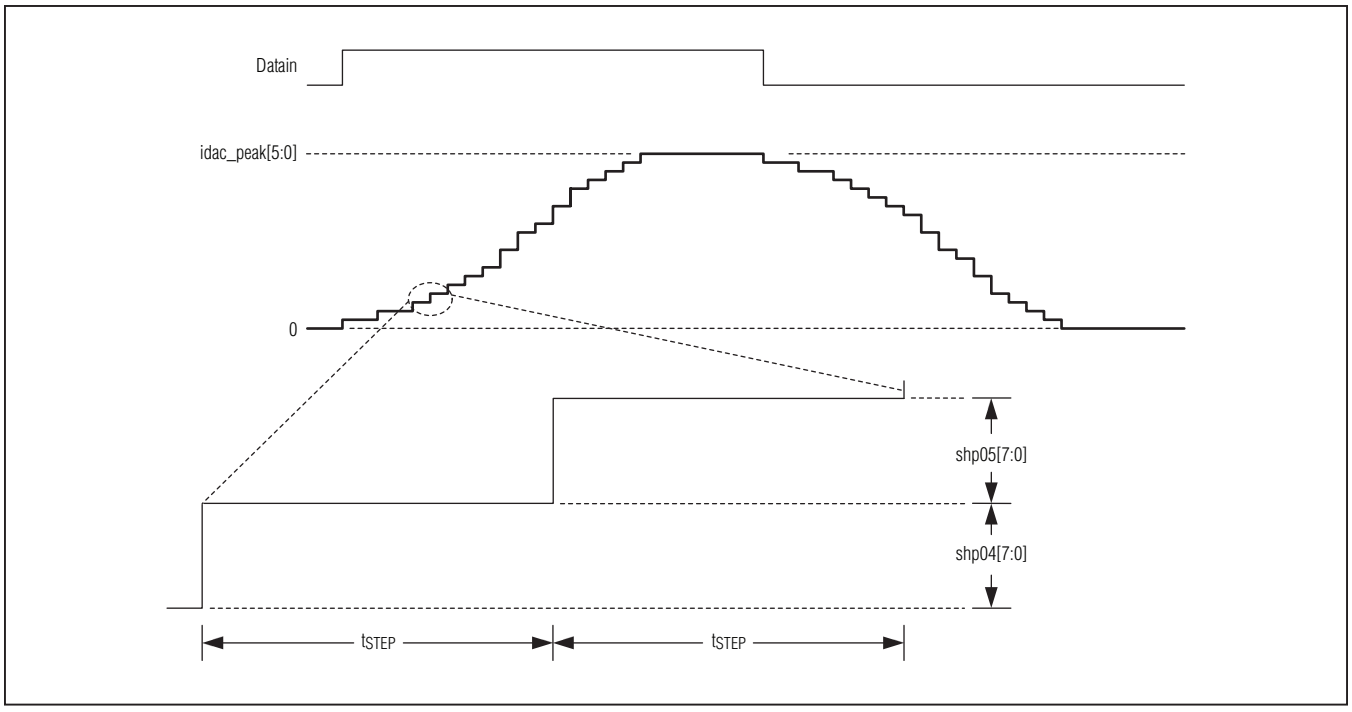


Figure 22. ASK Waveshaping Timing Diagram

Tx FSK Mode Amplitude Ramp

In Tx FSK mode, the carrier is modulated by the frequency-shaping function, as defined in the *Fractional-N Synthesizer* section. This frequency waveshaping is designed to minimize the occupied bandwidth of the transmit signal in Tx FSK mode. However, the occupied bandwidth might degrade if the PA turns on and off abruptly at the beginning and end of a burst. A PA amplitude ramp feature is available in Tx FSK mode to prevent the degradation of the occupied bandwidth. This feature is illustrated in Figure 23.

After the IC is enabled and the txready signal transitions high, the PA bias current ramps up linearly to the value fska[5:0] (TxConf0 register, 0x0C, bits 5:0) x I_lsb in increments of fskas[5:0] (TxConf1 register, 0x0D, bits 5:0) x I_lsb, as illustrated in Figure 24.

Similarly, the PA bias current ramps down linearly on the falling edge of the enable signal. Note that this PA ramp feature is also automatically invoked when hopping from one channel to another channel, as defined in the *Fractional-N Synthesizer section*.

The PA DAC word is updated at a rate defined by the tstep[7:0] bits, and this update time step is given by:

$$t_{STEP} = tstep[7:0]/mclk$$

To transmit the entire message at the desired power level, the user should wait until the PA ramp is completed before initiating the data sequence.

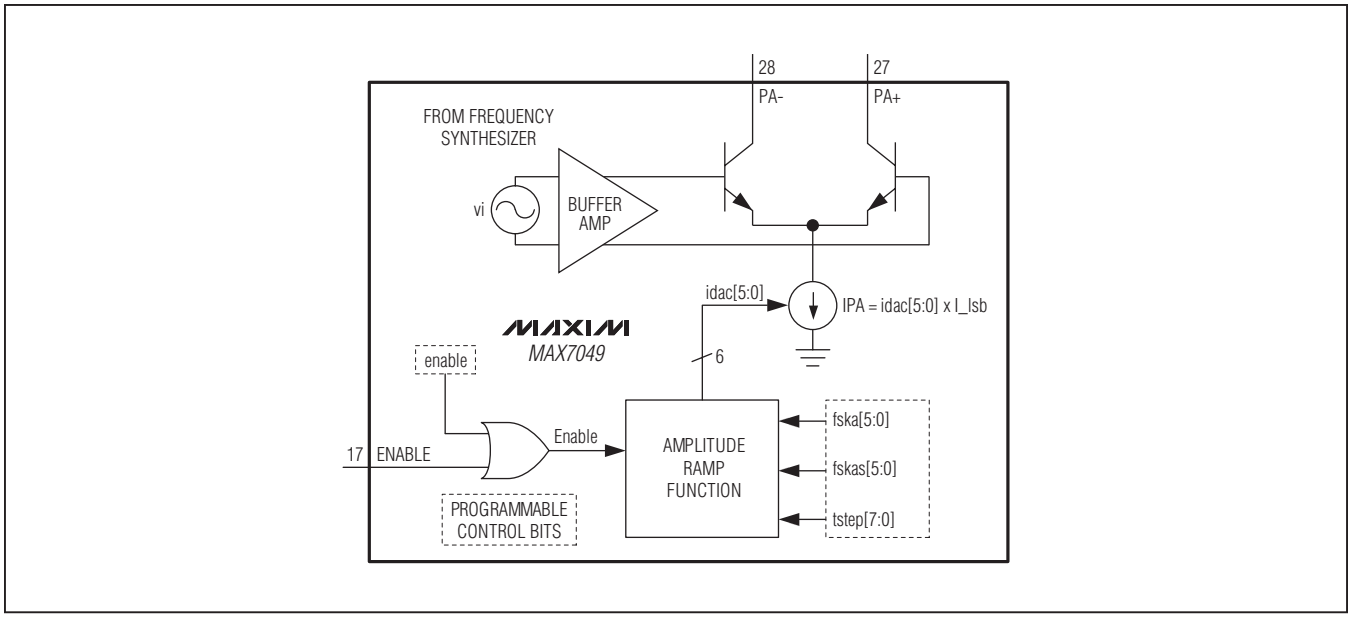


Figure 23. Tx FSK Amplitude Ramp Feature

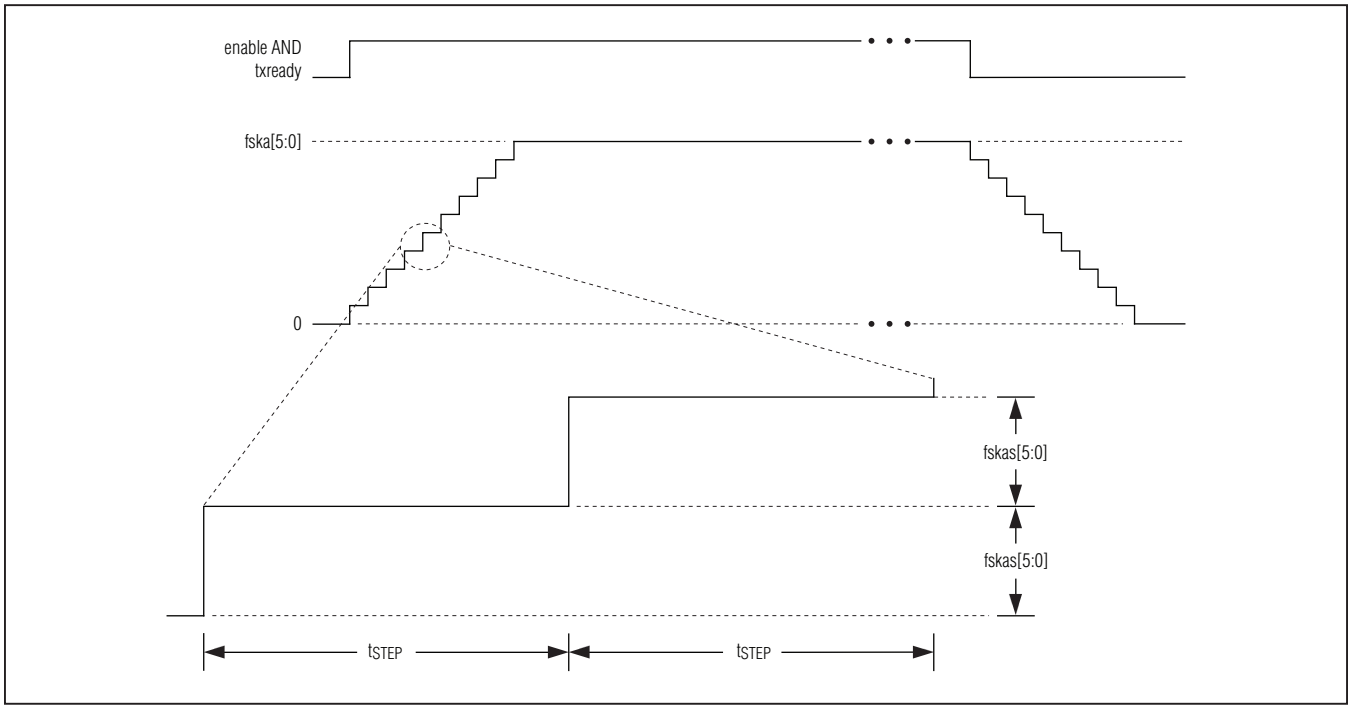


Figure 24. Tx FSK Amplitude Ramp Timing Diagram

Register Details

Table 10. Configuration Register Map

GROUP/FUNCTION		HEX	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	Ident	0x00	1	0	1	0	0	1	1	1
1	Conf0	0x01	—	—	—	mode	fsel_1	fsel_0	xtal_1	xtal_0
	Conf1	0x02	icont	ibsel	plldl_2	plldl_1	plldl_0	—	—	—
2	IOConf0	0x03	gp1isht	gp2isht	ckdiv_1	ckdiv_0	gp2s_3	gp2s_2	gp2s_1	gp2s_0
	IOConf1	0x04	sdos_3	sdos_2	sdos_1	sdos_0	gp1s_3	gp1s_2	gp1s_1	gp1s_0
	IOConf2	0x05	—	—	gp1md_1	gp1md_0	clksht	gp2md_2	gp2md_1	gp2md_0
3	FBase0	0x08	—	—	—	base_20	base_19	base_18	base_17	base_16
	FBase1	0x09	base_15	base_14	base_13	base_12	base_11	base_10	base_9	base_8
	FBase2	0x0A	base_7	base_6	base_5	base_4	base_3	base_2	base_1	base_0
	FLoad	0x0B	—	—	—	—	—	—	—	hop
4	TxConf0	0x0C	palopwr	wsoff	fska_5	fska_4	fska_3	fska_2	fska_1	fska_0
	TxConf1	0x0D	wsmlt_1	wsmlt_0	fskas_5	fskas_4	fskas_3	fskas_2	fskas_1	fskas_0
	TxTstep	0x0E	tstep_7	tstep_6	tstep_5	tstep_4	tstep_3	tstep_2	tstep_1	tstep_0

Table 10. Configuration Register Map (continued)

GROUP/FUNCTION		HEX	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
5	Shape00	0x0F	shp00_7	shp00_6	shp00_5	shp00_4	shp00_3	shp00_2	shp00_1	shp00_0
	Shape01	0x10	shp01_7	shp01_6	shp01_5	shp01_4	shp01_3	shp01_2	shp01_1	shp01_0
	Shape02	0x11	shp02_7	shp02_6	shp02_5	shp02_4	shp02_3	shp02_2	shp02_1	shp02_0
	Shape03	0x12	shp03_7	shp03_6	shp03_5	shp03_4	shp03_3	shp03_2	shp03_1	shp03_0
	Shape04	0x13	shp04_7	shp04_6	shp04_5	shp04_4	shp04_3	shp04_2	shp04_1	shp04_0
	Shape05	0x14	shp05_7	shp05_6	shp05_5	shp05_4	shp05_3	shp05_2	shp05_1	shp05_0
	Shape06	0x15	shp06_7	shp06_6	shp06_5	shp06_4	shp06_3	shp06_2	shp06_1	shp06_0
	Shape07	0x16	shp07_7	shp07_6	shp07_5	shp07_4	shp07_3	shp07_2	shp07_1	shp07_0
	Shape08	0x17	shp08_7	shp08_6	shp08_5	shp08_4	shp08_3	shp08_2	shp08_1	shp08_0
	Shape09	0x18	shp09_7	shp09_6	shp09_5	shp09_4	shp09_3	shp09_2	shp09_1	shp09_0
	Shape10	0x19	shp10_7	shp10_6	shp10_5	shp10_4	shp10_3	shp10_2	shp10_1	shp10_0
	Shape11	0x1A	shp11_7	shp11_6	shp11_5	shp11_4	shp11_3	shp11_2	shp11_1	shp11_0
	Shape12	0x1B	shp12_7	shp12_6	shp12_5	shp12_4	shp12_3	shp12_2	shp12_1	shp12_0
	Shape13	0x1C	shp13_7	shp13_6	shp13_5	shp13_4	shp13_3	shp13_2	shp13_1	shp13_0
	Shape14	0x1D	shp14_7	shp14_6	shp14_5	shp14_4	shp14_3	shp14_2	shp14_1	shp14_0
	Shape15	0x1E	shp15_7	shp15_6	shp15_5	shp15_4	shp15_3	shp15_2	shp15_1	shp15_0
	Shape16	0x1F	shp16_7	shp16_6	shp16_5	shp16_4	shp16_3	shp16_2	shp16_1	shp16_0
	Shape17	0x20	shp17_7	shp17_6	shp17_5	shp17_4	shp17_3	shp17_2	shp17_1	shp17_0
	Shape18	0x21	shp18_7	shp18_6	shp18_5	shp18_4	shp18_3	shp18_2	shp18_1	shp18_0
6	TestMux	0x3C	—	—	—	—	tmux_3	tmux_2	tmux_1	tmux_0
	Datain	0x3D	—	datain	—	—	—	—	—	—
	EnableReg	0x3E	—	—	—	—	tsensor	—	—	enable
7	TestBus0	0x40	tbus_15	tbus_14	tbus_13	tbus_12	tbus_11	tbus_10	tbus_9	tbus_8
	TestBus1	0x41	tbus_7	tbus_6	tbus_5	tbus_4	tbus_3	tbus_2	tbus_1	tbus_0
	Status0	0x42	txready	—	adcrdy	—	gpo1out	plllock	lockdet	ckalive
	Status1	0x43	—	—	—	tsdone	—	—	—	—

"—" Denotes a reserved bit. If a register contains reserved bits, write 0 to the reserved bit content.
Register 0x00 contents are always 0xA7, and can be used to identify the IC on the SPI bus.
Registers 0x40 through 0x43 are read-only registers, containing various states and status that can be read through the SPI.

Table 11. Group 0: Identification Register (Ident)

GROUP/FUNCTION		HEX	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	Ident	0x00	1	0	1	0	0	1	1	1

Table 12. Ident Register (0x00)

BIT	NAME	FUNCTION
7:0	ident[7:0]	Read-only register used for identification purposes. The content of this register is always 0xA7.

Table 13. Group 1: General Configuration Registers (Conf0, Conf1)

GROUP/FUNCTION		HEX	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
1	Conf0	0x01	—	—	—	mode	fsel_1	fsel_0	xtal_1	xtal_0
	Conf1	0x02	icont	ibsel	plldl_2	plldl_1	plldl_0	—	—	—

Table 14. Conf0 Register (0x01)

BIT	NAME	FUNCTION
4	mode	1-bit configuration for transmit mode: 0 = ASK 1 = FSK
3:2	fsel[1:0]	2-bit configuration for LO division ratio: 00 3 01 2 10 Not used 11 1
1:0	xtal[1:0]	2-bit crystal divider configuration. Based on a typical crystal selection of 16.0MHz, 19.2MHz, or 22.4MHz, these bits are usually configured to yield a constant 3.2MHz mclk frequency for timing control and driving characteristics of the digital section of the IC. For data rates up to 200kbps, an mclk frequency of up to 4.0MHz is needed. The typical settings are: Crystal xtal[1:0] 16.0MHz 00 Divide by 5 (16.0/5 = 3.2MHz) 19.2MHz 01 Divide by 6 (19.2/6 = 3.2MHz) 22.4MHz 10 Divide by 7 (22.4/7 = 3.2MHz) 20.0MHz 00 Divide by 5 (20.0/5 = 4.0MHz) 11 Divide by 8

Table 15. Conf1 Register (0x02)

BIT	NAME	FUNCTION
7	icont	Selects between low current (0 = 204µA) and high current (1 = 407µA) modes for the synthesizer charge pump, allowing for lower noise operation with the expense of extra current.
6	ibsel	Selects between low VCO core current and high VCO core current (1 = additional 1mA) in the synthesizer.
5-3	plldl[2:0]	3-bit configuration for extra delay after lock-detect flag (lockdet) from the synthesizer is asserted (assuming mclk = 3.2MHz): plldl[2:0] delay(µs) 000 0 001 20 010 40 011 60 100 80 101 100 110 120 111 140 After this delay, an internal signal called plllock is asserted high to determine the digital lock flag for the synthesizer.

Table 16. Group 2: GPO, Data Output, and Clock Output Registers (IOConf0, IOConf1, IOConf2)

GROUP/FUNCTION		HEX	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
2	IOConf0	0x03	gp1isht	gp2isht	ckdiv_1	ckdiv_0	gp2s_3	gp2s_2	gps2_1	gps2_0
	IOConf1	0x04	sdos_3	sdos_2	sdos_1	sdos_0	gp1s_3	gp1s_2	gp1s_1	gp1s_0
	IOConf2	0x05	—	—	gp1md_1	gp1md_0	clksht	gp2md_2	gp2md_1	gp2md_0

Table 17. IOConf0 Register (0x03)

BIT	NAME	FUNCTION
7	gp1isht	GPO1 current mode during sleep. If the IC GPO1 is configured to current drive mode (IOConf2 register, 0x05), writing 1 to this bit allows for the current mode operation even if the IC is in Sleep mode or disabled. If this bit is 0, current mode operation is only active when the IC is enabled.
6	gp2isht	GPO2 current mode during sleep. If the IC GPO2 is configured to current drive mode (IOConf2 register, 0x05), writing 1 to this bit allows for the current mode operation even if the IC is in Sleep mode or disabled. If this bit is 0, current mode operation is only active when the IC is enabled.
5:4	ckdiv[1:0]	2-bit configuration for clock output divider setting. A clock source selected by gp2s[3:0] is divided by the settings in these bits, according to the following: ckdiv[1:0] Divide by 00 1 01 2 10 4 11 8
3:0	gp2s[3:0]	4-bit configuration for GPO2 signal selection: gp2s[3:0] Output 0000 plllock 0001 mclk/(ckdiv divider) 0010 xtal/(ckdiv divider) 0011 xtal/16/(ckdiv divider) 0100 tbus[4] 0101 tbus[5] 0110 tbus[6] 0111 tbus[7] 1000 tbus[8] 1001 tbus[9] 1011 tbus[10] 1100 tbus[11] 1101 tbus[12] 1110 tbus[14] 1111 tbus[15] where: mclk is the master digital clock generated from the crystal divider block (xtal[1:0]); xtal is the crystal oscillator output clock; xtal/16 is a divided-by-16 version of the crystal oscillator frequency; tbus[15:0] is the 16-bit bus selected by tmux[3:0] (TestMux register, 0x3C, bits 3:0).

Table 18. Register IOConf1 (0x04)

<table>
<tr><th>BIT</th><th>NAME</th><th>FUNCTION</th></tr>
<tr><td>7:4</td><td>sdos[3:0]</td><td>4-bit SPI data output GPO mode selection. When $\overline{CS}$ is low, the SDO pin outputs the SPI data output, as described in the Serial Peripheral Interface (SPI) section. When $\overline{CS}$ is high, the SDO acts as a third GPO, according to:
<table>
<tr><th>$\overline{CS}$</th><th>sdos[3]</th><th>sdos[2]</th><th>sdos[1]</th><th>sdos[0]</th><th>output</th></tr>
<tr><td>0</td><td>x</td><td>x</td><td>x</td><td>x</td><td>SPI_Dout</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>tbus[0]</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>tbus[1]</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>tbus[2]</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>tbus[3]</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>tbus[4]</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>tbus[5]</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>tbus[6]</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>tbus[7]</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>tbus[8]</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>tbus[9]</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>tbus[10]</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>tbus[11]</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>tbus[12]</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>tbus[13]</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>tbus[14]</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>tbus[15]</td></tr>
</table>
tbus[15:0] is the 16-bit bus selected by tmux[3:0] (TestMux register, 0x3C, bits 3:0).</td></tr>
<tr><td>3:0</td><td>gp1s[3:0]</td><td>4-bit configuration for GPO1 signal selection:
<table>
<tr><th>gp1s[3]</th><th>gp1s[2]</th><th>gp1s[1]</th><th>gp1s[0]</th><th>output</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>tbus[0]</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>tbus[1]</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>tbus[2]</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>tbus[3]</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>tbus[4]</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>tbus[5]</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>tbus[6]</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>tbus[7]</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>tbus[8]</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>tbus[9]</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>tbus[10]</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>tbus[11]</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>tbus[12]</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>tbus[13]</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>tbus[14]</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>tbus[15]</td></tr>
</table>
tbus[15:0] is the 16-bit bus selected by tmux[3:0] (TestMux register, 0x3C, bits 3:0).</td></tr>
</table>

Table 19. Register IOConf2 (0x05)

BIT	NAME	FUNCTION
5:4	gp1md[1:0]	2-bit GPO1 mode selection: 0x buffer mode 10 80µA current mode 11 160µA current mode
3	clksht	Enable (1) or disable (0) clock output on GPO2 during sleep.
2:0	gp2md[2:0]	3-bit GPO2 mode selection. The GPO2 can provide a high-frequency clock output, and therefore its current capability is higher. 0xx buffer mode 100 1.0mA 101 2.0mA 110 3.0mA 111 4.0mA

Table 20. Group 3: Synthesizer Frequency Settings (FBase0, FBase1, FBase2, FLoad)

GROUP/FUNCTION		HEX	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	FBase0	0x08	—	—	—	base_20	base_19	base_18	base_17	base_16
	FBase1	0x09	base_15	base_14	base_13	base_12	base_11	base_10	base_9	base_8
	FBase2	0x0A	base_7	base_6	base_5	base_4	base_3	base_2	base_1	base_0
	FLoad	0x0B	—	—	—	—	—	—	—	hop

Registers 0x08, 0x09, and 0x0A set the 21-bit base value for the control of the synthesizer frequency. Bits 20:16 form the 5-bit integer part (base[20:16]), and bits 15:0 form the 16-bit fractional part (base[15:0]).

The synthesizer frequency is then given by:

$$f_{SYNTH} = f_{XTAL} \times (32 + base[20:0]/65,536)$$

where f_{XTAL} is the crystal frequency in MHz. The synthesizer frequency is then divided according to the fsel[1:0] settings (Conf0 register, 0x01, bits 3:2) to generate the LO frequency:

Table 21. Synthesizer Divider Settings

fsel[1:0]	LO DIVIDER
00	3
01	2
11	1

The synthesizer frequency range is from 863MHz to 945MHz, which translates to the base[20:0] values shown in Table 22.

Table 22. Synthesizer Programming Values

CRYSTAL (MHz)	$SYNTH_F$ (MHz)	MULTIPLIER FACTOR (dec)	base[20:0]
16.0	863	21.9375	0x15F000
	945	27.0625	0x1B1000
19.2	863	12.9479	0x0CF2AB
	945	17.2188	0x113800
22.4	863	6.5268	0x0686DB
	945	10.1875	0x0A3000
20	863	11.1500	0x0B2666
	945	15.2500	0x0F4000

The minimum and maximum frequency for each band is shown in Table 23.

Table 23. Frequency Ranges

$SYNTH_F$ (MHz)	300MHz (fsel = 00)	450MHz (fsel = 01)	900MHz (fsel = 11)
863	287.70	431.50	863.00
945	315.00	472.50	945.00

The hop bit allows for a parallel load of the three FBase registers. This is a self-reset bit that reverts to 0 when the operation is completed. This function can also be accomplished by use of the external HOP pin. A detailed description of the hop operation can be found in the appropriate sections of the transmitter detailed operations descriptions.

Table 24. FBase0 Register (0x08)

BIT	NAME	FUNCTION
4:0	base[20:16]	5-bit integer value for synthesizer.

Table 25. FBase1 Register (0x09)

BIT	NAME	FUNCTION
7:0	base[15:8]	8 MSBs of fractional value for synthesizer.

Table 26. FBase2 Register (0x0A)

BIT	NAME	FUNCTION
7:0	base[7:0]	8 LSBs of fractional value for synthesizer.

Table 27. FLoad (0x0B)

BIT	NAME	FUNCTION
0	hop	Hop bit. Loads the synthesizer fractional-N divider base value to base[20:0] written in registers 8 through 10. This is a self-reset bit, and is reset to zero after the operation is completed.

Table 28. Group 4: Transmiter Amplitude and Timing Parameters (TxConf0, TxConf1, TxTstep)

GROUP/FUNCTION		HEX	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
4	TxConf0	0x0C	palopwr	wsoff	fska_5	fska_4	fska_3	fska_2	fska_1	fska_0
	TxConf1	0x0D	wsmlt_1	wsmlt_0	fskas_5	fskas_4	fskas_3	fskas_2	fskas_1	fskas_0
	TxTstep	0x0E	tstep_7	tstep_6	tstep_5	tstep_4	tstep_3	tstep_2	tstep_1	tstep_0

These registers set general FSK/ASK parameters for PA amplitude and rate control (FSK), shaping control, and the step control used for amplitude or frequency shaping.

Table 29. TxConf0 Register (0x0C)

BIT	NAME	FUNCTION
7	palopwr	Reduces the PA input buffer current by 2mA when set to 1. Useful at low output power levels.
6	wsoff	Disables (1) or enables (0) waveshaping. If waveshaping is disabled, only shp00[7:0] (Shape00 register, 0x0F) and wsmlt[1:0] (TxConf1 register, 0x0D) are used to set the amplitude (ASK) or frequency (FSK) deviation.
5:0	fska[5:0]	6-bit final value for FSK PA amplitude (bias current) control.

Table 30. TxConf1 Register (0x0D)

BIT	NAME	FUNCTION
7:6	wsmlt[1:0]	2-bit scaler for shp00[7:0] (Shape00 register, 0x0F), effectively multiplying the value of Shape00 by: wsmlt[1:0] multiplier 0 0 1 0 1 2 1 0 4 1 1 8
5:0	fskas[5:0]	6-bit FSK amplitude (bias current) step for ramp-up and ramp-down operations. The PA amplitude increases/decreases by this amount for every 1/20th of the data rate time elapsed (TxTstep register, 0x0E), until it reaches the final fska[5:0] value when ramping up, or reaches 0 when ramping down.

Table 31. TxTstep Register (0x0E)

BIT	NAME	FUNCTION
7:0	tstep[7:0]	8-bit update value for waveshaping. This setting corresponds to 1/20th of the data rate, given in periods of the master digital clock (312.5ns for 3.2 MHz). tstep[7:0] = INT (mclk/(20 x DataRate)) For 80kbps < DataRate ≤ 160kbps, tstep[7:0] = 1, mclk = 3.2MHz For 40kbps < DataRate ≤ 80kbps, tstep[7:0] = 2, mclk = 3.2MHz For 160kbps < DataRate ≤ 200kbps, tstep[7:0] = 1, mclk = 4.0MHz For 4kbps, tstep = INT ($3.2 \times 10^6/(20 \times 4000)$) = 40 (0x28), mclk = 3.2MHz The maximum value for tstep[7:0] is 255, which allows for a minimum shaped data rate of 627bps. These values assume shaping during the entire bit interval. The tstep value can be set lower if possible for shaping during a portion of the bit interval.

This setting allows for the 20 sequential steps in either the amplitude (ASK) or frequency (FSK) waveshaping process, for each symbol of the transmitted data.

Table 32. Group 5: Transmitter Shaping Registers (Shape00–Shape18)

GROUP/FUNCTION		HEX	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
5	Shape00	0x0F	shp00_7	shp00_6	shp00_5	shp00_4	shp00_3	shp00_2	shp00_1	shp00_0
	Shape01	0x10	shp01_7	shp01_6	shp01_5	shp01_4	shp01_3	shp01_2	shp01_1	shp01_0
	Shape02	0x11	shp02_7	shp02_6	shp02_5	shp02_4	shp02_3	shp02_2	shp02_1	shp02_0
	Shape03	0x12	shp03_7	shp03_6	shp03_5	shp03_4	shp03_3	shp03_2	shp03_1	shp03_0
	Shape04	0x13	shp04_7	shp04_6	shp04_5	shp04_4	shp04_3	shp04_2	shp04_1	shp04_0
	Shape05	0x14	shp05_7	shp05_6	shp05_5	shp05_4	shp05_3	shp05_2	shp05_1	shp05_0
	Shape06	0x15	shp06_7	shp06_6	shp06_5	shp06_4	shp06_3	shp06_2	shp06_1	shp06_0
	Shape07	0x16	shp07_7	shp07_6	shp07_5	shp07_4	shp07_3	shp07_2	shp07_1	shp07_0
	Shape08	0x17	shp08_7	shp08_6	shp08_5	shp08_4	shp08_3	shp08_2	shp08_1	shp08_0
	Shape09	0x18	shp09_7	shp09_6	shp09_5	shp09_4	shp09_3	shp09_2	shp09_1	shp09_0
	Shape10	0x19	shp10_7	shp10_6	shp10_5	shp10_4	shp10_3	shp10_2	shp10_1	shp10_0
	Shape11	0x1A	shp11_7	shp11_6	shp11_5	shp11_4	shp11_3	shp11_2	shp11_1	shp11_0
	Shape12	0x1B	shp12_7	shp12_6	shp12_5	shp12_4	shp12_3	shp12_2	shp12_1	shp12_0
	Shape13	0x1C	shp13_7	shp13_6	shp13_5	shp13_4	shp13_3	shp13_2	shp13_1	shp13_0
	Shape14	0x1D	shp14_7	shp14_6	shp14_5	shp14_4	shp14_3	shp14_2	shp14_1	shp14_0
	Shape15	0x1E	shp15_7	shp15_6	shp15_5	shp15_4	shp15_3	shp15_2	shp15_1	shp15_0
	Shape16	0x1F	shp16_7	shp16_6	shp16_5	shp16_4	shp16_3	shp16_2	shp16_1	shp16_0
	Shape17	0x20	shp17_7	shp17_6	shp17_5	shp17_4	shp17_3	shp17_2	shp17_1	shp17_0
	Shape18	0x21	shp18_7	shp18_6	shp18_5	shp18_4	shp18_3	shp18_2	shp18_1	shp18_0

These registers set the amplitude (ASK) or frequency deviation (FSK) modulated by the incoming transmitted data. For every 1/20th of the bit rate defined by tstep[7:0], the following shape value is added to the previous accumulated result. All the shape values are deltas, and the final ASK amplitude or FSK deviation is given by the cumulative sum of all the shape registers.

In ASK, the initial value is 0. For FSK, the initial value is given by base[20:0]. There are 20 intervals (hence 19 shape registers) that are added on the 0-1 transition of the transmitted data or subtracted from on the 1-0 transition.

Table 33. Shape00 Register (0x0F)

BIT	NAME	FUNCTION
7:0	shp00[7:0]	First 8-bit value for waveshaping. This value is effectively multiplied by the wsmlt[1:0] setting (TxConf1 register, 0x0D). If the wsoff bit is high, this is the only value that is added or subtracted to perform either amplitude (ASK) or frequency (FSK) modulation.

Table 34. Shape01–Shape18 Registers (0x10–0x21)

BIT	NAME	FUNCTION
7:0	shp01[7:0] shp02[7:0] shp03[7:0] shp04[7:0] shp05[7:0] shp06[7:0] shp07[7:0] shp08[7:0] shp09[7:0] shp10[7:0] shp11[7:0] shp12[7:0] shp13[7:0] shp14[7:0] shp15[7:0] shp16[7:0] shp17[7:0] shp18[7:0]	18 8-bit values for waveshaping. These values, along with shp00[7:0], yield the 19 different values (20 intervals) used for waveshaping, one for each of the 20 updates occurring during each 0-1 or 1-0 transmitted data transition.

Table 35. Group 6: Control Registers (TestMux, Datain, EnableReg)

GROUP/FUNCTION		HEX	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
6	TestMux	0x3C	—	—	—	—	tmux_3	tmux_2	tmux_1	tmux_0
	Datain	0x3D	—	datain	—	—	—	—	—	—
	EnableReg	0x3E	—	—	—	—	tsensor	—	—	enable

This register group combines status bus control (tbus[15:0]), GPO controls, temperature sensor control, register control of pin function (txdata), and enable controls.

Table 36. TestMux Register (0x3C)

BIT	NAME	FUNCTION
3:0	tmux[3:0]	4-bit selection of tbus[15:0] (TestBus0 and TestBus1 registers, 0x40 and 0x41) contents. See the TestBus0 and TestBus1 register descriptions for a complete description of what can be observed through this 16-bit bus.

Table 37. Datain Register (0x3D)

BIT	NAME	FUNCTION
6	datain	Transmit datain bit. This is a register equivalent of the DATAIN pin. When either the DATAIN pin or datain bit is 1, the transmit data is 1. Only when both are 0 the transmit data is 0 (logical OR function). Keep 0 if only the external DATAIN pin is used, and keep DATAIN pin 0 if the internal datain bit is used.

Table 38. EnableReg Register (0x3E)

BIT	NAME	FUNCTION
3	tsensor	Writing a 1 to this bit starts the temperature sensor A/D conversion. This is a self-reset bit, where the bit is automatically reset when the conversion is finished. The result can then be read through the TestBus1 register (0x41). This function is available only in Sleep mode.
0	enable	Enables (1) or disables (0) the IC's transmitter operations. To enable the IC, SHDN must be driven low. This is a register equivalent of the ENABLE pin. When either the ENABLE pin or enable bit is 1, the IC transmit operation is enabled. Only when both are 0 the transmitter is disabled (logical-OR function). Keep 0 if only the external ENABLE pin is used, and keep ENABLE pin 0 if the internal enable is used.

Table 39. Group 7: Read-Only Status Registers (TestBus0, TestBus1, Status0, Status1)

GROUP/FUNCTION		HEX	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
7	TestBus0	0x40	tbus_15	tbus_14	tbus_13	tbus_12	tbus_11	tbus_10	tbus_9	tbus_8
	TestBus1	0x41	tbus_7	tbus_6	tbus_5	tbus_4	tbus_3	tbus_2	tbus_1	tbus_0
	Status0	0x42	txready	—	adcrdy	—	gpo1out	plllock	lockdet	ckalive
	Status1	0x43	—	—	—	tsdone	—	—	—	—

Registers 0x3F–0x43 are read-only registers used for A/D results, status, and test.

Table 40. TestBus0 Register (0x40)

BIT	NAME	FUNCTION
7:0	tbus[15:8]	8 MSBs of the internal 16-bit bus tbus[15:0], selected by tmux[3:0] (TextMux register, 0x3C, bits 3:0).

Table 41. Test Bus Signals (tbus[15:8])

tmux[3:0]	tbus[15]	tbus[14]	tbus[13]	tbus[12]	tbus[11]	tbus[10]	tbus[9]	tbus[8]
0x0	—	—	—	—	—	—	—	—
0x1	—	—	—	—	—	—	—	—
0x2	—	—	—	—	—	—	—	—
0x3	—	—	—	—	—	—	—	—
0x4	—	—	—	—	—	—	—	—
0x5	—	—	pabia[5]	pabia[4]	pabia[3]	pabia[2]	pabia[1]	pabia[0]
0x6	frac[15]	frac[14]	frac[13]	frac[12]	frac[11]	frac[10]	frac[9]	frac[8]
0x7	—	—	—	—	—	—	—	—
0x8	—	—	—	—	—	—	—	—
0x9	—	—	—	—	—	—	—	—
0xA	—	—	—	—	—	—	—	—
0xB	—	—	—	—	—	—	—	mclk
0xC	—	—	—	—	—	—	—	plllock
0xD	—	—	—	—	—	—	—	—
0xE	—	—	—	—	—	—	—	—
0xF	—	—	—	—	—	—	—	—

where:

tmux[3:0]	Signal	Description
0x0–0x4	—	Reserved signals for test purposes
0x5	pabia[5:0]	PA amplitude control bus
0x6	frac[15:8]	MSBs of fractional value sent to frequency synthesizer
0x7–0xA	—	Reserved signals for test purposes
0xB	mclk	Master digital clock
0xC	plllock	Synthesizer lock signal
0xD–0xF	—	Reserved signals for test purposes

Table 42. TestBus1 Register (0x41)

BIT	NAME	FUNCTION
7:0	tbus[7:0]	8 LSBs of the internal 16-bit bus tbus[15:0], selected by tmux[3:0] (TestMux register, 0x3C, bits 3:0).

Table 43. Test Bus Signals (tbus[7:0])

tmux[3:0]	tbus[7]	tbus[6]	tbus[5]	tbus[4]	tbus[3]	tbus[2]	tbus[1]	tbus[0]
0x0	tsdonef	tsadc[6]	tsadc[5]	tsadc[4]	tsadc[3]	tsadc[2]	tsadc[1]	tsadc[0]
0x1	—	—	—	—	—	—	—	—
0x2	—	—	—	—	—	—	—	—
0x3	—	—	—	—	—	—	—	—
0x4	—	—	—	—	—	—	—	—
0x5	palopwr	—	—	integ[4]	integ[3]	integ[2]	integ[1]	integ[0]
0x6	frac[7]	frac[6]	frac[5]	frac[4]	frac[3]	frac[2]	frac[1]	frac[0]
0x7	—	—	—	—	—	—	—	—
0x8	—	—	—	—	—	—	—	—
0x9	—	—	—	ents	—	—	—	tsdonef
0xA	—	—	—	—	—	—	—	—
0xB	—	—	—	—	—	—	—	—
0xC	—	lockdet	ckalive	—	—	—	txready	—
0xD	—	—	—	—	—	—	—	—
0xE	—	—	—	—	—	—	—	—
0xF	—	—	—	—	mclk	—	—	—

where:

tmux[3:0]	Signal	Description
0x0	tsdonef	Temperature sensor conversion done flag
	tsadc[6:0]	Temperature sensor A/D result
0x1–0x4	—	Reserved signals for test purposes
0x5	palopwr	PA low-power mode flag
	integ[4:0]	Integer value sent to frequency synthesizer
0x6	frac[7:0]	LSBs of fractional value sent to frequency synthesizer
0x7, 0x8	—	Reserved signals for test purposes
0x9	ents	Enable temperature sensor conversion signal
	tsdonef	Temperature sensor done flag
0xA, 0xB	—	Reserved signals for test purposes
0xC	lockdet	Synthesizer lock-detect signal
	ckalive	Crystal oscillator clock alive flag
	txready	Tx ready flag
0xD, 0xE	—	Reserved signals for test purposes
0xF	mclk	Master digital clock

Note that each of the signals available on the digital test bus can be observed on GPO1, GPO2, or SDO, as discussed in the *Digital Outputs* section.

Table 44. Status0 Register (0x42)

BIT	NAME	FUNCTION
7	txready	Transmit ready flag. After this bit goes to 1, the IC is ready to accept transitions on the DATAIN pin or on the datain bit inputs. Both these bits should be 0 before the txready flag is 1.
5	adcrdy	Internal test flag that signals the end of the A/D warmup time.
3	gpo1out	Register copy of the GPO1 pin logical state.
2	plllock	Synthesizer lock flag, after programmable plldl[2:0] expires.
1	lockdet	Synthesizer lock detect flag.
0	ckalive	Crystal oscillator clock alive flag, indicating clock activity from the crystal oscillator.

Table 45. Status1 Register (0x43)

BIT	NAME	FUNCTION
4	tsdone	Temperature sensor conversion done flag. When 1, the A/D conversion of the internal temperature sensor is completed.

Layout Considerations

A properly designed PCB is an essential part of any RF/microwave circuit. On high-frequency, high-impedance inputs and outputs, use minimum width lines and keep them as short as possible to minimize stray capacitance. Keeping the traces short also reduces parasitic inductance. Generally, 1in of PCB trace adds approximately 20nH of parasitic inductance. The parasitic inductance can have a dramatic effect on the effective inductance of a passive component. For example, a 0.5in trace connecting to a 100nH inductor adds an extra 10nH of inductance, or 10%.

To reduce parasitic inductance, use a solid ground plane below the signal traces. Also, use low-inductance connections to the ground plane for shunt matching and bypassing components, and place bypassing capacitors as close as possible to all power-supply pins. Use separate vias to the ground plane for all shunt matching and bypassing components to reduce unwanted common impedance coupling.

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX7049ATI+	-40°C to +125°C	28 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
28 TQFN-EP	T2855+3	21-0140	90-0023

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/11	Initial release	—