T-46-23-17

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Edition 1.0

FUJITSU

DATA SHEET

MB81C4253-10/-12/-15

1,048,576 BIT DUAL PORT CMOS DYNAMIC RAM

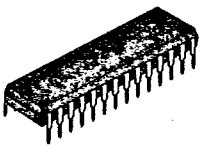
262,144 X 4 Bit Dual Port CMOS Dynamic RAM

The Fujitsu MB81C4253 is a fully decoded dual port CMOS Dynamic RAM (DRAM) organized as 262,144 words by 4 bits dynamic RAM port and 512 words by 4 bits serial access memory (SAM) port.

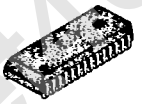
The MB81C4253 is ideally suited for mainframes, video imaging equipment, and other memory applications where very low power dissipation and high bandwidth are basic requirements of the design. Multiplexed row and column address inputs permit the MB81C4253 to behoused in 400mil wide 28 pin DIP, SOJ and ZIP. Pin outs conformed to the JEDEC approved pinout. The MB81C4253 features a Bit Masked Write operation whereby the user can inhibit writing to particular bits, Flash Write operation which is suitable for fast clear, and Mask Write Transfer operation whrereby the user can inhibit write transfer from SAM to RAM per plane.

The MB81C4253 is fabricated using silicon gate CMOS and Fujitsu's advanced triple-layer polysilicon process. This process, coupled with three-dimensional stacked capacitor memory cells, reduces the possibility of soft errors and extends the time interval between memory refreshes.

ADVANCE INFO.



DIP-28P-M06



LCC-28P-M06

T.B.D

ZIP-28P-M01

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PRODUCT LINE & FEATURES

Parameter		MB81C4253-10	MB81C4253-12	MB81C4253-15
Access Time	DRAM	100ns max.	120ns max.	150ns max.
	SAM	30ns max.	40ns max.	60ns max.
Cycle Time	DRAM	180ns min.	210ns min.	260ns min.
	SAM	30ns min.	40ns min.	60ns min.
Power Dissipation	DRAM ; Active SAM ; Standby	450mW max.	400mW max.	350mW max.
	DRAM ; Standby SAM ; Active	330mW max.	280mW max.	250mW max.
	DRAM ; Standby SAM ; Standby	22mW max.		

- Dual port organization
  262,144 words x 4 bits (DRAM port)
  512 words x 4 bits (SAM port)
- Silicon gate, CMOS, 1 transistor cell
- Single +5V power supply, +/−0.5V tolerance
- All inputs and outputs are TTL compatible
- 512 refresh cycles every 8.2 ms
- Bi-directional data transfer capability
- Fast serial access asynchronous to DRAM expect transfer operation
- Addressable start location (TAP) on serial shift register
- Realtime Read Transfer capability
- Mask Write Transfer capability
- Bit Masked Write Mode capability
- I/O switch by transfer cycle
- Fast page Mode, Read-Modify-Write Flash Write capability
- $\overline{RAS}$ only, $\overline{CAS}$-before-$\overline{RAS}$, or Hidden Refresh

ABSOLUTE MAXIMUM RATINGS (see NOTE)

Parameter	Symbol	Value	Unit
Voltage at any pin relative to VSS	V_{IN}, V_{OUT}	−1 to +7	V
Voltage of V_{CC} supply relative to VSS	V_{CC}	−1 to +7	V
Power Dissipation	PD	1.0	W
Short Circuit Output Current	I_{OUT}	50	mA
Storage Temperature	T_{STG}	−55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.