M54974P

Bi-CMOS 12-BIT SERIAL-INPUT LATCHED DRIVER

DESCRIPTION

The M54974P is a semiconductor integrated circuit consisting of 12 stages of CMOS shift registers and latches with serial inputs and serial or parallel outputs. It is based on Bi-CMOS process technology, and has 12 bipolar drivers at the parallel outputs.

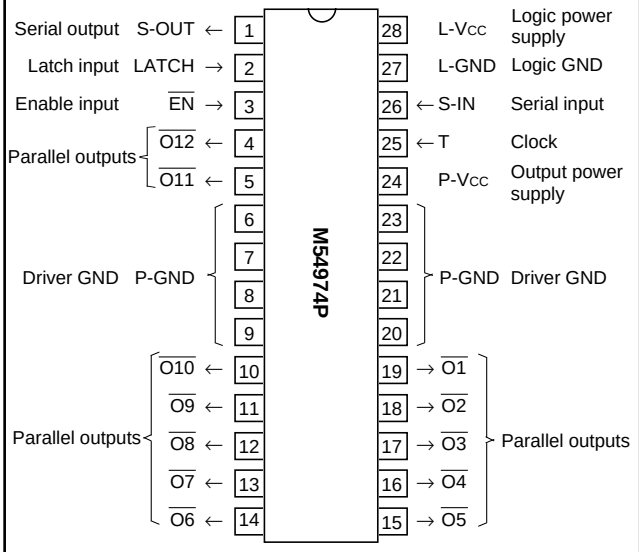
FEATURES

- Serial input and serial or parallel output
- Serial output enables cascade connection
- Built-in latch for each stage
- Enable input provides output control
- Low supply current (standby current $I_{CC} \leq 10\mu A$)
- Serial I/O level is compatible with typical CMOS devices
- Driver features: High withstand voltage ($BV_{CEO} \geq 30V$)
  Capable of large drive currents ($I_{O(max)}$=300mA)
- Wide operating temperature range T_a=-20 – +75°C

APPLICATION

Dot drivers for thermal print heads. Serial/parallel conversion. Drivers for relay and solenoids.

PIN CONFIGURATION (TOP VIEW)



Outline 28P4B

FUNCTION

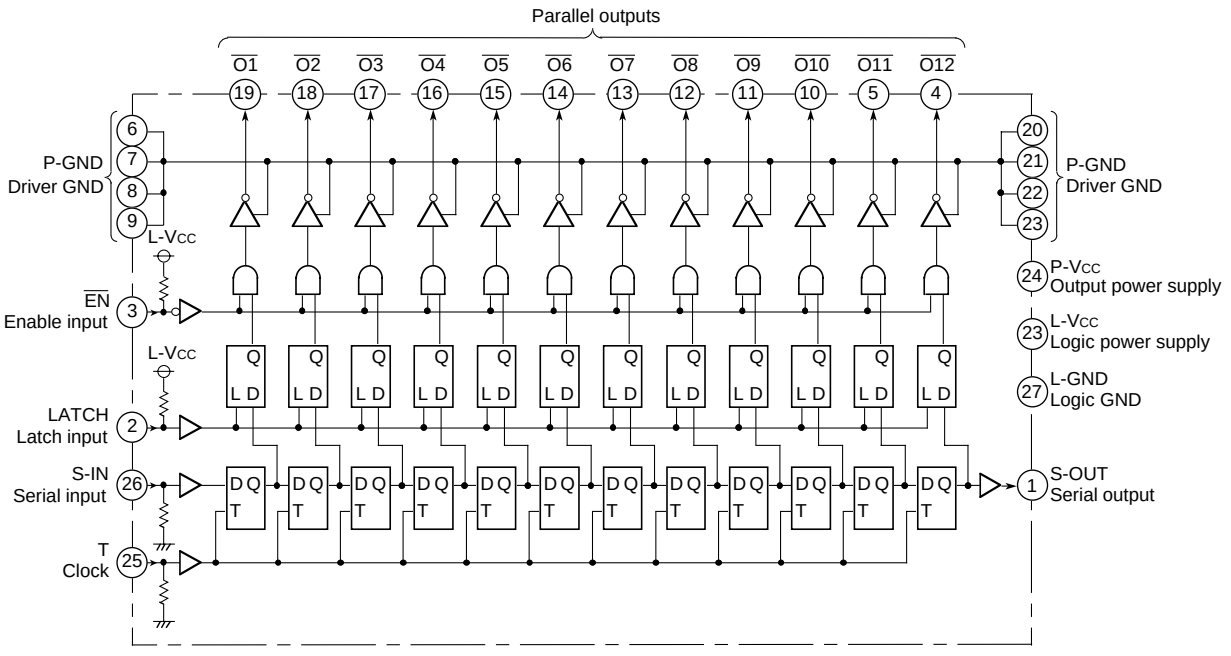
The M54974P consists of 12 stages of D-type flip flops connected to 12 latches.

Data is input to serial input S-IN, and clock pulses are applied to clock input T. When the clock changes from low to high, the input data enters the first shift register and data already in the shift registers is shifted sequentially.

The serial output S-OUT is used to connect multiple M54974Ps to expand the number of parallel outputs. S-OUT is connected to S-IN of the next stage.

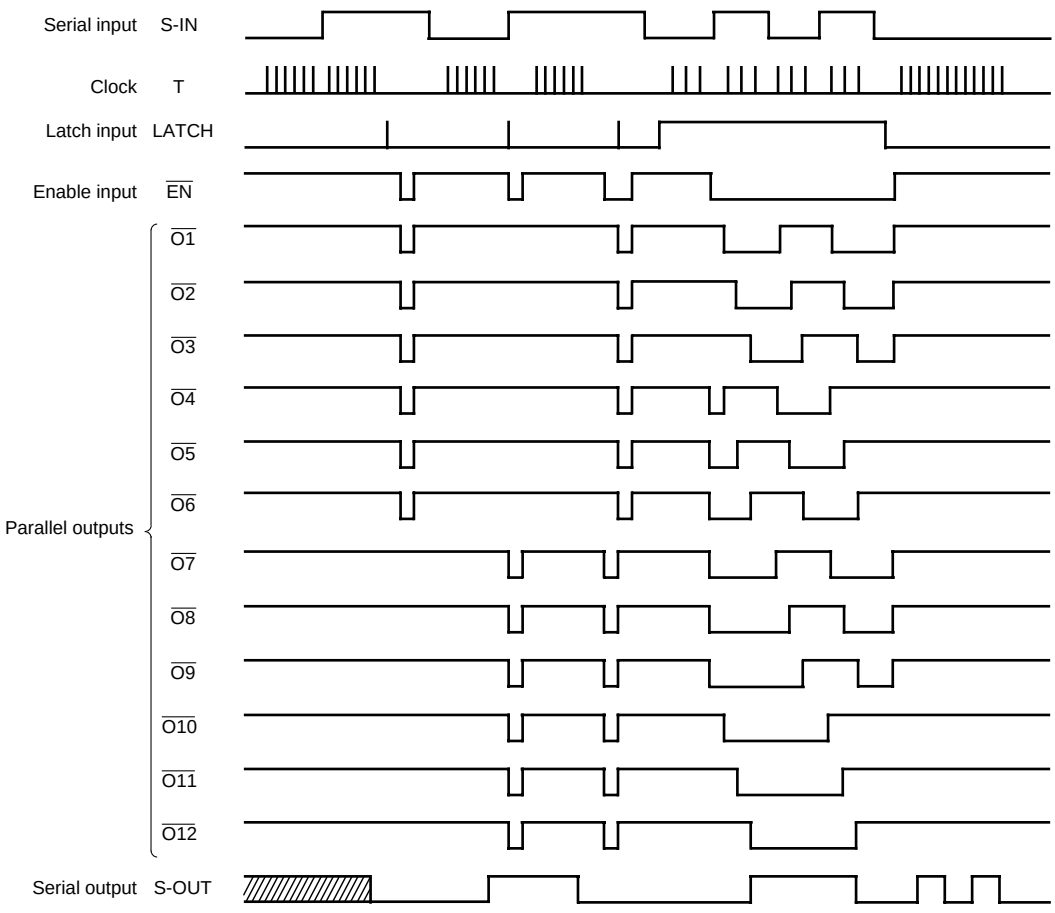
When the clock pulse changes from low to high, latch input (LATCH) is high and output enable input ($\overline{EN}$) is low the serial input data at S-IN appears at output $\overline{O1}$ and the other data already

BLOCK DIAGRAM



present is shifted sequentially to outputs $\overline{O2}$ through $\overline{O12}$.
The parallel outputs are inverted.
When the latch input is held low, the latch retains the stored data.
When the $\overline{EN}$ input is high, outputs $\overline{O1}$ through $\overline{O12}$ all turn off. As the internal logic is unstable when the power is turned on, the $\overline{EN}$ input should be kept high (setting the outputs $\overline{O1}$ through $\overline{O12}$ off) until input data is set and the internal logic is initialized.
L-GND is the GND of CMOS logic circuit and P-GND is the GND of output driver circuits $\overline{O1}$ through $\overline{O12}$ which employ bipolar transistors capable of large drive currents.

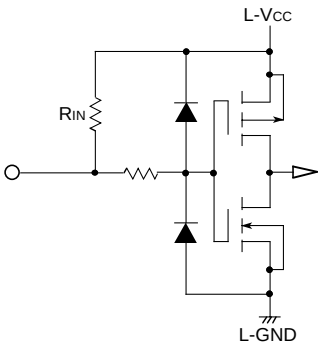
TIMING CHART



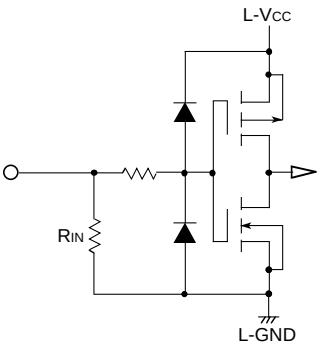
* The shaded area shows the unstable state.

INPUT/OUTPUT CIRCUIT DIAGRAM

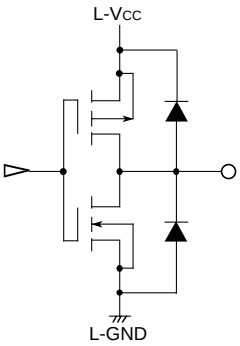
1 Inputs with pullup resistor
($\overline{EN}$, LATCH)



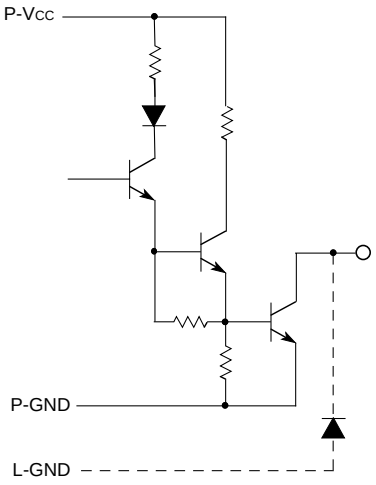
2 Inputs with pulldown resistor
(T, S-IN)



3 Serial output
(S-OUT)



4 Parallel outputs
($\overline{O1}$ – $\overline{O12}$)



ABSOLUTE MAXIMUM RATINGS (Ta=-20 to 75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	P-V_{CC}, L-V_{CC}	-0.5 – 8	V
V_I	Input voltage	S-IN, LATCH, T, $\overline{EN}$	-0.5 – V_{CC}+0.5	V
V_O	Output voltage	S-OUT	-0.5 – V_{CC}+0.5	V
		$\overline{O1}$ – $\overline{O12}$: OFF	-0.5 – 30	
I_O	Output current	$\overline{O1}$ – $\overline{O12}$	400	mA
P_d	Power dissipation	T_a=25°C	2.5	W
T_{opr}	Operating temperature		-20 – 75	°C
T_{stg}	Storage temperature		-55 – 125	°C

RECOMMENDED OPERATING CONDITION (Ta=-20 to 75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	Supply voltage	P-V_{CC}, L-V_{CC}	4	5	6	V
V_O	Output apply voltage	$\overline{O1}$ – $\overline{O12}$: OFF			30	V
I_O	Output current (per circuit)	All outputs go in the ON state simultaneously. Duty cycle < 50%, Ta < 25°C			300	mA

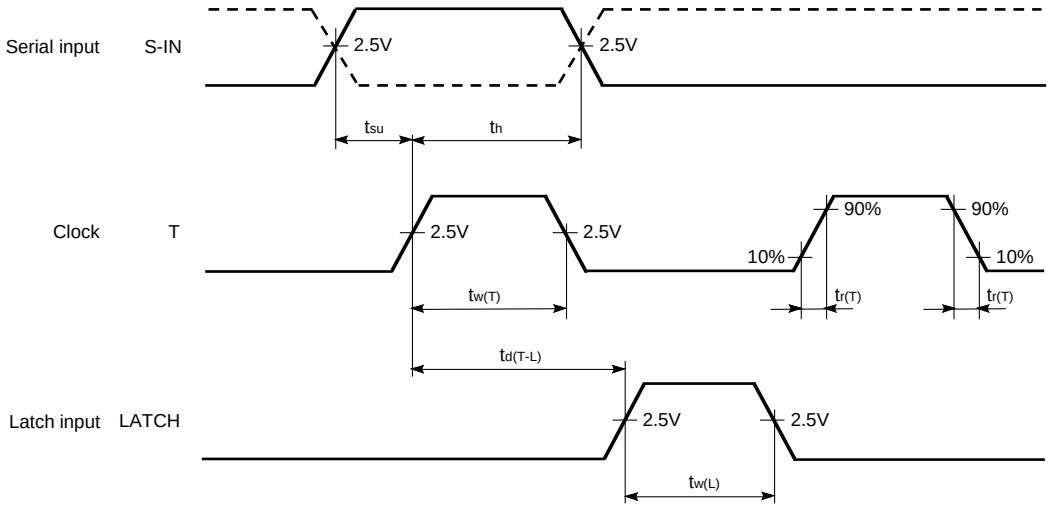
ELECTRICAL CHARACTERISTICS (Ta=25°C, L-V_{CC}=5V, P-V_{CC}=5V, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min.	Typ.	Max.	
V_{IH}	High-level input voltage		T_a=-20 – 75°C	0.7V_{CC}		V_{CC}	V
V_{IL}	Low-level input voltage			0		0.3V_{CC}	V
R_{IN}	Input resistance			50			kΩ
V_{OH}	High-level output voltage	S-OUT	|I_O|≤1μA	4.9			V
V_{OL}	Low-level output voltage	S-OUT				0.1	V
I_{OH}	High-level output current	S-OUT	V_{OH}=4.5V	-100			μA
I_{OL}	Low-level output current	S-OUT	V_{OL}=0.4V	400			μA
V_{OL1}	Low-level output voltage	$\overline{O1}$ – $\overline{O12}$	I_{OL}=120mA			0.4	V
V_{OL2}							
V_{OL3}			I_{OL}=400mA			0.7	V
I_{OLK}	Output leak current	$\overline{O1}$ – $\overline{O12}$	V_O=30V			50	μA
I_{CC1}	Supply current (L-V_{CC})		Input: open, All driver outputs: OFF			10	μA
I_{CC2}			One driver output is ON.			0.2	mA
I_{CC3}	Output supply current (P-V_{CC})		One driver output is ON.			14	mA

TIMING REQUIREMENTS (Ta=-20 to 75°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$f_{(T)}$	Clock frequency	Input duty: 40 – 60%			2	MHz
$t_{w(T)}$	Clock pulse width		200			ns
$t_{w(L)}$	Latch pulse width		200			ns
t_{su}	Data setup time		100			ns
t_h	Data hold time		100			ns
$t_{d(T-L)}$	Clock-latch time		400			ns
$t_{r(T)}$	Clock pulse rise time				500	ns
$t_{f(T)}$	Clock pulse fall time				500	ns

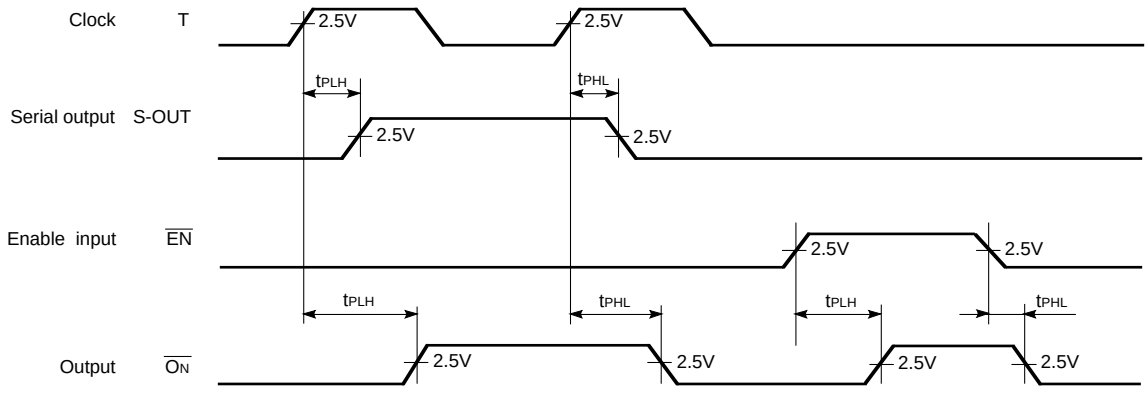
TIMING CHART



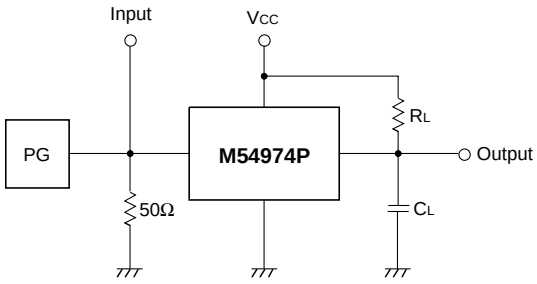
SWITCHING CHARACTERISTICS (Ta=25°C, V_{CC}=5V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
t_{PLH}	Low-to-high-level output propagation time, From input T to output S-OUT	V_{IH}=5V V_{IL}=0V R_L(S-OUT)=∞ R_L($\overline{ON}$)=100Ω (N=1–12) C_L=15pF		(0.15)	0.3	µs
t_{PHL}	High-to-low-level output propagation time, From input T to output S-OUT			(0.15)	0.3	µs
t_{PLH}	Low-to-high-level output propagation time, From input T to output $\overline{ON}$			(2)	10	µs
t_{PHL}	High-to-low-level output propagation time, From input T to output $\overline{ON}$			(1)	5	µs
t_{PLH}	Low-to-high-level output propagation time, From input $\overline{EN}$ to output $\overline{ON}$			(2)	10	µs
t_{PHL}	High-to-low-level output propagation time, From input $\overline{EN}$ to output $\overline{ON}$			(1)	5	µs

TIMING CHART



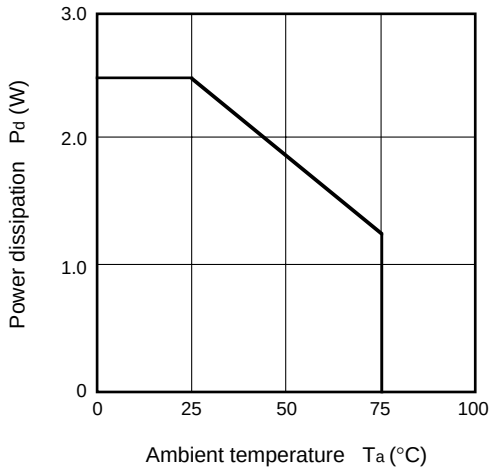
TEST CIRCUIT



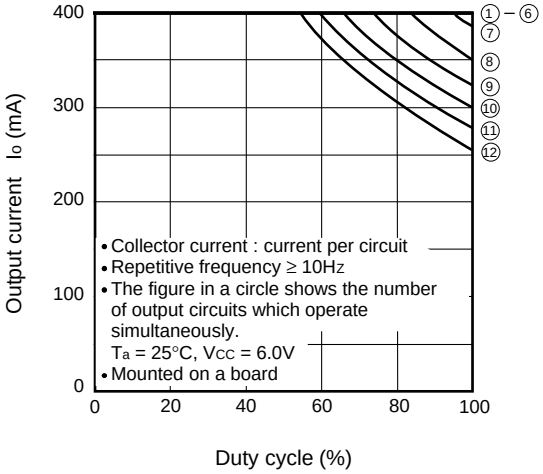
- The input waveform: $t_r \leq 20ns$, $t_f \leq 20ns$
- The capacitance C_L includes the stray wiring capacitance and probe input capacitance.

TYPICAL CHARACTERISTICS

Thermal derating
(Absolute maximum rating)



Duty cycle vs. allowable
output current



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