V53C102A FAMILY
HIGH PERFORMANCE, LOW POWER
1M x 1 BIT, STATIC COLUMN MODE
CMOS DYNAMIC RAM

HIGH PERFORMANCE V53C102A	70/70L	80/80L	10/10L
Max. $\overline{RAS}$ Access Time, (t_{RAC})	70 ns	80 ns	100 ns
Max. Column Address Access Time, (t_{CAA})	35 ns	40 ns	45 ns
Min. Static Column Mode Cycle Time, (t_{PC})	40 ns	50 ns	55 ns
Min. Read-Write Cycle Time, (t_{RC})	130 ns	150 ns	180 ns

LOW POWER V53C102AL	70L	80L	10L
Max. CMOS Standby Current, (I_{DD6})	1.0 mA	1.0 mA	1.0 mA

Features

- 1M x 1 organization
- $\overline{RAS}$ access time: 70, 80, 100 ns
- Low power dissipation for V53C102A-10
  - Operating Current—65 mA max.
  - TTL Standby Current—2.0 mA max.
- Low CMOS Standby Current
  - V53C102A—1.5 mA max.
  - V53C102AL—1.0 mA max.
- Read-Modify-Write, $\overline{RAS}$-Only Refresh, $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- Common I/O capability
- 512 Refresh cycles/8 ms
- On-chip substrate bias generator
- Static Column Operation for a sustained data rate greater than 22 MHz
- Standard packages are 18 pin Plastic DIP and 26/20 pin SOJ

Description

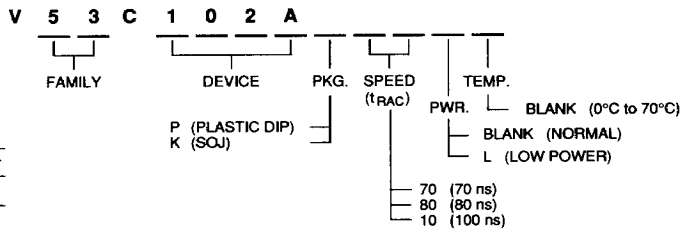
The V53C102A is a Static Column Mode, 1,048,576 word by one bit dynamic RAM. It is designed to operate from a single, 5 V ±10% tolerance power supply. Fabricated with Vitelic's VICMOS III technology, the device provides both high performance and high reliability over its operating range. Because it utilizes static circuitry, and its flow-through column address latches allow address pipelining, many critical system timing requirements are relaxed. It features Static Column decode for high data bandwidth and clock-free page operation, fast usable speed. Static Column operation allows random access of up to 512 bits within a row with cycle times as short as 45 ns. Because of static circuitry, $\overline{CAS}$ is not required to either clock or gate column addresses and, since $\overline{CAS}$ is not in the critical access time path, system design is easier and inherent device speed is more usable. These unique features make the V53C102A ideally suited for computer peripherals, control systems and graphics systems.

Refreshing can be accomplished by using $\overline{CAS}$ before $\overline{RAS}$, $\overline{RAS}$-only or normal read or write cycles.

An internal address counter obviates the need for externally supplied addresses during the $\overline{CAS}$ before $\overline{RAS}$ refresh mode. Externally supplied addresses are required during $\overline{RAS}$-only, or normal read or write cycles.

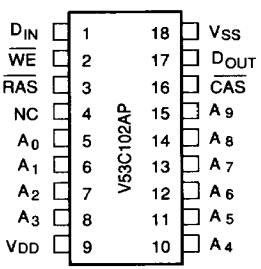
Device Usage Chart

Operating Temperature Range	Package Outline		Access Time (ns)			Power		Temperature Mark
	P	K	70	80	100	Low	Std.	
0°C to 70°C	•	•	•	•	•	•	•	Blank



Description	Pkg.	Pin Count
Plastic DIP	P	18
SOJ	K	26/20

18-Pin Plastic DIP PIN CONFIGURATION
Top View



26/20-Pin Plastic SOJ PIN CONFIGURATION
Top View