microelectronics group

Lucent Technologies
Bell Labs Innovations

TMUX03155 STS-3/STM-1 (AU-4) Multiplexer/Demultiplexer

Features

- Multiplexes three STS-1 signals into a SONET STS-3 signal.
- Multiplexes three AU-3 signals into an SDH STM-1 (AU-4) signal via a TUG-3 construction.
- Demultiplexes three STS-1 signals from a SONET STS-3 signal.
- Demultiplexes three AU-3 signals from an SDH STM-1 (AU-4) signal via a TUG-3 deconstruction.
- High-speed microprocessor interface configurable to operate with most commercial microprocessors.
- Detects STS-3/STM-1 (AU-4) loss-of-signal (LOS) conditions.
- Detects STS-3/STM-1 (AU-4) out-of-frame and loss-of-frame (OOF/LOF) conditions.
- Provides an 8-bit bus interface at the STS-1/AU-3 rate.
- Provides a bit serial, nibble-wide, or byte-wide interface at STS-3/STM-1 (AU-4) rate.
- Provides STS-3/STM-1 (AU-4) selectable scrambler/descrambler functions and B1/B2/B3 generation/detection.
- Accepts bit rate, nibble rate, or byte rate high-speed clocks (155.52 MHz, 38.88 MHz, or 19.44 MHz, respectively).
- −40 °C to +85 °C temperature range.
- 208-pin shrink quad flat pack (SQFP) package, or 208-pin plastic ball grid array (PBGA).
- 3.3 V operation with 5 V tolerant digital I/O.

Applications

- SONET/SDH line termination equipment
- SDH path origination and termination equipment
- SONET/SDH add/drop multiplexers
- SONET/SDH cross connects
- SONET/SDH test equipment

Description

The TMUX03155 STS-3/STM-1 (AU-4) multiplexer device provides two modes of operation: **STS-3** and **AU-4** modes. In STS-3 mode, the TMUX03155 device provides all of the functions necessary to multiplex and demultiplex up to three STS-1 signals to/from a SONET STS-3 signal. In AU-4 mode, the TMUX03155 provides the functionality to multiplex and demultiplex up to three AU-3 signals to/from an STM-1 (AU-4) signal. On the STS-3/STM-1 (AU-4) side, the device can be configured for either a 1-bit serial data interface, a 4-bit parallel (nibble-wide) data interface, or an 8-bit parallel (byte-wide) data interface. This allows the device to drive an OC3 optical signal directly or to allow for modular growth in terminal or add/drop applications. On the STS-1/AU-3 side, the TMUX03155 device provides a bus mode that can communicate with up to three STS-1/AU-3 devices at 19.44 Mbits/s. The TMUX03155 is designed to interface with the Lucent Technologies Microelectronics Group TMPR28051 device, or equivalent, providing complete mapping/unmapping from/to an STS-3/STM-1 (AU-4) signal for up to 84 DS1 or 63 E1 signals.

Automatic receive monitoring functions can be configured to provide an interrupt to the control system, or the device can be operated in a polled mode.

Built-in loopback at both the STS-1/AU-3 and STS-3/STM-1 (AU-4) interfaces provides maximum flexibility for use in a number of SONET/SDH products including path termination multiplexers, add/drop multiplexers, and digital cross connects.

A high-speed microprocessor interface and full user programmability on STS-1/AU-3 to STS-3/STM-1 (AU-4) slot insertion and drop provide maximum flexibility for I/O configuration.

Block Diagram

In the transmit direction, the device outputs a clock and sync and accepts bused data[7:0] and a parity signal from up to three devices. The device outputs one data bundle at the STS-3/STM-1 (AU-4) rate (clock, sync, data[7:0], and parity bit). A local clock and optional frame sync signal are needed for operation of the device. A transport overhead access channel (TOAC) is provided to allow overwriting of the transport overhead bytes in the output STS-3/STM-1 (AU-4) frame.

In the receive direction, the device accepts one STS-3/STM-1 (AU-4) bundle (clock, data, parity), and accepts a loss-of-signal indication from an external source. The device outputs three STS-1/AU-3 signals over a bus interface (clock, data, J0 time, parity). The STS-3/STM-1 (AU-4) input clock is used to clock this direction. A transport overhead access channel is provided for additional external monitoring of the incoming transport overhead of the STS-3/STM-1 (AU-4) frame. A pointer interpreter is provided to monitor path functions.

The device has loopback capabilities at the STS-1/AU-3 and STS-3/STM-1 (AU-4) interfaces. An 8-bit microprocessor interface, JTAG control logic, and in-circuit test capabilities are provided.
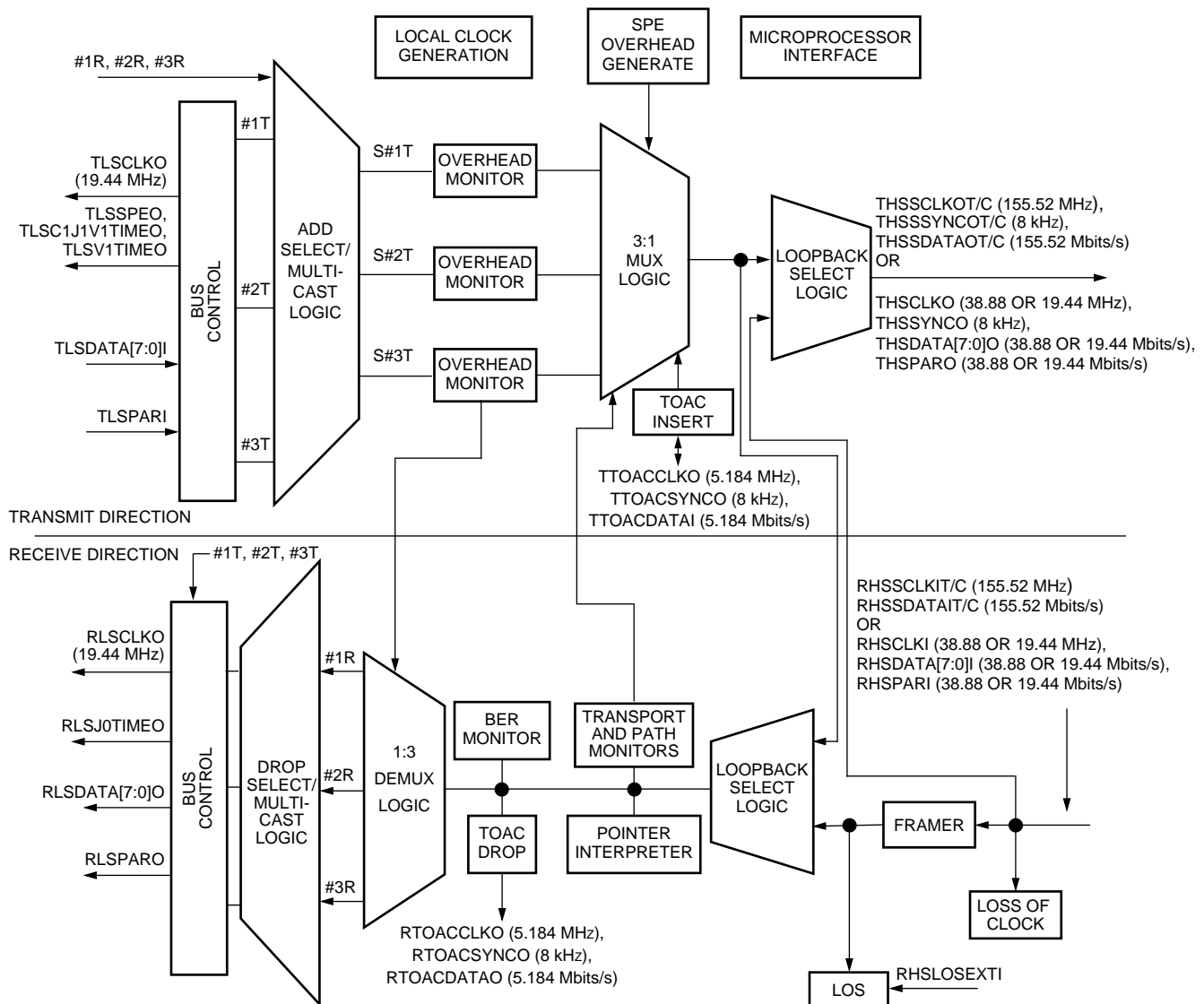
Figure 1. TMUX03155 Block Diagram

Lucent Technologies Inc.

Mode Control Signals

The device is controlled by four control signals: **T/RSONET_SDH** and **T/RSTS3_AU4** signals. These signals control:

■ The type of input signal to expect (low-speed (LS) side—STS-1/AU-3),

■ The expected high-speed (HS) input/output signal format—STS-3/STM-1 (AU-4), and

■ The default byte value in the outgoing HS frame.

These provisioning signals are summarized in Table 1 and Table 2.

Table 1. Transmit Mode Control Signals

TSTS3_AU4	TSONET_SDH	Description
0 = STS-3	0 = SONET	Three STS-1 inputs multiplexed to an STS-3 output.
1 = AU-4	0 = SONET	Three AU-3 signals multiplexed to an STM-1 (AU-4) signal.
0 = STS-3	1 = SDH	Three STS-1 inputs multiplexed to an STS-3 output.
1 = AU-4	1 = SDH	Three AU-3 signals multiplexed to an STM-1 (AU-4) signal.

Table 2. Receive Mode Control

RSTS3_AU4	RSONET_SDH	Description
0 = STS-3	0 = SONET	One STS-3 input demultiplexed to three STS-1 outputs.
1 = AU-4	0 = SONET	One STM-1 (AU-4) input demultiplexed to three AU-3 outputs.
0 = STS-3	1 = SDH	One STS-3 input demultiplexed to three STS-1 outputs.
1 = AU-4	1 = SDH	One STM-1 (AU-4) input demultiplexed to three AU-3 outputs.

Transmit Direction Overview

The following major functions are performed in the transmit direction: STS-1/AU-3 Bus Mode Input Retiming, Input Select Control, STS-1/AU-3 Inputs, Out-of-Frame (OOF) and Loss-of-Frame (LOF) Monitoring, Descramble Enable/Disable, Monitor B1 and B2 Errors, H4 Multiframe and Pointer Monitor (AU-4 Mode Only), STS-3 Generate, STM-1 (AU-4) Frame Generation (AU-4 Mode), Transport Overhead Access Channel (TOAC) Insert, STS-3/STM-1 (AU-4) Scramble Enable, STS-3/STM-1 (AU-4) Loopback Control, and STS-3/STM-1 (AU-4) Output Interface.

STS-1/AU-3 Bus Mode Input Retiming

The bus mode provides a single byte-wide bus and parity bit that is shared with up to three devices at 19.44 Mbits/s. The device will source a clock (19.44 MHz), synchronous payload envelope (SPE) indicator, J0J1V1 indicator, and V1 time indicator signals toward the downstream devices. These signals guarantee frame alignment between all three STS-1/AU-3 inputs and H4 byte multiframe values (AU-4 mode).

Input Select Control

This function determines which signals are multiplexed to form the STS-3/STM-1 (AU-4) signal. Loopback (STS-1/AU-3-R to STS-1/AU-3-T), input shuffle, and multicast operations are possible. The **selected STS-1/AU-3 inputs** are labeled S#1T, S#2T, and S#3T in Figure 1. When any one of the inputs is in loopback mode, all other inputs are timed off the receive high-speed clock.

Transmit Direction Overview (continued)

STS-1/AU-3 Inputs

The SONET/SDH STS-1/AU-3 frame is comprised of 9 rows x 90 columns that repeat at an 8 kHz rate. Each column is 1-byte wide. The frame contains three columns of transport overhead, one column of path overhead, and 86 columns of payload. For column byte definitions, see Table 3 below.

The 27 bytes of transport overhead from each STS-1/AU-3 input must be aligned* **(A1-1, A1-2, A1-3 must all be coincident from all three STS-1/AU-3 inputs)** and are allocated as shown below.

* Can be provided by the TMPR28051 mapper device.

Table 3. Expected STS-1/AU-3 Input Frame Format

	Transport Overhead			Payload	
	Col 1	Col 2	Col 3	Col 4	Col 5—90
Row 1	A1†‡	A2†‡	J0	J1	X
Row 2	B1†‡	E1	F1	B3	X
Row 3	D1	D2	D3	C2	X
Row 4	H1‡	H2‡	H3	G1	X
Row 5	B2†‡	K1	K2	F2	X
Row 6	D4	D5	D6	H4‡	X
Row 7	D7	D8	D9	Z3	X
Row 8	D10	D11	D12	Z4	X
Row 9	S1	M0	E2	Z5	X

† Monitored in STS-1 mode.
‡ Monitored in AU-4 mode.

Note: X = don't care (payload).

The path overhead (POH) can start anywhere within the SPE and cannot be accessed in the STS-3 mode.

In the AU-4 mode, the pointer is fixed at 522\D; therefore, the J1 byte will always be in row 1, column 4. The H4 byte is the only valid byte in the POH and all other bytes are ignored.

Out-of-Frame (OOF) and Loss-of-Frame (LOF) Monitoring

The device monitors for out-of-frame (OOF) and loss-of-frame (LOF) states on each selected STS-1/AU-3 input. Each input will be considered out-of-frame until **two** successive framing patterns (0xF628) separated in time by 125 μs occur without framing byte errors. Each selected STS-1/AU-3 input will be considered in frame until **five** (SDH)/**four** (SONET) successive frames separated in time by 125 μs occur with errored framing patterns. The device will be considered in the LOF state when an OOF condition persists for **24** consecutive frames (3 ms), or clear when the OOF condition is inactive for **24** consecutive frames (3 ms) with the correct framing patterns spaced 125 μs apart.

Descramble Enable/Disable

Each selected STS-1/AU-3 input can be descrambled according to the frame synchronous descrambling sequence $1 + x^6 + x^7$. Writing a logic 1 to the appropriate bit causes the selected STS-1/AU-3 signal to be descrambled.

Monitor B1 and B2 Errors

The device verifies B1 and B2 bit interleaved parity (BIP) values on each selected STS-1/AU-3 input. The device will count BIP errors or block errors under software control.

H4 Multiframe and Pointer Monitor (AU-4 Mode Only)

In this mode, all three input signals are required to have pointer values (H1, H2) with the same fixed value of 522\D. This ensures the J1 byte starts in row 1, column 4. The H4[1:0] multiframe bits must be the same from all inputs and equal to the internally expected value. This is required because the output STM-1 (AU-4) signal only has one H4 byte. The device will synchronize its H4 internal expected value to a 1 after detecting an embedded 2 kHz sync in the local frame sync signal.

Transmit Direction Overview (continued)

STS-3 Generate

In STS-3 mode, the device will create the overhead according to Table 4 below. The POH byte locations are not fixed and cannot be accessed.

Table 4. STS-3 Output Overhead Format

	STS-3 Overhead									
	Col. 1	**Col. 2**	**Col. 3**	**Col. 4**	**Col. 5**	**Col. 6**	**Col. 7**	**Col. 8**	**Col. 9**	**Col. 10—270**
Row 1	A1-1	A1-2	A1-3	A2-1	A2-2	A2-3	J0	Z0-2	Z0-3	
Row 2	B1	**B1-2***	**B1-3***	E1*	**E1-2***	**E1-3***	F1*	**F1-2***	**F1-3***	
Row 3	D1*	**D1-2***	**D1-3***	D2*	**D2-2***	**D2-3***	D3*	**D3-2***	**D3-3***	
Row 4	H1-1	H1-2	H1-3	H2-1	H2-2	H2-3	H3-1	H3-2	H3-3	Payload
Row 5	B2-1	B2-2	B2-3	K1	**K1-2***	**K1-3***	K2	**K2-2***	**K2-3***	
Row 6	D4*	**D4-2***	**D4-3***	D5*	**D5-2***	**D5-3***	D6*	**D6-2***	**D6-3***	
Row 7	D7*	**D7-2***	**D7-3***	D8*	**D8-2***	**D8-3***	D9*	**D9-2***	**D9-3***	
Row 8	D10*	**D10-2***	**D10-3***	D11*	**D11-2***	**D11-3***	D12*	**D12-2***	**D12-3***	
Row 9	S1*	Z1-2*	Z1-3*	Z2-1*	**Z2-2***	M1	E2*	**E2-2***	**E2-3***	

* Access through transmit TOAC.

Note: Bold type within the table is not defined in the standard and is labeled here for clarity.

The following values are assigned to the transmitted overhead bytes:

A1—11110110 (0xF6)
A2—00101000 (0x28)
J0—Programmable
Z0-2—Programmable
Z0-3—Programmable
B1—Variable value (BIP-8 parity)
F1—Programmable
H1-1, 2, 3—Passed through from respective STS-1
H2-1, 2, 3—Passed through from respective STS-1
H3-1, 2, 3—Passed through from respective STS-1
B2-1, 2, 3—Variable value (BIP-24)
K1—Programmable
K2—Programmable
S1—Programmable
M1—Variable value (Section FEBE—Number of B2 Errors)

All bytes not specified above either:

(1) are set to the fixed stuff value (0x00 (SONET)) or
(2) are TOAC value-inserted or
(3) have passed through from the selected STS-1 input, all under software control.

Transmit Direction Overview (continued)

STM-1 (AU-4) Frame Generation (AU-4 Mode)

In STM-1 mode, the device will create the overhead according to the following table. The path overhead bytes are created in this mode. The three AU-3 inputs are converted to TUG-3 format and inserted into a VC-4 that is multiplexed into an AU-4.

Table 5. STM-1 (AU-4) Output Overhead Format

	STM-1 (AU-4) Overhead									AU-4 Payload												
	Col.1	Col. 2	Col. 3	Col. 4	Col. 5	Col.6	Col. 7	Col. 8	Col. 9	POH 10	11	12	13	14	15	16	17	18	19	20	21	22—270
Row 1	A1-1	A1-2	A1-3	A2-1	A2-2	A2-3	J0	Z0-2	Z0-3	J1	FIXED STUFF	FIXED STUFF	NPI	NPI	NPI	FIXED STUFF	FIXED STUFF	FIXED STUFF	TUG-3 A	TUG-3 B	TUG-3 C	—
Row 2	B1	**B1-2***	**B1-3***	E1*	**E1-2***	**E1-3***	F1*	**F1-2***	**F1-3***	B3												—
Row 3	D1*	**D1-2***	**D1-3***	D2*	**D2-2***	**D2-3***	D3*	**D3-2***	**D3-3***	C2												—
Row 4	H1-1	Y	Y	H2-1	1*	1*	H3-1	H3-2	H3-3	G1			STUFF	STUFF	STUFF							—
Row 5	B2-1	B2-2	B2-3	K1	**K1-2***	**K1-3***	K2	**K2-2***	**K2-3***	F2												—
Row 6	D4*	**D4-2***	**D4-3***	D5*	**D5-2***	**D5-3***	D6*	**D6-2***	**D6-3***	H4												—
Row 7	D7*	**D7-2***	**D7-3***	D8*	**D8-2***	**D8-3***	D9*	**D9-2***	**D9-3***	Z3												—
Row 8	D10*	**D10-2***	**D10-3***	D11*	**D11-2***	**D11-3***	D12*	**D12-2***	**D12-3***	Z4												—
Row 9	S1*	**Z1-2***	**Z1-3***	Z2-1*	**Z2-2***	M1	E2*	**E2-2***	**E2-3***	Z5												—

* Access through transmit TOAC.

Note: Bold type within the table is not defined in the standard and is labeled here for clarity.

The following values are assigned to the transmitted overhead bytes:

A1—11110110 (0xF6)
A2—00101000 (0x28)
J0—Programmable
Z0-2—Programmable
Z0-3—Programmable
B1—Variable value (BIP-8 Parity)
F1—Programmable
H1-1—01101010
H2-1—00001010 (Pointer value of 522\D)
Y—10011011 (NDF, SS, PTR) - Concatenation indication
1—All ones pattern
H3-1, 2, 3—Default byte value (0xFF)
B2-1, 2, 3—Variable value BIP-24
K1—Programmable
K2—Programmable
S1—Programmable
M1—Variable value (Section FEBE—Number of B2 Errors)

Transmit Direction Overview (continued)

Transport Overhead Access Channel (TOAC) Insert

Path Bytes

J1—64-byte programmable sequence
B3—Variable value BIP-8
C2—Programmable
G1[7:4]—REICNT (B3 errors from receive side)
G1[3]—RDI indication
G1[2:0]—Default value
F2—Programmable
H4[1:0]—Position indicator (multiframe value (00/B to 11/B))
Z3—Programmable
Z4—Default value
Z5—Programmable

All bytes not specified above are either (1) set to the fixed stuff value 0xFF (SDH), or (2) TOAC value inserted, or (3) passed through from the selected AU-3 input, all under user control.

The device will allow the insertion of overhead data from the transmit TOAC under user control.

STS-3/STM-1 (AU-4) Scramble Enable

Scrambling of the STS-3/STM-1 (AU-4) signal is provisionable. A frame synchronous scrambling sequence $1 + x^6 + x^7$ is used.

STS-3/STM-1 (AU-4) B1, B2, and B3 BIP Generation

The device will generate a B1-BIP-8, B2-BIP-24, and a B3-BIP-8 (AU-4 mode only) on the output signal. Each BIP calculator can be programmed to insert an inverted BIP value.

STS-3/STM-1 (AU-4) Loopback Control

The output STS-3/STM-1 (AU-4) signal can be replaced by the receive STS-3/STM-1 (AU-4) signal under software control.

STS-3/STM-1 (AU-4) Output Interface

The transmit STS-3/STM-1 (AU-4) output can be serial at 155.52 Mbits/s, nibble at 38.88 Mbits/s, or byte parallel at 19.44 Mbits/s. The data is clocked out of the device on the rising edge of the clock. This clock can be inverted before leaving the device. When provisioned in the parallel or nibble mode, an even or odd parity bit is generated per transfer.

The output clock, sync, and data signals can be placed in a high-impedance state under user control. Unused outputs in serial and nibble mode will be placed in a high-impedance state automatically by the device.

Receive Direction Overview

The following functions are performed in the receive direction: Input Retime, STS-3/STM-1 (AU-4) Framing, Loss of Signal, Loopback Select Logic, STS-3/STM-1 (AU-4) Frame Synchronous Descrambling, TOAC Drop, B1, B2, and B3 Checking, Monitoring Functions, Pointer Interpretation, Data Demultiplex and Conversion, STS-1/AU-3 Output Byte Control, B1 and B2 Generate, STS-1/AU-3 Output Scramble, and Output Selection Logic.

Input Retime

The device accepts either a serial 155.52 MHz-Mbits/s, nibble 38.88 MHz-Mbits/s, or byte parallel 19.44 MHz-Mbits/s clock-data STS-3/STM-1 (AU-4) input. The user can select on which edge of the clock to retime the data. If in nibble or parallel mode, an odd/even parity bit is verified per transfer; otherwise, this indicator is disabled.

STS-3/STM-1 (AU-4) Framing

The device will frame on the input STS-3/STM-1 (AU-4) signal. The state of the framer as well as any changes to this state will be reported.

Framing Algorithm

The 32-bit (A1-2, A1-3, A2-1, A2-2) framing pattern will be used in the frame detection. The device will be considered out of frame until **two** successive framing patterns separated in time by 125 μs occur without framing byte errors.

The device will be considered in frame until **five (SDH)/four (SONET)** successive frames separated in time by 125 μs occur with errored framing patterns. If the framer transitions to the out-of-frame state, the framer will remain synchronized to the last known frame boundary or the latest detected unerrored framing pattern.

Receive Direction Overview (continued)

STS-3/STM-1 (AU-4) Framing (continued)

The device will be considered in the loss-of-frame state (LOF) when an OOF condition persists for **24** consecutive frames (3 ms). The device will transition out of the LOF state after receiving **24** consecutive frames with the correct framing patterns spaced 125 μs apart and the OOF condition is clear.

Loss of Signal

Before data is descrambled, the device will detect a loss-of-signal condition by monitoring a unique input signal pin or detecting a continuous all-zeros/ones pattern. The device will report this condition to the microprocessor interface.

Loopback Select Logic

The device can be configured to loopback the transmit STS-3/STM-1 (AU-4) or accept the local STS-3/STM-1 (AU-4) signal.

STS-3/STM-1 (AU-4) Frame Synchronous Descrambling

The device will descramble the received SONET/SDH data (minus the first row of SOH) according to the frame synchronous descrambling polynomial; specifically, $f(x) = 1 + x^6 + x^7$. Frame descrambling can be disabled under software control.

TOAC Drop

This channel drops all of the transport overhead bytes from the STS-3/STM-1 (AU-4) signal.

B1, B2, and B3 Checking

The device will monitor the incoming B1, B2, and B3 values for errors. These counters will either count bit or block errors.

Monitoring Functions

The following transport overhead and path overhead bytes are monitored for failures or changes in states ((J0, Z0-2, Z0-3, F1, K1K2 (APS bytes), S1, M1), (J1,C2, G1, F2, H4, Z3, Z5)). The bit error rate of the incoming STS-3/STM-1 (AU-4) signal is calculated to create **signal fail** and **signal degrade** indicators.

Pointer Interpretation

The device will evaluate the current pointer state for the normal state, Path AIS (PAIS) state, or loss of pointer (LOP) conditions, as well as pointer increments and decrements. **This state machine implements the pointer interpretation algorithm described in ETS 300 417-1-1: January 1996 - Annex B.**

Data Demultiplex and Conversion

The device will demultiplex the STS-3/STM-1 (AU-4) signal into three STS-1/AU-3 signals, respectively. In the AU-4 mode, a conversion between the AU-4 payload format and the AU-3 payload format is performed; this requires the location of the J1 byte to be known. In the STS-3 mode, the high-speed signal is byte-demultiplexed and no format conversion occurs.

STS-1/AU-3 Output Byte Control

The output overhead bytes are controlled in one of four ways:

1. Errors can be inserted,

2. Values from the high-speed STS-3/STM-1 signal can be copied or set to the byte default,

3. Values can be inserted under software control, or

4. Values can be inserted under hardware control.

Receive Direction Overview (continued)

STS-1/AU-3 Output Byte Control (continued)

Table 6 shows the specific control allowed for each overhead byte.

Table 6. STS-1/AU-3 Format and Overhead Control Summary

	Transport Overhead			Payload	
	Col. 1	**Col. 2**	**Col. 3**	**Col. 4**	**Col. 5—90**
Row 1	A1	A2[1]	J0[3]	J1[4]	X
Row 2	B1[1]	E1[2]	F1[2, 3]	B3	X
Row 3	D1[2]	D2[2]	D3[2]	C2[4]	X
Row 4	H1[1, 4]	H2[1, 4]	H3[4]	G1[4]	X
Row 5	B2[1]	K1[1, 3]	K2[1, 3]	F2[4]	X
Row 6	D4[2]	D5[2]	D6[2]	H4[4]	X
Row 7	D7[2]	D8[2]	D9[2]	Z3[4]	X
Row 8	D10[2]	D11[2]	D12[2]	Z4	X
Row 9	S1[2]	M0[1, 5]	E2[2]	Z5[4]	X

1. Error insert.
2. Input pass or default value.
3. Software overwrite.
4. Copy of the selected byte from the incoming STM-1 (AU-4) frame; otherwise, the bytes pass without being changed
   (POH can start anywhere within the SPE).
5. Hardware overwrite.

Note: X = don't care (payload).

B1 and B2 Generate

The B1 and B2 values of the outgoing STS-1/AU-3 signal are calculated. An error byte can also be forced into the B1 and B2 values on a per STS-1/AU-3 basis.

STS-1/AU-3 Output Scramble

The device allows scrambling of the output signals on a per-output basis.

Output Selection Logic

The demultiplexed signals can be routed to any output port or can be multicast to more than one port under software control.

Output Data Formatter

The device outputs one clock at 19.44 MHz, one J0 time signal, an 8-bit data bus, and an odd/even parity bit. The bus can be shared with up to three other devices. Each device determines its time slot using the J0 time signal. The byte coincident with the J0 time sync signal is always available for device number 1; subsequent bytes are available for device 2, device 3, and then device 1 again. The sense of the 19.44 MHz output clock can be inverted under user control.

Typical Uses

Section and Line Termination Multiplex

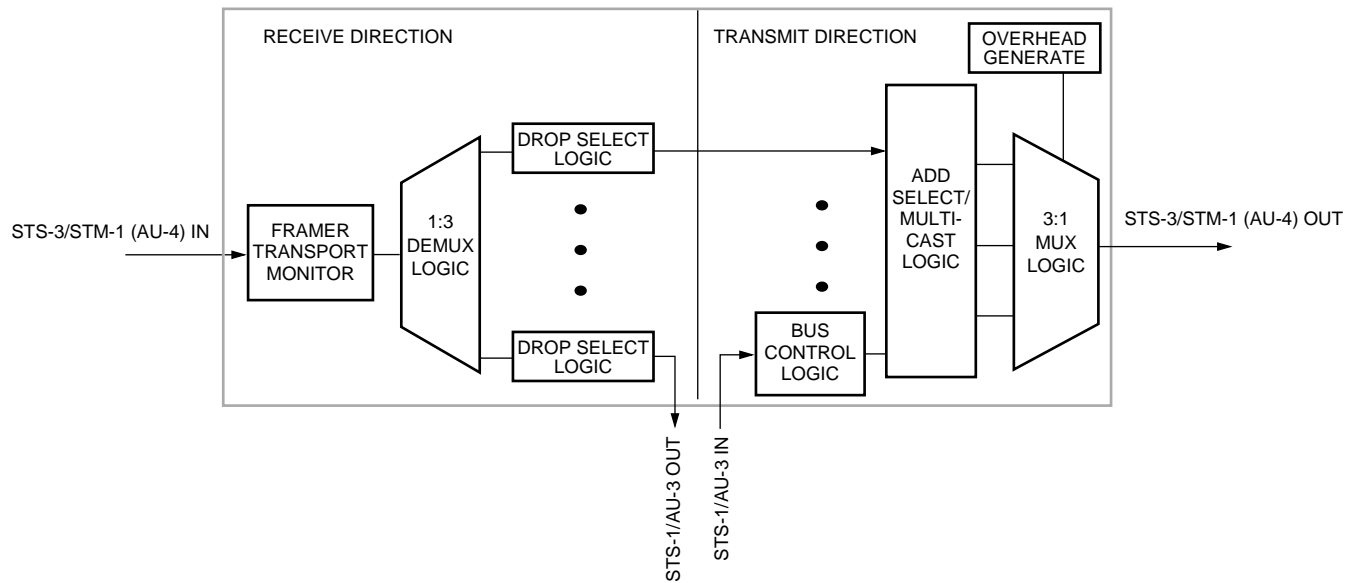Using the device without internal loopbacks results in a multiplex/demultiplex operation.
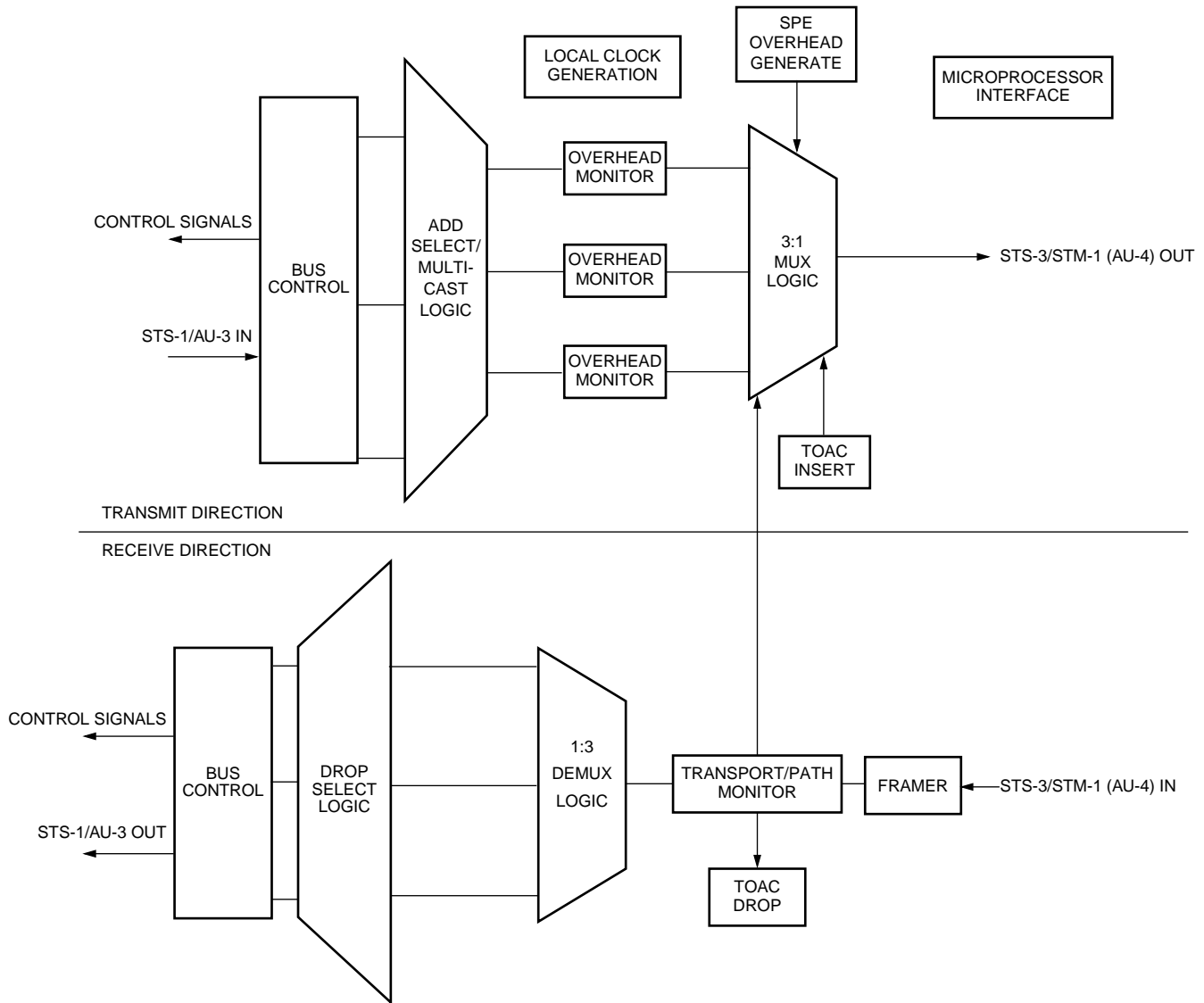
5-5296(F)r.10

Figure 2. Line Termination Multiplex

Typical Uses (continued)

Add/Drop Multiplex

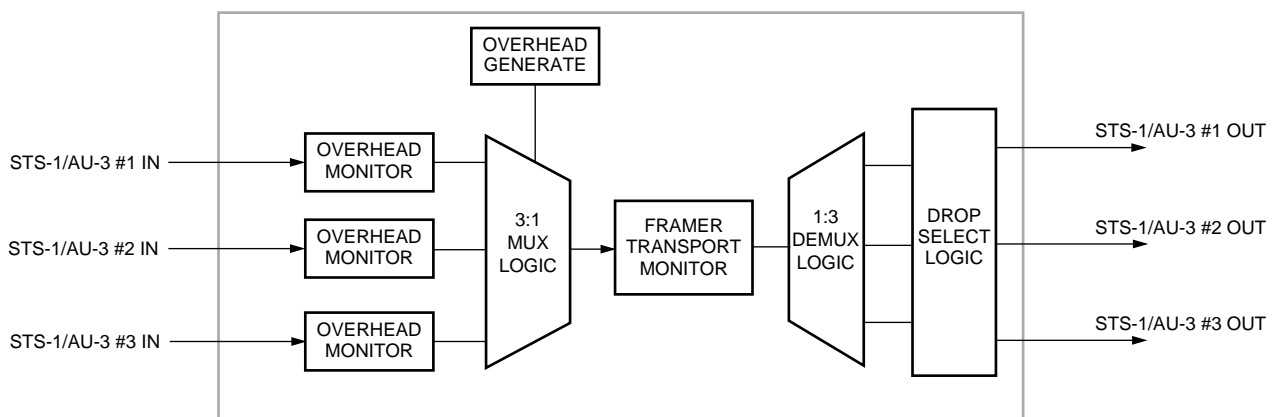Using the device with STS-1/AU-3 internal loopbacks results in an add/drop multiplex.

5-5297(F)r.7

Figure 3. Add/Drop Multiplex

Digital Cross Connect

Using the device with STS-3 internal loopback results in a digital cross connect.

5-5298(F)r.3

Figure 4. Digital Cross Connect

For additional information, contact your Microelectronics Group Account Manager or the following:

INTERNET: **http://www.lucent.com/micro**
E-MAIL: **docmaster@micro.lucent.com**
U.S.A.: Microelectronics Group, Lucent Technologies Inc., 555 Union Boulevard, Room 30L-15P-BA, Allentown, PA 18103
1-800-372-2447, FAX 610-712-4106 (In CANADA: **1-800-553-2448**, FAX 610-712-4106)
ASIA PACIFIC: Microelectronics Group, Lucent Technologies Singapore Pte. Ltd., 77 Science Park Drive, #03-18 Cintech III, Singapore 118256
Tel. (65) 778 8833, FAX (65) 777 7495
JAPAN: Microelectronics Group, Lucent Technologies Japan Ltd., 7-18, Higashi-Gotanda 2-chome, Shinagawa-ku, Tokyo 141, Japan
Tel. (81) 3 5421 1600, FAX (81) 3 5421 1700
EUROPE: Data Requests: MICROELECTRONICS GROUP DATALINE:**Tel. (44) 1189 324 299**, FAX (44) 1189 328 148
Technical Inquiries: GERMANY: **(49) 89 95086 0** (Munich), UNITED KINGDOM: **(44) 1344 865 900** (Bracknell),
FRANCE: **(33) 1 41 45 77 00** (Paris), SWEDEN: **(46) 8 600 7070** (Stockholm), FINLAND: **(358) 9 4354 2800** (Helsinki),
ITALY: **(39) 2 6601 1800** (Milan), SPAIN: **(34) 1 807 1441** (Madrid)

m i c r o e l e c t r o n i c s   g r o u p

February 1998
PN98-058TIC (Replaces PN97-123TIC)

Lucent Technologies
Bell Labs Innovations