Video Encoder

FEATURES

- Fully CCIR 624 performance compliance NTSC and PAL (B,D,G,H,I,M and N) video encoder
- Composite, S-video, Component Y/Cb/Cr (Sony, Matsushita, and SMPTE) or RGB output.
- Triple 10-bit digital to analog converter.
- Accepts 27 Mhz multiplexed 8-bit digital video inputs.
- Master or Slave 4-Field NTSC or 8-Field PAL video timing generation.
- CCIR 656 EAV SYNC extraction.
- Automatic NTSC or PAL timing detection in slave mode operation.
- Automatic or User Programmable Chroma Filter Selection.
- Macrovision Anti-Tapping Rev 7.01 support in AV3168 Only.
- Closed Caption Support.
- Contrast and Brightness control.

Clock Generation

- 3 outputs for 27 MHz video clock, 16.934, 18.432 and 36.864 Mhz audio clock, and 40.5, 54.0, 67.5 and 81.0 MHz general purpose clocks.
- Requires a single 27 Mhz crystal.

General

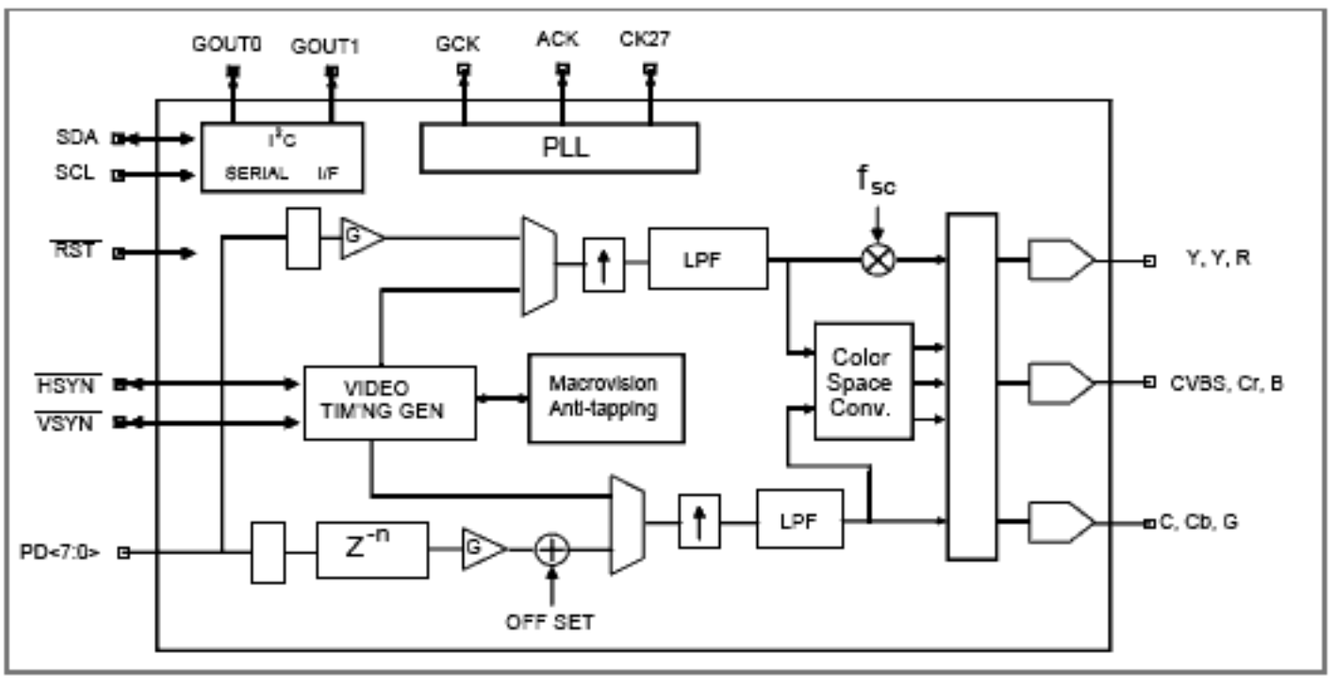
- CVBS and S-video DAC power down controls.
- I^2C compatible serial control bus.
- Single +5 volt power supply.

Application

- Digital Video Disk (DVD)
- Digital Set-Top Box
- PC Video, Multimedia

Ordering Information

AV3168/69-CL 44-pin PLCC



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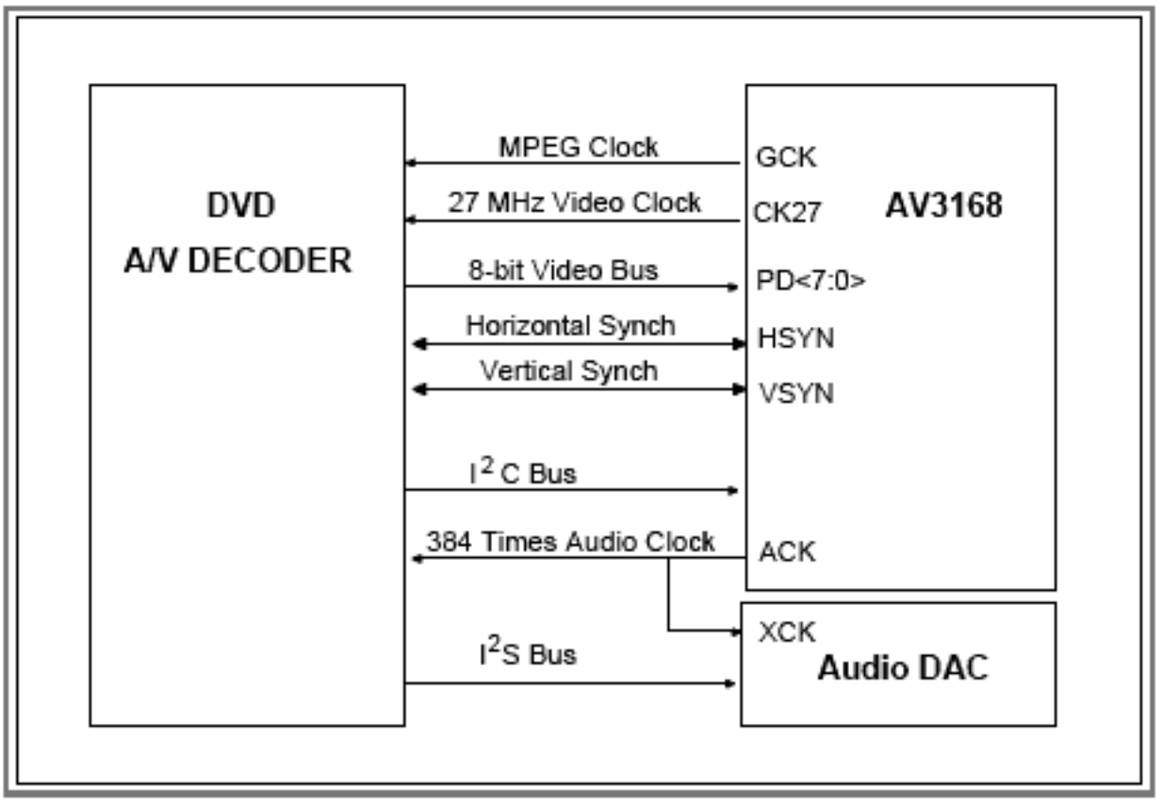
DESCRIPTION

The AV3168 is a mixed signal CMOS monolithic device. It comprise with a PAL and NTSC Video Encoder, Color Space Converter and Clock Generator, The Clock Generator outputs a video, an audio and a programmable general purpose clock. This IC implemented Macrovision Anti-tapping 7.01, intended for DVD and Settop Box applications.

The video encoder converts CCIR 601 8-bit multiplexed digital video into RGB, component YCbCr, encoded NTSC or PAL (BDGHIMN) signals. It contains three 10-bit DACs to support simultaneous S-video and composite video; or component video display. Brightness and Contrast control are also provided.

The Clock Generator outputs three clocks for video, audio and system to simplify the system configuration and maintain A/V synchronization.



Typical Application Connection

VIDEO PERFORMANCE

Item		Specification	
1	Attenuation of Luminance Signal	0 - 5 Mhz	+/- 0.1 dB
		6 Mhz	> 3dB
		9 Mhz	> 35 dB
2	Attenuation of NTSC Color Difference Signal	0.4 MHz	< 1dB
		1 MHz	5 dB
		2 MHz	> 25 dB
3	Attenuation of PAL Color Difference Signal	1.3 MHz	< 2dB
		3.6 MHz	> 20dB
4	Attenuation of Component Color Difference Signal	2 MHz	< 3 dB
		5 MHz	> 38 dB
5	Luma SNR		> 82 dB
6	Chroma SNR	AM	> 64 dB
		PM	> 60 dB
7	Differential Gain		< 0.5%
8	Differential Phase		< 1 degree
9	Y/C Delay		+/- 2 nsec.
10	Y/C Gain inequality		+/- 2%
11	Y/C Intermodulation		< 0.7 IRE
12	SCH		< 4 degree

AV3168 Detailed Block Diagram

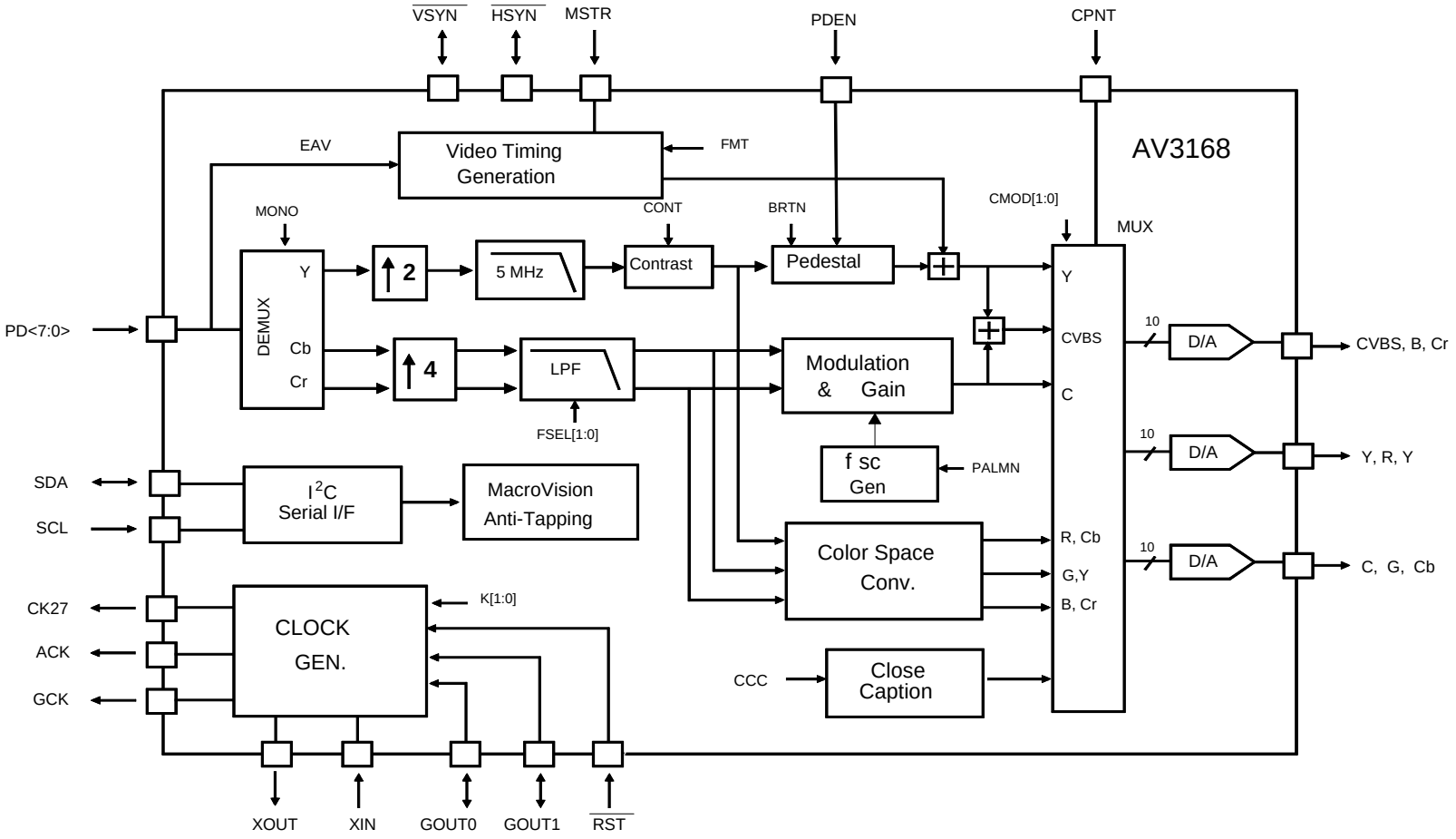
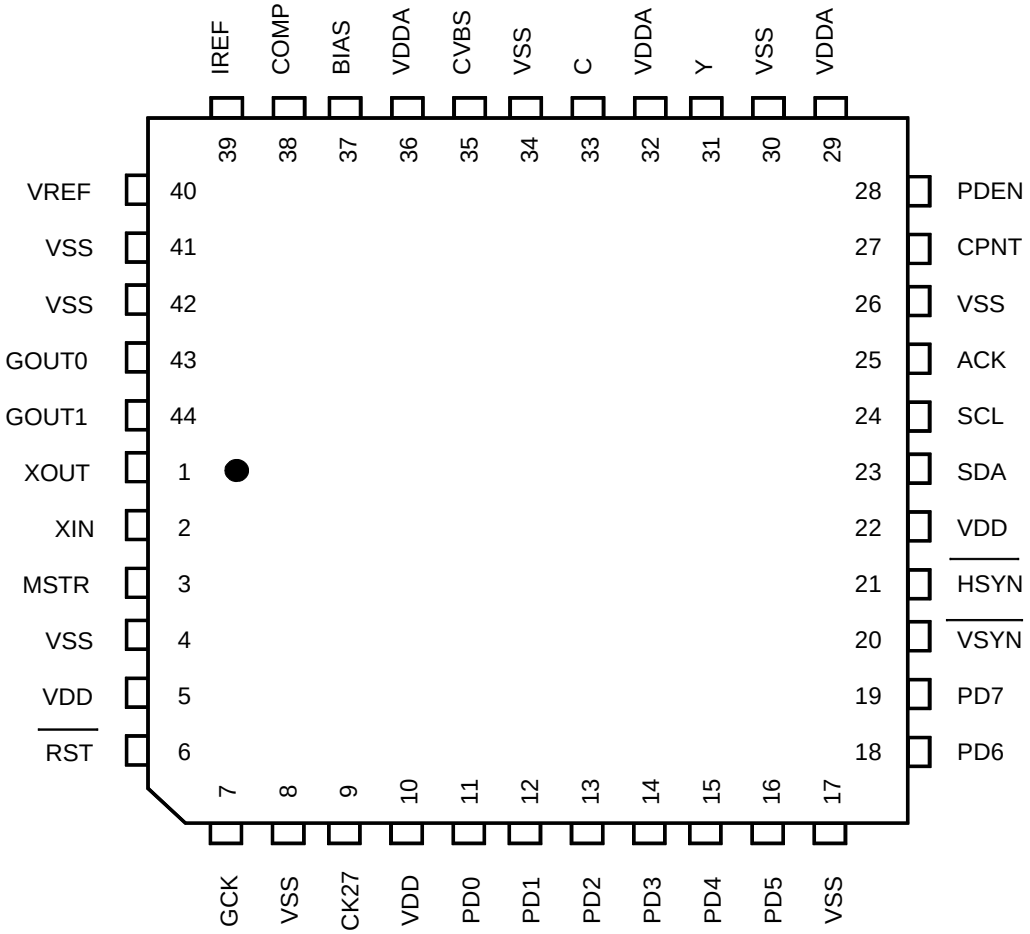


Figure 1

PIN DESCRIPTIONS



PIN DESCRIPTIONS

Pin Name	Pin #	Type	Description
DIGITAL VIDEO INPUT			
PD<7 -0>	11-16 18-19	I	Multiplexed Cb, Y, and Cr digital video input bus.
$\overline{\text{HSYN}}$	21	I/O	In Slave Mode (MSTR pin is low) Horizontal Synch input. In Master Mode (MSTR pin is high) Horizontal Synch output.
$\overline{\text{VSYN}}$	20	I/O	In slave mode (MSTR pin is low) Vertical Sync input. In master mode Vertical Sync output.
VIDEO CONTROL SIGNALS			
MSTR	3	I	Master Mode; If this pin is high, the chip outputs horizontal and vertical sync signals. Otherwise it receives both horizontal and vertical sync signals.
CPNT	27	I	Select either component or composite video output. 0: Simultaneous Composite and S-Video output. 1: Component video output either RGB or YCbCr determined by the register CR0[5:4].
PDEN	28	1	Pedestal enable pins. When this pin is high 7.5 IRE is added for the NTSC composite analog output.
VIDEO ANALOG OUTPUT, REFERENCE AND COMPENSATION			
CVBS	35	O	Analog video output Determined by the state of CPNT pin and CR0[5:4] CPNT CR0[5] CR0 [4] 0 X X: Composite video output 1 X 0: Cr output in YCbCr component mode 1 0 X: : 1 1 1: Blue color output in RGB mode
Y	31	O	Analog video output Determined by the state of CPNT pin and CR0[5:4] CPNT CR0[5] CR0 [4] 0 X X: S-Video Y output. 1 X 0: Y output in YCbCr component mode 1 0 X: : 1 1 1: R color output in RGB mode

PIN DESCRIPTIONS (Continued)

Pin Name	Pin #	Type	Description
C	33	O	Analog video output Determined by the state of CPNT pin and CR0[5:4] CPNT CR0[5] CR0 [4] 0 X X: S-Video C output. 1 X 0: Cb output in YCbCr component mode 1 0 X: : 1 1 1: Green color output in RGB mode
VREF	40	I/O	Voltage reference. It has an internal voltage reference circuit, but may be overridden by an external voltage reference input. A 0.1 uF ceramic capacitor is required between this pin and GND.
IREF	39	I	A resistor should be connected between this pin and GND to control the DAC output current. The recommended value is 198 (382) ohm 1% metal film resistor for double (single) end 75 ohm termination.
COMP	38	I	Compensation capacitor for the DAC internal reference amplifier. A 0.1 uF ceramic capacitor is required between this pin and VDDA.
BIAS	37	I/O	DAC bias voltage. A 0.1 uf ceramic capacitor must be used to de-couple this pin to VDDA.

SERIALCONTRL BUS

SCL	24	I	Serial bus clock
SDA	23	I/0	Serial bus address and data input and output pin. Open drain output.

CLOCK SIGNALS

GCK	7	O	General Purpose Clock. Clock frequency is determined by the state of GOUT[1:0] when $\overline{RST}$ pin is low. 00 : 40.5 MHz clock output. 0 1: 54.0 MHz clock output. 1 0: 67.5 Mhz clock output. 1 1: 81.0 MHz
CK27	9	O	27 MHz clock output pin.
ACK	25	I/O	384*fs Audio clock output pin. Controlled by CR2[1:0] 0 0: 384 * 48.0 KHz (18.432MHz) clock output. 0 1: 384 * 44.1 KHz (16.934MHz) clock output. 1 0. 384 * 96.0 KHz (36.864MHz) clock output. 1 1: 384 * 88.2 KHz (33.868MHz) clock output.

PIN DESCRIPTIONS (Continued)

Pin Name	Pin #	Type	Description
XIN	2	I	27 Mhz oscillator input
XOUT	1	O	27 Mhz oscillator output

MISCELLANEOUS SIGNALS

$\overline{RST}$	6	I	Active low chip reset input. Chip is in the power down mode when the $\overline{RST}$ is low.
GOUT1	44	I/O	Dual function pin. GCK frequency select pin when $\overline{RST}$ is low. General purpose output pin when $\overline{RST}$ is high
GOUT0	43	I/O	Dual function pin. GCK frequency select pin when $\overline{RST}$ is low. General purpose output pin when $\overline{RST}$ is high

POWER AND GROUND

VDD	10, 22, 5	+5V	Digital power supply.
VSS	8, 17, 26, 30, 34, 41, 42, 4	GND	Digital ground
VDDA	29, 32, 36.	+5V	Analog video power supply.

VIDEO TIMING GENERATION

The video encoder can operate as a master or a slave in the timing generation. In the master mode, the video encoder outputs SYNC signals. In the slave mode, the internal timing is lock to the external SYNC signals.

MASTER MODE

If the *MSTR* pin is high, the video encoder operates in the master mode. It uses the internal counters to generate the video timing and outputs HSYN and VSYN. The HSYNs are asserted for 64 pixel times. The negative transition of the HSYNs occur in the Cb slot.

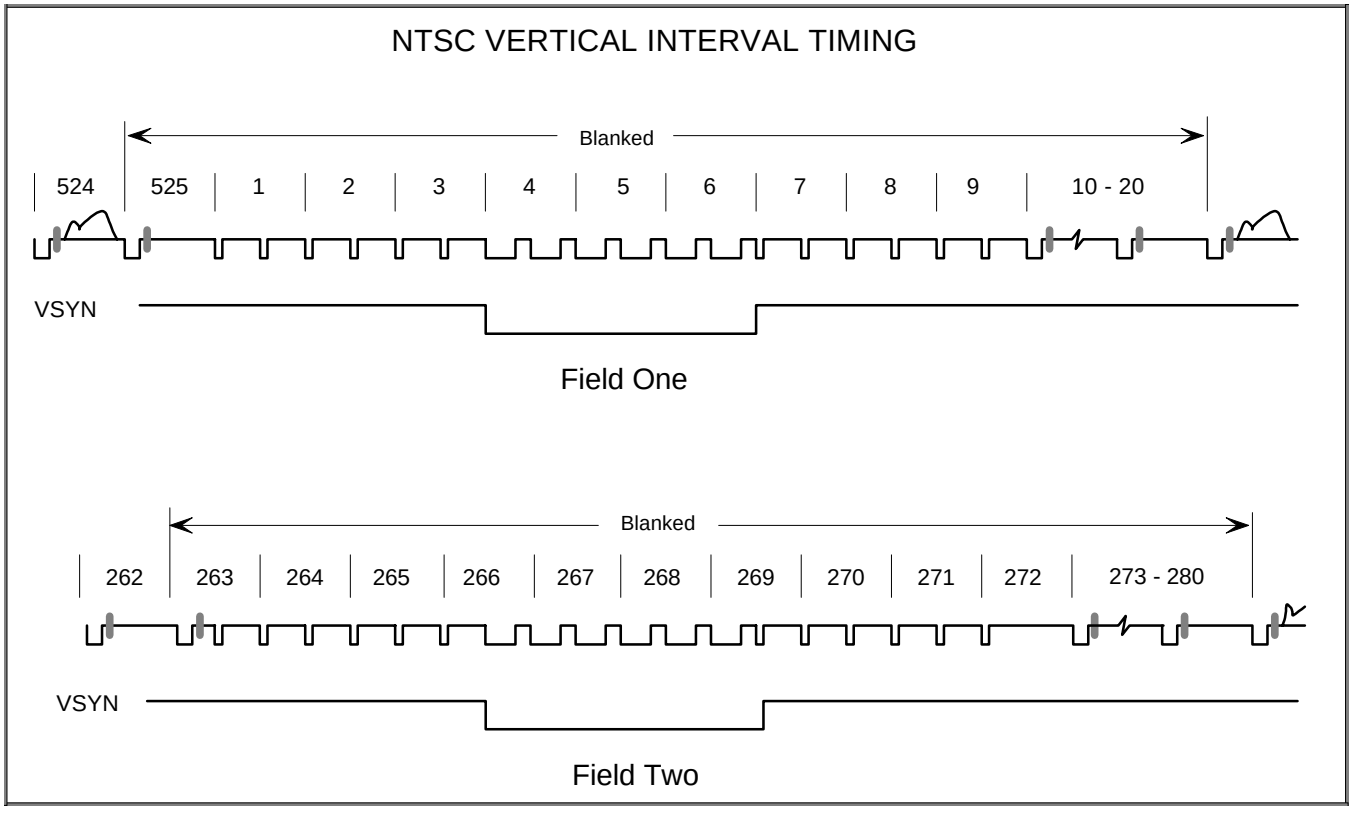
The VSYNs are asserted for 3 line times for NTSC and 2.5 for PAL. The co-incident negative transitions of HSYN and VSYN indicate the beginning of an odd field. The negative transition of the VSYN while the HSYN is high indicates the beginning of an even field.

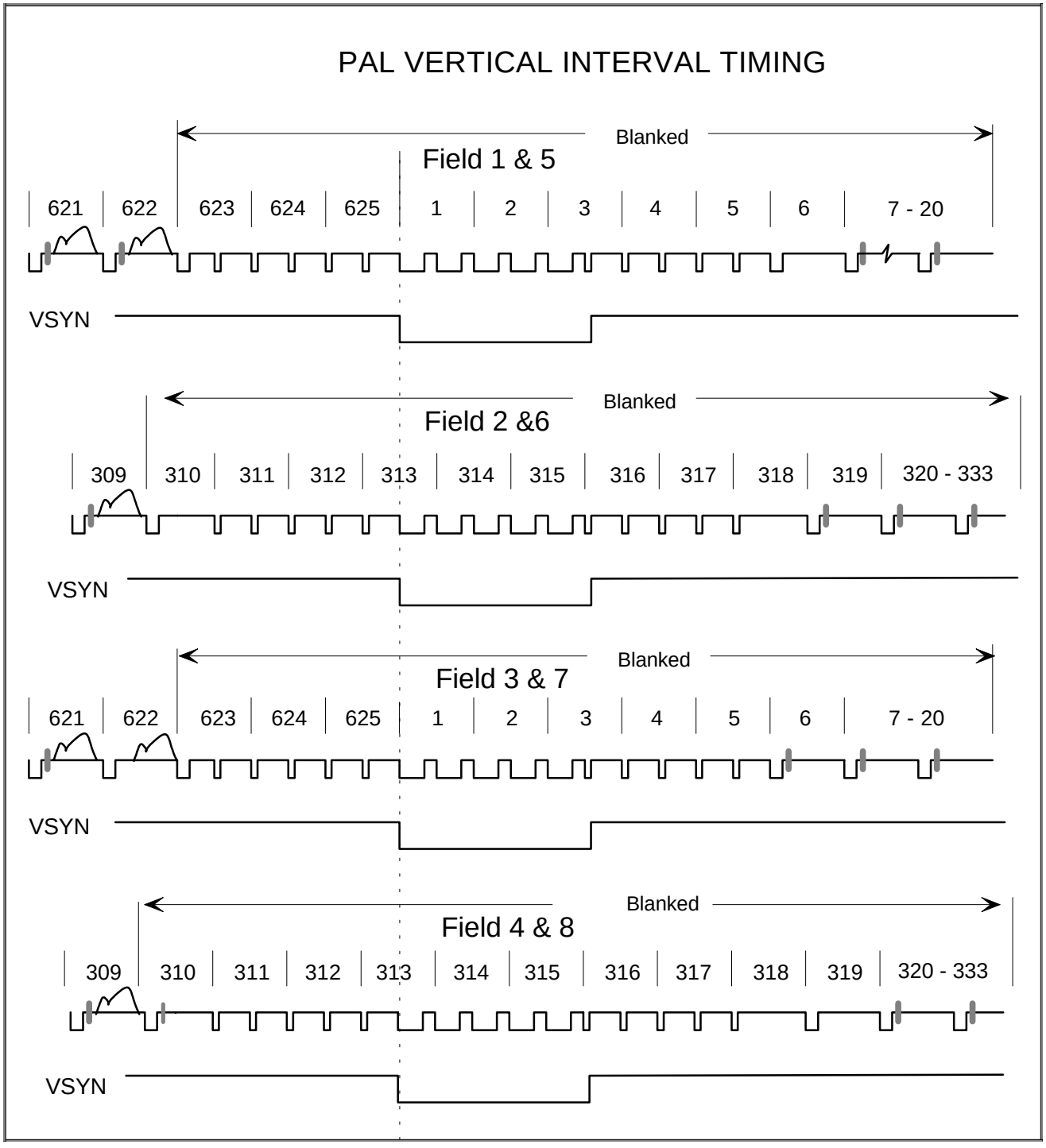
SLAVE MODE

In the slave mode operation, the decoder automatically detects the input format and locks the internal timing counters to the external synchronization signals. It support 2 types of synch inputs: (a) HSYN / VSYNC, or (b) CCIR656 EAV data.

If EAV is present, the video encoder synchronized to the EAV packets according to CCIR656 specifications to generate the video timing. HSYN and VSYN signals are ignored.

If EAV is not present, the Video Encoder uses the signals presented on HSYN and VSYN for line and field counter increment. If register CR0[3] is low the encoder assumes the negative transition of the HSYN should be co-incited with the Cb0 datum. If CR0[3] is high it assume the transition co-incited with Y0 datum.




PAL VERTICAL INTERVAL TIMING
Blanked
Field 1 & 5
621
622
623
624
625
1
2
3
4
5
6
7 - 20
VSYN
Blanked
Field 2 &6
309
310
311
312
313
314
315
316
317
318
319
320 - 333
VSYN
Blanked
Field 3 & 7
621
622
623
624
625
1
2
3
4
5
6
7 - 20
VSYN
Blanked
Field 4 & 8
309
310
311
312
313
314
315
316
317
318
319
320 - 333
VSYN

LUMINANCE PROCESSING

The luminance, Y, are interpolated to 27 Mhz sampling rate through a multi-tap linear poly-phase filter. The filter frequency response is flat from 0 to 5 MHz. Contrast and Brightness control are provided for minor adjustment only.

Contrast Control

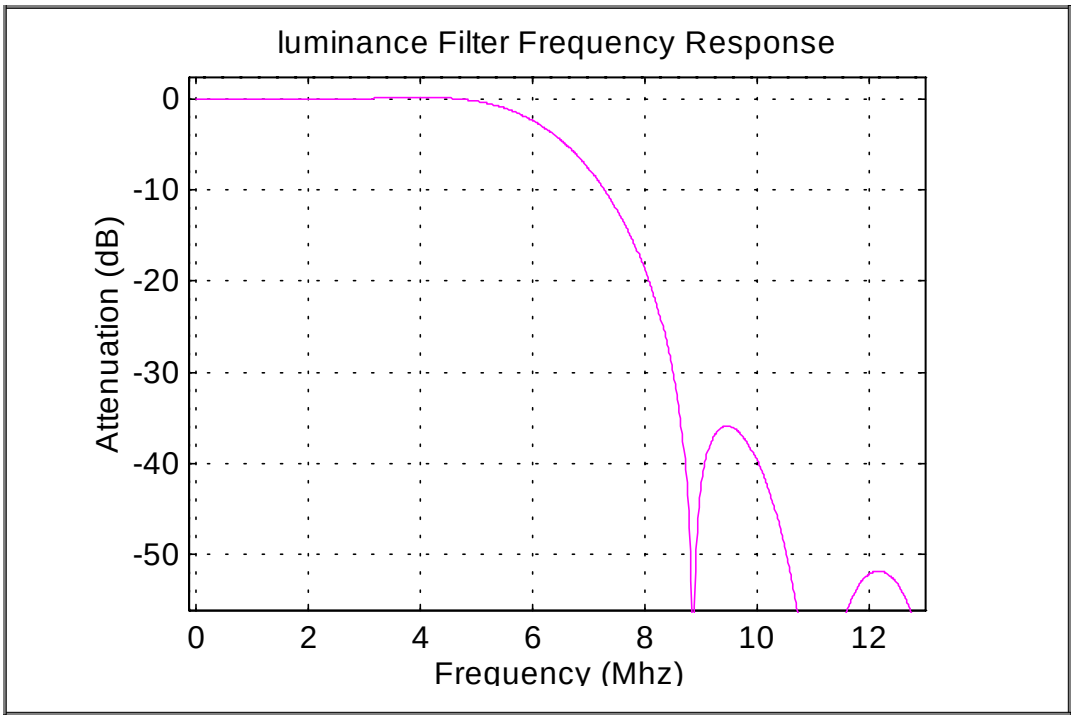
Item	CREG1<1:0>	Contrast
1	00	Normal
2	01	Less Contrast
3	10	Least Contrast
4	11	High Contrast

.

Brightness Control

Item	CREG1<3:2>	Contrast
1	00	Normal
2	01	Modest Brightness
3	10	High Brightness
4	11	Less Brightness

LUMINANCE FILTER



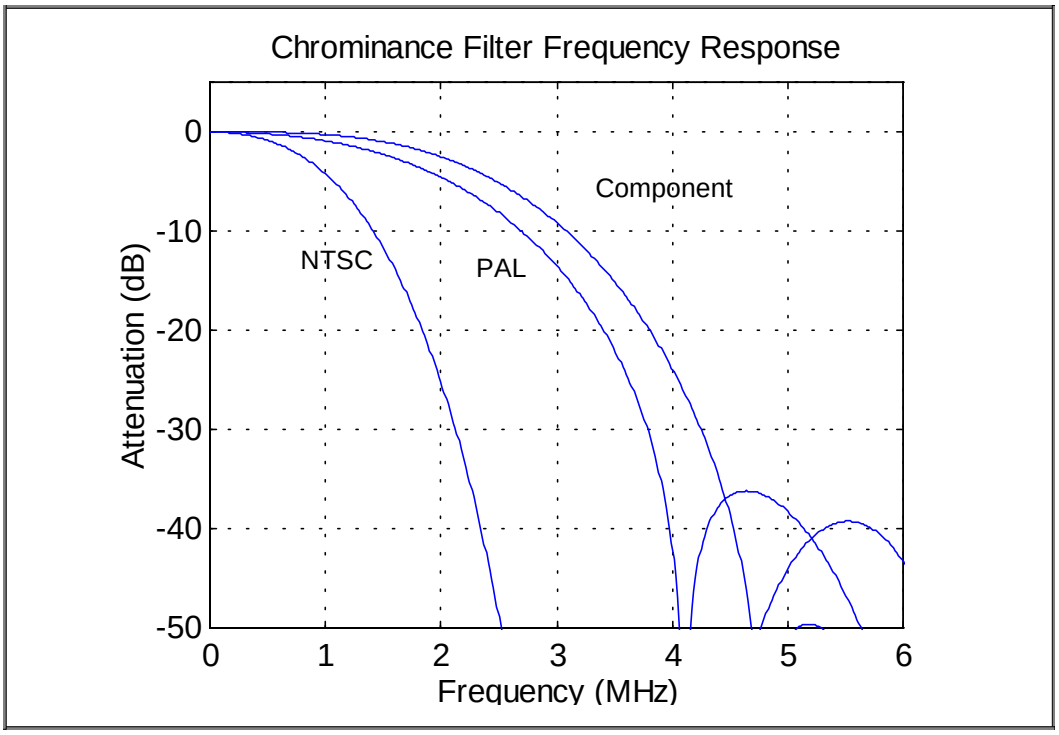
CHROMINANCE PROCESSING

The Cb and Cr signals are filtered and interpolated to 27 Mhz. The filter has 3 bandwidth: 0.675, 1.3 or 2 MHz. The filter bandwidth can be either auto select or user select via control register CREG<7:6>.

Chroma Filter Bandwidth Control

Item	CREG2<7:6>	Chroma Bandwidth
1	00	auto-select
2	01	0.675 Mhz
3	10	1.375 MHz.
4	11	2.0 MHz

CHROMINANCE FILTER



CLOCK FREQUENCY CONTROL

The system clock, GCK, output frequency is determined by the state of two general purpose output pins (GOUT0 and GOUT1) while the $\overline{RST}$ pin is low. The output frequencies are.

System Clock

Item	GOUT<1:0>	Frequency (MHz)
1	00	40.5
2	01	54.0
3	10	67.5
4	11	81.0

The ACK outputs 384 times 40.5, 48 or 96 KHz audio clock. The clock frequency is selected via Control Register. CR2 <1:0>

.

Audio Clock

Item	CR2<1:0>	Audio Sampling Frequency (KHz)	Clock Frequency (MHz)
1	00	48.0	18.432
2	01	44.1	16.934
3	10	96.0	36.864
4	11	88.2	33.869

CONTROL and CLOSED CAPTION REGISTER DESCRIPTION

The AV3168 contains three 8-bit registers for timing generation, luma and chroma processing control, clock generation and power management. Additionally it contains 4 Closed Caption Data Registers. These registers are programmed via the 7-bit address I^2C bus. I^2C Address = 0X65. *(I2C bus Address = 0x64 for AV3169*). The protocol is 7- bit chip address followed by 8- bit register address and 8-bit register data.

Control Register 0, CR0 (Address: 0x0, Default Value: 0x00)

Item	Register Bits	Mnemonic	#bits	Description
1	CR0[7:6]	FSEL[1:0]	2	Chroma Filter Selection 00: Automatic bandwidth assignment based on the output format selection (default) 01: 0.675 MHz bandwidth 10: 1.36 MHz bandwidth 11: 2 MHz bandwidth
2	CR0[5:4]	CMOD[1:0]	2	Component Output Selection. Valid only If pin 27 CPNT pin is '1'. 00: Sony Betacam (Default) 01: Mashushita M-II 10: SMPTE 11: RGB
3	CR0[3]	SDLY	1	Input Hsyn negative transition position 0: The Negative HSYNC transition coincided with Cb_0 datum (Default) 1: The Negative HSYNC transition co-incited with Y_0 datum.
4	CR0[2]	SCH	1	Subcarrier horizontal sync phase control (SCH) 0: Subcarrier reset every 4 fields for NTSC and every 8 field for PAL (Default), SCH =0 according CCIR 624 Spec. 1: Subcarrier free running.
5	CR0[1]	PALMN	1	Enable South American PALM and PALN 0: Non-South American Mode, PAL(BDGHI), or NTSC (Default). 1: South American Mode (Pal-M, Pal-N)
6	CR0[0]	FMT0	1	Used in master mode only to select either 525 or 625 line system timing. 0: 525-line M system (Default) 1: 626-line system.

Control Register 1, CR1 (Address: 0x01, Default Value: 0x00)

Item	Register Bits	Mnemonic	#bits	Description
1	CR1[7]	VBIOFF	1	Vertical Blanking Interval disable. 1: Vertical interval (VBI) is not blanked 0: VBI Blanked (Default) For M system line 1-21, 262-284, 525 are blanked. For 625 line system line 1-22, 311-335, 624 - 625 are blanked.
2	CR1[6:5]	CCC	2	Close Caption enable 00: Disable Closed Caption Data (Default) 10: Enable Closed Caption Data on odd field only. 01: Enable Closed Caption Data on even field only. 11: Enable Closed Caption Data on all fields
3	CR1[4]	YDLY	1	Luma Delay Control 0: Luma output not delayed (Default) 1: Luma output delayed by 74ns
4	CR1[3:2]	BGT	2	Brightness Control 00: Brightness Control Off (Default) 01: Moderate Brightness Gain 10: Most Brightness Gain 11: Least Brightness Gain
5	CR1[1:0]	CON	2	Contrast Control 00: Contrast Control Off (Default) 01: 15/16 * Luma Gain 10: 14/16 * Luma Gain 11: 17/16 * Luma Gain

Control Register 2, CR2 (Address: 0x02, Default Value: 0x00)

Item	Register Bits	Mnemonic	#bits	Description
1	CR2[7]	BW	1	Monochrome Display 0: Color Display (Default) 1: Monochrome Display
2	CR2[6]	PWDCV	1	Composite DAC Power Down control. 0: Enable CVBS DAC (Default) 1: Power Down CVBS DAC
3	CR2[5]	PWDYC	1	S-video DACs Power Down control. 0: S-video DAC On (Default) 1: S-video DAC Power Down

Control Register 2, CR2 (Address: 0x02, Default Value: 0x00)

Item	Register Bits	Mnemonic	#bits	Description
4	CR2[4]	GOUTEN	1	General purpose register GOUT<1:0> Output Enable. 0: Pin 44 and 43 in high impedance state. 1: Gout<1:0> are output to pin 44 and 43.
5	CR2[3:2]	GOUT[1:0]	2	General purpose output registers. These registers connected to pin 44 and 43 respectively.
6	CR2[1:0]	K[1:0]	2	Audio clock, ACK, output frequency select 00: 48 * 384 KHz 01: 44.1 * 384 KHz 10: 96.0 * 384 KHz 11: 88.2 * 384 KHz

Extended Closed Caption Register 0 (Address: 0x03, Default Value: 0x00)

Register	Mnemonic	#bits	Description
ECC[15:8]	ECC[15:8]	8	Extended Closed Caption Data (Upper byte)

Extended Closed Caption Register 1 (Address: 0x04, Default Value: 0x00)

Register	Mnemonic	#bits	Description
ECC[7:0]	ECC[7:0]	8	Extended Closed Caption Data (Lower byte)

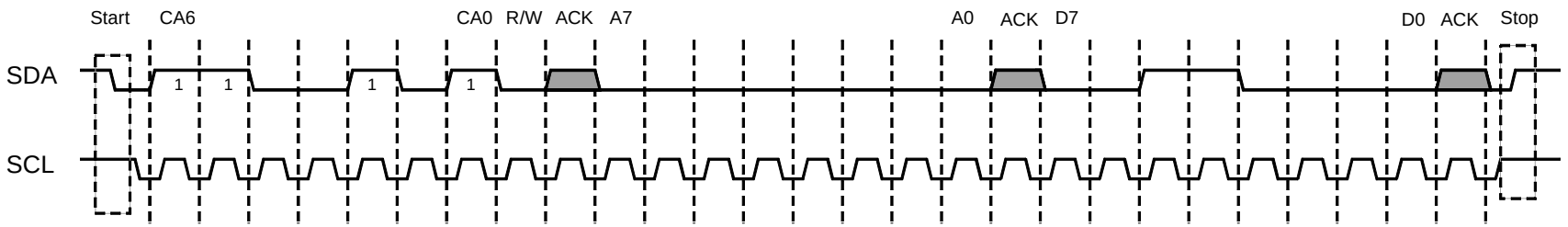
Closed Caption Register 0 (Address: 0x05, Default Value: 0x00)

Register	Mnemonic	#bits	Description
CC[15:8]	CC[15:8]	8	Closed Caption Data (Upper byte)

Closed Caption Register 1 (Address: 0x06, Default Value: 0x00)

Register	Mnemonic	#bits	Description
CC[7:0]	CC[7:0]	8	Closed Caption Data (Lower byte)

I^{2}C Bus Control Register write example:

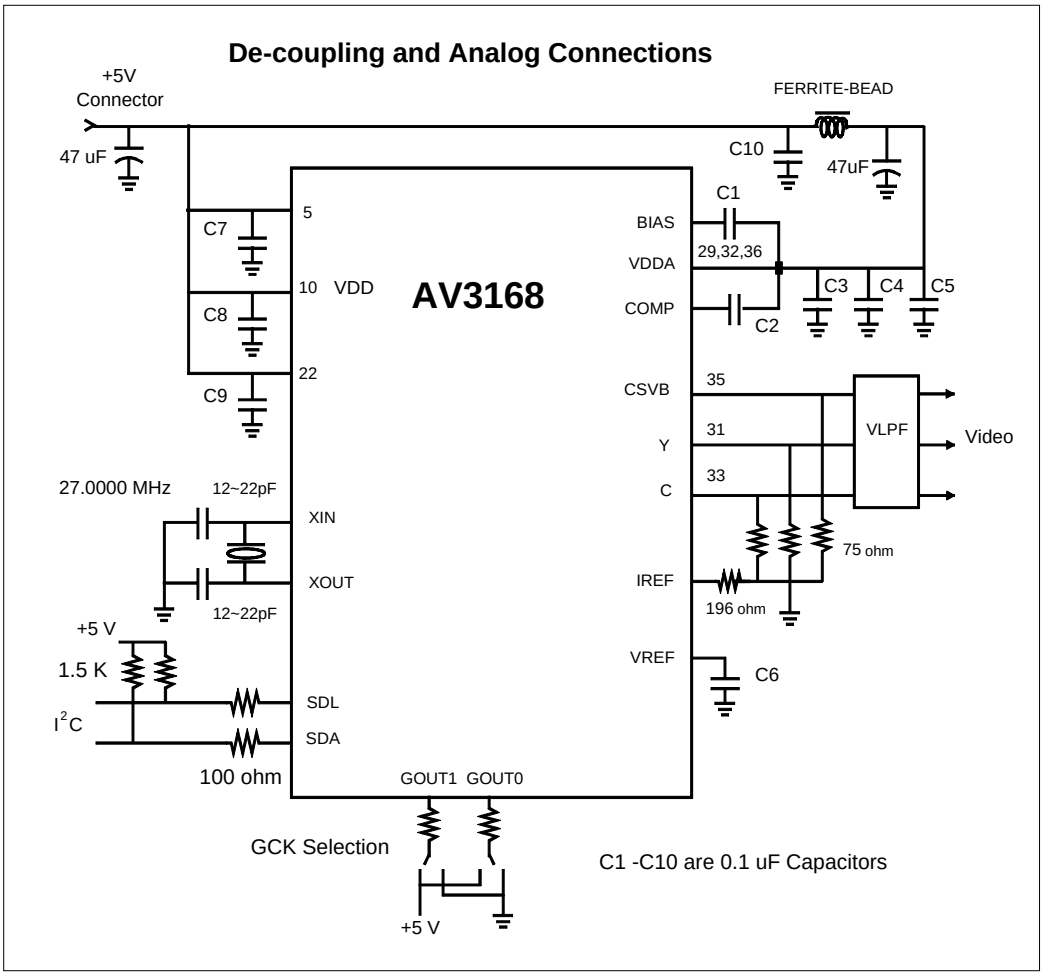


Chip adrress: CA<6:0> = 65H

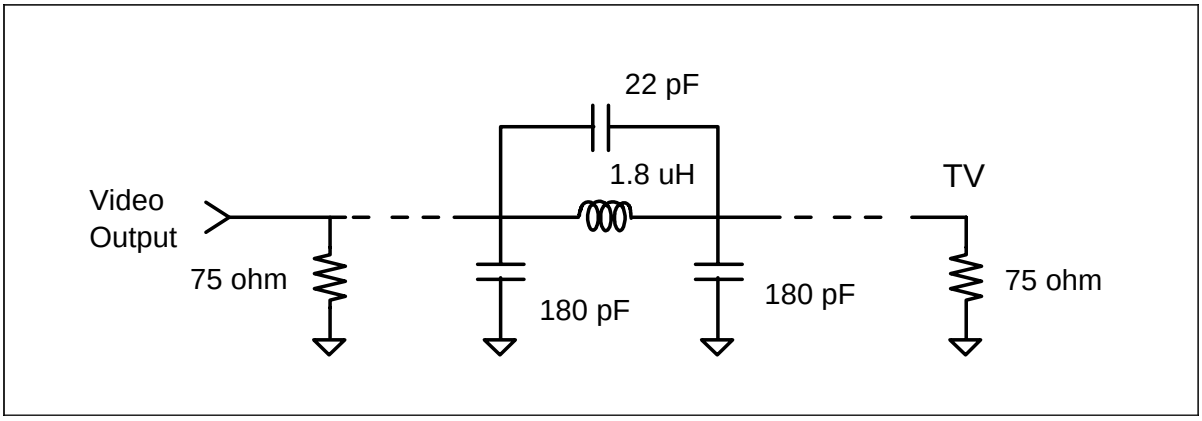
Register address: A<7:0> = 00H

DATA: D<7:0> = 30H

APPLICATION CIRCUIT



Reconstruction Filter (VLPF) for The Double End 75 Ohm Termination



DIGITAL VIDEO INPUT PORT TIMING DIAGRAM

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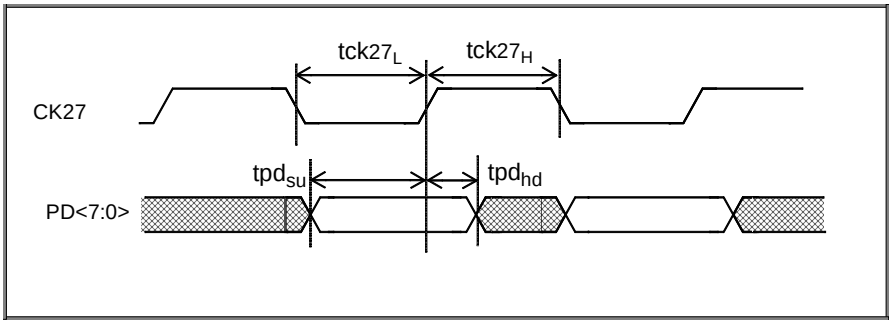

Figure 1: Pixel Bus

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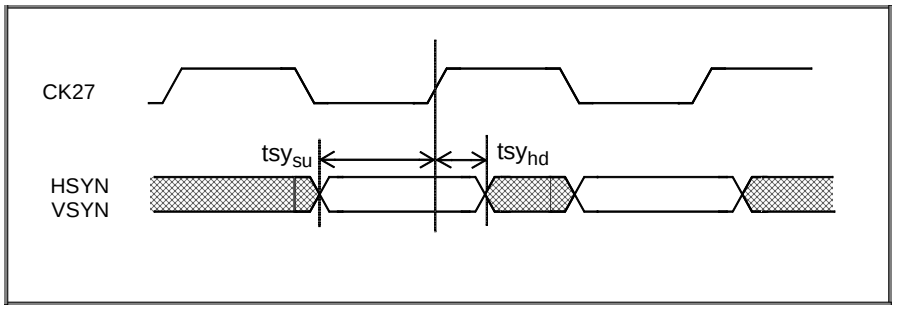


Figure 2: Horizontal Sync and Vertical Sync Signals

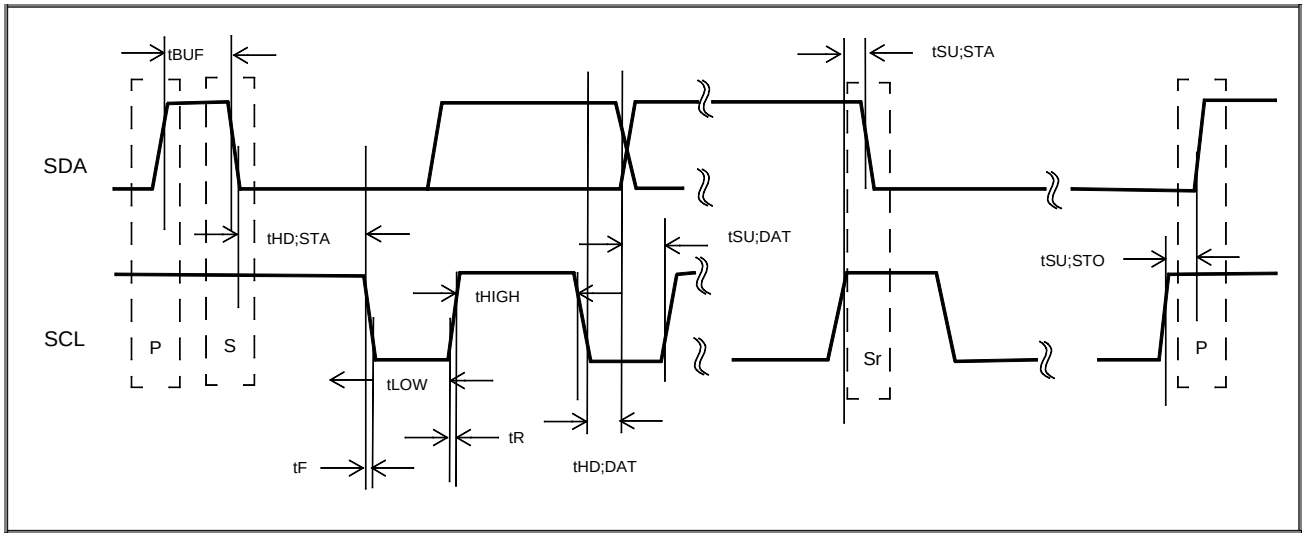


Figure 3: I 2C Serial Port Timing

ABSOLUTE MAXIMUM RATINGS

Symbol	Characteristics	Min	Max	Units
V_{DD}	Power Supply Voltage (Measured to GND)	-0.5	+7.0	V
V_i	Digital Input Applied Voltage[2]	GND-0.5		V
A_i	Digital Input Forced Current[3,4]	-100	100	mA
V_o	Digital Output Applied Voltage[2]	GND-0.5	V_{DD}+0.5	V
A_o	Digital Output Forced Current[3,4]	-100	100	mA
TDsc	Digital Short Circuit Duration (single output high state to Vss)		1	Sec
TA_{SC}	Analog Short Circuit Duration (single output to VSS1)		infinite	Sec
T_a	Ambient Operating Temperature Range	-25	+125	^oC
Tstg	Storage Temperature Range	-65	+150	^oC
T_j	Junction Temperature (Plastic Package)	-65	+150	^oC
Tsol	Lead Soldering Temperature (10 sec., 1/4” from pin)		300	^oC
Tvsol	Vapor Phase Soldering (1 minute)		220	^oC
T_{stor}	Storage Temperature	-65	+150	^oC

Notes:

1. Absolute maximum ratings are limiting values applied individually, while all other parameters are within specified operating conditions.

2. Applied voltage must be current limited to specified range, and measured with respect to VSS.

3. Forcing voltage must be limited to specified range.

4. Current is specified as conventional current, flowing into the device.

RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristics	Min	Typical	Max	Units
V_{DD}	Power supply voltage	4.35	5	5.25	V
V_{ref}	Reference voltage		1.235		V
Iref	Reference current		3.15		mA
R_L	Analog output load		37.5	70	Ω
T_a	Ambient operating temperature range	0		70	°C

ELECTRICAL CHRACTERISTICS

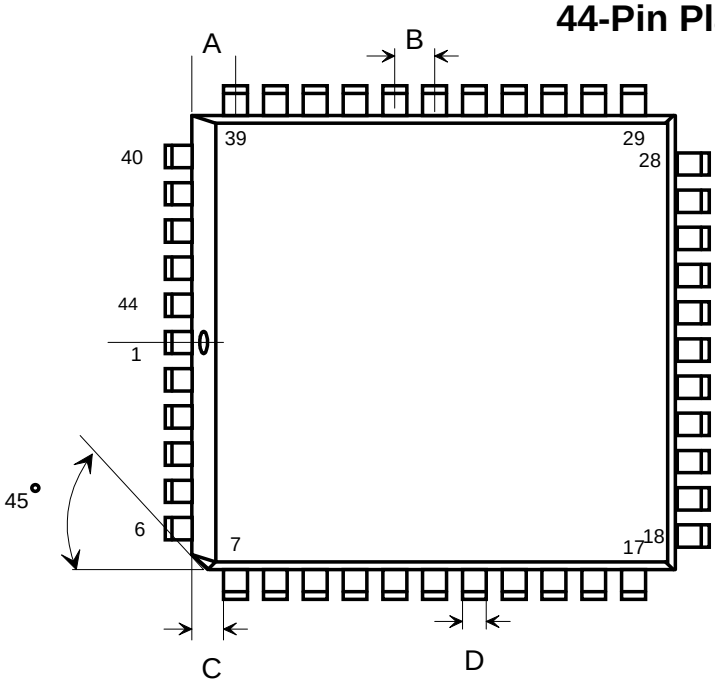
Symbol	Characteristics	Min	Typ	Max	Units
Supply					
I_{DD}	Total Power Supply Current, Analog + Digital		130	TBD	mA
I_{DDQ}	Total Power Supply Current, DAC Power Down		37	TBD	mA
Digital Characteristics					
V_{IH}	Digital Input Voltage, Logic HIGH, TTL Compatible Inputs.	2.0		V_{DD}	V
V_{IL}	Digital Input Voltage, Logic LOW, TTL Compatible Inputs	V_{SS}		0.8	V
I_{IH}	Digital Input Current, Logic HIGH, (V_{IN}=4.0V)			10	µA
I_{IL}	Digital Input Current, Logic LOW, (V_{IN}=0.4V)			-10	µA
C_{IN}	Digital Input Capacitance (f=1Mhz, V_{IN}=2.4V)			7	pF
V_{OH}	Digital Output Voltage, Logic HIGH, CMOS Compatible Outputs (I_{OH}= -1mA)	3.7		V_{DD}	V
V_{OL}	Digital Output Voltage, Logic LOW, CMOS Compatible Outputs (I_{OL}=4.0 mA)	V_{SS}		0.4	V
I_{OZH}	Hi-Z Leakage Current, HIGH, V_{DD}=Max, V_{IN}=$V_{DD)}$			10	µA
I_{OZL}	Hi-Z Leakage Current, LOW, V_{DD}=Max, V_{IN}=$V_{SS)}$			-10	µA
C_I	Digital Input Capacitance (T^A=25°C, f=1Mhz)			8	pF
C_O	Digital Output Capacitance (T^A=25°C, f=1Mhz)			10	pF
Video Clock and Oscillator Signal					
FX	Crystal Oscillator Input Frequency	-30 ppm	27.0000	+30 ppm	Mhz
F27	27 Mhz Clock,CK27, Frequency		27.0000		Mhz
$tck27_H$	CK27 Pulse Width, HIGH	10	18.5		ns

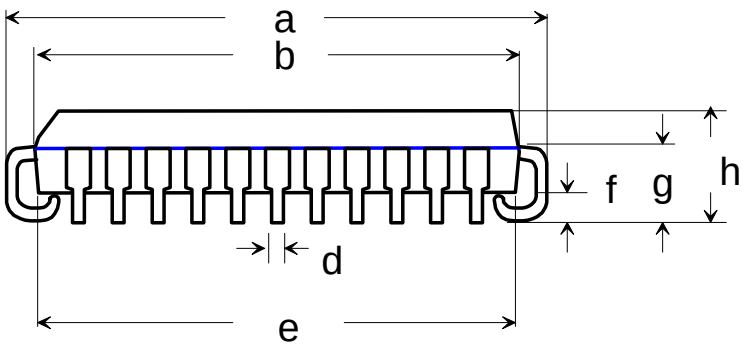
Symbol	Characteristics	Min	Typ	Max	Units
$tck27_L$	CK27 Pulse Width, LOW	14.5	18.5		ns
Video Bus Master Mode Timing					
tpd_{su}	Digital Pixel Data P<7:0> Input Setup Time	8			ns
tpd_{hd}	Digital Pixel Data P<7:0> Input Hold Time	3			ns
tsy_{su}	HSYN and VSYN Output Setup Time	10			ns
tsy_{hd}	HSYN and VSYN Output Setup Time	6			ns
Video Bus Slave Mode Timing					
tpd_{su}	Digital Pixel Data P<7:0> Input Setup Time	8			ns
tpd_{hd}	Digital Pixel Data P<7:0> Input Hold Time	3			ns
tsy_{su}	HSYN and VSYN Input Setup Time	8			ns
tsy_{hd}	HSYN and VSYN Input Setup Time	3			ns
Miscellaneous Digital Signals					
$t_{\overline{pwd}}$	$\overline{RST}$, active low reset time		1		μs
Serial Port Timing					
fsc	SCL Clock Frequency			100	kHz
tsu;sta	Start condition set up time	4.7			us
thd;sta	Start condition hold time	4.0			us
tsu;sto	Stop condition set up time	4.0			us
tLOW	SCL Low time	4.7			us
tHIGH	SCL High time	4.0			us
tr	SCL & SDA rise time			1.0	us
tf	SCL & SDA fall time			0.3	us
tsu;DAT	Data set-up time	250			ns
thd;DAT	Data hold time	0			ns
tvd;DAT	SCL LOW to data out valid			3.4	us
tBUF	Bus Free time	4.7			us
Analog Video (DAC) Outputs					
RES	DAC Resolution		10		bits
PSRR	Power Supply Rejection Ratio (Full Scale Output) COMP=0.1 μF, f=DC to 1 Mhz, V_{RIP}= 100 mV p-p.)	TBD			dB
V_{RO}	Voltage Reference (VREF) Output	1.112	1.235	1.359	V
Z_R	Voltage Reference Output Impedance	10			KΩ
K_{DAC}	DAC Gain Factor	10.31	10.85	11.39	

Symbol	Characteristics	Min	Typ	Max	Units
K_{IMBAC}	$K_{DAC\ Imbalance\ Between\ DACs}$	-1		+1	%
I_{REF}	DAC Reference Current (I_{REF}=Nominal)		3.15		mA
R_{REF}	Reference Resistor (V_{RO}=Nominal)		196		Ω
V_{BLANK}	Blanking Level Output Voltage (NTSC and PAL Modes)		0.300		V
V_{OC}	Video Output Compliance Voltage	-0.3		1.6	V
C_{OUT}	Video Output Capacitance (I_{out}=0 mA, f=1Mhz)		20		pF
R_L	Total Output Load Resistance		37.5		Ω
T_{DOV}	Analog Output Delay		20		ns

PACKAGING INFORMATION

44-Pin Plastic Leaded Chip Carrier (PLCC)





Dimensions

	max	norm	min	unit		max	norm	min	unit
A	2.15			mm.	d	0.53	0.406	0.33	mm.
B		1.27		mm.	e	16.00	15.748		mm.
C	1.22		1.07	mm.	f			0.51	mm.
D	0.81	0.736		mm.	g	3.04	2.565		mm.
a	17.65	17.526		mm.	h	4.57	4.368		mm.
b	16.66	16.612		mm.					