Semiconductor Inc.
System IC SBU

HV7131D-COF

CMOS IMAGE SENSOR
With 8-bit ADC

DESCRIPTION

HV7131D-COF is a highly integrated single chip CMOS color image sensor module with HV7131D CMOS color image sensor using Hynix 0.5um CMOS process developed for image application to realize high efficiency R/G/B photo sensor. The sensor has 648X488 pixel array, and in general color interpolation method using 3x3 spatial mask with window size 642X482 pixels may be used for VGA(640X480) display mode. Each compact active pixel element has high photo-sensitivity and converts photon energy to analog voltage signal. The sensor has three on-chip 8 bit Digital to Analog Convert (DAC) and 648 comparators to digitize the pixel output. The three on-chip 8 bit DAC can be used for independent R/G/B gain control. Hynix proprietary on-chip Correlated Double Sampling (CDS) circuit can reduce Fixed Pattern Noise (FPN) dramatically. The whole 8 bit digital color raw data is directly available on the package pins and just a few control signals are needed for whole chip control so that it is very easy to configure CMOS imaging system.

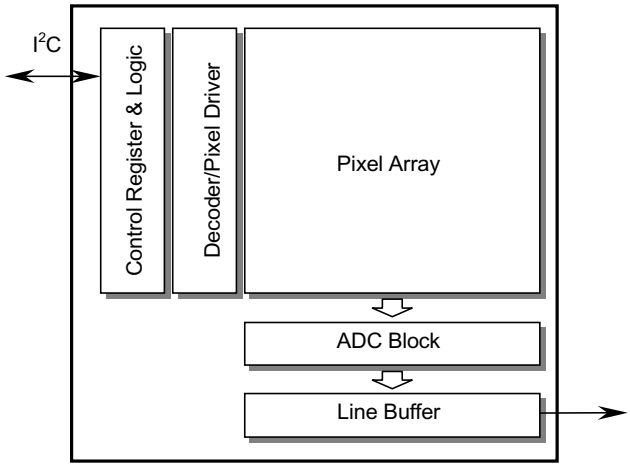
FEATURES

- 648 x 488 pixel array size
- Active pixel size: 8um x 8um
- High efficiency R/G/B color photo sensors
- Integrated 8-bit ADC for direct digital output
- Low power 3.3V operation (5V tolerant I/O)
- Integrated pan control and window sizing
- Clock speed up to 15MHz
- Programmable frame rate and synchronous format
- Full function control through standard I^2C bus
- Built-in Automatic Gain Control AGC
- 24 pin COF
- Bayer RGB color pattern
- Anti-blooming circuit
- Flexible exposure time control
- Integrated on-chip timing and drive control
- 1/3" optical format

TECHNICAL SPECIFICATION

Pixel resolution	642x482
Pixel size	8x8um^2
Fill factor	30%
Format	VGA
Sensitivity	3,150mV/lux·sec
Supply voltage for analog	3.3V
Supply voltage for digital	3.3V
Supply voltage for 5V tolerant input	5.0V
Power Consumption (max.)	80mW @10MHz
Operating temperature	0~40 Centigrade
Technology	0.5um 2metal CMOS

FUNCTIONAL BLOCK DIAGRAM



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ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

- Supply voltage(Analog, Digital) : 3.0 V ~ 3.6 V
- Voltage on any input pins : 0 V ~ 5.0 V
- Operating Temperature(Centigrade) : 0 ~ 40
- Storage Temperature(Centigrade) : -30 ~ 80

Note : Input pins are 5V tolerant. Stresses exceeding the absolute maximum ratings may induce failure.

DC Operating Conditions

Symbol	Parameter	Units	Min.	Max.	Load[pF]	Notes
V_{dd}	Internal operation supply voltage	Volt	3.0	3.6		
V_{ih}	Input voltage logic "1"	Volt	2.0	5	6.5	
V_{il}	Input voltage logic "0"	Volt	0	0.8	6.5	
V_{oh}	Output voltage logic "1"	Volt	2.15	3.6	60	
V_{ol}	Output voltage logic "0"	Volt	0.4	0.4	60	
T_a	Ambient operating temperature	Celsius	0	40		

AC Operating Conditions

Symbol	Parameter	Max Operation Frequency	Units	Notes
MCLK	Main clock frequency	15	MHz	1
SCK	I^2C clock frequency	400	KHz	2

1. MCLK can be divided according to Clock Divide Register for internal clock.
2. SCK is driven by host processor. For the detail serial bus timing, refer to I^2C Spec.

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ELECTRO-OPTICAL CHARACTERISTICS

Color temperature of light source: 3200K / IR cut-off filter (CM-500S, 1mm thickness) is used. --- 8)

Parameter	Units	Min.	Typical	Max.	Note
Sensitivity	mV / lux·sec	2,100	3,150		1)
Dark Signal	mV/sec		5	100	2)
Output Saturation Signal	mV	1,200	1,250		3)
Dynamic Range	dB			48	4)
Output Signal Shading	%		8	13	5)
Dark Signal Shading	mV/sec		3	300	6)
Frame Rate	fps			45	7)

The above characteristics are measured with the HV7131D packaged from CLCC.

Note:

1) Measured at 28lux illumination for exposure time 10 ms.
2) Measured at zero illumination for exposure time 50 ms. (T_{temp} = 40 Centigrade)
3) Measured at V_{dd} =3.3V and 100lux illumination for exposure time 50msec.
4) 48dB is limited by 8-bit ADC.
5) Variance of average value of 4x4 pixels response of each block over all equal blacks at 50% saturation level illumination for exposure time 10msec.
6) Range between V_{max} and V_{min} at zero illumination for exposure time 50msec, where V_{max} and V_{min} are the maximum and minimum values of each block's response, respectively.
7) Measured at MCLK 15MHz.
   Integration time must be set in order for effective window height not to exceed window height.
   It's because effective window height is directly proportional to integration time.
8) We recommend the IR cut-off filter with transmittance 50% at cut-off frequency 650nm for the real applications.

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OPTICAL CHARACTERISTICS (LENS SPECIFICATION)

Parameter		Units	Characteristics
Number of Elements		piece	3 (2Plastic & 1Glass)
Focal Length		mm	6.6 +/- 5%
F Number		--	Min. 2.0
MTF(20%)		linepair/mm	Min. 100 (at Center) Min. 65 (at Full Field)
Relative Illumination		%	Min. 80 (at Full Field)
TV Distortion		%	Max. 2.5
View Angle		degree	Typ. 52 (Diagonal)
IR cut-off filter	Cut-off frequency	nm	645 +/- 10 (Transmittance 50%)
	Thickness	mm	0.7 +/- 0.05

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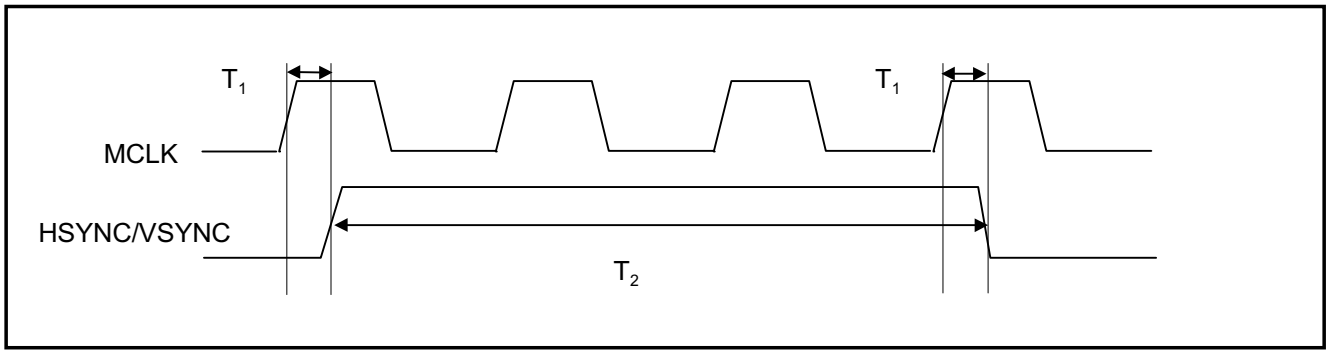
INPUT / OUTPUT AC CHARACTERISTICS

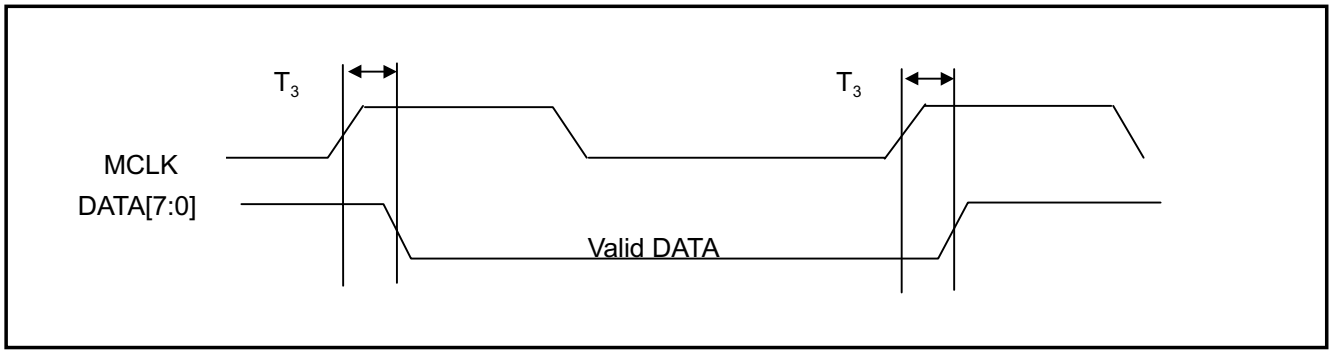
- All output timing delays are measured with output load 60[pF].
- Output delay include the internal clock path delay[6ns] and output driving delay that changes in respect to the output load, the operating environment, and a board design.
- Due to the variable valid time delay of the output, output signals may be latched in the negative edge of MCLK for the stable data transfer between the image sensor and a host for less than 15MHz operation.

MCLK to HSYNC/VSYNC Timing



T_1 : MCLK rising to HSYNC/VSYNC valid maximum Time : 18ns [output load: 60pF]
T_2 : HSYNC/VSYNC valid Time : minimum 1clock(subject to T_1, T_2 timing rule)

MCLK to DATA Timing



T_3 : MCLK rising to DATA Valid maximum Time : 18ns [output load: 60pF]
Note) HSYNC signal is high when valid data is on the DATA bus.

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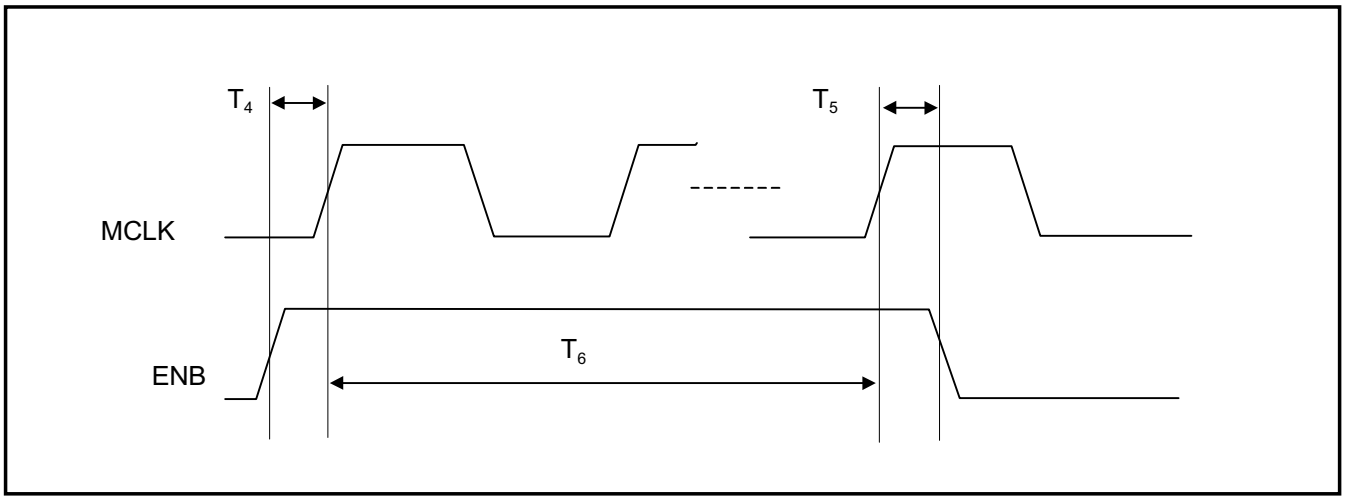
INPUT / OUTPUT AC CHARACTERISTICS (Continue)

ENB Timing



T_4 : ENB Setup Time : 5[ns]

T_5 : ENB Hold Time : 5[ns]

T_6 : ENB Valid Time : minimum 2 Clock

RESET Timing

Must in Valid(active low) state at least 8 MCLK periods

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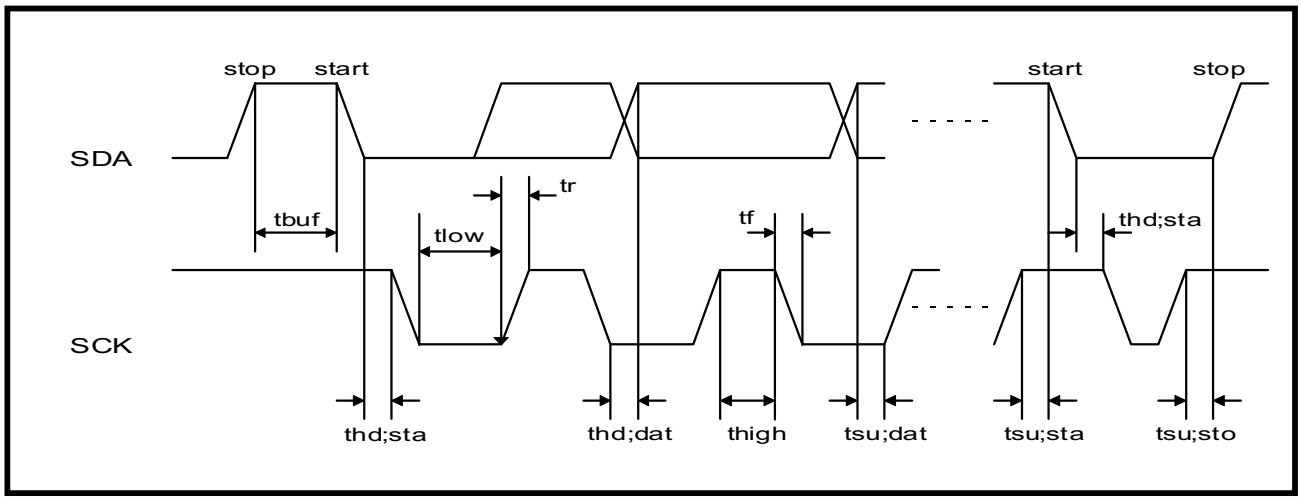
INPUT / OUTPUT AC CHARACTERISTICS (Continue)

I²C Bus (Programming Serial Bus) Timing



I²C Bus Interface Timing

Parameter	Symbol	Min.	Max.	Unit
SCK clock frequency	f_{sck}	0	400	KHz
Time that I²C bus must be free before a new transmission can start	t_{buf}	1.2	-	us
Hold time for a START	$t_{hd};s_{ta}$	1.0	-	us
LOW period of SCK	t_{low}	1.2	-	us
HIGH period of SCK	t_{high}	1.0	-	us
Setup time for START	$t_{su};s_{ta}$	1.2	-	us
Data hold time	$t_{hd};d_{at}$	1.3	-	us
Data setup time	$t_{su};d_{at}$	250	-	ns
Rise time of both SDA and SCK	t_r	-	250	ns
Fall time of both SDA and SCK	t_f	-	300	ns
Setup time for STOP	$t_{su};s_{to}$	1.2	-	us
Capacitive load of each bus lines(SDA,SCK)	C_b	-	-	pf

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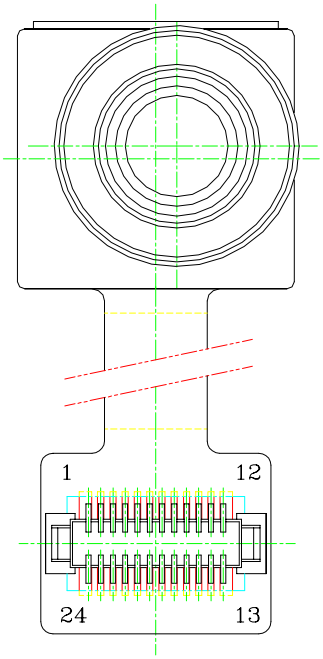
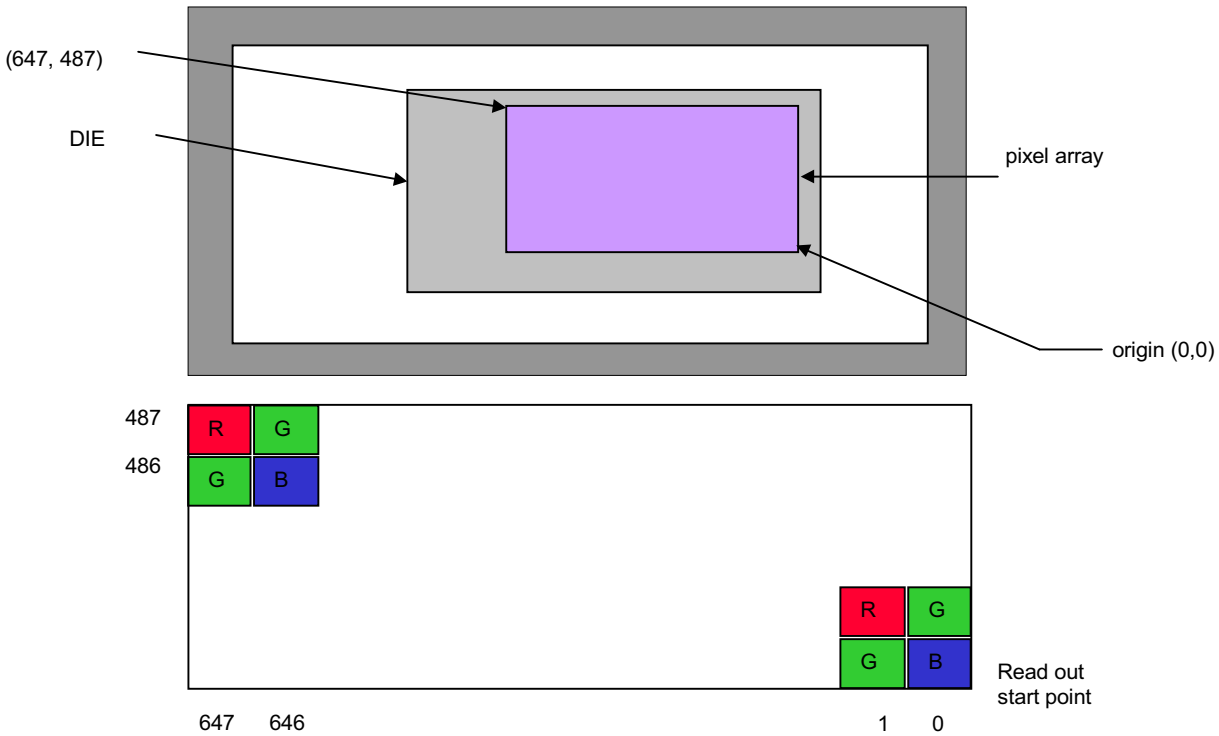
PIN CONFIGURATION (24 pin COF Top View)



PIN NO.	NAME	PIN NO.	NAME
1	AGND	13	DVDD
2	DGND	14	RESET
3	DATA7	15	VSYNC
4	DATA6	16	HSYNC
5	DATA5	17	SDA
6	DATA4	18	DGND
7	DATA3	19	SCK
8	DATA2	20	DGND
9	DATA1	21	ENB
10	DATA0	22	MCLK
11	DGND	23	VDD5
12	DGND	24	AVDD

COLOR PATTERN



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PIN DESCRIPTION (24 pin COF)

PIN	NAME	I/O	DESCRIPTION
1	AGND	I	Analog Ground
2	DGND	I	Digital I/O Ground
3	DATA7	O	Image Data bit 7
4	DATA6	O	Image Data bit 6
5	DATA5	O	Image Data bit 5
6	DATA4	O	Image Data bit 4
7	DATA3	O	Image Data bit 3
8	DATA2	O	Image Data bit 2
9	DATA1	O	Image Data bit 1
10	DATA0	O	Image Data bit 0
11	DGND	I	Digital I/O Ground
12	DGND	I	Digital Core Ground
13	DVDD	I	Digital Supply Voltage 3.3V
14	RESET	I	Hardware Reset Signal, Active Low
15	VSYNC	O	Vertical synchronization signal / Frame start output ; Signal pulse at start of image data frame with programmable blanking duration
16	HSYNC /DVALID	O	Horizontal synchronization signal / Data valid output ; Data valid when 'H' with programmable blanking duration
17	SDA	I/O	I^2C Data ; I^2C standard data I/O port
18	DGND	I	Digital I/O Ground
19	SCK	I	I^2C clock ; I^2C clock control from I^2C master
20	DGND	I	Digital I/O Ground
21	ENB	I	Sensor Enable Signal ; 'H' enable normal operation 'L' disable
22	MCLK	I	Master Clock (up to 15MHz) ; Global master clock for image sensor internal timing control
23	VDD5	I	I/O bias voltage for 5V tolerant *1)
24	AVDD	I	Analog Supply Voltage 3.3V

Note : *1) Tie to DVDD for 3.3V operation / Tie to 5V for 5V tolerant operation

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REGISTER DESCRIPTION

MODE_A[8'h00]

Represent device identity. High nibble: Sensor Array Size, Low Nibble: Revision Number

For HV7131D, identity value is 8'h00, [VGA: 0, Revision 0]

MODE_B[8'h01]

This is operating mode select register. Each bit's description is as below.

Bit	Function	Description
0	Integration time unit	Selects integration time unit between line unit and pixel unit. Commonly line unit is used for its large step control, but under high luminance or when precise control is needed in the case such as anti-flicker, pixel unit control is used. Default is line unit mode[0].
1	Single Frame mode	Selects continuous frame output and single frame output. When single shot mode is selected, only one frame data is produced and the sensor goes to idle mode. Default is continuous frame output mode[0].
2	Window Mode	Selects imaging array size between programmable window size and full size [648x488]. Default is window size mode[1] and current window default size is 641x482. [Window size is determined by RowStartAddress, Column StartAddress, WindowWidth, WindowHeight Registers.]
3	HSYNC output mode	Selects HSYNC output mode between "data valid mode" and "data valid with clock mode". Default is data valid mode[0].
4,5	Output data type	Selects output data type among (data – reference), data only or reference only. Internally the sensor produces reference data and image data respectively, and image data is deducted by reference data in order to reduce Fixed Pattern Noise. Generally the technique is called Correlated Double Sampling(CDS). Default is data - reference (CDS) [00].
6,7	Operation Mode	Selects sensor operation mode among normal sensing mode and chip test related modes. In normal use, the mode should be set to normal mode[00]. Default is normal operation mode[00].

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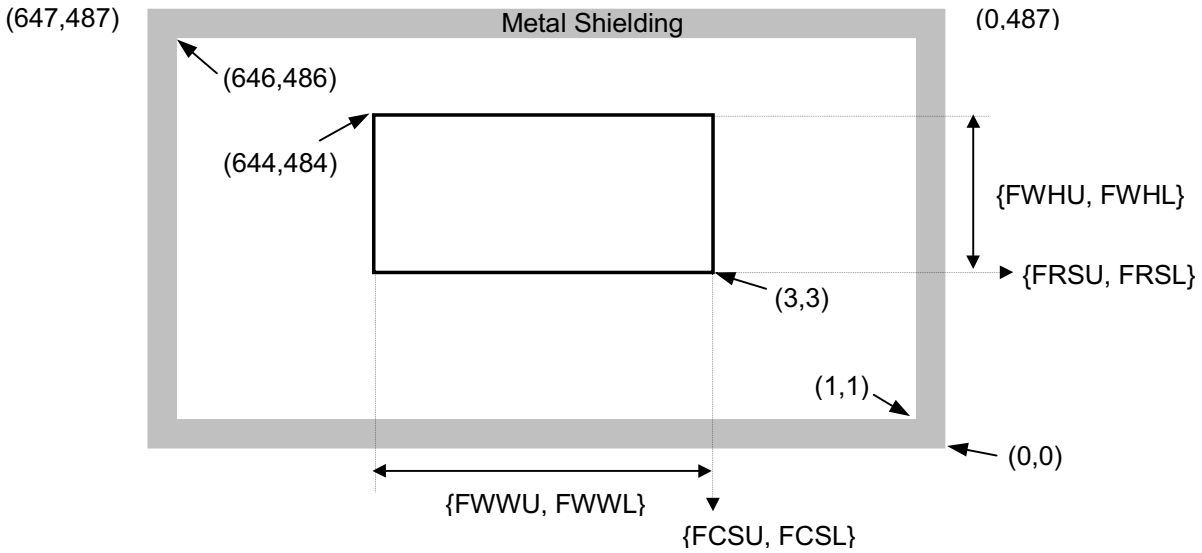
MODE_C[8'h02]

This is operating mode select register. Each bit's description is as below

Bit	Function	Description
1	Display Mode	Selects Color mode or Black/White Mode In Black/White mode, gain control is controlled by G Gain Register Value

FRAME SIZE CONTROL REGISTERS

HV7131D may image any user specified window area within image sensor array(648x488). This is called panning function, and for this function, FRS(Frame Row Start), FCS(Frame Column Start), FWH(Frame Window Height), and FWW(Frame Window Width) are used. Panning window can be programmed as below.



Note1) Metal shielded pixel element produce black level data, and effective image array size 646 x 486. In general, color interpolation algorithm using 3x3 spatial mask for mosaic CFA single sensor require that pixels around the edge of a programmed image window are used for just color interpolation of neighbor pixels. Accounting for this fact, image array window should be programmed to larger value than the size that is to be displayed. For example, in order to make 640X480 24bit color image data, 642X482 pixel array is necessary. That is to say, you can use the maximum window size as 642{FWWL, FWWL}X 482{FWHU, FWHL} and you must use Row Start Address and Column Start Address from (3, 3) to (644, 484) for getting 642X482 raw image data.

Note2) You have to change the frame register value as below to get the full 640X480 window size.

{FRSU, FRSL}	3	{FWHU, FWHL}	482
{FCSU, FCSL}	3	{FWWU, FWWL}	642

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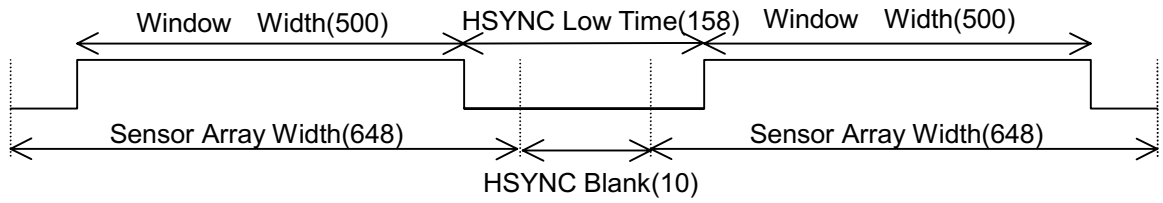
TIMING CONTROL REGISTERS

- **HSYNC blank register[8'h20-8'h21]**

The HSYNC Blank register defines data blank time between current line and next line by pixel clock unit. The value programmed to HSYNC blank register defines HSYNC Low Time with (Sensor Array Width – Window Width) clocks added. For example, if Window Width = 500, HSYNC Blank = 10, then HSYNC Low Time is HSYNC Blank + (Sensor Array Width – Window Width), 10 + (648 – 500) = 158 clocks.



For more timing details, refer to Frame Timing Diagram section.

- **VSYNC blank register[8'h22-8'h23]**

The VSYNC blank register defines the active high duration of VSYNC output by pixel clock unit.
The active high VSYNC indicates frame boundary between continuous frames. For VSYNC-HSYNC timing relation in the frame transition, please refer to Frame Timing Diagram section.

- **Integration time value register[8'h25-8'h27]**

Integration time value register defines the time during which active pixel element evaluates photon energy that is converted to digital data output by internal ADC processing. Integration time is equivalent to exposure time in general camera so that integration time need to be increased in dark environment and decreased in light environment. Integration time unit is selected between pixel unit and line unit by MODE_B[0] bit. When line unit mode is selected, only two lower bytes of Integration time value register[8'h26-8'h27] are accounted in the internal sensor logic because representable maximum integration time, Maximum Value(2^{16}-1) * Sensor Array Width(648) * Clock Period(100ns for 10Mhz) = 4.246 sec, is quite big enough to adapt to any very dark environment. For pixel unit mode, whole three bytes value are used for integration time, Integration Time Value(8'h25-8'h27) * Clock Period, and representable maximum value is Maximum Value(2^{24}-1) * Clock Period(100ns for 10Mhz) = 1.677sec.

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● **Master clock divider register**

This four bits register is used to divide external pixel clock for internal use. The actual pixel operating frequency used in the sensor is the same as external pixel frequency divided by divisor as below.

Register value	Divisor	Register value	Divisor	Register value	Divisor
0	1	4	16	8	256
1	2	5	32	9	512
2	4	6	64	10	1024
3	8	7	128	11	2048

CHARATERISTICS ADJUSTMENT REGISTERS

Each sensor has a little different photo-diode characteristics so that the sensor provides internal adjustment registers that calibrate internal sensing circuit in order to get optimal performance. There are three kinds of registers as below.

● **Reset level register[8'h30]**

The register controls the voltage level that is initially compared to pixel analog voltage, and the initial voltage level is called as "reference voltage level". Internal DAC analog voltage decrements from reference voltage level until the pixel analog voltage output is lager than DAC analog voltage. Appropriate reference voltage level varies from various factors, such as process variation, luminance, etc. If the register value is set to too large or too small value, vertical fixed pattern noise may be produced. Therefore this register value must be programmed to appropriate value in order to avoid FPN. For the automatic reset level control, please refer to Reset Level Statistics Register Section. High register value means high reference voltage and large digital output. Program value range is 0~63,

● **RGB gain registers[8'h31-8'h33]**

There are three color gain registers for R, G, B pixels, respectively. These registers are used to amplify digital pixel output . If the gain register value is decreased, digital pixel output is increased. That is, under dark light condition the pixel output is not enough to get right image so that we must amplify the output value by decreasing gain value to get good image. These registers may be used for white balance and color effect with independent R,G,B color control. Program value range is 0~63.

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- **Pixel bias voltage register[8'h34]**

The register controls pixel analog voltage decrement degree by controlling bias current of pixel output sensing load transistor. With the reset level register(8'h30) it is used to adjust ADC circuit output characteristics. The larger register value causes the higher bias current to increase pixel output decrement degree, and commonly the register default value is used. Program value range is 0~7.

RESET LEVEL STATISTICS REGISTER

- **Low Reset Level Count[8'h57-8'h58]**

This two-byte register has a value representing a eighth (1/8) of pixels that have reset value less than 3 during one frame time and is updated when VSYNC gets active. With high reset level counter register it can be used as a parameter for external automatic reset level control logic that update the appropriate value in the reset level register to automatically compensate die to die overall reset level variation.

- **High Reset Level Count[8'h59-8'h5a]**

This two byte register has a value representing a eighth (1/8) of pixels that have reset value larger than 123 during one frame time and is updated when VSYNC gets active. With low reset level counter register it can be used as a parameter for external automatic reset level control logic that update the appropriate value in the reset level (30H) register to automatically compensate die to die overall reset level variation.

RGB OFFSET REGISTERS[8'h50-8'h52]

These registers control offset value of RGB digital output to make color effect. Normally these register values are set to default zero.

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REGISTER ADDRESS AND DEFAULT VALUE

<table>
<tr><th>Group</th><th>Symbol</th><th>Address</th><th>Description</th></tr>
<tr><td rowspan="2">Mode-Registers</td><td>MODE_A</td><td>00H</td><td>Device Identity (Read only : 00H)</td></tr>
<tr><td>MODE_B</td><td>01H</td><td>Operating Mode Selection (Default : 04H)
<table>
<tr><td>b0</td><td>0</td><td>Line Unit Integration</td></tr>
<tr><td></td><td>1</td><td>Pixel Unit Integration</td></tr>
</table>
<table>
<tr><td>b1</td><td>0</td><td>Continuous Frame</td></tr>
<tr><td></td><td>1</td><td>Single Shot Frame</td></tr>
</table>
<table>
<tr><td>b2</td><td>0</td><td>Full Image (648X488)</td></tr>
<tr><td></td><td>1</td><td>Windowed Image</td></tr>
</table>
<table>
<tr><td>b3</td><td>0</td><td>HSYNC only</td></tr>
<tr><td></td><td>1</td><td>HSYNC & Internal Clock</td></tr>
</table>
<table>
<tr><th>b5</th><th>b4</th><th>Output Data Type</th></tr>
<tr><td>0</td><td>0</td><td>Data_Level - Reference_Level</td></tr>
<tr><td>0</td><td>1</td><td>Reference_Level</td></tr>
<tr><td>1</td><td>0</td><td>Data_Level</td></tr>
<tr><td>1</td><td>1</td><td>reserved</td></tr>
</table>
<table>
<tr><th>b7</th><th>b6</th><th>Operating Mode</th></tr>
<tr><td>0</td><td>0</td><td>Normal Mode</td></tr>
<tr><td>0</td><td>1</td><td>Reserved</td></tr>
<tr><td>1</td><td>0</td><td>Reserved</td></tr>
<tr><td>1</td><td>1</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>MODE_C</td><td>02H</td><td>
<table>
<tr><td>b1</td><td>0</td><td>Color Output</td></tr>
<tr><td></td><td>1</td><td>Black & White Output</td></tr>
</table></td></tr>
<tr><td>Internal Test Register</td><td colspan="2">53H, 55H, 56H,
60H, 61H
[Reserved]</td><td>Test Registers for Image Sensor Future Enhancement
[These register should not be used in normal operation]</td></tr>
</table>

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REGISTER ADDRESS AND DEFAULT VALUE (continue)

Group	Symbol	Address	Description		
Frame-Registers	FRSU	10H	Row Start Address (Upper byte) Default :	00H	[3]
	FRSL	11H	Row Start Address (Lower byte)	03H	
	FCSU	12H	Column start Address (Upper byte)	00H	[3]
	FCSL	13H	Column start Address (Lower byte)	03H	
	FWHU	14H	Window Height (Upper byte)	01H	[482]
	FWHL	15H	Window Height (Lower byte)	E2H	
	FWWU	16H	Window Width (Upper byte)	02H	[641]
	FWWL	17H	Window Width (Lower byte)	81H	
Timing-Register	THBU	20H	HSYNC Blanking Duration value (Upper byte)	Default :00H	
	THBL	21H	HSYNC Blanking Duration value (Lower byte)	03H	
	TVBU	22H	VSYNC Blanking Duration value (Upper byte)	00H	
	TVBL	23H	VSYNC Blanking Duration value (Lower byte)	03H	
	TITU	25H	Integration Time value (Upper byte)	00H	
	TITM	26H	Integration Time value (Middle byte)	01H	
	TITL	27H	Integration Time value (Lower byte)	F4H	
	TMCD	28H	Master Clock Divider	00H	
Adjust-Register	ARLV	30H	Reset Level Value	38H	
	ARCG	31H	Red Color Gain	1EH	
	AGCG	32H	Green Color Gain	1EH	
	ABCG	33H	Blue Color Gain	1EH	
	APBV	34H	Pixel Bias Voltage Control	02H	
Offset Register	OFSR	50H	R Offset Register (Test purpose Only)	00H	
	OFSG	51H	G offset Register (Test purpose Only)	00H	
	OFSB	52H	B offset Register (Test purpose Only)	00H	
Reset Level Statistics Register	LoREfNOH	57H	Low Reset Level Counter [<3] (Upper byte)	(Read Only)	
	LoREfNOL	58H	Low Reset Level Counter [<3] (Lower byte)	(Read Only)	
	HiRefNOH	59H	High Reset Level Counter [>123] (Upper byte)	(Read Only)	
	HiRefNOL	5AH	High Reset Level Counter [>123] (Lower byte)	(Read Only)	

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PROGRAMMING SEQUENCE FOR CMOS IMAGE SENSOR

- **Single Register Byte Programming**

S	22H	A	01H	A	mode inform	A	P
*1	*2	*3	*4	*5	*6	*7	*8

⇨ Set "Operating Mode" register into Window mode

*1. Drive: I^2C start condition

*2. Drive: 22H(001_0001 + 0) [device address + R/W bit]

*3. Read: acknowledge from sensor

*4. Drive: 01H [sub-address]

*5. Read: acknowledge from sensor

*6. Drive: 04H [mode information]

*7. Read: acknowledge from sensor

*8. Drive: I^2C stop condition

- **Multiple Register Byte Programming using Auto increment Mode**

S	22H	A	01H	A	02H	A	65H	A	P
*1	*2	*3	*4	*5	*6	*7	*8	*9	*10

⇨ You can program multiple configuration registers with single I2C bus cycle.

⇨ Set "Row Start Address" register as 265H

*1. Drive: I^2C start condition

*2. Drive: 22H(001_0001 + 0) [device address + R/W bit]

*3. Read: acknowledge from sensor

*4. Drive: 10H [sub-address]

*5. Read: acknowledge from sensor

*6. Drive: 02H [row start address upper byte]

*7. Read: acknowledge from sensor

*8. Drive: 65H [row start address lower byte]

*9. Read: acknowledge from sensor

*10. Drive: I^2C stop condition

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PROGRAMMING SEQUENCE FOR CMOS IMAGE SENSOR (continue)

- **Reading Register Value**

S	22H	A	01H	A	S	23H	A	Read Data	A	P
*1	*2	*3	*4	*5	*6	*7	*8	*9	*10	

⇨ Single Read or Auto-Increment Read

⇨ Set "Reset Level Value" register

*1. Drive: I^2C start condition

*2. Drive: 22H(001_0001 + 0) [device address + R/W bit(be careful. R/W=0)]

*3. Read: acknowledge from sensor

*4. Drive: 10H [sub-address]

*5. Read: acknowledge from sensor

*6. Drive: I^2C start condition

*7. Drive: 23H(001_0001 + 1) [device address + R/W bit(be careful. R/W=1)]

*8. Read: acknowledge from sensor

*9. Read: Read Data from sensor

*10. Drive: acknowledge to sensor(if there is no more read data Ack=1, else Ack=0)

*11. Drive: I^2C stop condition

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FRAME TIMING DIAGRAMS

There are two frame timing cases,

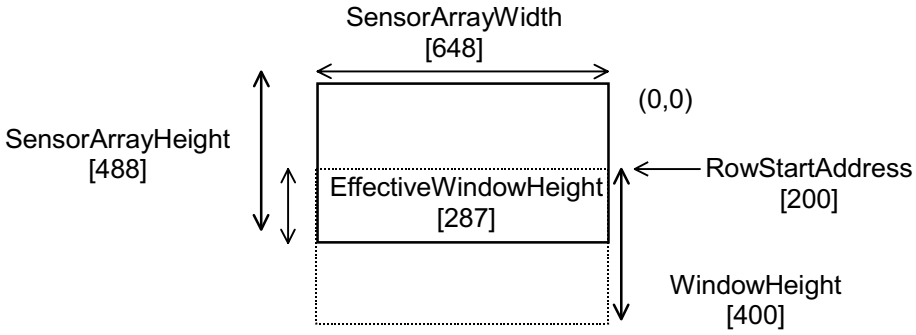
- Integration Time < EffectiveWindowHeight * Scale
- Integration Time > EffectiveWindowHeight * Scale

EffectiveWindowHeight is equal to the number of data lines generated in a frame and is defined to be selected by

```
if((RowStartAddress + WindowHeight + 1) <= SensorArrayHeight)
        EffectiveWindowHeight = WindowHeight;
else
        EffectiveWidnowHeight = (SensorArrayHeight - RowStartAddress - 1);
```

The above selection logic is somewhat confusing in respect of general counting measure. It's partly due to the mixed use of indexing start points, i.e. '0' and '1' in the chip design. Therefore in order to avoid the confusion it is desirable to just follows the equation when you estimate the frame rate.

For example, RowStartAddress = 200 and WindowHeight = 400, EffectiveWindowHeight is 287 and 287 data lines per a frame are generated.



Scale is selected according to Integration Time Mode by

```
If(PixelMode)    Scale = SensorArrayWidth; // For H7131B[648x488], SensorArrayWidth is 648
else             Scale = 1;
```

When Integration Time > (EffectiveWindowHeight * Scale), next frame VSYNC does not follow immediately after current frame's last line has been produced. Instead, one of the following two idle time slots is inserted according to Integration Time Mode before next frame VSYNC gets active.

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< Idle Slots >

- Line Mode: (Integration Time - EffectiveWindowHeight) * 1024 clks
- Pixel Mode: (Integration Time - EffectiveWindowHeight *Scale)
  = (Integration Time - EffectiveWindowHeight *SensorArrayWidth) clks

Each Frame Timing of the above cases may be decomposed into four timing segments

- Initial Data Setup Time after ENB gets active
- Even Line
- Odd Line
- Frame Transition

The subsections will describe frame timing diagram for said frame time cases, (Integration Time < Effective Window Height * Scale) and (Integration Time > Effective Window Height * Scale).

1. Frame Timing Diagram for Integration Time < (EffectiveWindowHeight * Scale)

Frame timing related registers are programmed to suit for the above condition as follows

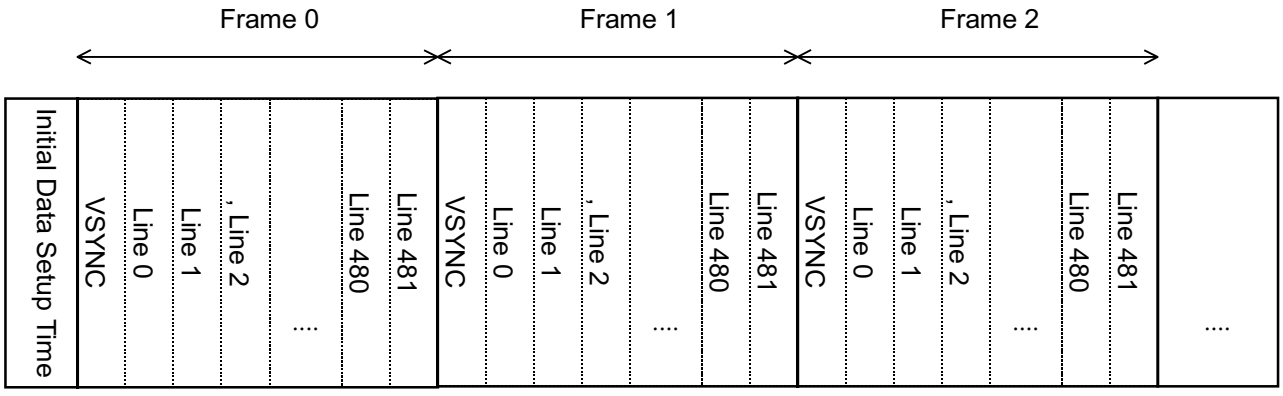
RowStartAddress = 3; WindowHeight = 482;

ColumnStartAddress = 3; WindowWidth = 642;

IntegrationTime = 400 [Line Mode];

EffectiveWindowHeight is “482” for (SensorArrayHeight > (RowStartAddress + WindowHeight + 1)), i.e. 488 > (3 + 482 + 1), is met, and Scale is “1” for integration time is line mode. Therefore, (Integration Time < EffectiveWindowHeight * Scale), i.e. 400 < 482 * 1, is met.

Overall Frames Sequence



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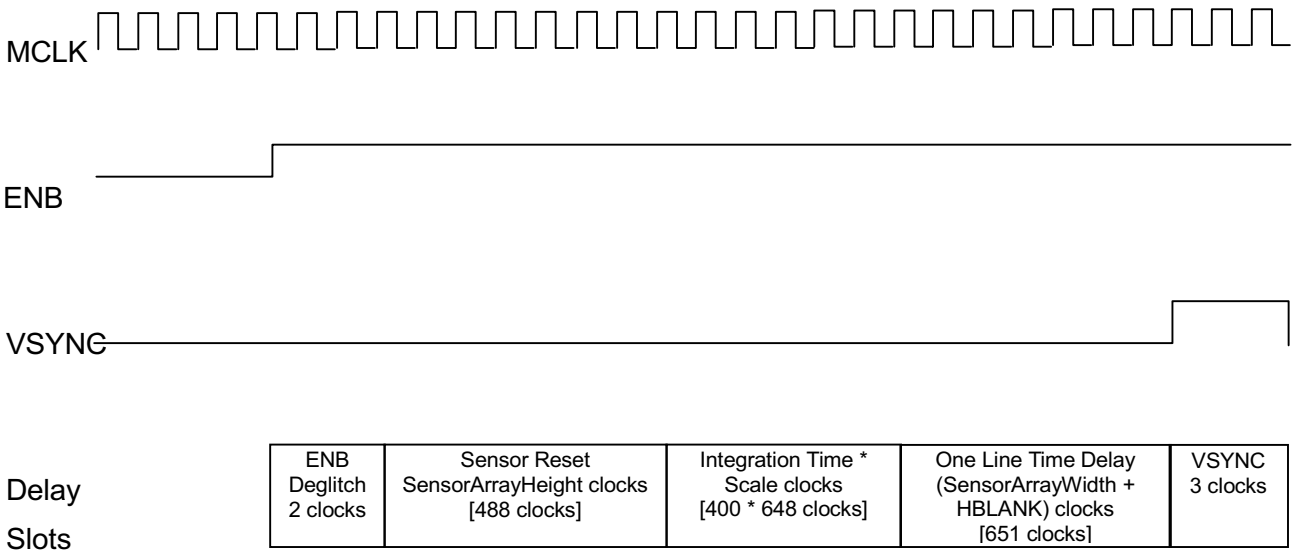

Fig. 1 Initial Data Setup Time after ENB gets active

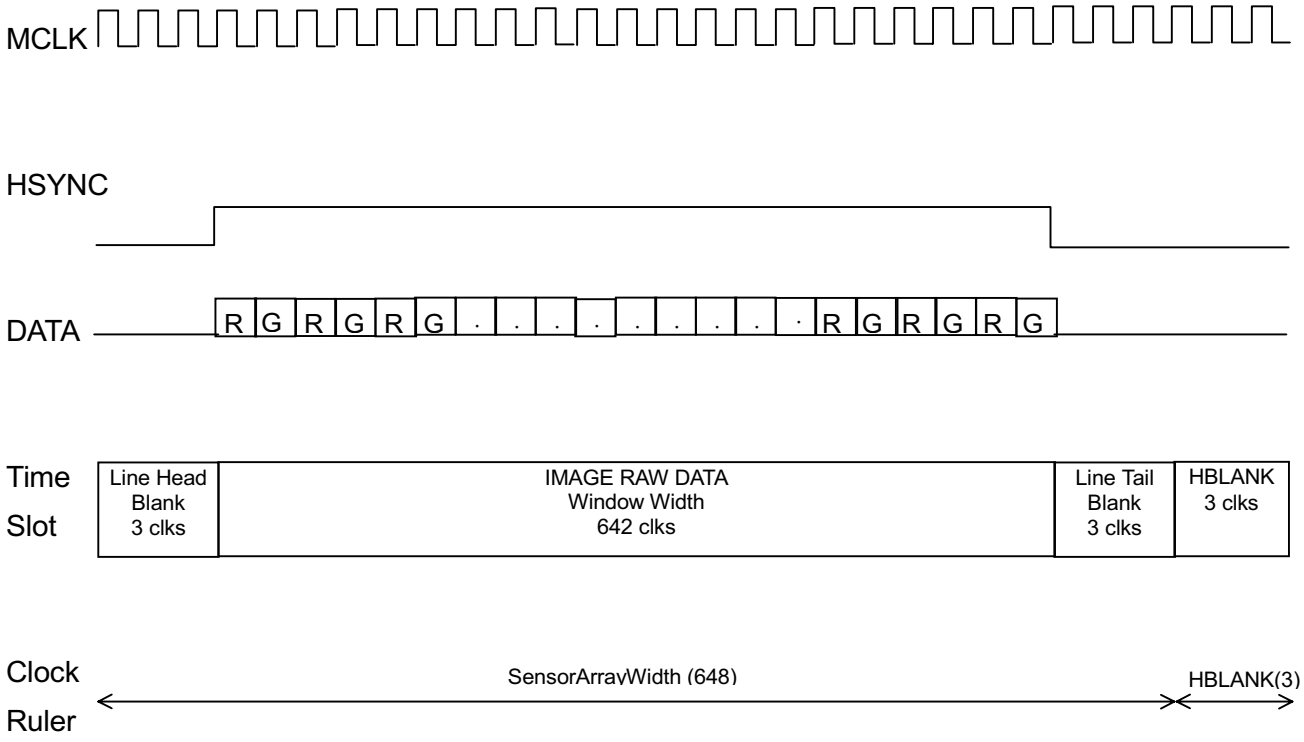

Fig.2 Even Line Data Timing

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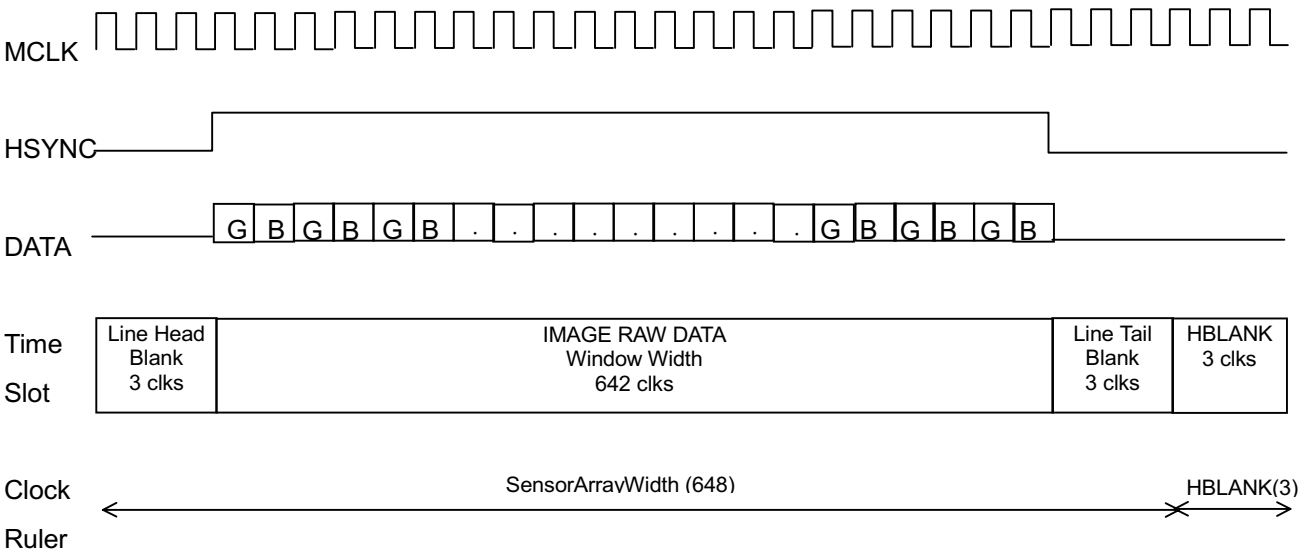
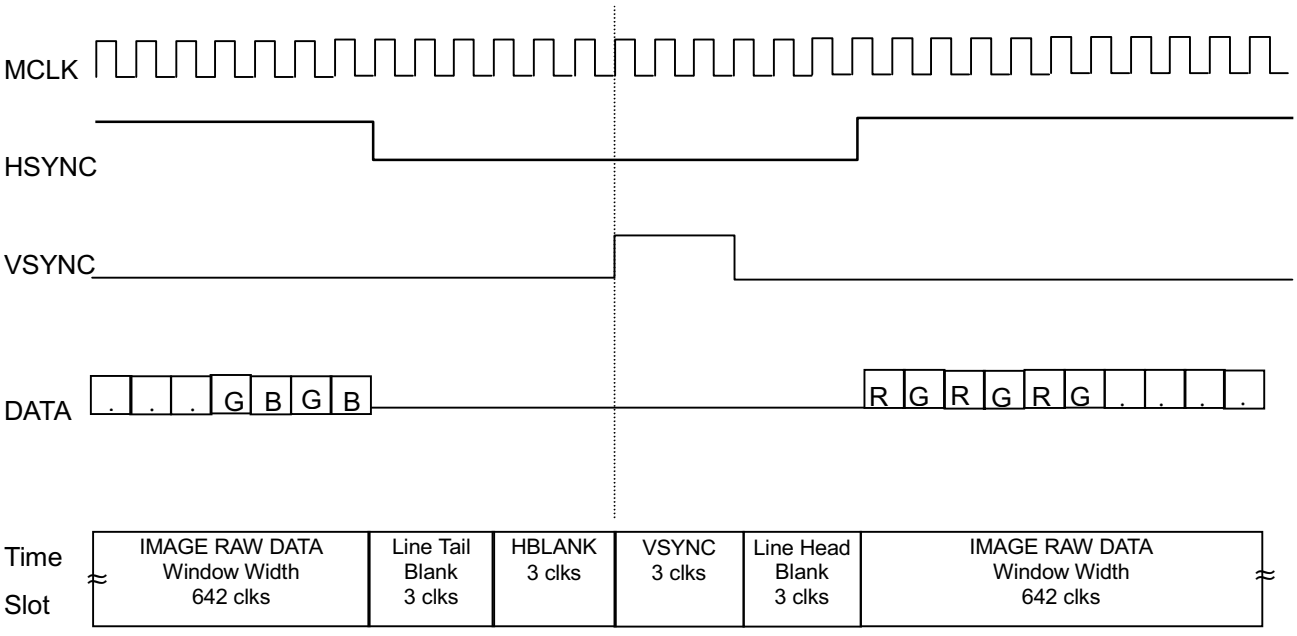


Fig.3 Odd Line Data Timing



Integration Time < EffectiveWindowHeight * Scale

Fig.4 Frame Transition Timing

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2. Frame Timing Diagram for Integration Time > (EffectiveWindowHeight * Scale)

Frame timing related registers are programmed to suit for the above condition as follows

RowStartAddress = 3; WindowHeight = 482;

ColumnStartAddress = 3; WindowWidth = 642;

IntegrationTime = 600 [Line Mode];

EffectiveWindowHeight is “482” for (SensorArrayHeight > (RowStartAddress + WindowHeight + 1)), i.e. 488 > (3 + 482 + 1), is met, and Scale is “1” for integration time is line mode. Therefore, (Integration Time < EffectiveWindowHeight * Scale), i.e. 600 > 482 * 1, is met, and Idle Slot of Line Mode, i.e. (600 - 482) * 1024 clocks idle slot, is inserted before the next frame initiation.

Overall Frames Sequence

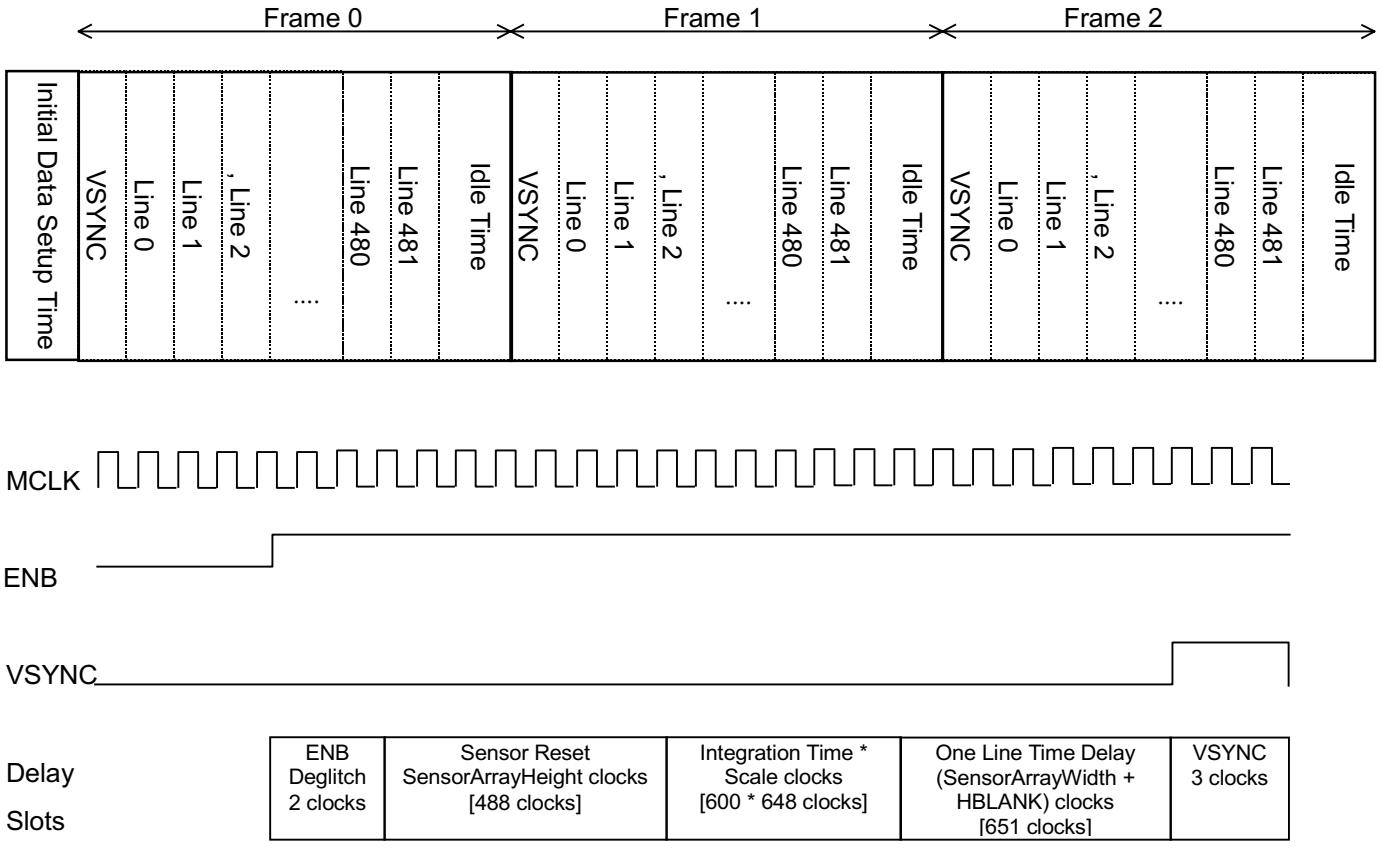

Fig. 5 Initial Data Setup Time after ENB gets active

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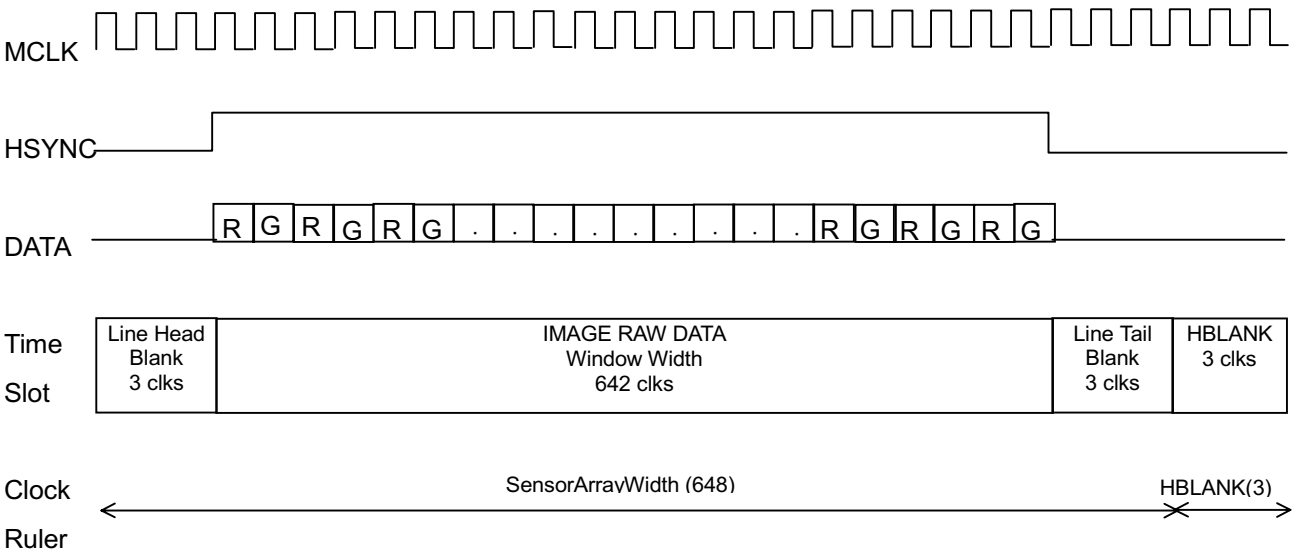

Fig.6 Even Line Data Timing

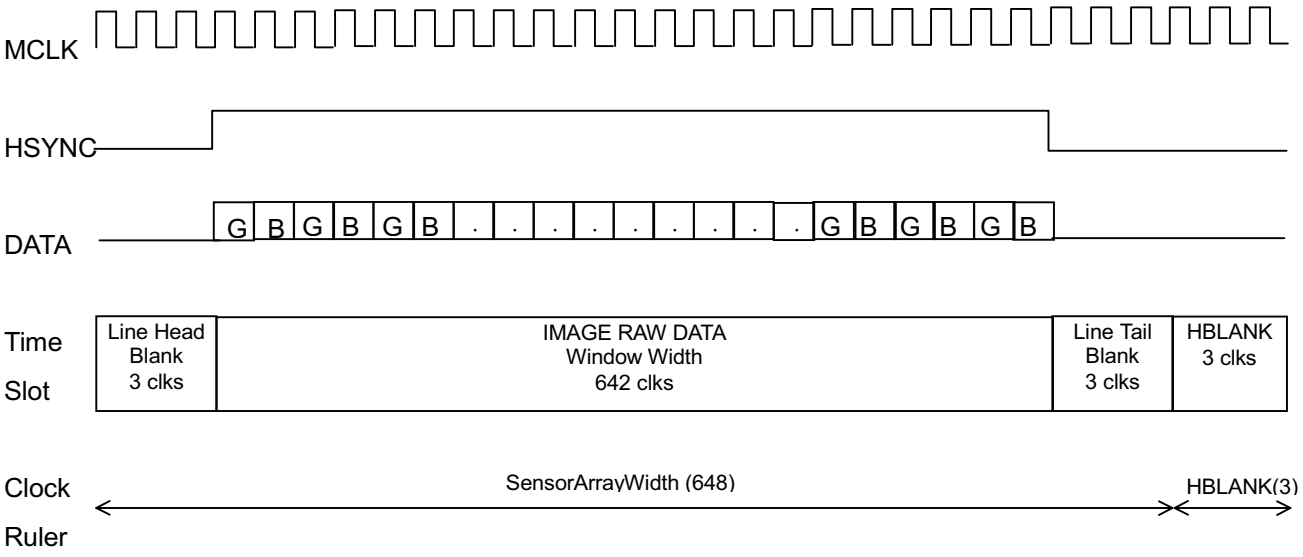

Fig.7 Odd Line Data Timing

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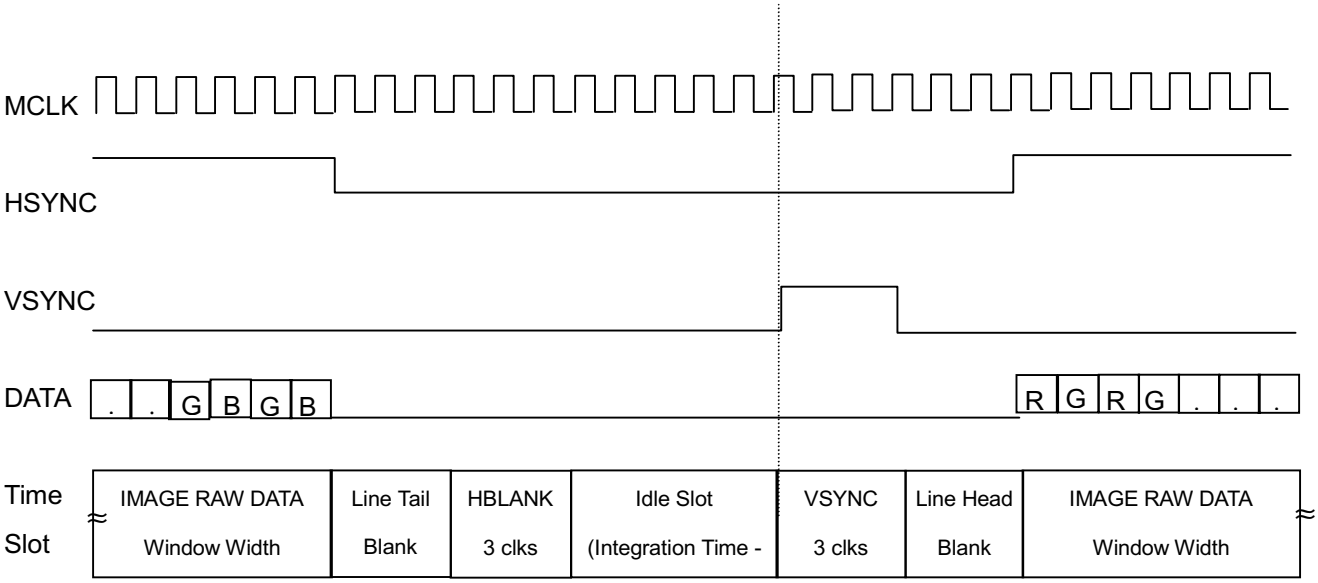

Integration Time > EffectiveWindowHeight * Scale

Fig.8 Frame Transition Timing

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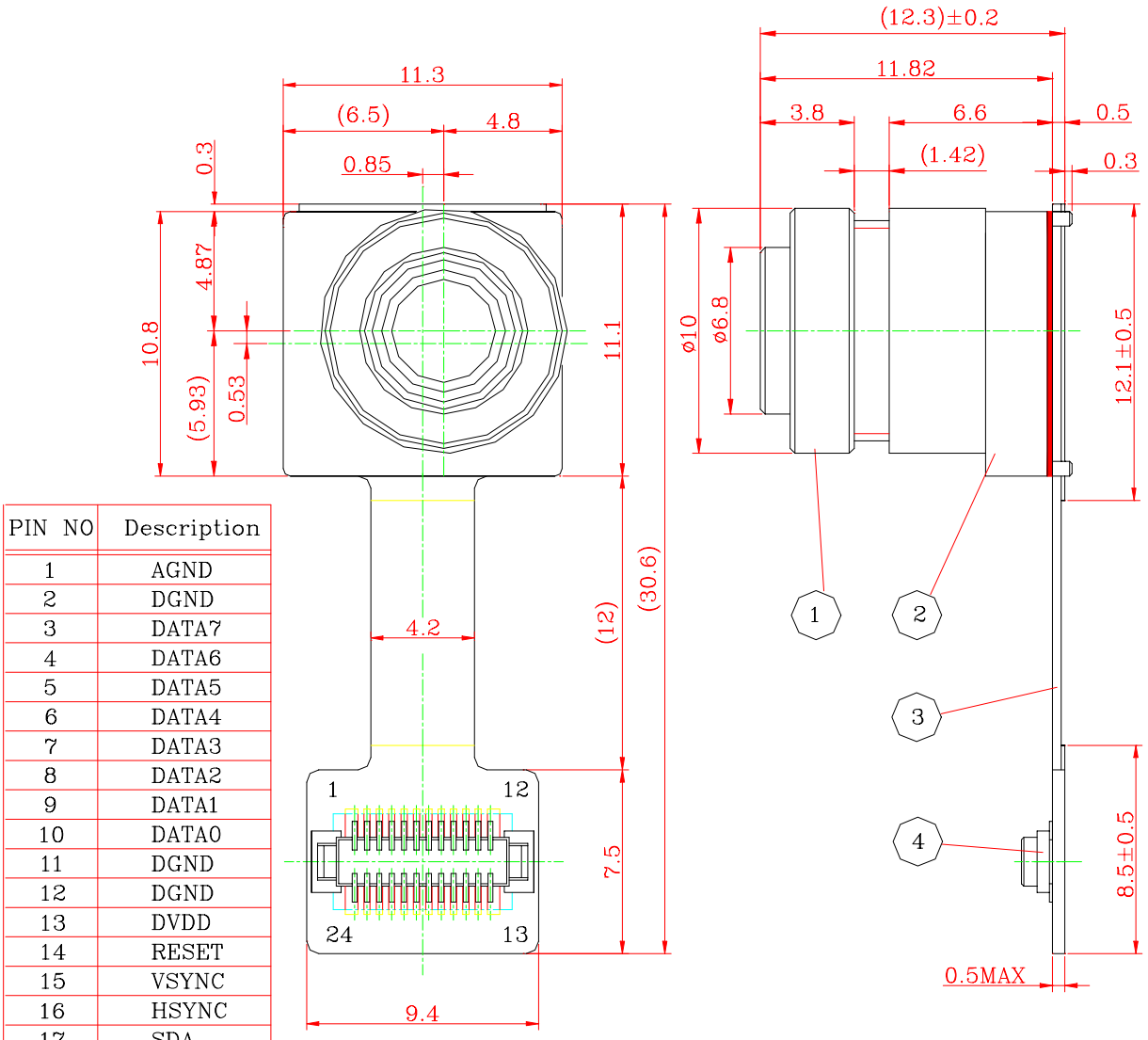
MODULE DISMENSION (24 pin COF)

UNIT: mm

NO	ITEM	REMARK	Q'TY
1	Lens	ø10x8.04 (2P1G)	1
2	Lens Holder	11.3x10.8x7.4	1
3	FPC		1
4	Connector	AXK5F2435J	1



PIN NO	Description
1	AGND
2	DGND
3	DATA7
4	DATA6
5	DATA5
6	DATA4
7	DATA3
8	DATA2
9	DATA1
10	DATA0
11	DGND
12	DGND
13	DVDD
14	RESET
15	VSYNC
16	HSYNC
17	SDA
18	DGND
19	SCK
20	DGND
21	ENB
22	MCLK
23	VDD5
24	AVDD

Standard Tolerance : +/- 0.1, Unit : mm

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MEMO

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