N-Channel Lateral DMOS FETs

(Available Only In Extended Hi-Rel Flow)

PRODUCT SUMMARY				
$V_{(BR)DS}$ Min (V)	$V_{GS(th)}$ Max (V)	$r_{DS(on)}$ Max (Ω)	C_{rss} Max (pF)	t_{ON} Max (ns)
20	1.5	70 @ V_{GS} = 5 V	0.5	2

FEATURES

- Quad SPST Switch with Zener Input Protection
- Low Interelectrode Capacitance and Leakage
- Ultra-High Speed Switching—t_{ON}: 1 ns
- Ultra-Low Reverse Capacitance: 0.2 pF
- Low Guaranteed r_{DS} @ 5 V
- Low Turn-On Threshold Voltage

BENEFITS

- High-Speed System Performance
- Low Insertion Loss at High Frequencies
- Low Transfer Signal Loss
- Simple Driver Requirement
- Single Supply Operation

APPLICATIONS

- Fast Analog Switch
- Fast Sample-and-Holds
- Pixel-Rate Switching
- Video Switch
- Multiplexer
- DAC Deglitchers
- High-Speed Driver

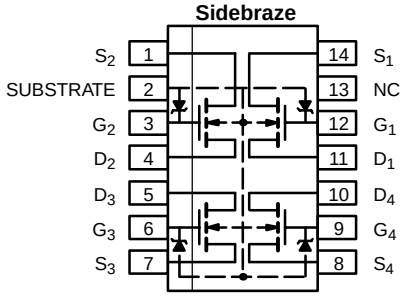
DESCRIPTION

The SD5000I-2 monolithic switch features four individual double-diffused enhancement-mode MOSFETs built on a common substrate. This bidirectional device provides low on-resistance and low interelectrode capacitances to minimize insertion loss and crosstalk.

Built on Vishay Siliconix' proprietary DMOS process, the SD5000I-2 utilizes lateral construction to achieve low capacitance and ultra-fast switching speeds. For manufacturing reliability, these devices feature poly-silicon gates protected by Zener diodes.

The SD5000I is available only in the "–2" extended hi-rel flow. The Vishay Siliconix "–2" flow complies with the requirements of MIL-PRF-19500 for JANTX discrete devices.

Dual-In-Line
Sidebraze



Top View

Applications Information—See Applications Note AN502

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C UNLESS OTHERWISE NOTED)

Gate-Drain, Gate-Source Voltage . . . . . +30 V/–25 V
Gate-Substrate Voltage . . . . . +30 V/–0.3 V
Drain-Source Voltage . . . . . 20 V
Drain-Source-Substrate Voltage . . . . . 25 V
Drain Current . . . . . 50 mA
Lead Temperature ($^1/_{16}$" from case for 10 seconds) . . . . . 300°C

Storage Temperature . . . . . –65 to 150°C
Operating Junction Temperature . . . . . –55 to 150°C
Power Dissipation[a, b]: (Package) . . . . . 500 mW
(Each Device) . . . . . 300 mW

Notes:
a. Derate 4 mW/°C above 25°C

SPECIFICATIONS[a]

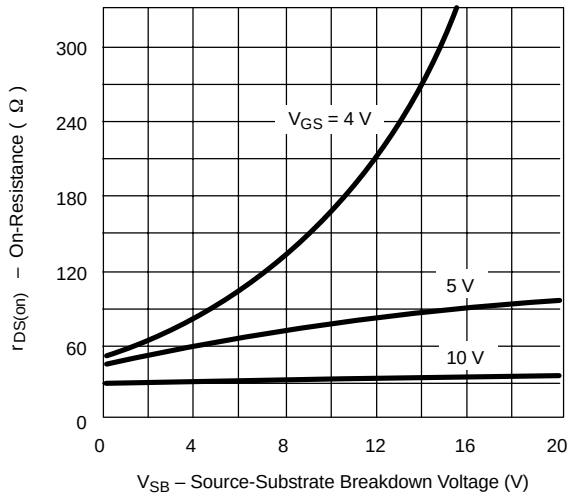
Parameter	Symbol[b]	Test Conditions[b]		Limits Min	Limits Typ[c]	Limits Max	Unit
Static							
Drain-Source Breakdown Voltage	$V_{(BR)DS}$	V_{GS} = V_{BS} = –5 V, I_D = 10 nA		20	30		V
Source-Drain Breakdown Voltage	$V_{(BR)SD}$	V_{GD} = V_{BD} = –5 V, I_S = 10 nA		20	22		
Drain-Substrate Breakdown Voltage	$V_{(BR)DBO}$	V_{GB} = 0 V, I_D = 10 nA, Source Open		25	35		
Source-Substrate Breakdown Voltage	$V_{(BR)SBO}$	V_{GB} = 0 V, I_S = 10 μA, Drain Open		25	35		
Drain-Source Leakage	$I_{DS(off)}$	V_{GS} = V_{BS} = –5 V	V_{DS} = 10 V		0.4		nA
			V_{DS} = 15 V		0.7		
			V_{DS} = 20 V		0.9	10	
Source-Drain Leakage	$I_{SD(off)}$	V_{GD} = V_{BD} = –5 V	V_{SD} = 10 V		0.5		
			V_{SD} = 15 V		0.8		
			V_{SD} = 20 V		1	10	
Gate Leakage	I_{GBS}	V_{DB} = V_{SB} = 0 V, V_{GB} = 30V			0.01	100	
Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 μA, V_{SB} = 0 V		0.1	0.8	1.5	V
Drain-Source On-Resistance	$r_{DS(on)}$	V_{SB} = 0 V, I_D = 1 mA	V_{GS} = 5 V		58	70	Ω
			V_{GS} = 10 V		38		
			V_{GS} = 15 V		30		
			V_{GS} = 20 V		26		
Resistance Match	$\Delta r_{DS(on)}$		V_{GS} = 5 V		1	5	
Dynamic							
Forward Transconductance	g_{fs}	V_{DS} = 10 V, V_{SB} = 0 V, I_D = 20 mA, f = 1 kHz		10	12		mS
Gate-Node Capacitance	$C_{(GS+GD+GB)}$	V_{DS} = 10 V, f = 1 MHz, V_{GS} = V_{BS} = –15 V			2.5	3.5	pF
Drain-Node Capacitance	$C_{(GD+DB)}$				2.0	3	
Source-Node Capacitance	$C_{(GS+SB)}$				3.7	5	
Reverse Transfer Capacitance	c_{rss}				0.2	0.5	
Crosstalk		f= 3 kHz			–107		dB
Switching							
Turn-On Time	$t_{d(on)}$	V_{SB} = 5 V, V_{IN} 0 to 5 V, R_G = 25 Ω, V_{DD} = 5 V, R_L = 680 Ω			0.5	1	ns
	t_r				0.6	1	
Turn-Off Time	$t_{d(off)}$				2		
	t_f				6		

Notes:
a. T_A = 25°C unless otherwise noted.
b. B is is the body (substrate) and $V_{(BR)}$ is breakdown.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

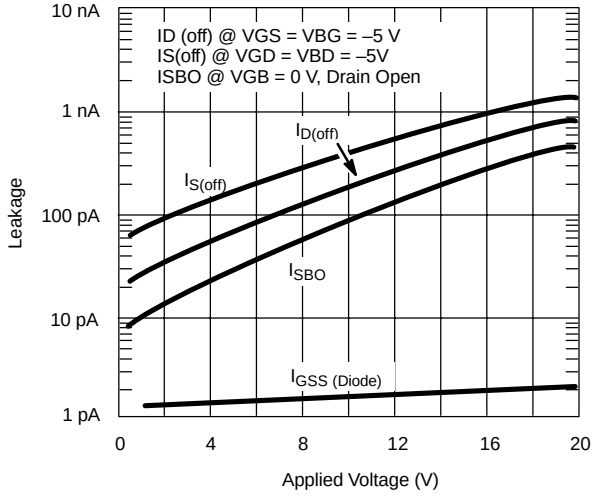
DMCA

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

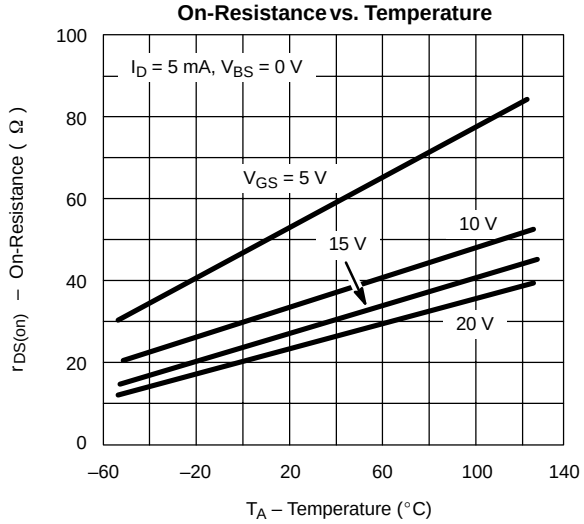
On-Resistance vs. Gate-Source Voltage



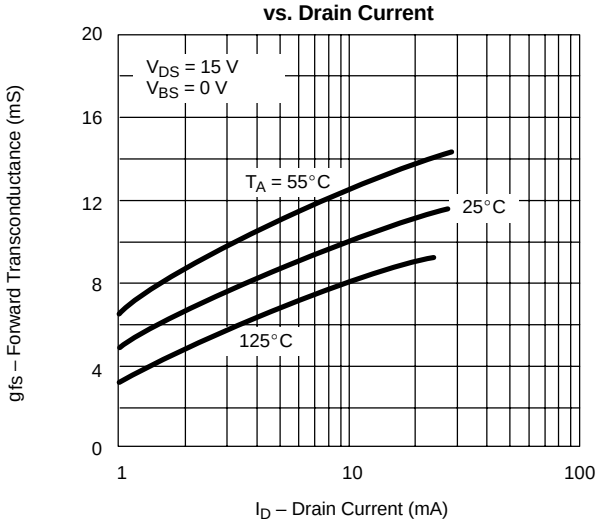
Leakage Current vs. Applied Voltage



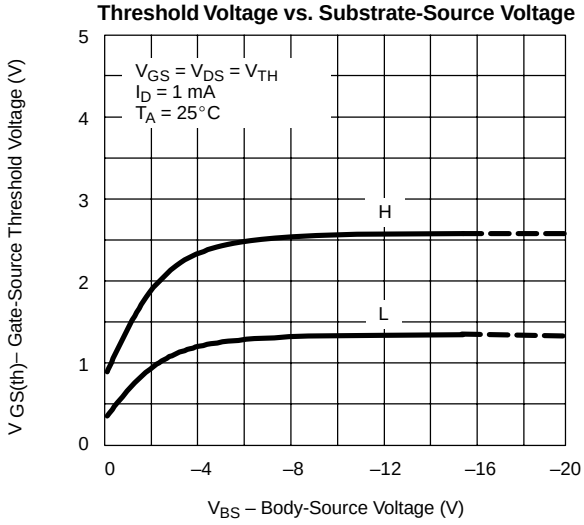
On-Resistance vs. Temperature



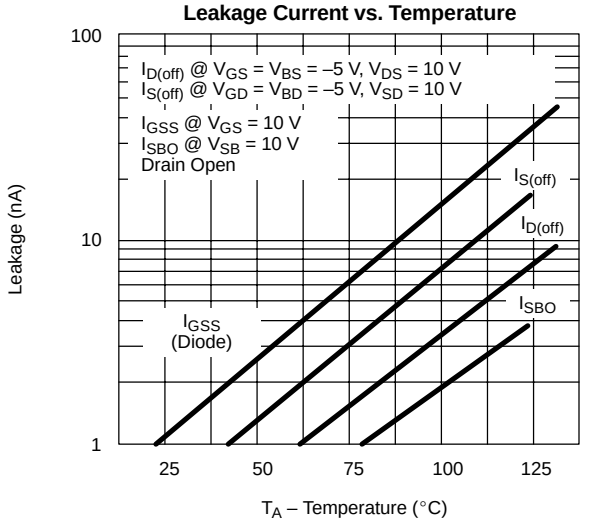
Common-Source Forward Transconductance vs. Drain Current



Threshold Voltage vs. Substrate-Source Voltage

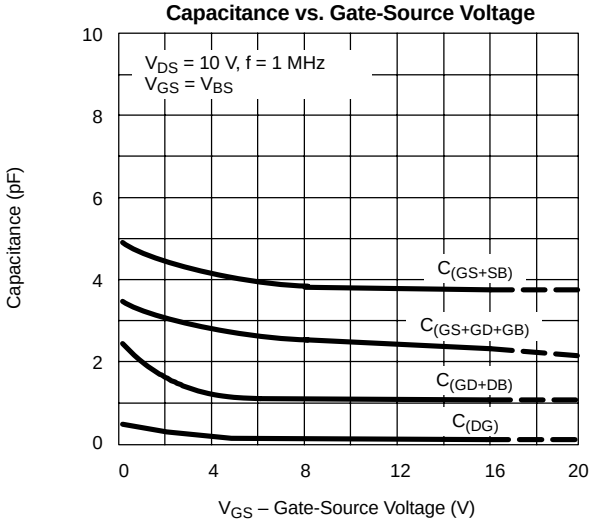


Leakage Current vs. Temperature

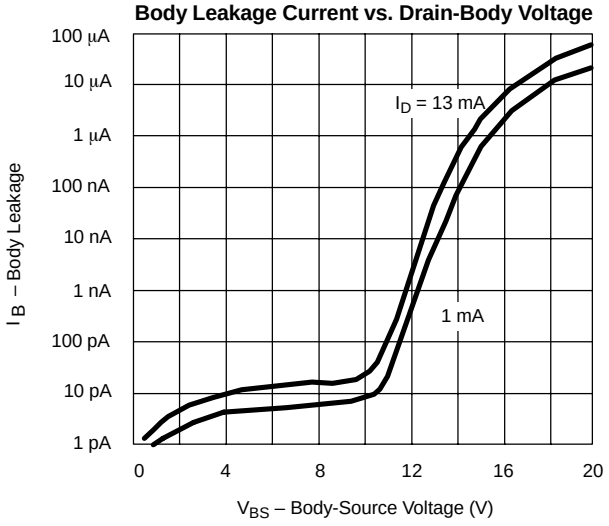


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

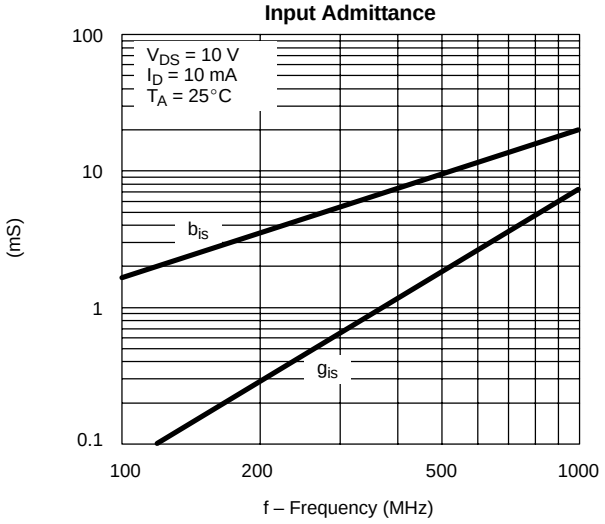
Capacitance vs. Gate-Source Voltage



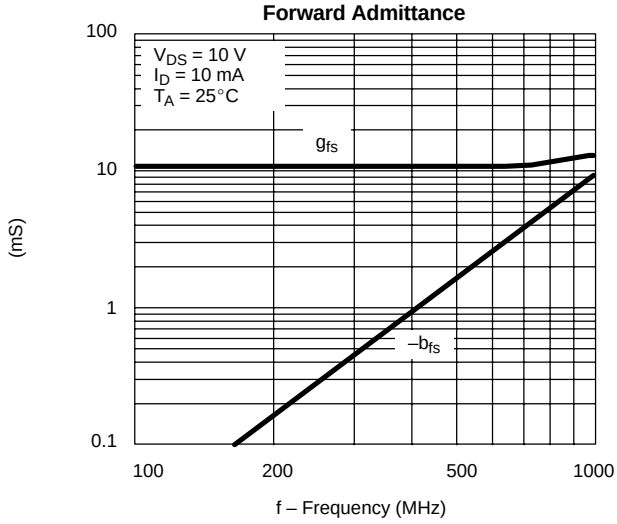
Body Leakage Current vs. Drain-Body Voltage



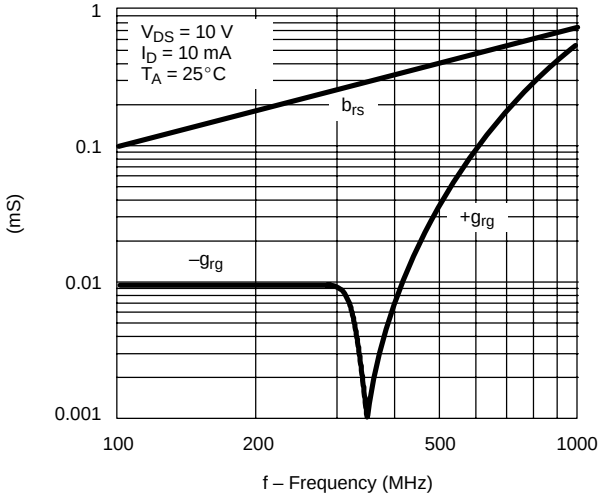
Input Admittance



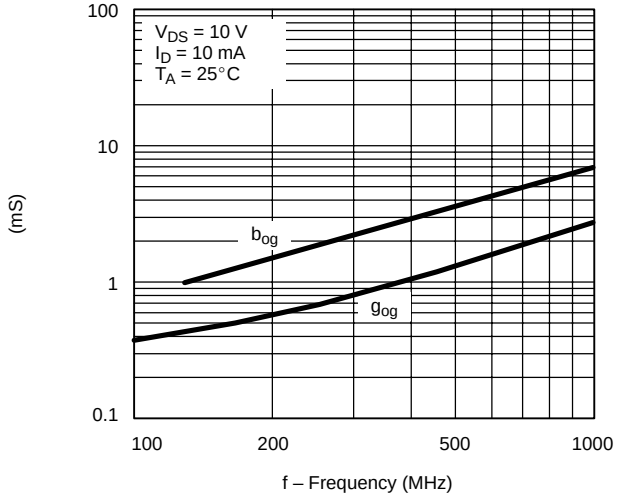
Forward Admittance



Reverse Admittance

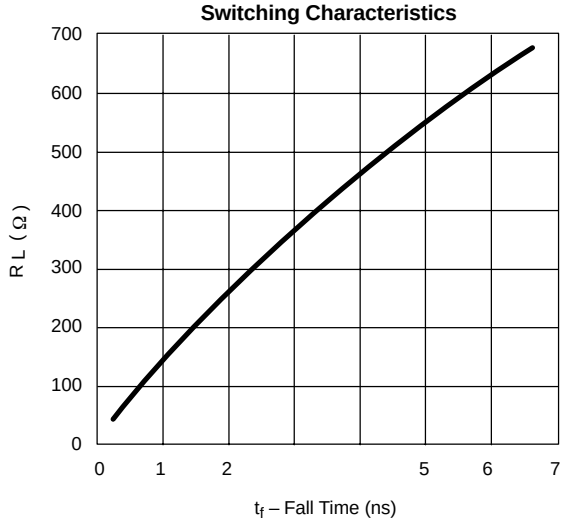


Output Admittance

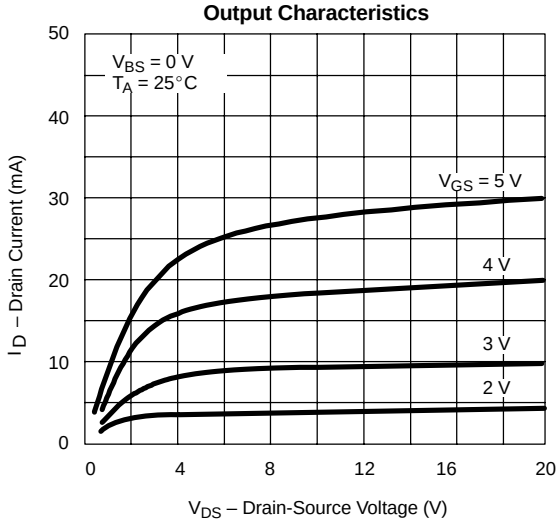


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

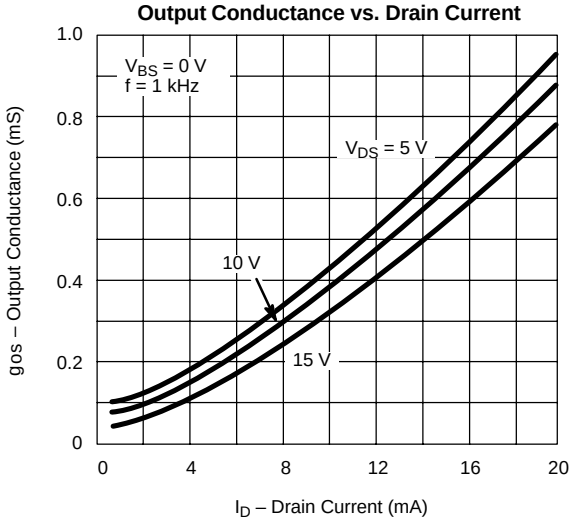
Switching Characteristics



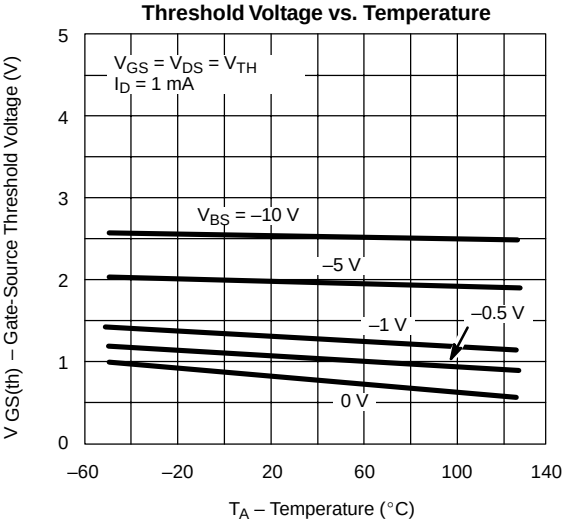
Output Characteristics



Output Conductance vs. Drain Current



Threshold Voltage vs. Temperature



SWITCHING TIME TEST CIRCUIT