SPDC12L00010

10 A DC/DC converter module

Preliminary Data

Features

- MTBF 1 000 000 (T_A = 25 °C)
- 10 A max output current
- Input voltage range from 1.8 V to 14 V
- Supply voltage range from 4.5 V to 14 V
- Fixed or adjustable output voltage down to 0.6 V
- Fixed frequency voltage mode control
- Adjustable switching frequency
- Soft-start and inhibit
- Selectable UVLO threshold (5 V or 12 V bus)
- Master/slave synchronization with 180° phase shift
- Pre-bias start-up capability
- Selectable source/sink or source only capability after soft-start
- Power Good output with programmable delay
- Over voltage protection with selectable latched/not-latched mode
- Thermal shut-down
- Operating temperature range -40 °C ÷ 85 °C

Applications

- Laptop
- Blade servers
- RAID systems
- Network routers
- Cellular base stations
- Industrial equipment
- Test instrumentation
- Medical diagnostic equipment
- Points of load regulation

Table 1. Device summary

Order code	Output voltage [V]	Input voltage [V]	Output ripple [mVpp]	Efficiency [%]	Notes
SPDC12L00010	0.6 ÷ 5	1.8 ÷ 14	40	70 ÷ 93	Progr. output voltage

Contents

1 Description

The ST SPDC12L00010 high density 10 A DC-DC converter is a complete step-down power supply. A single LGA package includes ST switching controller, power FETs, inductor and all the support components. SPDC12L00010 operates over a wide input voltage range of 1.8 V to 14 V, supporting an output range of 0.6 V to 5 V. High level of integration and synchronous rectification allows the SPDC12l00010 to deliver up to 10 A continuous current at up to 93% efficiency, without external heat sink or airflow.

The device is a complete stand alone surface mount power supply, that can be handled and assembled like a standard integrated circuit. Moreover its low profile design permits the SPDC12L00010 to be soldered onto the back side of a printed circuit board, freeing up valuable board space.

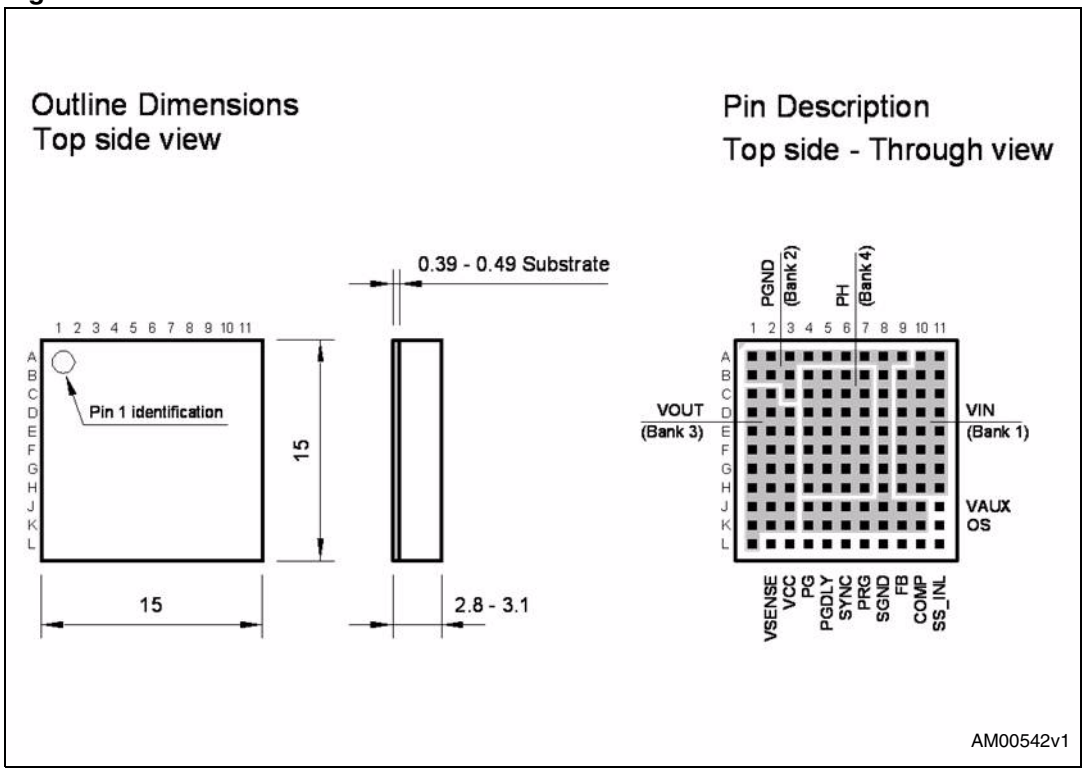
SPDC12L00010 is self protected against over voltage and short circuit conditions. A built in adjustable soft-start and inhibit guarantee correct functionality whatever the load is. Pre-bias start up capability is in place as well Power Good output with programmable delay to avoid false signals.

The device is packaged in a thermally enhanced, compact (15 x 15 mm) and low profile (3 mm) over molded land grid array (LGA) package, suitable for automated assembly by standard surface mount equipment. The SPDC12L00010 is Pb-Free and RoHS compliant.

2 Pin settings

2.1 Pin connection and mechanical data (dimensions in mm)

Figure 1. Pin connection



2.2 Pin description

Table 2. Pin description

Name	Function	Description
J11	VAUX	Auxiliary voltage. Internally regulated 5 V voltage. It is used to supply the internal drivers and the voltage reference.
K11	OS	Oscillator set. Connecting a resistor from this pin to SGND or to VAUX, the switching frequency can be increased or decreased. In OVP status the pin is pulled to 4.5 V (latched mode only).
L2	VSENSE	Voltage sense. Using this pin it is possible to recover the voltage drop on Vout track.
L3	VCC	VCC. Controller voltage supply pin. The operative voltage range for the internal controller is 4.5 V to 14 V

Table 2. Pin description (continued)

Name	Function	Description
L4	PG	Power Good. This pin is an open collector output, with a 10 kΩ pull-up resistor connected to VAUX. It is pulled low if the output voltage is not within specified thresholds (90%-110%).
L5	PGDLY	Power Good delay. A capacitor connected between this pin and SGND, introduce a delay between the internal PG comparator and the external signal rising edge. No delay can be introduced on the falling edge of PG signal.
L6	SYNC	Synchronization. This is the master/slave pin. Two or more devices can be synchronized connecting the SYNC pins together.
L7	PRG	Program. This pin allows following settings: - Enable/disable the current sink mode capability after soft-start; - Enable/disable the OVP latch mode; - Setting UVLO threshold for 5 V or 12 V bus.
L8	SGND	Signal ground. All references are referred to these pins, internally connected to PGND.
L9	FB	Feed-back. This pin is connected to the error amplifier inverting input.
L10	COMP	Compensation. This pin is connected to the error amplifier output.
L11	SS_INL	Soft-start_inhibit low The soft-start time is programmed connecting an external capacitor from this pin to SGND; This pin can be used to inhibit the module.
Bank 1	VIN	DC input voltage. See *Section 5.18 on page 18* for mandatory condition.
Bank 2	PGND	Return for input/output voltage source.
Bank 3	VOUT	Regulated power output. See *Section 5.19 on page 18* for mandatory condition.
Bank 4	PH	Phase This pins area is foreseen for module power losses dissipation; see *Section 5.20 on page 19* for details.

3 Maximum ratings

3.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{K11}	OS to SGND and PGND	-0.3 to 6	V
V_{L2}	VSENSE to SGND and PGND	-0.3 to 18	V
V_{L3}	VCC to SGND and PGND	-0.3 to 18	V
V_{L4}	PG to SGND and PGND	-0.3 to 18	V
V_{L5}	PGDLY to SGND and PGND	-0.3 to 6	V
V_{L6}	SYNC to SGND and PGND	-0.3 to 6	V
V_{L7}	PRG to SGND and PGND	-0.3 to 6	V
V_{L9}	FB to SGND and PGND	-0.3 to 6	V
V_{L10}	COMP to SGNG and PGND	-0.3 to 6	V
V_{L11}	SS_INL to SGND and PGND	-0.3 to 6	V
V_i	VIN to SGND and PGND	-0.3 to 18	V
V_o	VOUT to SGND and PGND	-0.3 to 18	V
I_o	Maximum output current	Int. limited	A

3.2 Thermal data

Table 4. Table 3. Thermal data

Symbol	Parameter	Value	Unit
T_{STG}	Storage temperature range	-40 ÷ 105	°C
T_{OP}	Operating temperature range	-40 ÷ 85	°C

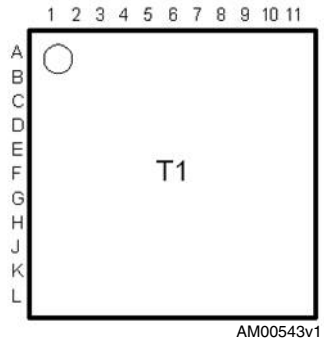
3.3 Thermal de-rating

The thermal de-rating is obtained reducing the maximum output current, to limit the module temperature to the maximum allowable value.

Since a lot of parameters affect the module power dissipation, the best way to get a precise thermal de-rating is to measure the module temperature in the final application condition.

For this purpose, the case top side must be monitored at the central point T1 (see *Figure 2*); the maximum temperature allowable value at T1 is 125 °C.

Figure 2. Measurement points for thermal de-rating (top side)



All data reported in the following tables are valid for free air condition and module placed on 25 cm_2, 4 layers, 1.6 mm FR4 printed circuit board.

Table 5. Thermal de-rating for Vout = 5.0 V

Symbol	Parameter	Test condition	Value	Unit
I_o	Output current	V_{IN} = 8 V T_A = 75 °C	TBD	A
		V_{IN} = 8 V T_A = 80 °C	TBD	
		V_{IN} = 8 V T_A = 85 °C	TBD	
I_o	Output current	V_{IN} = 10 V T_A = 70 °C	TBD	A
		V_{IN} = 10 V T_A = 75 °C	TBD	
		V_{IN} = 10 V T_A = 80 °C	TBD	
		V_{IN} = 10 V T_A = 85 °C	TBD	
I_o	Output current	V_{IN} = 12 V T_A = 60 °C	TBD	A
		V_{IN} = 12 V T_A = 65 °C	TBD	
		V_{IN} = 12 V T_A = 70 °C	TBD	
		V_{IN} = 12 V T_A = 75 °C	TBD	
		V_{IN} = 12 V T_A = 80 °C	TBD	
		V_{IN} = 12 V T_A = 85 °C	TBD	

Table 5. Thermal de-rating for Vout = 5.0 V (continued)

Symbol	Parameter	Test condition	Value	Unit
I_o	Output current	V_{IN} = 14 V T_A = 50 °C	TBD	A
		V_{IN} = 14 V T_A = 55 °C	TBD	
		V_{IN} = 14 V T_A = 60 °C	TBD	
		V_{IN} = 14 V T_A = 65 °C	TBD	
		V_{IN} = 14 V T_A = 70 °C	TBD	
		V_{IN} = 14 V T_A = 75 °C	TBD	
		V_{IN} = 14 V T_A = 80 °C	TBD	
		V_{IN} = 14 V T_A = 85 °C	TBD	

Table 6. Thermal de-rating for Vout = 3.3 V

Symbol	Parameter	Test condition	Value	Unit
I_o	Output current	V_{IN} = 8 V T_A = 80 °C	TBD	A
		V_{IN} = 8 V T_A = 85 °C	TBD	
I_o	Output current	V_{IN} = 10 V T_A = 75 °C	TBD	A
		V_{IN} = 10 V T_A = 80 °C	TBD	
		V_{IN} = 10 V T_A = 85 °C	TBD	
I_o	Output current	V_{IN} = 12 V T_A = 70 °C	TBD	A
		V_{IN} = 12 V T_A = 75 °C	TBD	
		V_{IN} = 12 V T_A = 80 °C	TBD	
		V_{IN} = 12 V T_A = 85 °C	TBD	
I_o	Output current	V_{IN} = 14 V T_A = 65 °C	TBD	A
		V_{IN} = 14 V T_A = 70 °C	TBD	
		V_{IN} = 14 V T_A = 75 °C	TBD	
		V_{IN} = 14 V T_A = 80 °C	TBD	
		V_{IN} = 14 V T_A = 85 °C	TBD	

Table 7. Thermal de-rating for Vout = 2.5 V

Symbol	Parameter	Test condition	Value	Unit
I_o	Output current	V_{IN} = 10 V T_A = 80 °C	TBD	A
		V_{IN} = 10 V T_A = 85 °C	TBD	
I_o	Output current	V_{IN} = 12 V T_A = 75 °C	TBD	A
		V_{IN} = 12 V T_A = 80 °C	TBD	
		V_{IN} = 12 V T_A = 85 °C	TBD	
I_o	Output current	V_{IN} = 14 V T_A = 70 °C	TBD	A
		V_{IN} = 14 V T_A = 75 °C	TBD	
		V_{IN} = 14 V T_A = 80 °C	TBD	
		V_{IN} = 14 V T_A = 85 °C	TBD	

Table 8. Thermal de-rating for Vout = 1.8 V

Symbol	Parameter	Test condition	Value	Unit
I_o	Output current	V_{IN} = 10 V T_A = 80 °C	TBD	A
		V_{IN} = 10 V T_A = 85 °C	TBD	
I_o	Output current	V_{IN} = 12 V T_A = 80 °C	TBD	A
		V_{IN} = 12 V T_A = 85 °C	TBD	
I_o	Output current	V_{IN} = 14 V T_A = 80 °C	TBD	A
		V_{IN} = 14 V T_A = 85 °C	TBD	

Table 9. Thermal de-rating for Vout = 1.2 V

Symbol	Parameter	Test condition	Value	Unit
I_o	Output current	V_{IN} = 14 V T_A = 80 °C	TBD	A
		V_{IN} = 14 V T_A = 85 °C	TBD	

4 Electrical characteristics

Table 10. Electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
V_r	Ripple voltage	V_{IN} = 12 V, I_o = 10 A, C_o = 2x330 µF BW = 20 MHz		40		mVpp
I_o	Output current	V_{IN} = 1.8 ÷ 14 V	0		10	A
I_{ol}	Current limit	V_{IN} = 1.8 ÷ 14 V		12		A
I_q	Total quiescent current	V_{CC} = 12 V, I_o = 0 A		65		mA
$I_{qst\text{-}by}$	Total stand-by quiescent current	V_{SS_INL} < 0.5 V		5		mA
I_{CCq}	V_{CC} quiescent current	V_{CC} = 12 V, I_o = 0 A, OS = open, V_{SS_INL} > 0.5 V		35		mA
$I_{CCqst\text{-}by}$	V_{CC} stand-by quiescent current	V_{CC} = 12 V, I_o = 0 A, OS = open, V_{SS_INL} < 0.5 V		5		mA
f_s	Switching frequency	V_{CC} = 12 V, I_o = 10 A, T_A = 0 ÷ 85 °C	678	729	780	kHz
V_{FB}	Feedback voltage (Reference voltage)	T_A = -40 ÷ 85 °C	0.593	0.6	0.605	V
V_{AUX}	Auxiliary voltage	V_{CC} = 5.5 ÷ 14 V, I_{AUX} = 1 ÷ 100 mA	4.5	5	5.5	V
V_{SS_INL}	Inhibit threshold	Device OFF			0.5	V
I_{SS_INL}	Soft-start current	V_{SS_INL} = 2 V	7	10	13	µA
		V_{SS_INL} = 0 ÷ 0.5 V	20	30	45	
V_{PG}	Power Good voltage low	I_{PG} = -5 mA		0.5		V
V_{PGhth}	Power Good high threshold (V_{FB}/0.6)	V_{FB} rising	108	110	112	%
V_{PGlth}	Power Good low threshold (V_{FB}/0.6)	V_{FB} falling	88	90	92	%
V_{OVhth}	Overvoltage high threshold (V_{FB}/0.6)	V_{FB} rising		120		%
V_{OVlth}	Overvoltage low threshold (V_{FB}/0.6)	V_{FB} falling		117		%
V_{CConth}	V_{CC} turn-on threshold	5 V BUS, V_{IN} > 1.7 V	4.0	4.2	4.4	V
		12 V BUS, V_{IN} > 1.7 V	8.3	8.6	8.9	
$V_{CCoffth}$	V_{CC} turn-off threshold	5 V BUS, V_{IN} > 1.7 V	3.6	3.8	4.0	V
		12 V BUS, V_{IN} > 1.7 V	7.4	7.7	8.0	
V_{INhth}	V_{IN} high threshold	V_{IN} rising	1.1	1.25	1.47	V
V_{INlth}	V_{IN} low threshold	V_{IN} falling	0.9	1.05	1.27	V

5 Application information

5.1 Input voltage

There are two voltage supply pins:

VCC (pin L3), for controller voltage supply;

VIN (bank 1), for power circuit voltage supply.

VCC and VIN can be connected and supplied together;

if VIN is lower than 4.5 V, VCC must be supplied separately.

The recommended maximum operating DC input voltage is 14 V.

5.2 Auxiliary voltage

VAUX (pin J11) pin must be used to supply PRG and OS setting resistors.

No capacitor is required.

5.3 Inhibit function

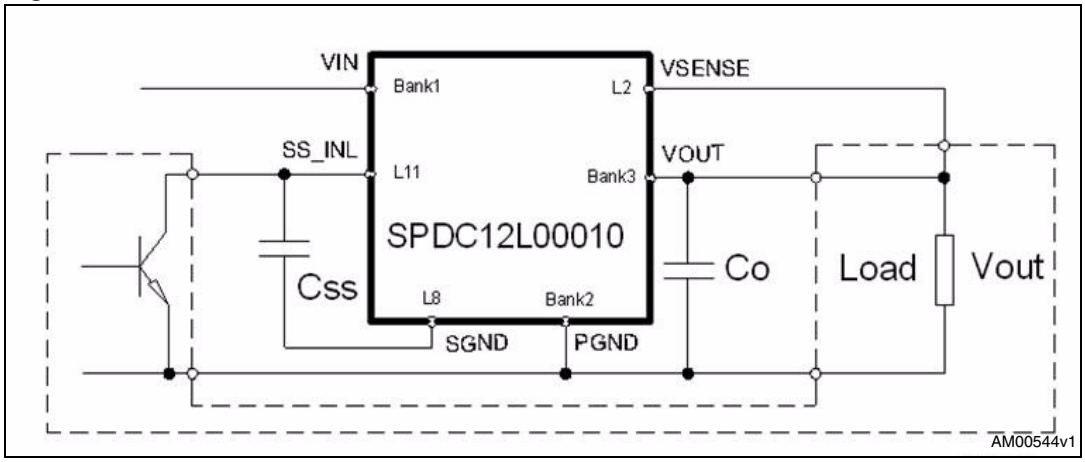
SS_INL (pin L11) allows putting the device in stand-by mode.

With SS_INL lower than 0.5 V, the device is disabled and the current consumption is reduced to 5 mA, for VIN = 12 V.

With SS_INL higher than 0.5 V the device is enabled.

Since SS_INL has soft-start function, it is mandatory to implement the inhibit function using an open collector device (i.e. small signal transistor), to not influence the module behavior (see *Figure 3*).

Figure 3. Inhibit function



5.4 Soft-start

The soft-start phase begins when both VCC and VIN raise above their turn-on thresholds, otherwise the SS_INL pin is internally shorted to SGND.

A ramp is generated at SS_INL pin during start-up, charging the external capacitor CSS with an internal current generator.

The initial value for this current is 30 μA and it charges the capacitor up to 0.5 V, after that, it is reduced to 10 μA until the final charge value approximately 4 V.

In the meanwhile, the controller internal voltage reference raises to its final value, following the SS_INL pin voltage slope.

During soft-start, the module provides a constant current protection, limiting the output current at the maximum value, without entering in HICCUP mode.

If there is not current limitation, the output voltage slope follows the SS_INL pin slope.

The output voltage rise time, can be set choosing proper CSS value.

The soft-start phase ends when the SS_INL pin voltage reaches 3.5 V.

A capacitor CSS = 3 3 nF is present on the module, to perform a minimum soft-start time, suitable for Co = 10000 μF max. output capacitor;

in this condition and with 10 A output current resistor load, the output voltage rise time is around 5ms, but the complete soft-start time is around 10ms.

Using the minimum output capacitor Co = 660 μF and with 10 A resistor load, the output voltage rise time is around 2 ms.

5.5 Multiple units synchronization

Using more than one unit on the same circuit, it is possible to synchronize the switching frequency oscillators, connecting all SYNC (pin L6) together.

The device with the higher switching frequency will be the Master, while the other will be the Slaves.

The best way to synchronize two or more devices is to set same switching frequency, in any case, the switching frequencies can differ for a maximum of 50% of the lowest one.

Using and external clock signal, to synchronize one or more devices working at a different switching frequency, it is recommended to follow the below formula:

$$f_{sw} \leq f_{ext} \leq 1.3 f_{sw}$$

The phase shift between master and slaves is approximately 180°.

5.6 Power Good signal and Power Good delay

The output voltage is monitored by FB (pin L9), if it is not within ± 10% (typ.) of the programmed value, the PG (pin L4) output is forced low.

The PG signal can be delayed by adding an external capacitor on PGDLY (pin L5), the delay can be calculated with the following formula:

$$PG_{delay} = 0.5 \times C_{PGDLY}(pF) \quad [\mu s]$$

5.7 Oscillator setting

The switching frequency is internally fixed to 729 kHz, this value can be slightly varied using an external resistor R_{OS} connected between OS (pin K11) and SGND (L8) or VAUX (pin J11).

Since the OS pin is maintained at fixed voltage (typ. 1.2), the frequency is increased/decreased proportionally to the current sunk/sourced from/into the pin.

In particular, connecting R_{OS} to SGND the frequency is increased according the following formula:

$$f_{SW} = 729 + (9.88 \times 10^6 / R_{OS}) \quad [kHz]$$

Connecting R_{OS} to VAUX the frequency is reduced according to the following formula:

$$f_{SW} = 729 - (30.1 \times 10^6 / R_{OS}) \quad [kHz]$$

5.8 Current sink-mode

Connecting a proper resistor (see par. *Section 5.10 on page 15*) from PRG (pin L7) to VAUX (pin J11), it is possible to select the sink-mode operation, that means to allow the output current to reverse its polarity into the converter output inductor.

If the sink-mode is enabled, the converter can sink current from the load after soft-start;

If the sink-mode is disabled, the converter never sinks current.

Note: When output low current operation is required (Iout < 2 A), sink-mode operation is recommended, this condition improves output voltage transient response and reduces output voltage ripple.

5.9 Under voltage lock out

Connecting a proper resistor (see par. *Section 5.10*) from PRG (pin L7) to VAUX (pin J11), it is possible to select two different thresholds for UVLO:

4.2 V/3.8 V for 5 V input range;

8.6 V/7.7 V for 12 V input range.

5.10 Program setting

Connecting a resistor from PRG (pin L7) to VAUX (pin J11), it is possible to select different operation modes, according to the following table:

Table 11. Program setting

R_{PRG}	UVLO.	OVP	Sink-mode
n.c.	5 V range	Not latched	Not
11 kΩ		Not latched	Yes
6.2 kΩ		Latched	Not
4.3 kΩ		Latched	Yes
2.7 kΩ	12 V range	Not latched	Not
1.8 kΩ		Not latched	Yes
1.2 kΩ		Latched	Not
0 Ω		Latched	Yes

5.11 Voltage sensing

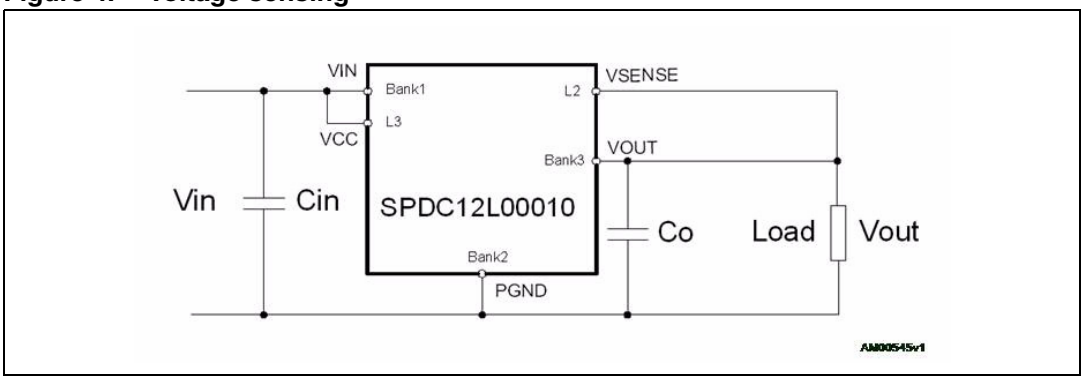
Using VSENSE (pin L2) it is possible to recover the voltage drop on VOUT PCB track.

Connect VSENSE in a point closed to the load (see *Figure 4*).

Using VSENSE connection, it will not recover the voltage drop on PGND PCB track.

Leaving VSENSE floating, the output voltage will be sensed at VOUT (bank 3).

Figure 4. Voltage sensing



5.12 Output voltage programming

Adding a resistor Rx between FB (pin L9) and SGND (L8) or between FB and VSENSE (pin L2), it is possible to change the output voltage.

Connecting the resistor to SGND the output voltage increase (see *Figure 5* a);

Connecting the resistor to VSENSE the output voltage decrease (see *Figure 5* b).

Calculate the resistor for increasing output voltage with the following formula:

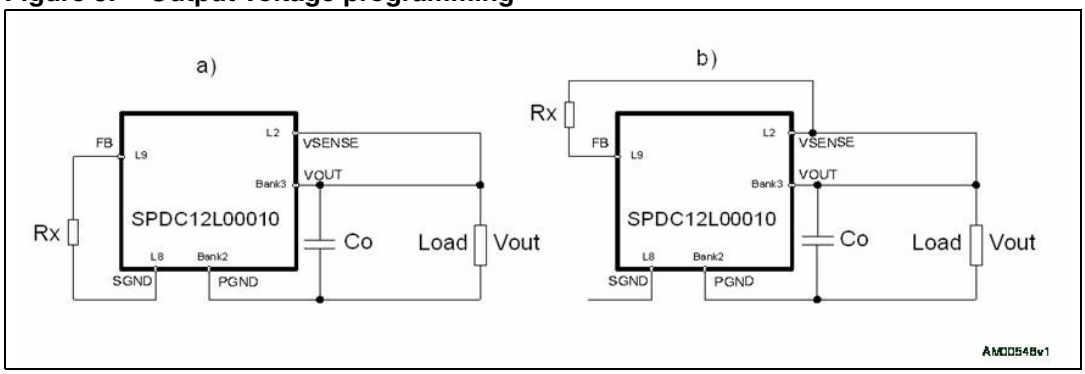
$R_x = 0.6 / (V_{OUT} - 1.2)$ [kΩ] valid for $V_{OUT} > 1.2$ V

Calculate the resistor for decreasing output voltage with the following formula:

$R_x = (V_{OUT} - 0.6) / (1.2 - V_{OUT})$ [kΩ] valid for $0.6 < V_{OUT} < 1.2$ V

The module output voltage is 1.2 V with R_x = n.c.

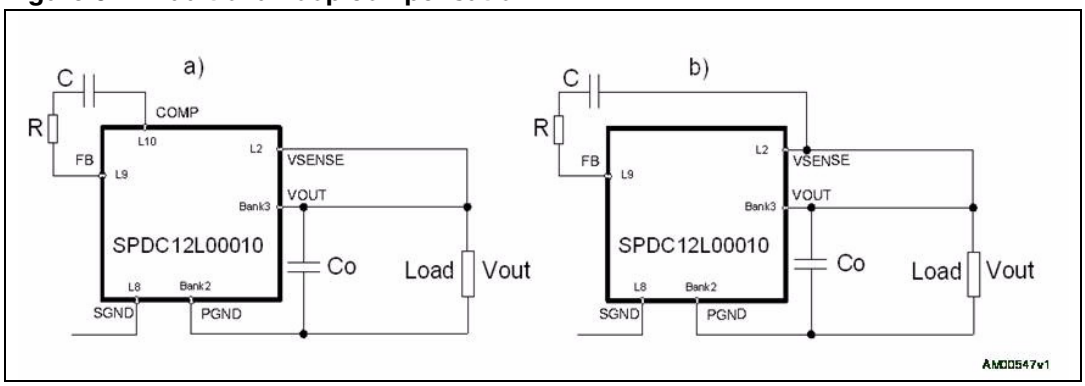
Figure 5. Output voltage programming



5.13 Additional loop compensation

If required by particular load condition, it is possible to change the feedback loop compensation, adding a pole with an external R-C network between FB (pin L9) and COMP (pin L10) (see *Figure 6* a), or adding a zero with an external R-C network between FB and VSENSE (pin L2) (see *Figure 6* b).

Figure 6. Additional loop compensation



5.14 Output over voltage protection

The device provides OVP:

when the voltage sensed on FB (pin L9) reaches a value greater than 20% of reference, the on module low side driver is turned ON and the converter stop switching operation.

If the OVP not latched mode has been set, the on module low side MOSFET is kept ON, as long as the over voltage condition is detected.

If OVP latched mode has been set, the low side MOSFET is turned ON and the OS (pin K11) is forced high (4.5 V typ.), until VCC is toggled.

It must be taken in account that there is an electrical network between the output terminal and FB, therefore the voltage at this pin is not a perfect replica of output voltage.

If the converter is set to sink current, the low side MOSFET could be turned ON before the output voltage exceeds the over voltage threshold (109% typ.), because the error amplifier will change its balance in advance.

If the sink-mode is disabled, the low side MOSFET will be turned ON only when the OVP operate, in this case a delay between the output voltage rising and the FB rising can appear and the OVP can operate late (126% typ.).

5.15 Current limitation

The device realizes the over current protection sensing the current on board high side MOSFET and on board low side MOSFET, therefore two current limits are set:

peak current limit and valley current limit.

The peak current protection is active when the high side MOSFET is turned ON, the valley current protection is enabled when the low side MOSFET is turned ON.

After soft-start is completed, if an over current occurs, the device enters in HICCUP mode:

both high side and low MOSFETs are turned OFF;

the soft-start capacitor is discharged with a 10 μA constant current;

when the voltage on SS_INL (pin L11) reaches 0.5 V the soft-start phase restart.

During the soft-start phase the OCP provides a constant current protection.

5.16 Thermal shutdown

When the controller junction temperature reaches 150 ± 10 °C, the device shutdown.

Both MOSFET are turned OFF and the soft-start capacitor is discharged.

The device does not restart until the junction temperature goes down to 120 °C and until the voltage on the soft-start capacitor reaches 0.5 V.

5.17 Signal ground and power ground

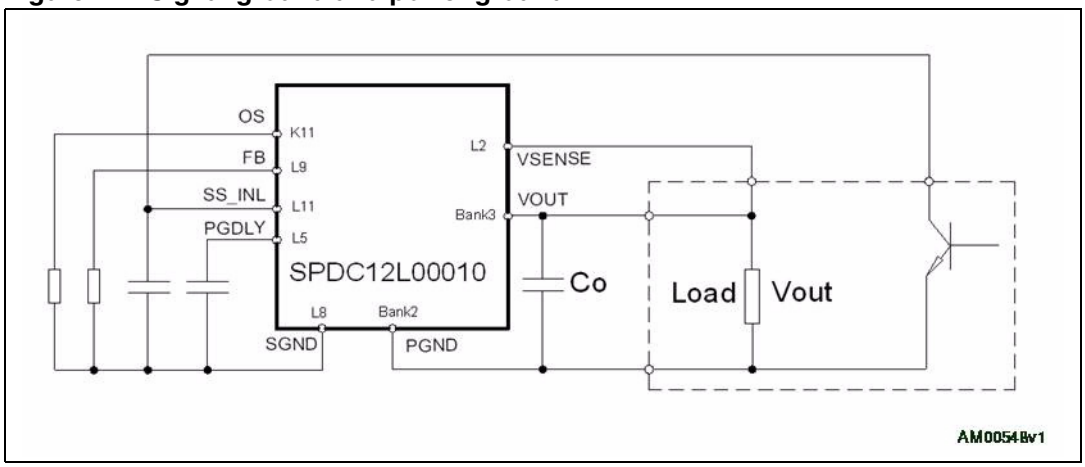
SGND (L8) and PGND (bank 2) are connected together on the module.

Connect to SGND the capacitor for PGDLY and SS_INL, the resistor for FB and OS.

Connect to PGND the return for SS_INL.

It is important to not create a ground loop between SGND, PGND and other GND present on the application circuit (see *Figure 7*).

Figure 7. Signal ground and power ground



5.18 Input capacitors

The input capacitor present on the module is not able to sustain the input RMS current.

Connect 2 x 2.2 µF 16 V X7R ceramic capacitor (Cin) closed to the input pins VIN and PGND (bank 1 and bank 2), to satisfy minimum functional requirement.

Connect proper low impedance capacitors to reduce the input ripple current, according to the application requirement.

5.19 Output capacitors

The output capacitors present on the module are able to sustain output RMS current.

Connect 2 x 330 µF POSCAP SANYO capacitor (Co) or equivalent, closed to the output pins VOUT and PGND (bank 3 and bank 2), to guarantee output voltage stability and specified voltage ripple.

5.20 Phase connection

On the module bottom, there is an area relative to PH (bank 4) connection:

this area is internally connected to the high side MOSFET source and to the low side MOSFET drain;

this electrical point is used to dissipate heat generated by the two MOSFETs.

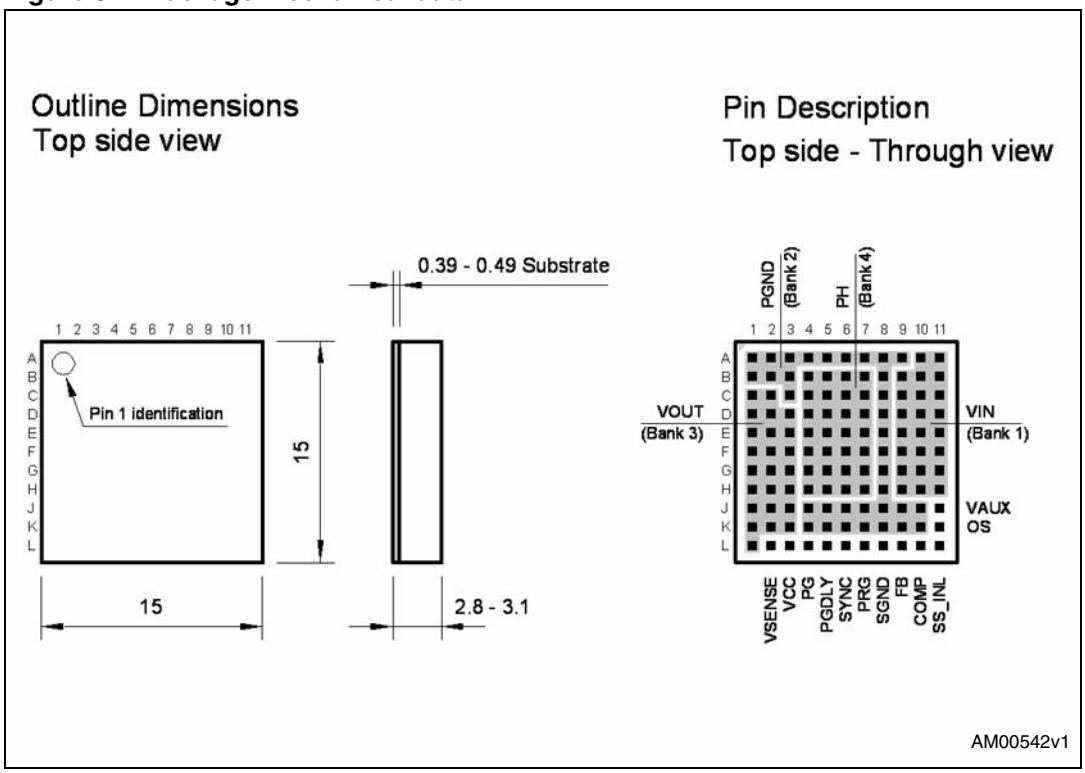
Connect PH (bank 4), to an insulated copper area on the mother board, to ensure proper heat sink.

Since the PH signal contains very fast voltage transients, it is recommended to take in account possible inducted noise on mother board, i.e.: it is advised against to lead under the module printed circuit board tracks with susceptible signals.

6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

Figure 8. Package mechanical data



6.1 Soldering

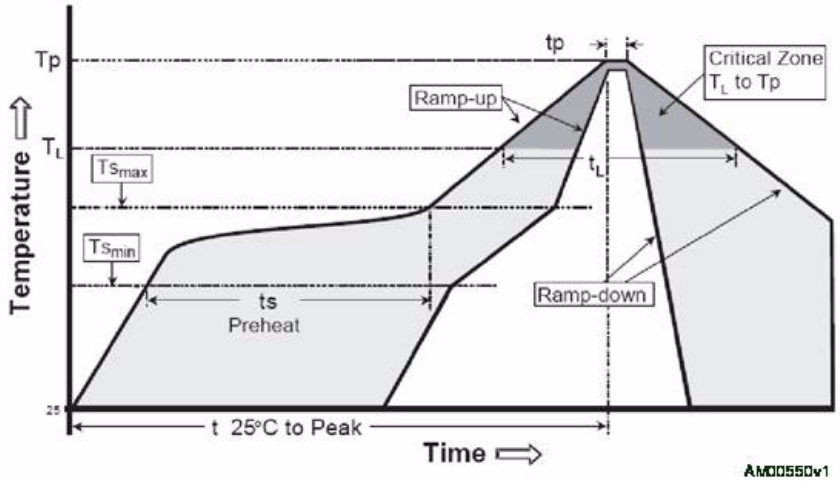
Soldering phase has to be execute with care: in order to avoid undesired melting phenomenon, particular attention has to be take on the set up of the peak temperature.

Here following some suggestions for the temperature profile based on IPC/JEDEC J-STD-020C, July 2004 recommendations.

Table 12. Soldering

Profile feature	PB free assembly
Average ramp up rate (T_{SMAX} to TP)	3 °C / sec max
Preheat Temperature min (T_S min) Temperature max (T_S max) Time (t_S min to t_S max) (t_S)	 150 °C 200 °C 60 – 100 sec
Time maintained above: Temperature T_L Time t_L	 217 °C 40 – 70 sec
Peak temperature (T_p)	240 + 0 °C
Time within 5 °C of actual peak temperature (t_P)	10 – 20 sec
Ramp down rate	6 °C / sec
Time from 25 °C to peak temperature	8 minutes max

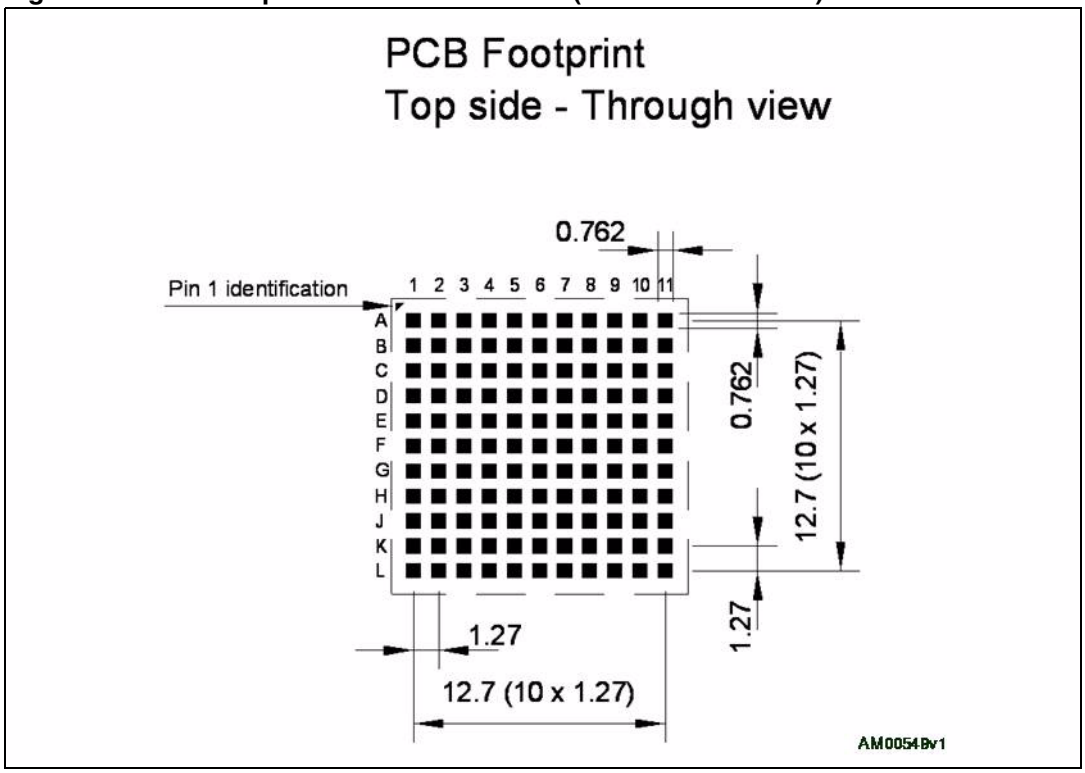
Figure 9. Soldering



6.2 PCB footprint

Use *Figure 10* as suggested PCB footprint.

Figure 10. PCB footprint for SPDC12L00010 (dimensions in mm)



7 Revision history

Table 13. Document revision history

Date	Revision	Changes
17-Oct-2008	1	First release

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