CYPRESS SEMICONDUCTOR

CYM1240

256K x 4 Static RAM Module

Features

- **High-density 1-megabit SRAM module**
- **High-speed CMOS SRAMs**
  - **Access time of 25 ns**
- **Low active power**
  - **2.6W (max.)**
- **SMD technology**
- **TTL-compatible inputs and outputs**
- **Low profile**
  - **Max. height of 0.3 in.**
- **Small PCB footprint**
  - **0.62 sq. in.**

Functional Description

The CYM1240 is a very high performance 1-megabit static RAM module organized as 256K words by 4 bits. The module is constructed using four 256K x 1 static RAMs in leadless chip carriers mounted onto a ceramic substrate with pins. It is socket-compatible with monolithic 256K x 4 SRAMs.
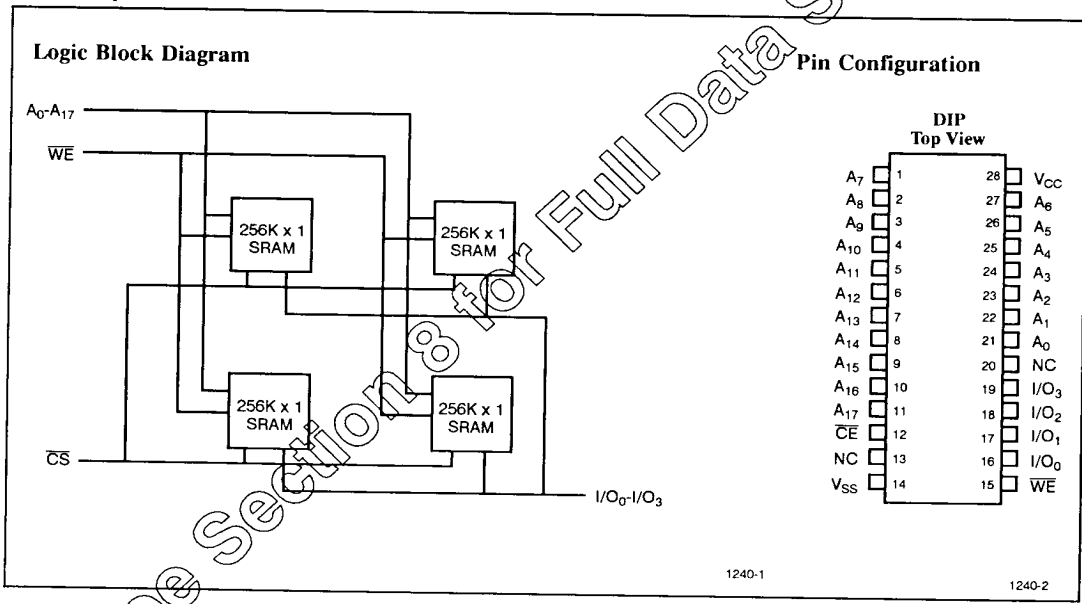
Writing to the memory module is accomplished when the chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the four input/output pins (I/O_0 through I/O_3) of the device is written into the memory location specified on the address pins (A_0 through A_{17}).

Reading the device is accomplished by taking chip select ($\overline{CS}$) LOW while $\overline{WE}$ remains inactive or HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the appropriate data input/output pins.

The data input/output pins remain in a high-impedance state when $\overline{CS}$ is HIGH or $\overline{WE}$ is LOW.

Logic Block Diagram

1240-1

Pin Configuration

DIP Top View

A_7	1	28	V_{CC}
A_8	2	27	A_6
A_9	3	26	A_5
A_{10}	4	25	A_4
A_{11}	5	24	A_3
A_{12}	6	23	A_2
A_{13}	7	22	A_1
A_{14}	8	21	A_0
A_{15}	9	20	NC
A_{16}	10	19	I/O_3
A_{17}	11	18	I/O_2
$\overline{CE}$	12	17	I/O_1
NC	13	16	I/O_0
V_{SS}	14	15	$\overline{WE}$

1240-2

Selection Guide

		1240-25	1240-30	1240-35	1240-45
Maximum Access Time (ns)		25	30	35	45
Maximum Operating Current (mA)	Commercial	480	480	480	480
	Military	480	480	480	480
Maximum Standby Current (mA)	Commercial	160	160	160	160
	Military	160	160	160	160

Shaded area contains preliminary information.