NAND01G-N

1 Gbit (x8/x16) 2112 Byte Page NAND Flash Memory and 512 Mbit (x16) LPSDRAM, 1.8V, Multi-Chip Package

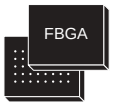
PRELIMINARY DATA

Features summary

- Multi-chip Package
  - NAND Flash Memory
  - 512 Mbit or 1 Gbit (x8/x16) Large Page Size NAND Flash Memory
  - 512 Mbit (x16) SDR or DDR LPSDRAM
- Temperature range
  - -30 up to 85 °C
- Supply voltage
  - NAND Flash : V_{DDF} = 1.7V to 1.95V
  - LPSDRAM: V_{DDD} = V_{DDQD} = 1.7V to 1.9V
- Electronic Signature
- ECOPACK® packages

Flash Memory

- Nand Interface
  - x8 or x16 bus width
  - Multiplexed address/data
- Page size
  - x8 device: (2048 + 64 spare) Bytes
  - x16 device: (1024 + 32 spare) Words
- Block size
  - x8 device: (128K + 4K spare) Bytes
  - x16 device: (64K + 2K spare) Words
- Page Read/Program
  - Random access: 25µs (max)
  - Sequential access: 50ns (min)
  - Page program time: 300µs (typ)
- Copy Back Program mode
  - Fast page copy without external buffering
- Fast Block Erase
  - Block Erase time: 2ms (typ)
- Chip Enable ‘don’t care’
  - for simple interfacing with microcontrollers
- Status Register



TFBGA107 10.5 x 13 x 1.2mm
TFBGA149 10 x 13.5 x 1.2mm

SDR/DDR LPSDRAM

- Interface: x16 bus width
- Programmable Partial Array Self Refresh
- Auto Temperature Compensated Self Refresh
- Deep Power Down mode
- 1.8V LVCMOS interface
- Quad internal Banks controlled by BA0 and BA1
- Wrap sequence: Sequential/Interleaved
- Automatic and Controlled Precharge
- Auto Refresh and Self Refresh
- 8,192 Refresh Cycles/64ms
- Burst Termination by Burst Stop command and Precharge Command

This is preliminary information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

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Table 1. Product List

Reference	Part Number	NAND Product	LPSDRAM Product(1)	Package
NAND01G-N	NAND01GR3N6	1Gbit 1.8V (x8)	SDR 512Mbit (x16) 1.8V, 133MHz	TFBGA107
	NAND01GR4N5	1Gbit 1.8V (x16)	DDR 512Mbit (x16) 1.8V, 133 MHz	TFBGA149

1. SDR = Single Data Rate; DDR = Double Data Rate.

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1 Summary description

The NAND01G-N is a family that combine two memory devices in a Multi-Chip Package: a 1 Gbit NAND Flash memory and 512 Mbit LPSDRAM with 2Kbyte Pages.

The NAND Flash memory and LPSDRAM components have separate power supplies and grounds. They also have separate control, address and input/output signals, which allows simultaneous access to both devices at any moment.

They are distinguished by two Chip Enable inputs: $\overline{E}_F$ for the NAND Flash memory and $\overline{E}_D$ for the LPSDRAM.

The Multi-Chip Packages are available with a 1.8V supply. See *Table 1* for a complete list of the products available.

All devices are stacked and are offered in:

- TFBGA107 (10.5 x 13 x 1.2mm)
- TFBGA149 (10 x 13.5 x 1.2mm)

They are supplied with all the NAND Flash memory bits erased (set to '1').

This datasheet should be read in conjunction with the NAND Flash and LPSDRAM datasheets.

NAND Flash component

NAND01G-N devices contain a 1 Gbit (x8/x16) 2112 Byte/1056 Word Page, NAND Flash Memory. For detailed information on how to use the devices, see the NANDxxx-B datasheet which is available from your local STMicroelectronics distributor.

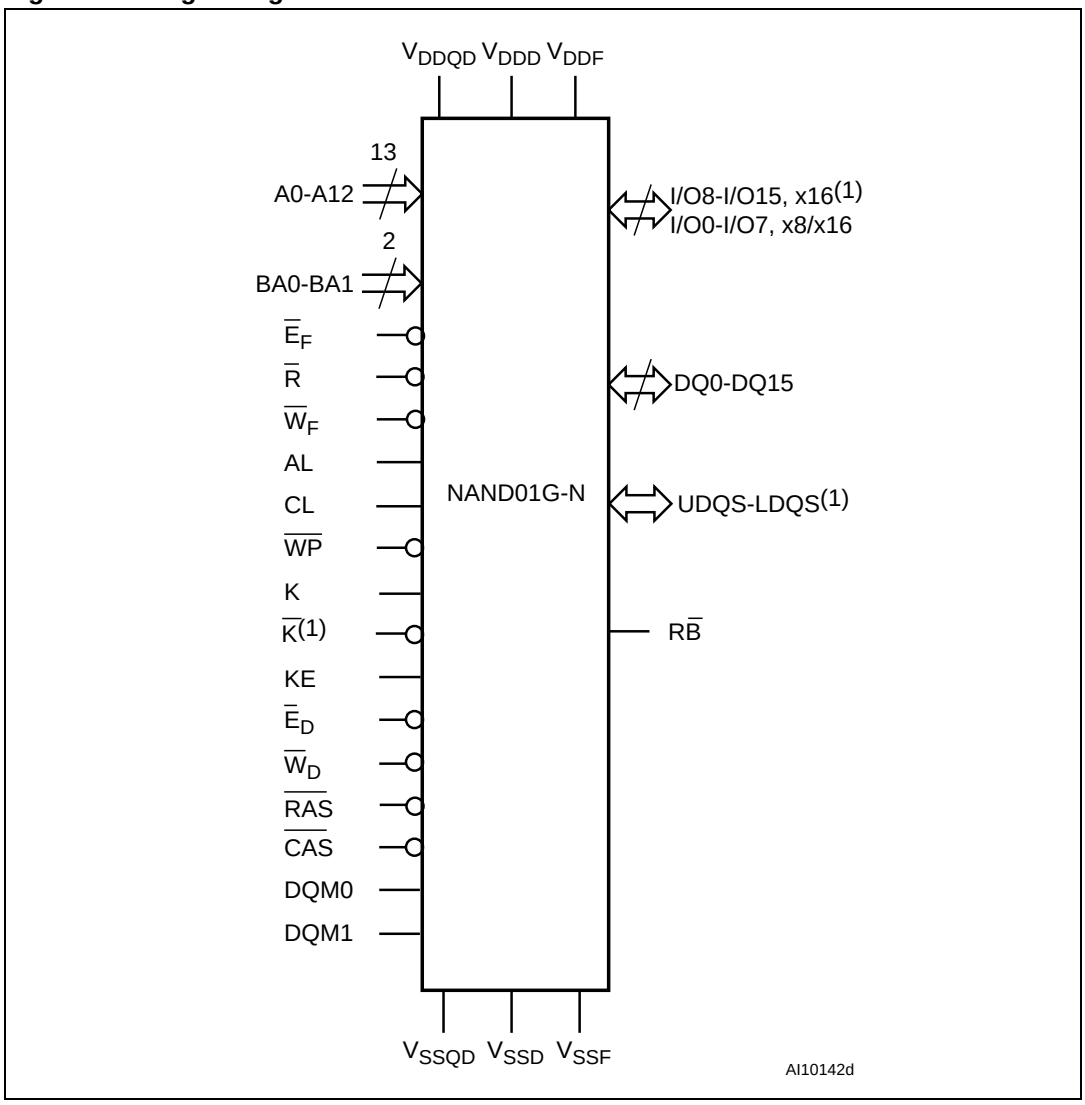
LPSDRAM component

NAND01G-N devices contain a 512 Mbit (x16) LPSDRAM. For detailed information on how to use the devices, see:

- M65KA512AB: SDR 512Mb (x16)
- M65KG512AB: DDR 512Mb (x16)

All above ST datasheets available from ST divisional Marketing.

Figure 1. Logic Diagram



1. Available on NAND01GR4N5 only.

Table 2. Signal Names

NAND Flash memory	
I/O0-I/O7	Data Input/Outputs for x8 and x16 devices
I/O8-I/O15	Data Inputs/Outputs for x16 devices
AL	Address Latch Enable
CL	Command Latch Enable
$\overline{E}_F$	Chip Enable
$\overline{R}$	Read Enable
$R\overline{B}$	Ready/Busy (open-drain output)
$\overline{W}_F$	Write Enable
$\overline{WP}$	Write Protect
V_{DDF}	Supply Voltage
V_{SSF}	Ground
LPSDRAM	
A0-A12	Address Inputs A10 determines the Precharge mode.
BA0-BA1	Bank Select Inputs
DQ0-DQ15	Data Inputs/Outputs
UDQS-LDQS(1)	Data Strobe Inputs/Outputs
K	Clock Input
$\overline{K}$(1)	Clock Input
KE	Clock Enable Input
$\overline{E}_D$	Chip Select inputs
$\overline{W}_D$	Write Enable Input
$\overline{RAS}$	Row Address Strobe Input
$\overline{CAS}$	Column Address Strobe Input
DQM0	DQ Mask Enable Input (controls DQ0-DQ7)
DQM1	DQ Mask Enable Input (controls DQ8-DQ15)
V_{DDD}	Supply Voltage
V_{DDQD}	Input/Output Supply Voltage
V_{SSD}	Ground
V_{SSQD}	Input/Output Ground
NC	Not Connected Internally
DU	Do Not Use

1. Available on NAND01GR4N5 only.

Figure 2. TFBGA107 connections, x16 Bus Width (Top view through package)

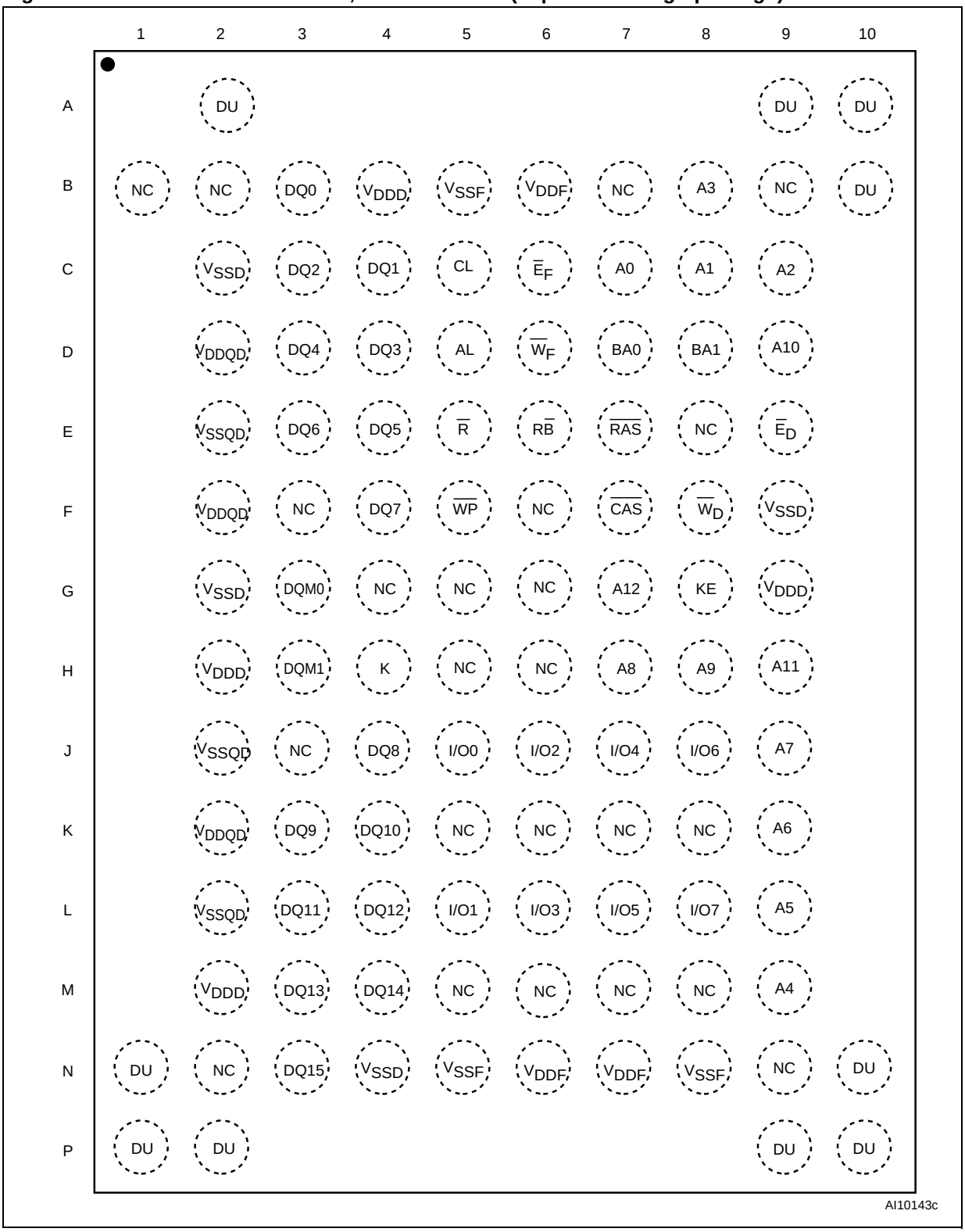
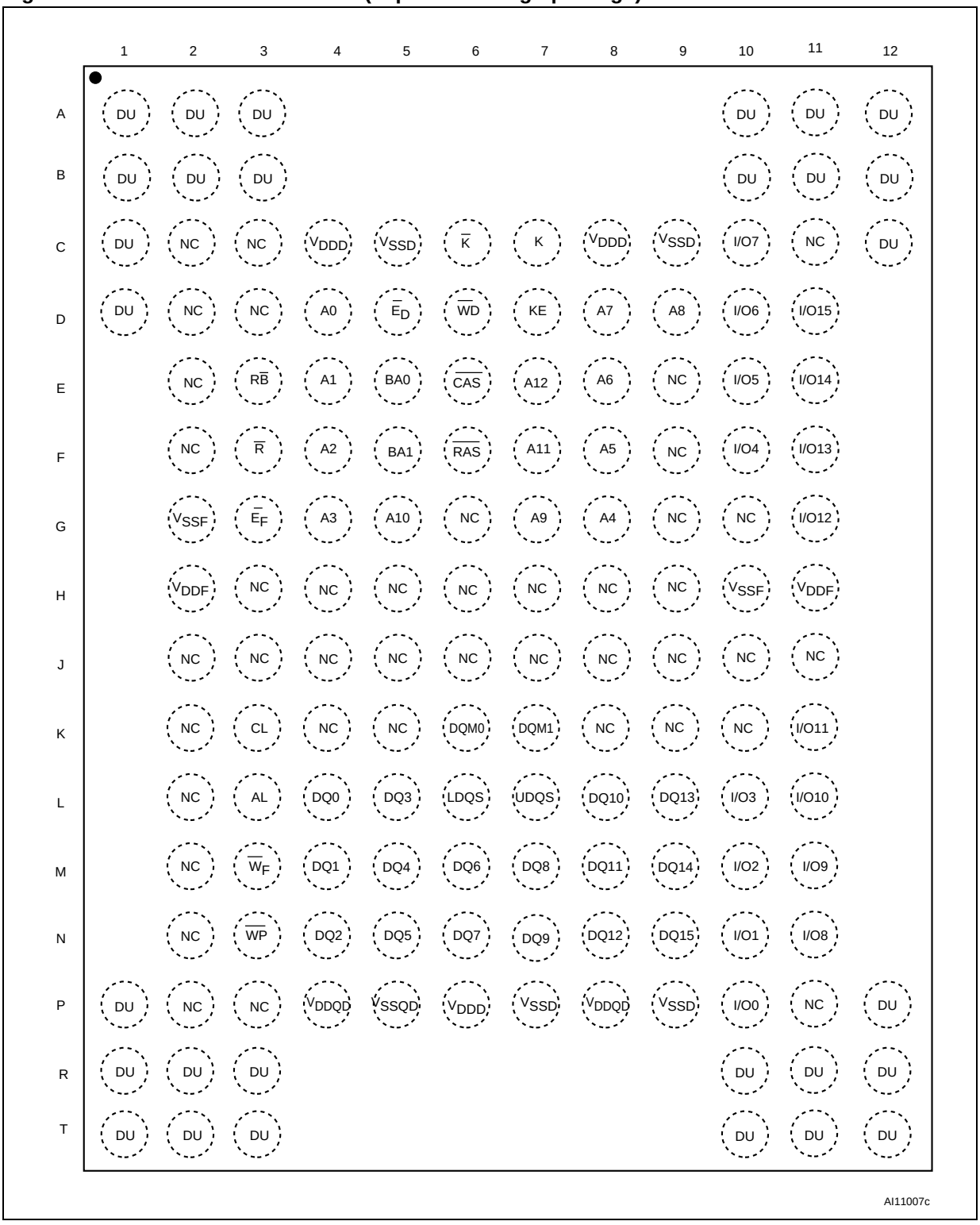


Figure 3. TFBGA149 Connections (Top view through package)



2 Signals description

See *Figure 1* in conjunction with *Table 2*, for a brief overview of the signals connected to this device.

For extra details on the signals, refer to the NAND Flash and the LPSDRAM datasheets.

2.1 Flash memory Inputs/Outputs (I/O0-I/O7)

Input/Outputs 0 to 7 are used by the NAND Flash memory to input the selected address, output the data during a Read operation or input a command or data during a Write operation. The inputs are latched on the rising edge of Write Enable. I/O0-I/O7 are left floating when the NAND Flash memory is deselected or the outputs are disabled.

2.2 Flash memory Inputs/Outputs (I/O8-I/O15)

Input/Outputs 8 to 15 are only available in x16 NAND Flash devices. They are used to output the data during a Read operation or input data during a Write operation. Command and Address Inputs only require I/O0 to I/O7.

The inputs are latched on the rising edge of Write Enable. I/O8-I/O15 are left floating when the device is deselected or the outputs are disabled.

2.3 Flash memory Address Latch Enable (AL)

The Address Latch Enable activates the latching of the Address inputs in the Command Interface of the NAND Flash memory. When AL is high, the inputs are latched on the rising edge of Write Enable.

2.4 Flash memory Command Latch Enable (CL)

The Command Latch Enable activates the latching of the Command inputs in the Command Interface of the NAND Flash memory. When CL is high, the inputs are latched on the rising edge of Write Enable.

2.5 Flash memory Chip Enable ($\overline{E}_F$)

The NAND Flash memory Chip Enable input activates the memory control logic, input buffers, decoders and sense amplifiers. When Chip Enable is low, V_{IL}, the NAND Flash memory device is selected. If Chip Enable goes high, v_{IH}, while the NAND Flash memory is busy, the device remains selected and does not go into standby mode.

2.6 Flash memory Read Enable ($\overline{R}$)

The NAND Flash memory Read Enable pin, $\overline{R}$, controls the sequential data output during Read operations. The falling edge of $\overline{R}$ also increments the internal column address counter by one.

2.7 Flash memory Write Enable ($\overline{W}_F$)

The NAND Flash memory Write Enable input, $\overline{W}$, controls writing to the Command Interface, Input Address and Data latches. Both addresses and data are latched on the rising edge of Write Enable.

2.8 Flash memory Write Protect ($\overline{WP}$)

The Write Protect pin is a NAND Flash memory input that gives a hardware protection against unwanted program or erase operations. When Write Protect is Low, V_{IL}, the NAND Flash memory device does not accept any program or erase operations.

It is recommended to keep the Write Protect pin Low, V_{IL}, during power-up and power-down.

2.9 Flash memory Ready/Busy ($R\overline{B}$)

The Ready/Busy output, $R\overline{B}$, is an open-drain NAND Flash memory output that can be used to identify if the P/E/R Controller is currently active.

When Ready/Busy is Low, V_{OL}, a read, program or erase operation is in progress. When the operation completes Ready/Busy goes High, V_{OH}.

The use of an open-drain output allows the Ready/Busy pins from several memories to be connected to a single pull-up resistor. A Low will then indicate that one, or more, of the memories is busy.

2.10 Flash memory V_{DDF} supply voltage

V_{DDF} provides the power supply to the internal core of the NAND Flash memory device. It is the main power supply for all operations (read, program and erase).

2.11 Flash memory V_{SSF} ground

Ground, V_{SSF}, is the reference for the power supply for the NAND Flash memory. It must be connected to the system ground.

2.12 LPSDRAM Address Inputs (A0-A12)

The A0-A12 Address Inputs are used by the LPSDRAM to select the row or column to be made active. If a row is selected, all thirteen, A0-A12 Address Inputs are used. If a column is selected, only the nine least significant Address Inputs, A0-A8, are used. In this latter case, A10 determines whether Auto Precharge is used. If A10 is High (set to '1') during Read or Write, the Read or Write operation includes an Auto Precharge cycle. If A10 is Low (set to '0') during Read or Write, the Read or Write cycle does not include an Auto Precharge cycle.

2.13 LPSDRAM Bank Select Address Inputs (BA0-BA1)

The BA0 and BA1 Banks Select Address Inputs are used by the LPSDRAM to select the bank to be made active.

The LPSDRAM must be enabled, the Row Address Strobe, $\overline{RAS}$, must be Low, V_{IL}, the Column Address Strobe, $\overline{CAS}$, and $\overline{W}$ must be High, V_{IH}, when selecting the addresses.

2.14 LPSDRAM Data Inputs/Outputs (DQ0-DQ15)

On the LPSDRAM, DQ0-DQ15 output the data stored at the selected address during a Read operation, or are used to input the data during a write operation.

2.15 LPSDRAM Chip Select ($\overline{E}_D$)

The Chip Select input $\overline{E}$ activates the LPSDRAM state machine, address buffers and decoders when driven Low, V_{IL}. When High, V_{IH} the device is not selected.

2.16 LPSDRAM Column Address Strobe ($\overline{CAS}$)

The Column Address Strobe, $\overline{CAS}$, is used in conjunction with Address Inputs A8-A0 and BA1-BA0, to select the starting column location prior to a Read or Write.

2.17 LPSDRAM Row Address Strobe ($\overline{RAS}$)

The Row Address Strobe, $\overline{RAS}$, is used in conjunction with Address Inputs A11-A0 and BA1-BA0, to select the starting address location prior to a Read or Write.

2.18 LPSDRAM Write Enable ($\overline{W}_D$)

The LPSDRAM Write Enable input, $\overline{W}$, controls writing to the LPSDRAM.

2.19 LPSDRAM Clock Input (K)

The Clock signal, K, is used to clock the Read and Write cycles on the LPSDRAM. During normal operation, the Clock Enable pin, KE, is High, V_{IH}. The clock signal K can be suspended to switch the device to the Self-Refresh, Power-Down or Deep Power-Down mode by driving KE Low, V_{IL}.

2.20 LPSDRAM Clock Input ($\overline{K}$)

The Clock signal, $\overline{K}$, is only available on the DDR LPSDRAM. It is used in conjunction with the Clock signal, K.

All LPSDRAM input signals except DQM0/DQM1, UDQS/LDQS and DQ0-DQ15 are referred to the cross point of K rising edge and $\overline{K}$ falling edge.

2.21 LPSDRAM Clock Enable (KE)

The Clock Enable, KE, pin is used by the LPSDRAM to control the synchronizing of the signals with Clock signal K (and $\overline{K}$ on DDR LPSDRAM). If KE is High, V_{IH}, the next Clock rising edge is valid. When KE is Low, V_{IL}, the signals are no longer clocked and data Read and Write cycles are extended. KE is also involved in switching the device to the Self-Refresh, Power-Down and Deep Power-Down modes.

2.22 LPSDRAM Lower/Upper Data Input/Output Mask (DQM0, DQM1)

Data Mask Enable Inputs are used to mask the Read or Write data.

2.23 Lower/Upper Data Read/Write Strobe Input/Output (LDQS, UDQS)

LDQS and UDQS are only available on the DDR LPSDRAM. They can be either input or output signals and act as write data strobe and read data strobe respectively. LDQS and UDQS are the strobe signals for DQ0 to DQ7 and DQ8 to DQ15, respectively.

2.24 LPSDRAM V_{DDD} supply voltage

V_{DDD} provides the power supply to the internal core of the LPSDRAM. It is the main power supply for all operations (Read and Write).

2.25 LPSDRAM V_{DDQD} supply voltage

V_{DDQD} provides the power supply to the I/O pins of the LPSDRAM and enables all Outputs to be powered independently of V_{DDD}. V_{DDQD} can be tied to V_{DDD} or can use a separate supply.

It is recommended to power-up and power-down V_{DDD} and V_{DDQD} together to avoid certain conditions that would result in data corruption.

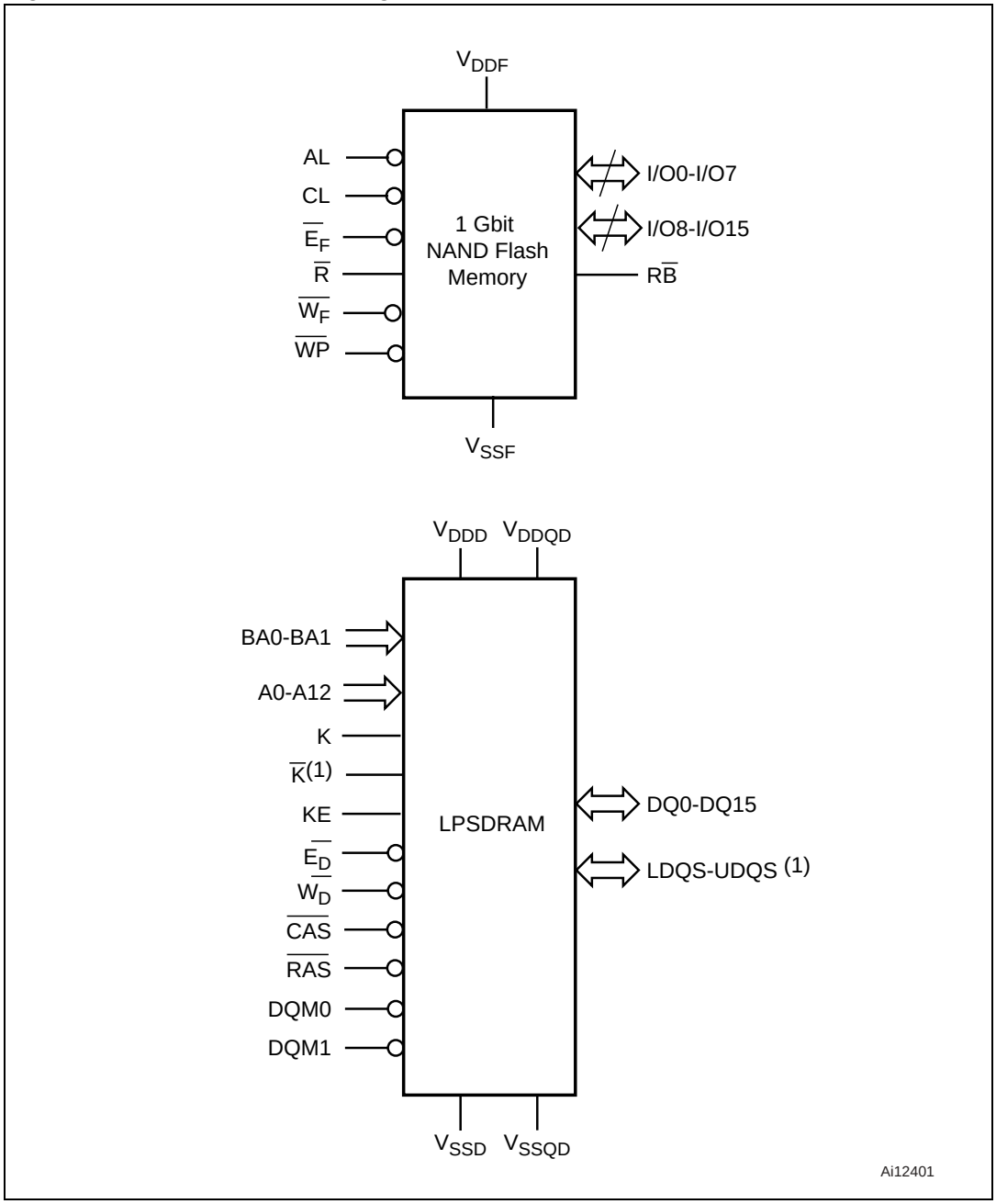
2.26 LPSDRAM V_{SSD} ground

Ground, $V_{SSD,}$ is the reference for the core power supply for the LPSDRAM. It must be connected to the system ground.

3 Functional description

The NAND Flash memory and LPSDRAM components have separate power supplies and grounds. They also have separate control signals, addresses and data input/outputs, which allows simultaneous access to both devices at any moment.

Figure 4. Functional Block Diagram



1. Available on Root Part Number 2 only.

4 Maximum rating

Stressing the device above the rating listed in the Absolute Maximum Ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 3. Absolute Maximum Ratings

Symbol	Parameter		Value		Unit
			Min	Max	
T_A	Ambient Operating Temperature		-30	85	°C
T_{BIAS}	Temperature Under Bias(1)		TBD	TBD	°C
T_{STG}	Storage Temperature		-55	125	°C
V_{IO}	NAND Flash Input or Output Voltage	1.8V	-0.6	2.7	V
	LPSDRAM Input or Output Voltage	1.8V	-1.0	2.6	V
V_{DDF}	NAND Flash Supply Voltage	1.8V	-0.6	2.7	V
V_{DDD}, V_{DDQD}	LPSDRAM Supply Voltage	1.8V	-1.0	2.6	V
LPSDRAM Short Circuit Output Current	I_{OS}		50		mA
LPSDRAM Power Dissipation	PD		1		W

1. TBD stands for ‘To Be Determined’.

5 Package mechanical

Figure 5. TFBGA107 10.5x13mm - 10x14 active ball array, 0.80mm pitch, package outline

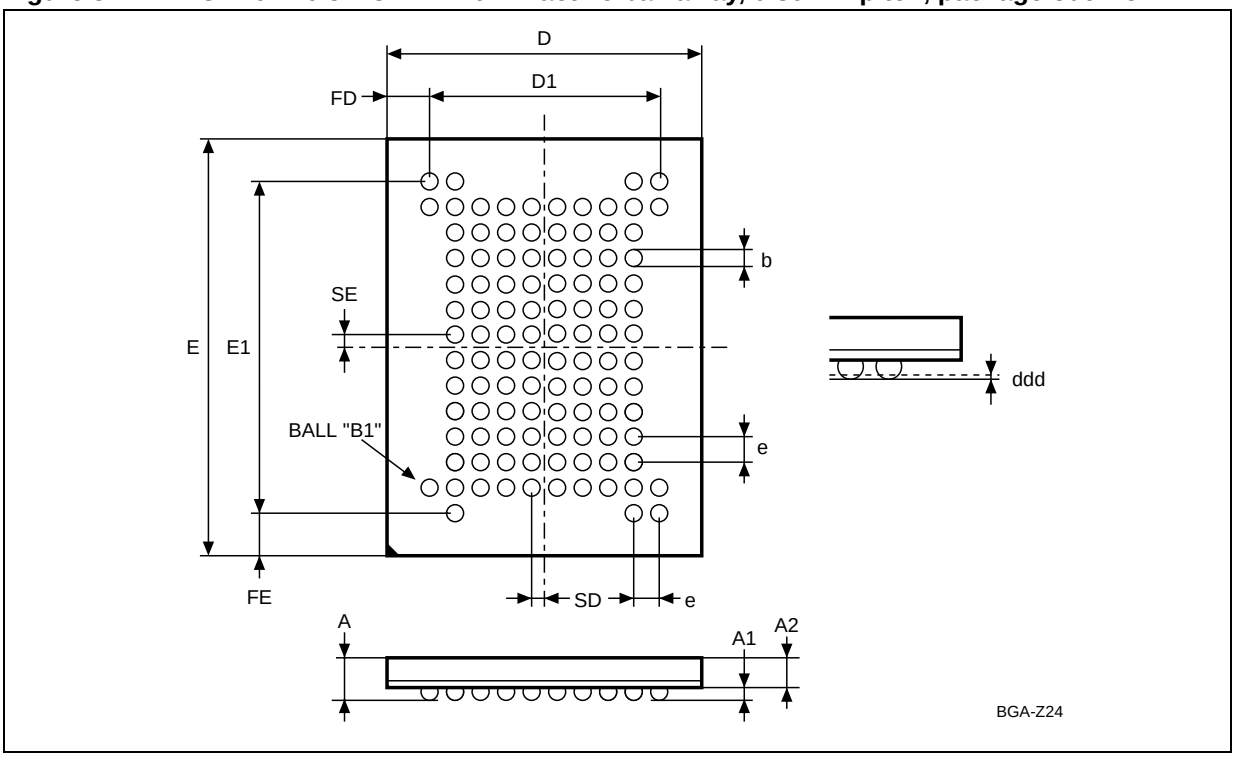
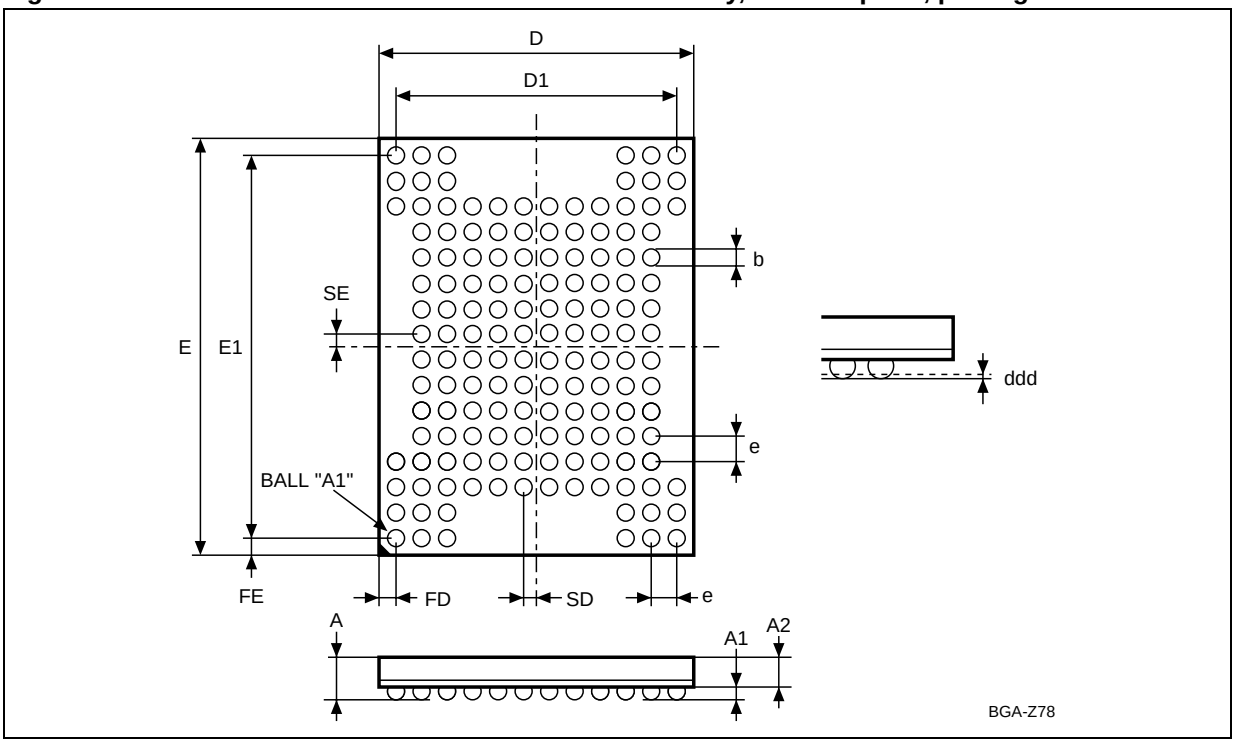


Table 4. TFBGA107 10.5x13mm - 10x14 active ball array, 0.80mm pitch, mechanical data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.047
A1		0.25			0.010	
A2	0.80			0.031		
b	0.45	0.40	0.50	0.018	0.016	0.020
D	10.50	10.40	10.60	0.413	0.409	0.417
D1	7.20			0.283		
ddd			0.10			0.004
E	13.00	12.90	13.10	0.512	0.508	0.516
E1	10.40			0.409		
e	0.80	–	–	0.031	–	–
FD	1.65			0.065		
FE	1.30			0.051		
SD	0.40			0.016		
SE	0.40			0.016		

Figure 6. TFBGA149 10x13.5mm - 12x16 active ball array, 0.80mm pitch, package outline



1. Drawing not to scale.

Table 5. TFBGA149 10x13.5mm - 12x16 active ball array, 0.80mm pitch, mechanical data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.200			0.0472
A1		0.250			0.0098	
A2	0.800			0.0315		
b	0.450	0.400	0.500	0.0177	0.0157	0.0197
D	10.000	9.900	10.100	0.3937	0.3898	0.3976
D1	8.800			0.3465		
ddd			0.100			0.0039
E	13.500	13.400	13.600	0.5315	0.5276	0.5354
E1	12.000			0.4724		
e	0.800	–	–	0.0315	–	–
FD	0.600			0.0236		
FE	0.750			0.0295		
SD	0.400	–	–	0.0157	–	–
SE	0.400	–	–	0.0157	–	–

6 Part numbering

Table 6. Ordering Information Scheme

Example: NAND01G R 3 N 6 A ZB 5 E

Device Type

NAND Flash Memory

NAND Flash Density

01G = 1Gb

NAND Flash Operating Voltage

R = 1.7V to 1.95V

Bus Width

3 = x8

4 = x16

Family Identifier

N = 2112 Byte Page NAND Flash + LPSDRAM

Device Options

5 = DDR LPSDRAM 512Mbit (x16), 133 Mhz, BGA149

6 = SDR LPSDRAM 512Mbit (x 16), 133Mhz, BGA107

Product Version

A

Package

ZB = TFBGA

ZC = LFBGA

Reserved

Option

E = ECOPACK Package, Standard Packing

F = ECOPACK Package, Tape & Reel Packing

Devices are shipped from the factory with the Flash memory content bits, in valid blocks, erased to '1'. For further information on any aspect of this device, please contact your nearest ST Sales Office.

7 Revision history

Table 7. Document Revision History

Date	Version	Revision Details
18-Oct-2004	0.1	First Issue
19-Oct-2004	0.2	*Figure 1: Logic Diagram* modified. *Table 1: Product List* modified.
26-Oct-2005	0.3	NAND512-N device removed from the document.TFBGA137 packages removed from document. SDR 256Mb (x32) and SDR 512Mb (x32) devices removed from document. NAND01GR3N3 removed throughout document. LDQM and UDQM replaced respectively by DQM0 and DQM1throughout document. DRAM changed to LPSDRAM throughout document. LFBGA107 added throughout document. NAND01GR3N1, NAND01GR3N2, NAND01GR3N6, NAND01GR4N5 added throughout document.
31-Jan-2006	1.0	Note 1 below *Table 2: Signal Names* and *Figure 1: Logic Diagram* added to cover both part numbers. *Figure 2: TFBGA107 connections, x16 Bus Width (Top view through package)* and *Figure 3: TFBGA149 Connections (Top view through package)* updated. *Section 2: Signals description* and *Section 3: Functional description* added. 256Mb LPSDRAM removed. LFBGA107 (12 x 13 x 1.4mm) and LFBGA149 (10 x 13.5 x 1.4mm) replaced by TFBGA107 (10.5x13x1.2mm) and TFBGA149 (10x13.5x1.2mm), respectively.

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