*Product Specification*

# *AHA G.709-2.5 FEC Decoder Core*

PSFECDecoderCore_0702

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# 1.0 INTRODUCTION

This G709D-2.5 core is specifically designed to efficiently perform the Reed-Solomon decoding function specified by the ITU G.709 standard. The core requires no configuration, no initialization, and no re-synchronization procedure or includes any unnecessary features that would add area, power, or complexity to your design.

## 1.1 FEATURES

***PERFORMANCE:***

- 2.5 Gbits/sec operation in .13 micron CMOS process
- 40 K gates in .13 micron using a typical standard cell library
- 332 Mhz clock at 2.5 Gbits/sec
- 8 bit input and output data interfaces
- Complete error reporting for Bit Error Rate calculation and feedback into threshold detection circuits

***FLEXIBILITY:***

- One-edge, one-clock fully synchronous design without multi-cycle paths
- Supports both streaming of data and gaps between blocks
- Separate FIFO for increased flexibility and simplified IC floor planning
- 319 clock latency through the core (1 block + 64 clocks)

***DELIVERABLES:***

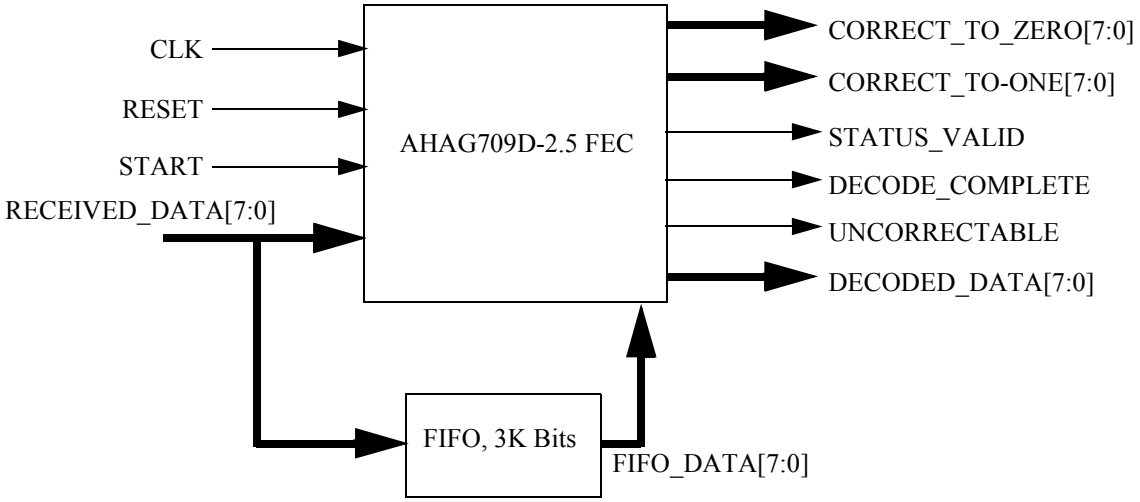
- G.709D-2.5 FEC core (VHDL)
- Timing constraints (DesignCompiler and Ambit format)
- Test bench and verification vectors (VHDL)
- Single use license of AHA's Reed-Solomon Patents

***PATENTS:***

- Design uses one or more of the following US Patents: 5,170,399; 5,099,482; 4,873,688; 5,396,502

# 2.0 FUNCTIONAL DESCRIPTION

**Figure 1: BLOCK DIAGRAM:**




## 2.1 DECODING

The core implements a G.709D Reed-Solomon code (255,239) decoder. This code is capable of correcting up to 8 (t = 8) byte-errors in a 255-byte block. The core has two phases of operation, a Data Input phase and a Data Correct phase. During the Data Input phase the block data is read one byte at a time. The data coming in on this phase is not stored internal to the core, but is stored in the external FIFO. This phase takes 255 clocks. The Data Correct phase requires 64 clocks after the last byte of the block is read to begin to output the corrected data. The original data is read from the FIFO, corrected and output.

The first byte of a block is received with a start signal. FIFO data is required to start arriving 317 clocks later. The block is output when the data valid signal is asserted. decode_complete will assert with the first transfer. Two clocks after the block is output the status valid signal asserts indicating that the correction count signals and the uncorrectable signal are valid.

## 2.2 REED SOLOMON CODE PARAMETERS

Generator polynomial:

$$G(z) = \prod_{i=0}^{15} (z - \alpha^i)$$

Where $\alpha$ is a root of the binary primitive polynomial $x^8 + x^4 + x^3 + x^2 + 1$.

Parity bytes are represented by:

$$R(z) = R_{15} \cdot z_{15} + R_{14} \cdot z_{14} \ldots + R_1 \cdot z_1 + R_0$$

Where $R_j$ (j = 0 to 15) is the parity byte represented by an element out of GF(256) and $R_{15}$ corresponds to the byte 240 in the FEC sub-row and $R_0$ to byte 255.

# 3.0 SIGNAL DESCRIPTIONS

## 3.1 INPUT INTERFACE

| *Signal* | *Type* | *Description* |
|---|---|---|
| CLK | I | System Clock. 332 MHz core clock. All inputs are registered on the rising edge. |
| RESET | I | System Hard Reset. Assertion of this signal will cause loss of all data currently in the core. RESET must remain active for 3 clocks. |
| RECEIVED_DATA[7:0] | I | Data input. Data is registered on the rising edge of CLK every clk. A block is received one byte at a time. |
| START | I | Block start signal. This signal is asserted with the first transfer of a block. Start signals should be at least 255 clocks apart, but can be more then 255 clocks apart. This signal should be deasserted during all other clocks. |
| FIFO_DATA[7:0] | I | FIFO data. Delayed version of the received_data data stream. This signal is delayed 317 clocks. |

## 3.2 OUTPUT INTERFACE

| *Signal* | *Type* | *Description* |
|---|---|---|
| DECODE_COMPLETE | O | Decoding complete. Active when the first byte of the G.709 frame is on the DECODE_DATA data bus and is inactive on all subsequent transfers. |
| DECODED_DATA[7:0] | O | Decoded data. A block is transferred out one byte at a time. The first byte is available when DECODE_COMPLETE is asserted. |
| STATUS_VALID | O | Status valid signal. Active for a single CLK two CLKs following the completion of the frame to indicate when the UNCORRECTABLE, CORRECT_TO_ZERO and CORRECT_TO_ONE signals are valid |
| UNCORRECTABLE | O | Uncorrectable block flag. Valid when STATUS_VALID is asserted. When asserted the block is not correctable. |
| CORRECT_TO_ZERO[7:0] | O | Number of bits corrected from '1' to '0' in the block. Valid when STATUS_VALID is asserted. |
| CORRECT_TO_ZERO[7:0] | O | Number of bits corrected from '0' to '1' in the block. Valid when STATUS_VALID is asserted. |

# 4.0 TIMING DIAGRAMS

**Figure 2: Input Interface Timing**

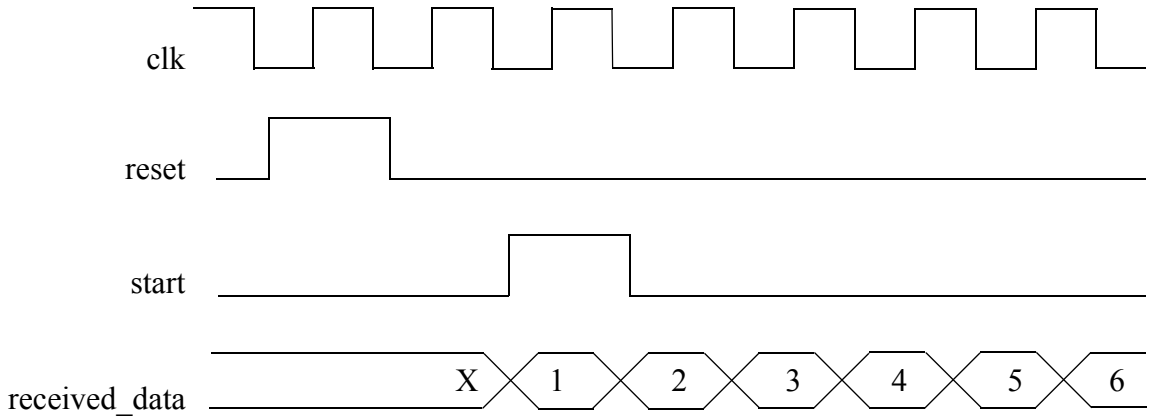


**Figure 3: Output Interface Timing, Start of output transfer**

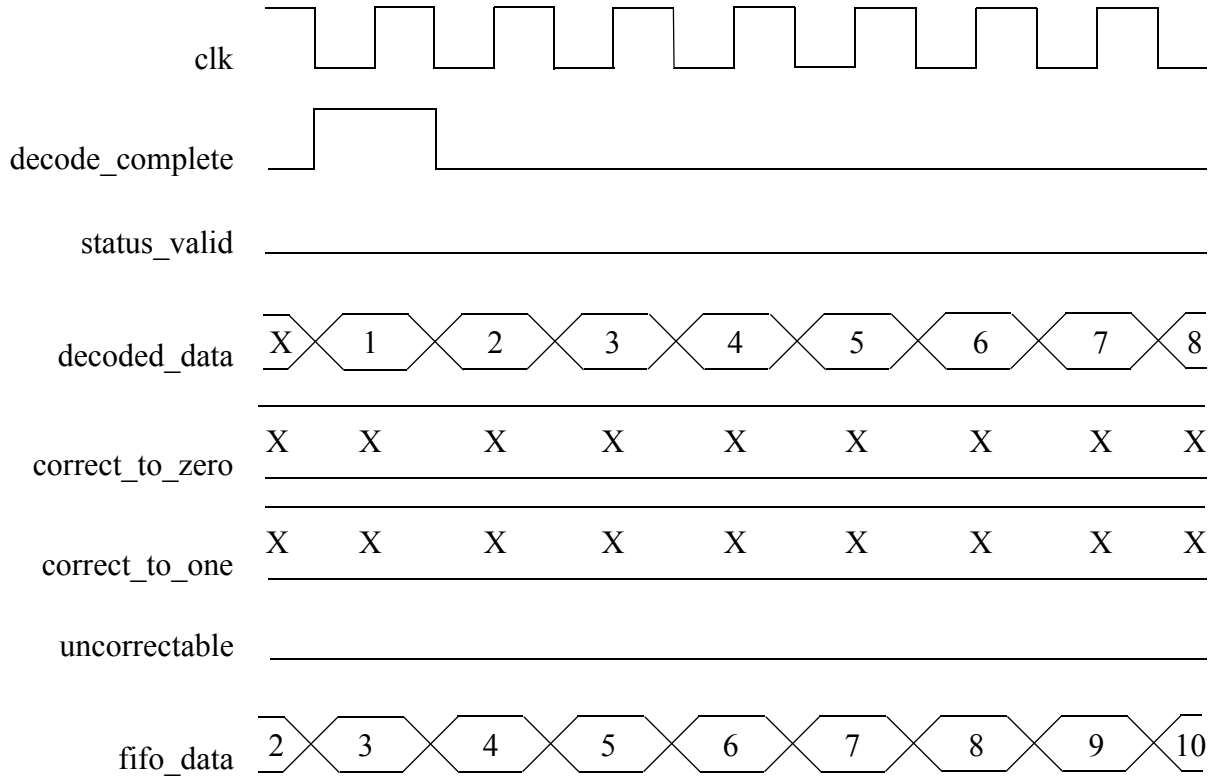



**Figure 4: Output Interface Timing, End of output transfer**