

# BUK7L06-34ARC

## N-channel TrenchPLUS standard level FET

Rev. 05 — 17 February 2009

Product data sheet

## 1. Product profile

### 1.1 General description

Standard level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. The devices include internal gate resistors and TrenchPLUS diodes for clamping and ElectroStatic Discharge (ESD) protection. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

### 1.2 Features and benefits

- Low conduction losses due to low on-state resistance
- Q101 compliant
- Reduced component count due to integrated gate resistor

### 1.3 Applications

- 12 V loads
- Automotive systems
- General purpose power switching
- Motors, lamps and solenoids

### 1.4 Quick reference data

Table 1. Quick reference

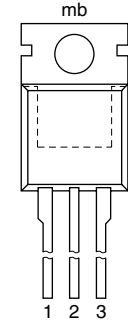
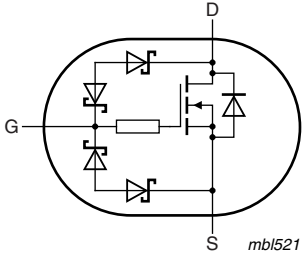
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_D$	drain current	$V_{GS} = 10\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 1</a> ; see <a href="#">Figure 3</a>	[1]	-	-	147 A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 2</a>	[2]	-	-	250 W
<b>Static characteristics</b>						
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$ ; $I_D = 30\text{ A}$ ; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 13</a> ; see <a href="#">Figure 14</a>	-	5.1	6	mΩ

[1] Current is limited by power dissipation chip rating.

[2] Refer to document 9397 750 12572 for further information.

## 2. Pinning information

**Table 2. Pinning information**

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p><b>SOT78C (TO-220AB)</b></p>	 <p><i>mb1521</i></p>
2	D	drain		
3	S	source		
mb	D	mounting base; connected to drain		

## 3. Ordering information

**Table 3. Ordering information**

Type number	Package		Version
	Name	Description	
BUK7L06-34ARC	TO-220AB	plastic single-ended package; heatsink mounted; 1 mounting hole; 3-leads	SOT78C

## 4. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

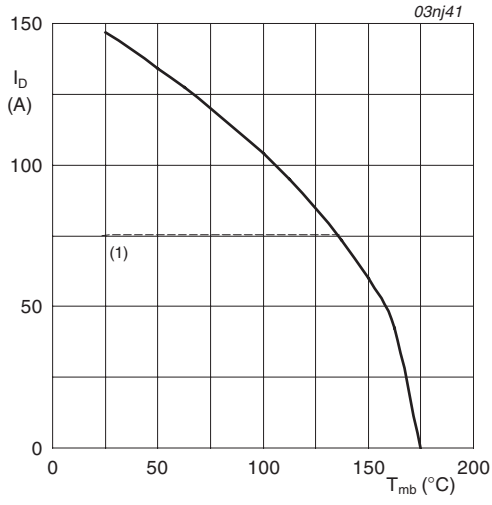
Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 175\text{ °C}$	[1]	-	34 V
$V_{DGR}$	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	[1]	-	34 V
$V_{GS}$	gate-source voltage		-20	20	V
$I_D$	drain current	$T_{mb} = 25\text{ °C}$ ; $V_{GS} = 10\text{ V}$ ; see <a href="#">Figure 1</a> ; see <a href="#">Figure 3</a>	[2][3]	-	147 A
		$T_{mb} = 100\text{ °C}$ ; $V_{GS} = 10\text{ V}$ ; see <a href="#">Figure 1</a>	[4]	-	75 A
		$T_{mb} = 25\text{ °C}$ ; $V_{GS} = 10\text{ V}$ ; see <a href="#">Figure 1</a> ; see <a href="#">Figure 3</a>	[4]	-	75 A
$I_{DM}$	peak drain current	$T_{mb} = 25\text{ °C}$ ; $t_p \leq 10\text{ }\mu\text{s}$ ; pulsed; see <a href="#">Figure 3</a>	-	590	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 2</a>	-	250	W
$I_{DG(CL)}$	drain-gate clamping current	pulsed; $t_p = 5\text{ ms}$ ; $\delta = 0.01$	-	50	mA
$I_{GS(CL)}$	gate-source clamping current	continuous	-	10	mA
		pulsed; $t_p = 5\text{ ms}$ ; $\delta = 0.01$	-	50	mA
$T_{stg}$	storage temperature		-55	175	°C
$T_j$	junction temperature		-55	175	°C
<b>Source-drain diode</b>					
$I_S$	source current	$T_{mb} = 25\text{ °C}$	[2][3]	-	147 A
			[4]	-	75 A
$I_{SM}$	peak source current	$t_p \leq 10\text{ }\mu\text{s}$ ; pulsed; $T_{mb} = 25\text{ °C}$	-	590	A
<b>Avalanche ruggedness</b>					
$E_{DS(CL)S}$	non-repetitive drain-source clamping energy	$I_D = 75\text{ A}$ ; $V_{DS} \leq 34\text{ V}$ ; $V_{GS} = 10\text{ V}$ ; $R_{GS} = 50\text{ }\Omega$ ; unclamped; $T_{j(\text{init})} = 25\text{ °C}$	-	1	J
<b>Electrostatic discharge</b>					
$V_{esd}$	electrostatic discharge voltage	HBM; $C = 250\text{ pF}$ ; $R = 1.5\text{ k}\Omega$	-	8	kV
		HBM; $C = 100\text{ pF}$ ; $R = 1.5\text{ k}\Omega$	-	8	kV

[1] Voltage is limited by clamping.

[2] Current is limited by power dissipation chip rating.

[3] Refer to document 9397 750 12572 for further information.

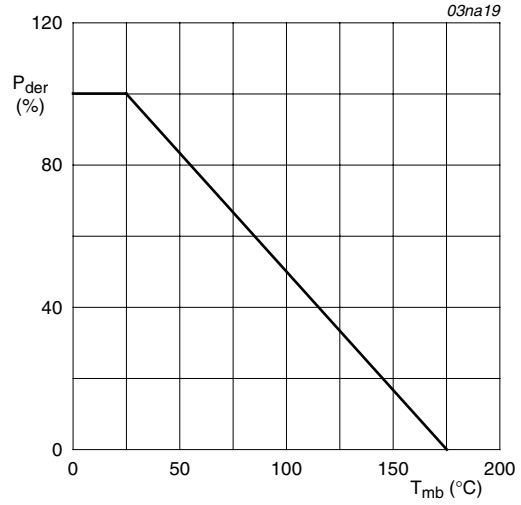
[4] Continuous current is limited by package.



$$V_{GS} \geq 10V$$

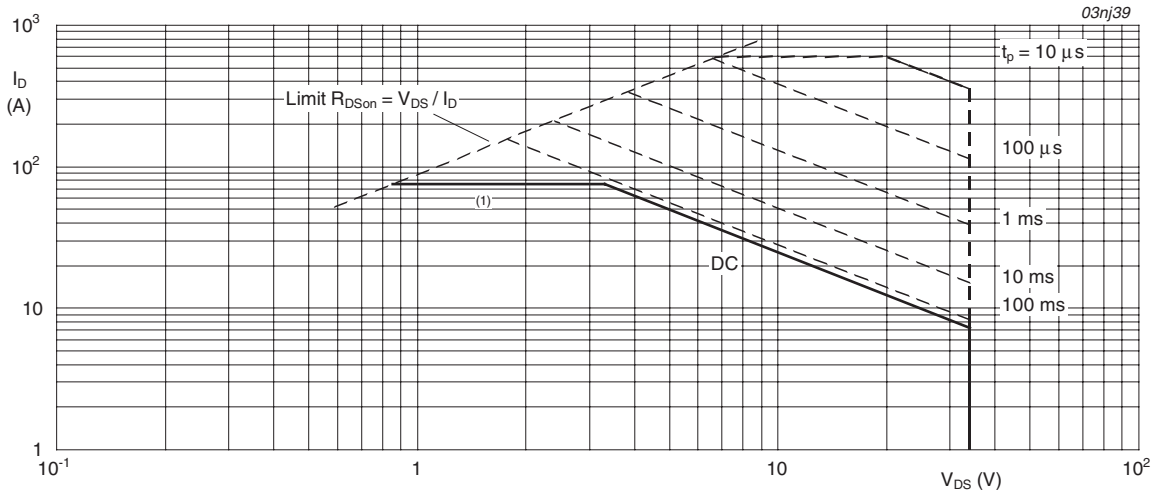
**(1) Capped at 75 A due to package.**

**Fig 1. Normalized continuous drain current as a function of mounting base temperature**



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ C)}} \times 100\%$$

**Fig 2. Normalized total power dissipation as a function of mounting base temperature**



$$T_{mb} = 25^\circ C; I_{DM} \text{ is single pulse}$$

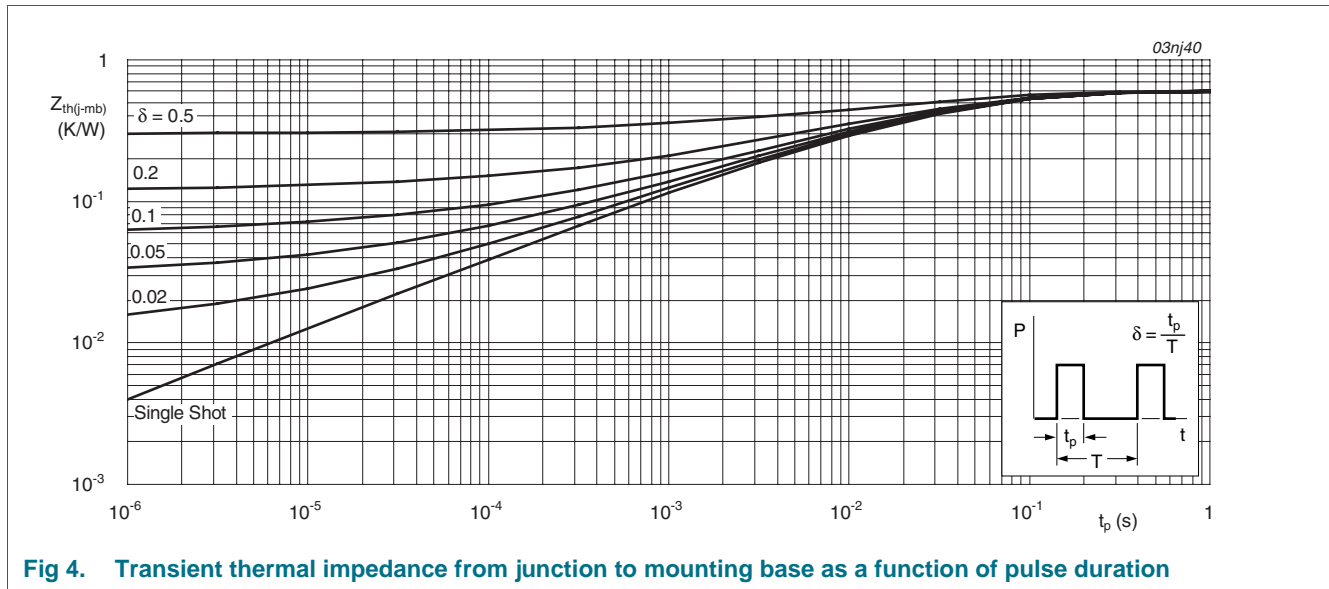
**(1) Capped at 75 A due to package.**

**Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage**

## 5. Thermal characteristics

**Table 5. Thermal characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	vertical in free air	-	60	-	K/W
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see <a href="#">Figure 4</a>	-	0.33	0.6	K/W



**Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration**

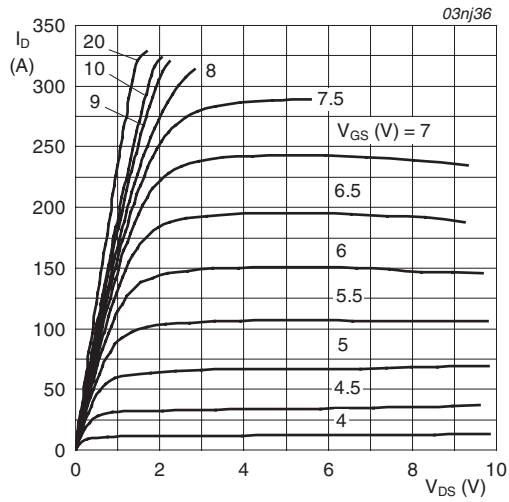
## 6. Characteristics

**Table 6. Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DG}$	drain-gate (Zener diode) breakdown voltage	$I_D = 2 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	34	-	45	V
		$I_D = 2 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$	34	-	45	V
$V_{DS(CL)}$	drain-source clamping voltage	$I_{GS(CL)} = -2 \text{ mA}; I_D = 1 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 10</a> ; see <a href="#">Figure 18</a>	-	41	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 11</a> ; see <a href="#">Figure 12</a>	2.2	3	3.8	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 150 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 11</a> ; see <a href="#">Figure 12</a>	1.5	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 11</a> ; see <a href="#">Figure 12</a>	1.2	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 11</a> ; see <a href="#">Figure 12</a>	-	-	4.2	V
$I_{DSS}$	drain leakage current	$V_{DS} = 16 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.1	2	$\mu\text{A}$
		$V_{DS} = 16 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 150 \text{ }^\circ\text{C}$	-	5	50	$\mu\text{A}$
		$V_{DS} = 16 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ\text{C}$	-	30	250	$\mu\text{A}$
$V_{(BR)GSS}$	gate-source breakdown voltage	$I_G = 1 \text{ mA}; V_{DS} = 0 \text{ V}; T_j > -55 \text{ }^\circ\text{C}; T_j < 175 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 18</a> ; see <a href="#">Figure 19</a>	20	22	-	V
		$I_G = -1 \text{ mA}; V_{DS} = 0 \text{ V}; T_j > -55 \text{ }^\circ\text{C}; T_j < 175 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 18</a> ; see <a href="#">Figure 19</a>	20	22	-	V
$I_{GSS}$	gate leakage current	$V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	5	1000	nA
		$V_{DS} = 0 \text{ V}; V_{GS} = -10 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	5	1000	nA
		$V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V}; T_j = 175 \text{ }^\circ\text{C}$	-	-	50	$\mu\text{A}$
		$V_{DS} = 0 \text{ V}; V_{GS} = -10 \text{ V}; T_j = 175 \text{ }^\circ\text{C}$	-	-	50	$\mu\text{A}$
		$V_{DS} = 0 \text{ V}; V_{GS} = 16 \text{ V}; T_j = 175 \text{ }^\circ\text{C}$	-	-	150	$\mu\text{A}$
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 30 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 13</a> ; see <a href="#">Figure 14</a>	-	5.1	6	m $\Omega$
		$V_{GS} = 10 \text{ V}; I_D = 30 \text{ A}; T_j = 175 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 13</a> ; see <a href="#">Figure 14</a>	-	-	11.4	m $\Omega$
		$V_{GS} = 16 \text{ V}; I_D = 30 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	-	4	5.3	m $\Omega$
$R_G$	internal gate resistance (AC)	$f = 1 \text{ MHz}$	-	11	-	$\Omega$
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 25 \text{ A}; V_{DS} = 27 \text{ V}; V_{GS} = 10 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 16</a>	-	82	-	nC
$Q_{GS}$	gate-source charge		-	15	-	nC
$Q_{GD}$	gate-drain charge		-	31	-	nC
$C_{iss}$	input capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 17</a>	-	3400	4533	pF
$C_{oss}$	output capacitance		-	1080	1296	pF
$C_{rss}$	reverse transfer capacitance		-	660	904	pF

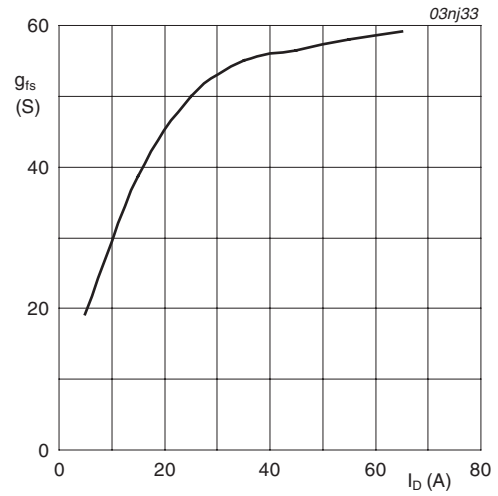
Table 6. Characteristics ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{d(on)}$	turn-on delay time	$V_{DS} = 30\text{ V}; R_L = 1.2\ \Omega; V_{GS} = 10\text{ V};$	-	27	-	ns
$t_r$	rise time	$R_{G(ext)} = 10\ \Omega; T_j = 25\text{ }^\circ\text{C}$	-	108	-	ns
$t_{d(off)}$	turn-off delay time		-	196	-	ns
$t_f$	fall time		-	167	-	ns
$L_D$	internal drain inductance	from drain lead 6 mm from package to center of die; $T_j = 25\text{ }^\circ\text{C}$	-	4.5	-	nH
		from contact screw on mounting base to center of die; $T_j = 25\text{ }^\circ\text{C}$	-	3.5	-	nH
$L_S$	internal source inductance	from source lead to source bond pad; $T_j = 25\text{ }^\circ\text{C}$	-	7.5	-	nH
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 25\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C};$ see <a href="#">Figure 15</a>	-	0.85	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 20\text{ A}; dI_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V};$	-	62	-	ns
$Q_r$	recovered charge	$V_{DS} = 30\text{ V}; T_j = 25\text{ }^\circ\text{C}$	-	44	-	nC



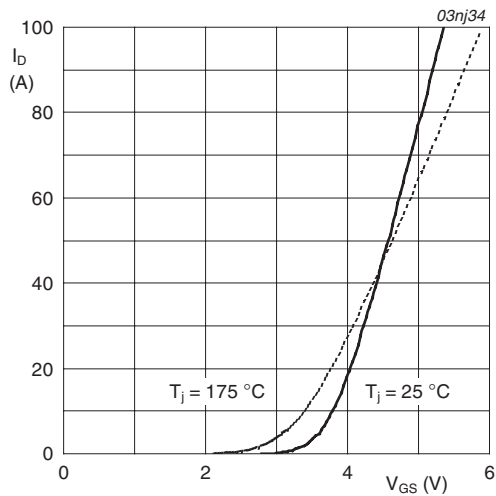
$T_j = 25^\circ\text{C}; t_p = 300\mu\text{s}$

**Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values**



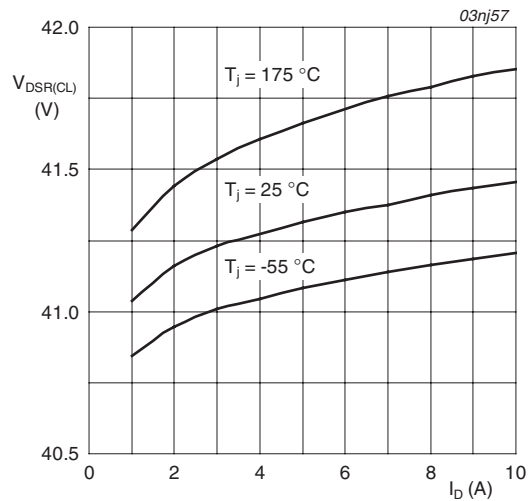
$T_j = 25^\circ\text{C}; V_{DS} = 25\text{V}$

**Fig 6. Forward transconductance as a function of drain current; typical values**



$V_{DS} = 25\text{V}$

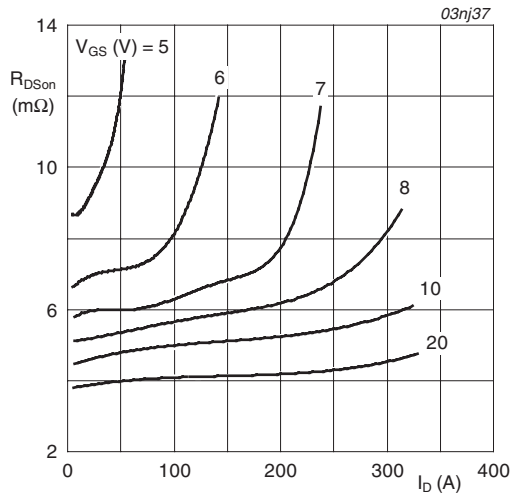
**Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values**



$I_G = -2\text{mA}$

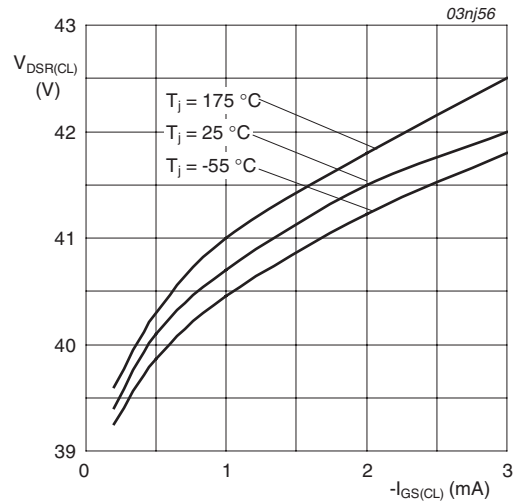
**Fig 8. Drain-source clamping voltage as a function of drain current; typical values**





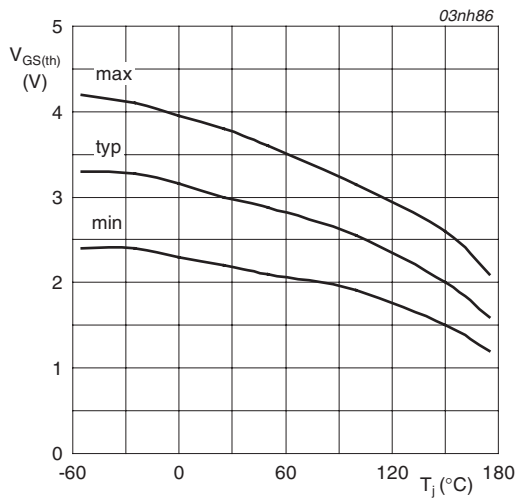
$T_j = 25^\circ\text{C}; t_p = 300\mu\text{s}$

**Fig 9. Drain-source on-state resistance as a function of drain current; typical values**



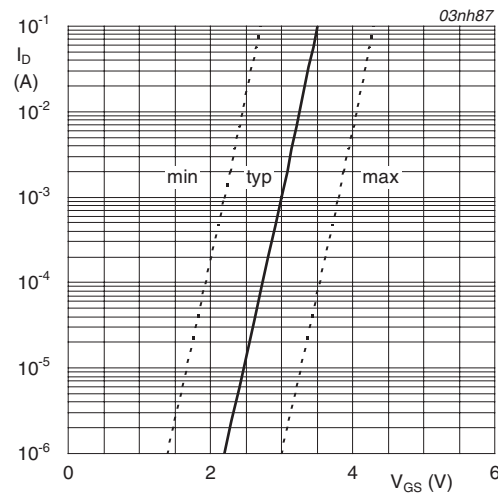
$I_D = 10\text{A}$

**Fig 10. Drain-source clamping voltage as a function of gate-source clamping current; typical values**



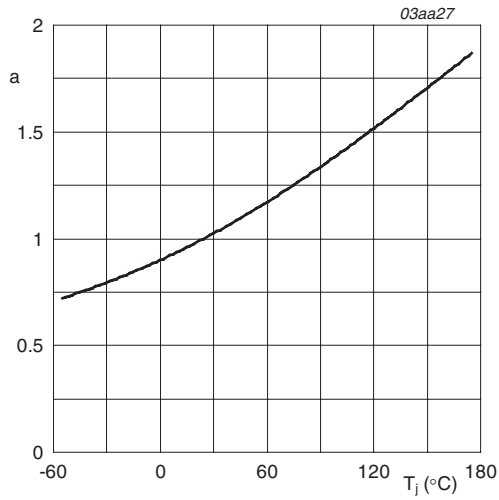
$I_D = 1\text{mA}; V_{DS} = V_{GS}$

**Fig 11. Gate-source threshold voltage as a function of junction temperature**



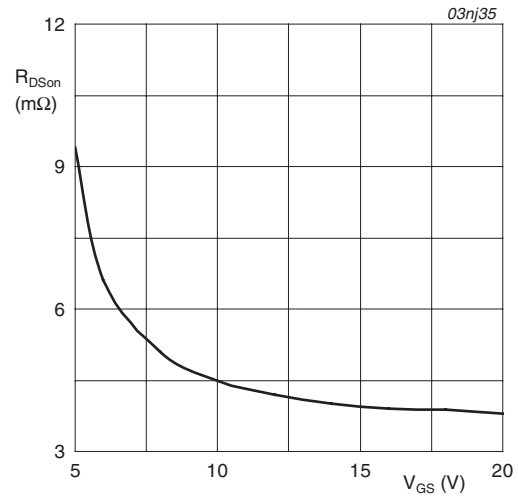
$T_j = 25^\circ\text{C}; V_{DS} = V_{GS}$

**Fig 12. Sub-threshold drain current as a function of gate-source voltage**



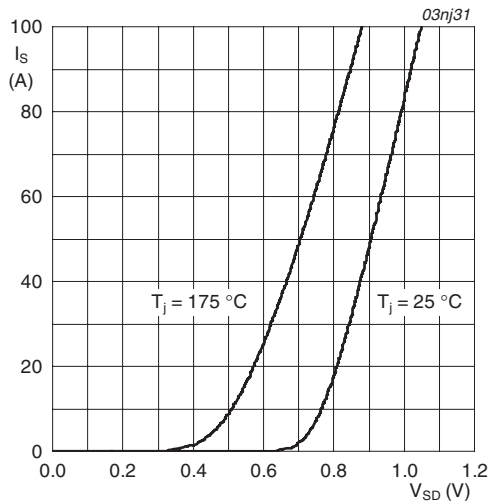
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ C)}}$$

**Fig 13. Normalized drain-source on-state resistance factor as a function of junction temperature**



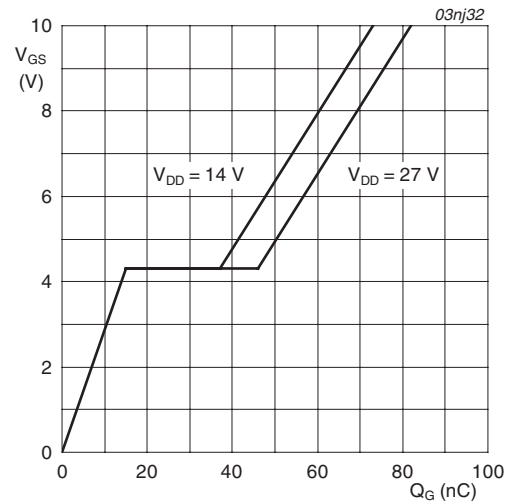
$T_j = 25^\circ C; I_D = 30A$

**Fig 14. Drain-source on-state resistance as a function of gate-source voltage; typical values**



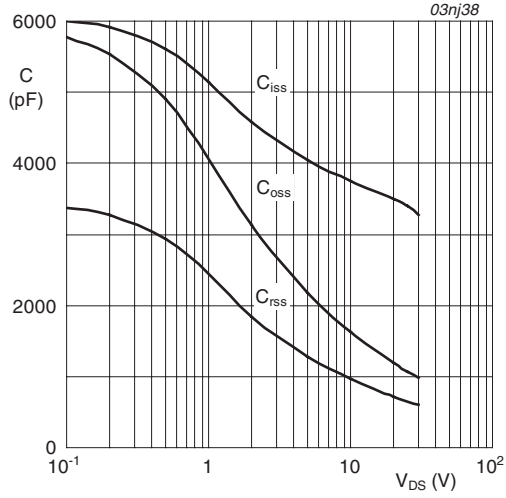
$V_{GS} = 0V$

**Fig 15. Source current as a function of source-drain voltage; typical values**



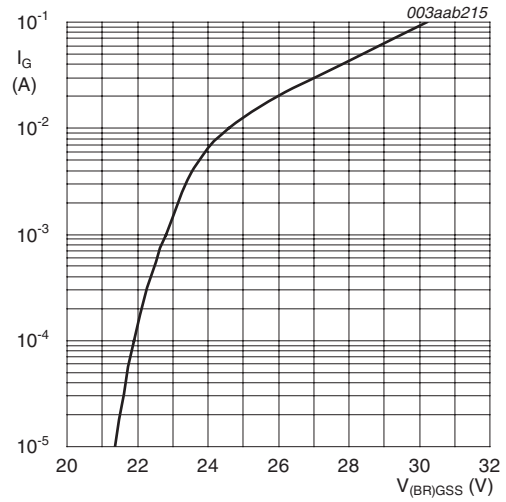
$T_j = 25^\circ C; I_D = 25A$

**Fig 16. Gate-source voltage as a function of gate charge; typical values**

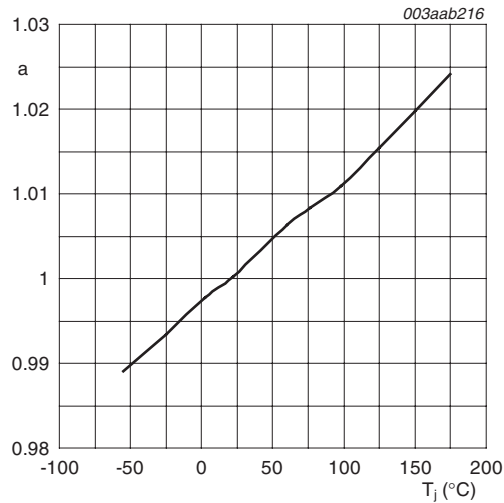


$V_{GS} = 0V; f = 1MHz$

**Fig 17. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**



**Fig 18. Source-gate clamping current as a function of source-gate clamping voltage; typical values**



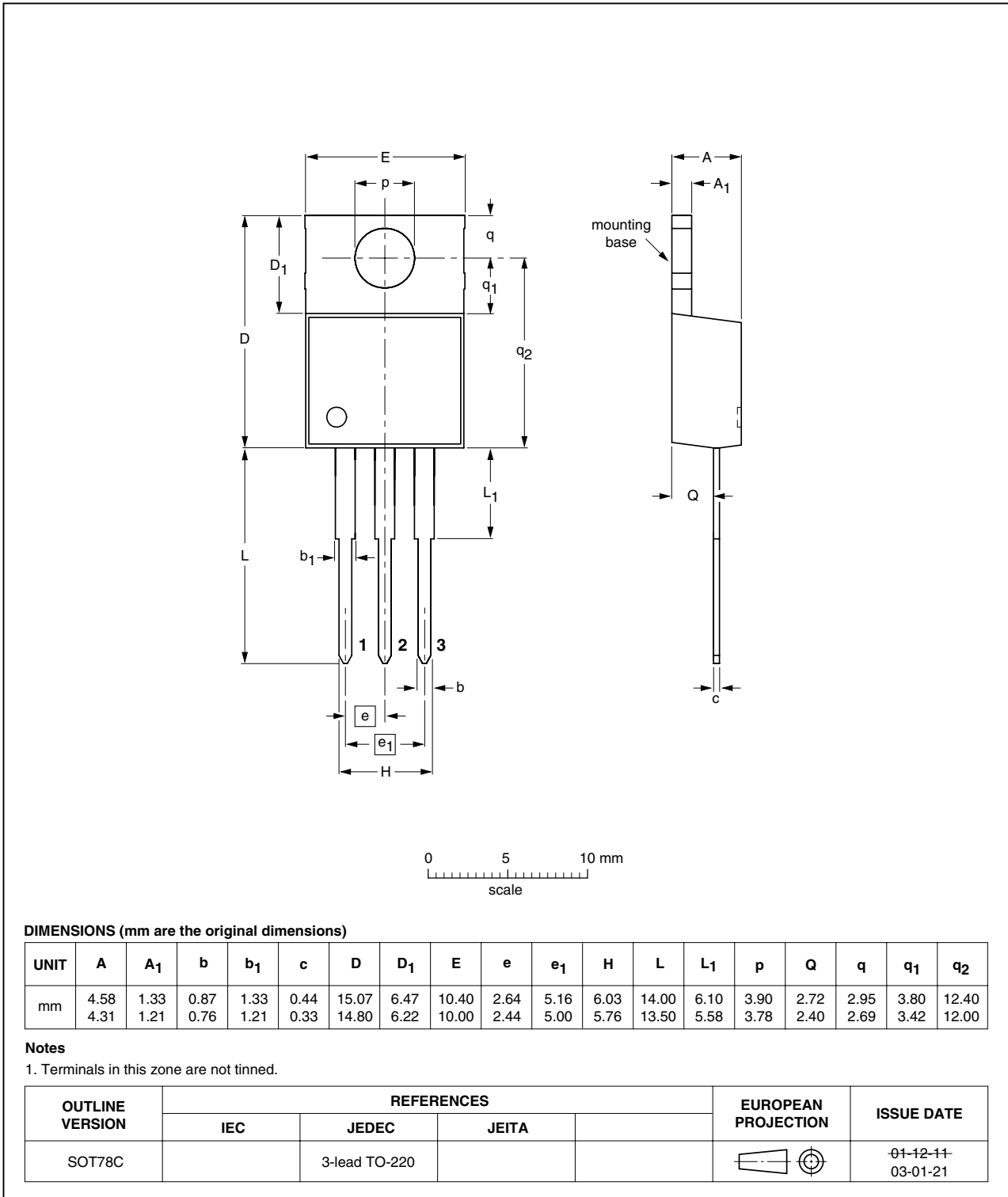
$$a = \frac{V_{(BR)GSS}}{V_{(BR)GSS(25^{\circ}C)}}$$

**Fig 19. Normalized source-gate clamping voltage as a function of junction temperature; typical values**

**7. Package outline**

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3 leads

**SOT78C**



**Fig 20. Package outline SOT78C (TO-220)**

## 8. Revision history

**Table 7. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK7L06-34ARC_5	20090217	Product data sheet	-	BUK7L06-34ARC_4
Modifications:	<ul style="list-style-type: none"> <li>• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>• Legal texts have been adapted to the new company name where appropriate.</li> </ul>			
BUK7L06-34ARC_4	20051213	Product data sheet	-	BUK7L06_34ARC-03
BUK7L06_34ARC-03 (9397 750 12162)	20031203	Product data sheet	-	BUK7L06_34ARC-02
BUK7L06_34ARC-02 (9397 750 11471)	20030521	Product data sheet	-	BUK7L06_34ARC-01
BUK7L06_34ARC-01 (9397 750 11177)	20030414	Product data sheet	-	-

## 9. Legal information

### 9.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

## 11. Contents

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