DATA SHEET

OM5926HN
I²C-bus SIM card interface

Product specification

2003 Feb 19

Philips
Semiconductors

PHILIPS

CONTENTS

I²C-bus SIM card interface OM5926HN

1 FEATURES

- Subscriber Identification Module (SIM) card interface in accordance with GSM11.11, GSM11.12 (Global System for Mobile communication) and ISO 7816 requirements
- V_{CC} regulation (3 or 5 V ±8%) with controlled rise and fall times
- One protected and buffered pseudo-bidirectional I/O line (I/O referenced to V_{CC} and SIMI/O referenced to V_{DDI})
- Clock generation (up to 10 MHz) with synchronous start and frequency quadrupling
- Clock stop LOW, clock stop HIGH or 1.25 MHz (from internal oscillator) for cards Power-down mode
- Automatic activation and deactivation sequences of an independent sequencer
- Automatic processing of pin RST with the counting of the 41928 CLK cycles for the beginning of the Answer-To-Reset (ATR)
- Warm reset command
- Supply voltage supervisor for power-on reset, spike killing and emergency deactivation in case of supply drop-out
- DC-to-DC converter (doubler, tripler or follower) allowing operation in a 3 or 5 V environment ($2.5 \leq V_{DD} \leq 6$ V)
- Enhanced Electrostatic Discharge (ESD) protection on card side (6 kV minimum)
- Power-down mode with several active features and current reduction
- Off mode with 5 μA current
- Control from a microcontroller via a 400 kHz slave I²C-bus (address 48H)
- Interface signals supplied by an independent voltage ($1.5 \leq V_{DDI} \leq 6$ V).

2 APPLICATIONS

- GSM mobile phones.

3 GENERAL DESCRIPTION

The OM5926HN is a low cost one chip SIM interface, in accordance with GSM11.11, GSM11.12 with card current limitation. Controlled by the I²C-bus, it is optimized in terms of board space, external components count and connection count (see Chapter 13).

Due to the integrated DC-to-DC converter, the device ensures full cross-compatibility between 3 or 5 V cards and 3 or 5 V environments. The very low power consumption in Power-down mode and Off mode saves battery power.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
OM5926HN	HVQFN20	plastic, heatsink very thin quad flat package; no leads; 20 terminals; body 5 × 5 × 0.85 mm	SOT662-1

5 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage on pins V_{DDS} and V_{DDP}		2.5	–	6	V
I_{DD}	supply current on pins V_{DDS} and V_{DDP}	Off mode; V_{DD} = 3 V	–	–	5	µA
		Power-down mode; V_{DD} = 3V; V_{CC} = 5 V; I_{CC} = 100 µA; SIMCLK connected to PGND or V_{DDI}; CLK is stopped	–	–	500	µA
		active mode; V_{DD} = 3 V; V_{CC} = 3 V; I_{CC} = 6 mA; f_{CLK} = 3.25 MHz	–	–	18	mA
		active mode; V_{DD} = 3 V; V_{CC} = 5 V; I_{CC} = 10 mA; f_{CLK} = 3.25 MHz	–	–	50	mA
		active mode; V_{DD} = 5 V; V_{CC} = 3 V; I_{CC} = 6 mA; f_{CLK} = 3.25 MHz	–	–	10	mA
		active mode; V_{DD} = 5 V; V_{CC} = 5 V; I_{CC} = 10 mA; f_{CLK} = 3.25 MHz	–	–	30	mA
V_{DDI}	interface signal supply voltage		1.5	–	6	V
V_{CC}	card supply voltage	5 V card; active mode; 0 < I_{CC} < 15 mA; 40 nAs dynamic load on 200 nF capacitor	4.6	5	5.4	V
		3 V card; active mode; 0 < I_{CC} < 10 mA; 24 nAs dynamic load on 200 nF capacitor	2.75	3	3.25	V
		5 V card; PDOWN = 1; I_{CC} < 5 mA	4.6	–	5.4	V
		3 V card; PDOWN = 1; I_{CC} < 5 mA	2.75	–	3.25	V
SR	slew rate on V_{CC} (rise and fall)	$C_{L(max)}$ = 200 nF	0.05	–	0.25	V/µs
t_{de}	deactivation time		–	–	120	µs
t_{act}	activation time		–	–	150	µs
$f_{i(SIMCLK)}$	clock input frequency		0	–	20	MHz
T_{amb}	operating ambient temperature		–40	–	+85	°C

6 BLOCK DIAGRAM

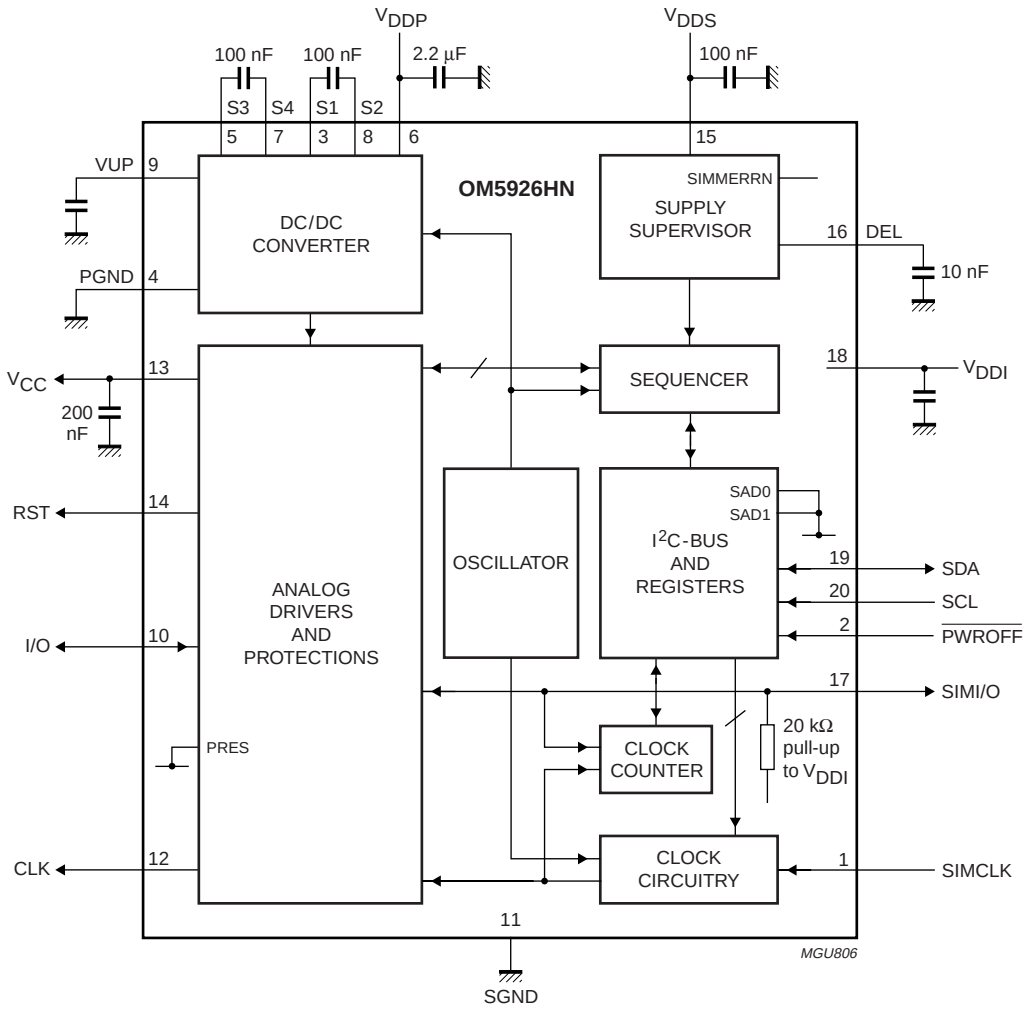


Fig.1 Block diagram.

7 PINNING INFORMATION

7.1 Pinning

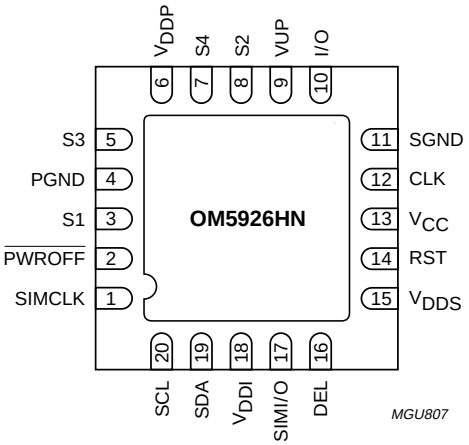


Fig.2 Pin configuration (bottom view).

7.2 Pin description

Table 1 HVQFN20 package

SYMBOL	PIN	DESCRIPTION
SIMCLK	1	external clock input
$\overline{\text{PWROFF}}$	2	control input for entering the Off mode (active LOW)
S1	3	capacitor connection for the DC-to-DC converter (between S1 and S2)
PGND	4	power ground
S3	5	capacitor connection for the DC-to-DC converter (between S3 and S4)
V_{DDP}	6	power supply voltage
S4	7	capacitor connection for the DC-to-DC converter (between S3 and S4)
S2	8	capacitor connection for the DC-to-DC converter (between S1 and S2)
VUP	9	DC-to-DC converter output (must be decoupled with a 100 nF capacitor to ground)
I/O	10	input/output to and from the card reader (C7)
SGND	11	signal ground
CLK	12	clock output to the card reader (C3)
V_{CC}	13	supply voltage to the card reader (C1)
RST	14	reset output to the card reader (C2)
V_{DDS}	15	signal supply voltage
DEL	16	external capacitor connection for the delay on the voltage supervisor
SIMI/O	17	input/output to and from the microcontroller (internal 20 kΩ pull-up resistor connected to V_{DDI})
V_{DDI}	18	supply voltage for the interface signals with the system
SDA	19	I²C-bus serial data input/output
SCL	20	I²C-bus serial clock input

8 FUNCTIONAL DESCRIPTION

The block diagram of the OM5926HN is shown in Fig.1. The functional blocks will be described in the following sections. It is assumed that the reader of this specification is familiar with GSM11.11 and ISO 7816 terminology.

8.1 I²C-bus control

The I²C-bus is used:

- To configure the clock to the card in active mode ($\frac{1}{4}f_{SIMCLK}$ and f_{SIMCLK})
- To configure the clock to the card in power reduction mode (stop LOW, stop HIGH or ±1.25 MHz derived from the internal oscillator)
- For selecting operation with a 3 or 5 V card
- For starting or stopping sessions (cold reset)
- For initiating a warm reset
- For entering or leaving the Power-down mode
- To request the card status (hardware problem occurred, unresponsive card after activation, supply drop-out detected by the voltage supervisor, card powered or not)
- To configure the SIMI/O and I/O pins in the high-impedance state.

8.1.1 STRUCTURE OF THE I²C-BUS DATA FRAMES

- Commands to the OM5926HN:
  - START/ADDRESS/WRITE
  - COMMAND BYTE
  - STOP.

  The fixed address is 0100100. The command bits are described in Table 2. Commands are executed on the rising edge of the 9th SCL pulse of the command byte.
- Status from the OM5926HN (see Table 4). The fixed address is 0100100.

Table 2 Description of the command bits; note 1

BIT	SYMBOL	DESCRIPTION
0	START/STOP	Logic 1 initiates an activation sequence and a cold reset procedure. Logic 0 initiates a deactivation sequence.
1	WARM	Logic 1 initiates a warm reset procedure. It will be automatically reset by hardware when the card starts answering, or when the 2 times 41928 CLK pulses have expired without answer from the card.
2	3 V/5 VN	Logic 1 sets the card supply voltage V_{CC} to 3 V. Logic 0 sets the card supply voltage V_{CC} to 5 V.
3	PDOWN	Logic 1 applies on the CLK pin the frequency defined by bits CLKPD1 and CLKPD2, and enters a reduced current consumption mode. Logic 0 sets the circuit back to normal mode.
4	CLKPD1	These 2 bits determine the clock to the card at Power-down as shown in Table 3.
5	CLKPD2	
6	DT/DFN	Logic 0 sets f_{CLK} to $\frac{1}{4}f_{SIMCLK}$ (in active mode). Logic 1 sets f_{CLK} to f_{SIMCLK}.
7	I/OEN	Logic 1 will transfer I/O to SIMI/O. Logic 0 sets I/O and SIMI/O to the high-impedance state.

Note

1. All bits are cleared at reset.

Table 3 Clock selection to the card at power-down

CLKPD2	CLKPD1	FUNCTION
0	0	clock stop LOW
0	1	clock is $\frac{1}{2}f_{osc}$
1	0	clock stop HIGH
1	1	don't use

Table 4 Description of the status bits; note 1

BIT	SYMBOL	DESCRIPTION
0	–	Bit 0 is not used and is fixed to logic 1.
1	–	Bit 1 is not used and is fixed to logic 0.
2	–	Bit 2 is not used and is fixed to logic 0.
3	SUPL	Logic 1 when the voltage supervisor has signalled a fault. Logic 0 when the status is read-out.
4	–	Bit 4 is not used and is fixed to logic 0.
5	MUTE	Logic 1 when a card has not answered after 2 times 41928 CLK cycles. Logic 0 when the status is read-out.
6	EARLY	Logic 1 when a card has answered between 200 and 352 CLK cycles. Logic 0 when the status is read-out.
7	ACTIVE	Logic 1 when the card is power-on. Logic 0 when the card is power-off.

Note

1. In the event of supply drop-out during a session, the card will be automatically deactivated, bit START = 0 and the corresponding status bit = 1. The status bit will be logic 0 when the microcontroller reads out the status register, on the 7th SCL pulse. After a supply drop-out, bit SUPL = 1.

8.2 Power supply

The circuit operates within a supply voltage range of 2.5 to 6 V. The supply pins are V_{DDS} and SGND. Pins V_{DDP} and PGND only supply the DC-to-DC converter for the analog drivers to the card and must be decoupled externally because of the large current spikes that the card and the DC-to-DC converter can create. An integrated spike killer ensures the card contacts remain inactive during power-up or power-down. An internal voltage reference is generated which is used for the DC-to-DC converter, the voltage supervisor and the V_{CC} generator.

All interface signals with the microcontroller ($\overline{\text{PWROFF}}$, SIMCLK, SCL, SDA and SIMI/O) are referenced to a separate supply pin V_{DDI}, which may be different from V_{DD} ($1.5 \leq V_{DDI} \leq 6$ V).

The pull-up resistors on bus lines SDA and SCL may be referenced to a voltage higher than V_{DDI}. This allows the use of peripherals which do not operate at V_{DDI}.

The voltage supervisor (see Fig.3) senses V_{DDS} and generates an alarm pulse when V_{DD} is too low to ensure proper operation. The alarm pulse width (t_W) is defined by an external capacitor connected to pin DEL (1 ms per 1 nF typical).

During the alarm pulse, the I²C-bus is unresponsive but will become operational at the end of the alarm pulse. Bit SUPL is set as long as the status has not been read.

The alarm pulse will also block any spurious signals on the card contacts during microcontroller reset, and will force an automatic deactivation of the contacts in the event of supply drop-out.

If a supply drop-out occurs during a session, the START bit is cleared and an automatic deactivation is initiated.

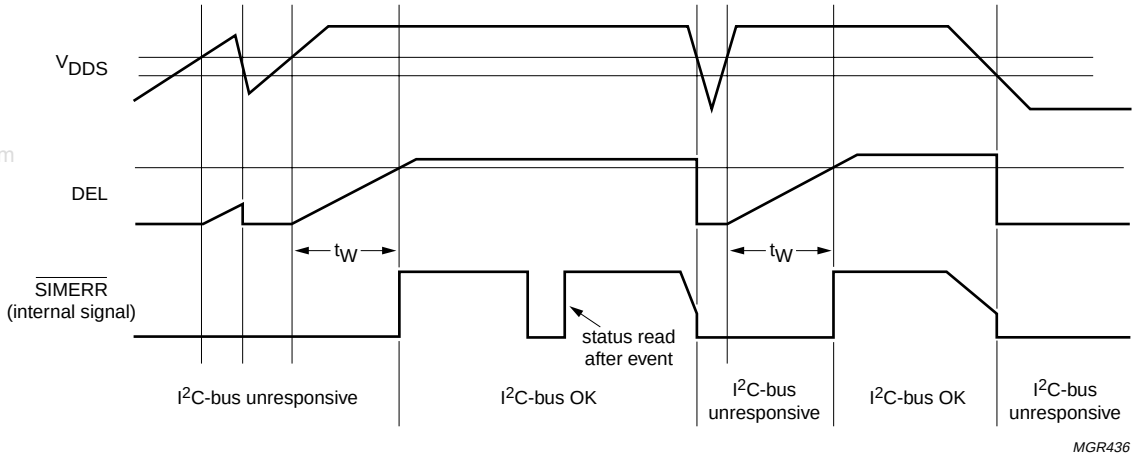


Fig.3 Voltage supervisor.

8.3 DC-to-DC converter

The whole circuit is powered by V_{DDS}, except for the V_{CC} generator, the other card contact buffers and the interface signals.

The DC-to-DC converter acts as a doubler or a tripler, depending on the supply voltage V_{DD} and the card supply voltage V_{CC}. There are basically four possible situations:

- V_{DD} = 3 V and V_{CC} = 3 V; the DC-to-DC converter acts as a doubler with a regulation of V_{VUP} at approximately 4.5 V
- V_{DD} = 3 V and V_{CC} = 5 V; the DC-to-DC converter acts as a tripler with a regulation of V_{VUP} at approximately 6.5 V
- V_{DD} = 5 V and V_{CC} = 3 V; the DC-to-DC converter is disabled and V_{DD} is applied to pin VUP
- V_{DD} = 5 V and V_{CC} = 5 V; the DC-to-DC converter acts as a doubler with a regulation of V_{VUP} at approximately 6.5 V.

The recognition of the supply voltage is done by the OM5926HN at approximately 3.3 V.

When a card session is requested by the microcontroller, the sequencer will first start the DC-to-DC converter, which is a switched capacitors type, clocked by an internal oscillator at a frequency f_{osc} of approximately 2.5 MHz. The output voltage V_{VUP} is regulated at approximately 4.5 or 6.5 V and subsequently fed to the V_{CC} generator. V_{CC} and PGND are used as a reference for all other card contacts.

8.4 Power-down mode

The Power-down mode is used for current consumption reduction when the card is in sleep mode.

For entering the Power-down mode, the microcontroller must first select the state of CLK (stop LOW, stop HIGH or 1.25 MHz from the internal oscillator) using the CLKPD1 and CLKPD2 bits. Subsequently, the microcontroller sends the command PDOWN, CLK is switched to the value predefined by the CLKPD1 and CLKPD2 bits, and SIMCLK may be stopped (HIGH or LOW).

If the selected CLK is stopped, the biasing currents in the buffers to the card will be reduced. The voltage supervisor and all control functions remain active. The maximum current taken by the card when CLK is stopped should be less than 5 mA.

Before leaving the Power-down mode, the clock signal must first be applied to SIMCLK, then the PDOWN bit must be set to logic 0.

8.5 Off mode

The Off mode is entered when the $\overline{\text{PWROFF}}$ signal is LOW. In this mode, no function is valid. This mode avoids switching off the power supply of the device, and gives a current consumption less than 5 μA. Before entering the Off mode, the card must be deactivated.

The Off mode is left when the $\overline{\text{PWROFF}}$ signal returns to HIGH. This re-initializes the voltage supervisor, and has the same effect as a reset of the device.

8.6 Sequencer and clock counter

The sequencer handles the activation and deactivation sequences in accordance with GSM11.11 and ISO 7816, even in the event of an emergency (card take-out, short-circuit and supply drop-out). The sequencer is clocked with the internal oscillator frequency (f_{osc}).

The activation is initiated with the START command (only if the card is present, and if the voltage supervisor does not detect a fault on the supply). During activation, V_{CC} goes HIGH and subsequently I/O is enabled and CLK is started with RST = LOW. The clock counter counts the CLK pulses until a start bit is detected on I/O.

After 41928 CLK pulses, if no start bit on I/O has been detected, the sequencer toggles RST to HIGH and counts another 41928 CLK pulses. If, again, no start bit has been detected, the MUTE bit is set in the Status register.

If a start bit has been detected during the two 41928 CLK pulses slots, the clock counter is stopped, RST is kept at the same level and the session can go on between the card and the system.

The clock counter ignores any start bit during the first 200 CLK pulses of both slots. If a start bit is detected between 200 and 352 CLK pulses of both slots, then the EARLY bit is set in the Status register.

The deactivation is initiated either by the microcontroller (STOP command), or automatically by the OM5926HN in the event of a short-circuit or supply voltage drop-out detected by the voltage supervisor. During deactivation, RST will go LOW, CLK is stopped, I/O is disabled and V_{CC} goes LOW.

8.7 Clock circuitry

The clock to the card is either derived from the SIMCLK pin (2 to 20 MHz) or from the internal oscillator.

During a card session, f_{CLK} may be chosen to be $\frac{1}{4}f_{SIMCLK}$ or f_{SIMCLK} depending on the state of the DT/DFN bit.

For the card Sleep mode, CLK may be chosen stop LOW, stop HIGH or $\frac{1}{2}f_{osc}$ (1.25 MHz) with bits CLKPD1 and CLKPD2. This predefined value will be applied to CLK when the PDOWN bit is set to logic 1.

The first CLK pulse has the correct width, and all frequency changes are synchronous, ensuring that no pulse is smaller than 45% of the shortest period.

The duty cycle is within 45 and 55% in the stable state, the rise and fall times are less than 8% of the period and precautions must be taken to ensure that there is no overshoot or undershoot.

8.7.1 ACTIVATION SEQUENCE

Figure 4 shows the activation sequence. When the card is inactive, V_{CC}, CLK, RST and I/O are LOW, with low-impedance with respect to ground. The DC-to-DC converter is stopped. SIMI/O is pulled HIGH at V_{DDI} via the 20 kΩ pull-up resistor. When all conditions are met (supply voltage, card present, no hardware problems), the microcontroller may initiate an activation sequence by setting the START bit to logic 1 (t_0) via the I²C-bus:

1. The DC-to-DC converter is started (t_1).
2. V_{CC} starts rising from 0 to 3 V or 0 to 5 V, according to the state of the 3 V/5 VN control bit, with a controlled rise time of 0.17 V/µs typically (t_2).
3. I/O buffer is enabled in reception mode (t_3).
4. CLK is sent to the card reader with RST = LOW, and the count of 41928 CLK pulses is started ($t_4 = t_{act}$).
5. If a start bit is detected on I/O, the clock counter is stopped with RST = LOW. If not, RST = HIGH, and a new count of 41928 CLK pulses is started (t_5).

If a start bit is detected on I/O and the clock counter is stopped with RST = HIGH, the card session may continue. If not, the MUTE bit is set in the Status register. The microcontroller may initiate a deactivation sequence by setting the START bit to logic 0.

If a start bit is detected during the first 200 CLK pulses of each count slot, then it will not be taken into account. If a start bit is detected during 200 and 352 CLK pulses of each slot, then bit EARLY is set in the status register. The microcontroller may initiate a deactivation sequence by setting the START bit to logic 0.

The sequencer is clocked by $\frac{1}{64}f_{osc}$ which leads to a time interval T of 25 µs typically. Thus $t_1 = 0$ to $\frac{1}{2}$ T; $t_2 = t_1 + \frac{3}{2}$ T; $t_3 = t_1 + \frac{7}{2}$ T; $t_4 = t_1 + 4$ T and t_5 depends on the SIMCLK frequency.

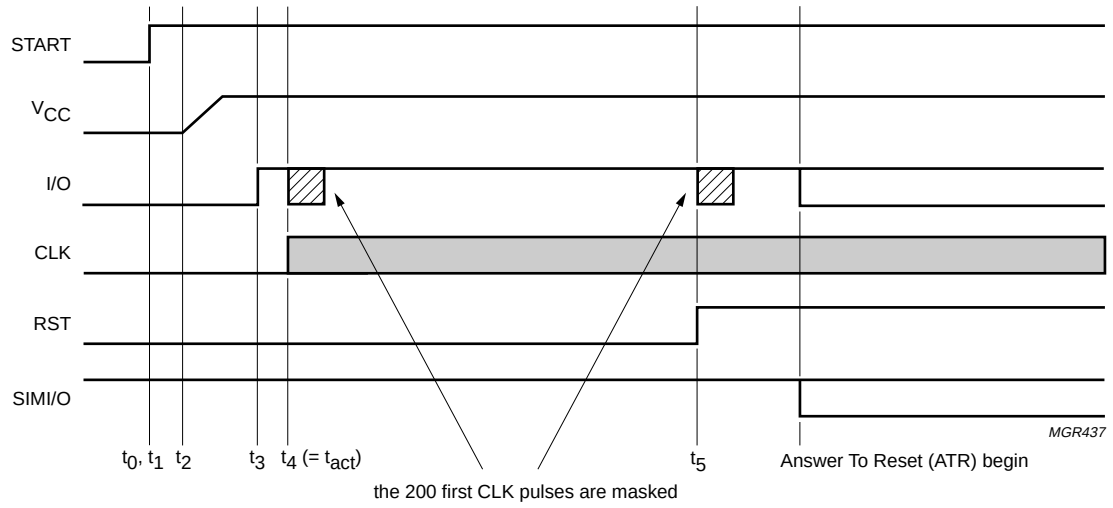


Fig.4 Activation sequence.

8.7.2 DEACTIVATION SEQUENCE

Figure 5 shows the deactivation sequence. When the session is completed, the microcontroller sets the START bit to logic 0. The circuit will then execute an automatic deactivation sequence:

1. Card reset, RST goes LOW (t_{10}).
2. CLK is stopped (t_{11}).
3. I/O goes LOW (t_{12}).
4. V_{CC} falls to 0 V with typically 0.17 V/µs slew rate (t_{13}). The deactivation is completed when V_{CC} reaches 0.4 V (t_{de}).
5. The DC-to-DC converter is stopped and CLK, RST, V_{CC} and I/O become low-impedance with respect to PGND (t_{14}).

$t_{10} < {}^{1}/_{64}$ T; $t_{11} = t_{10} + {}^{1}/_{2}$ T; $t_{12} = t_{10} + T$; $t_{13} = t_{12} + 5$ µs and $t_{14} = t_{10} + 4$ T.

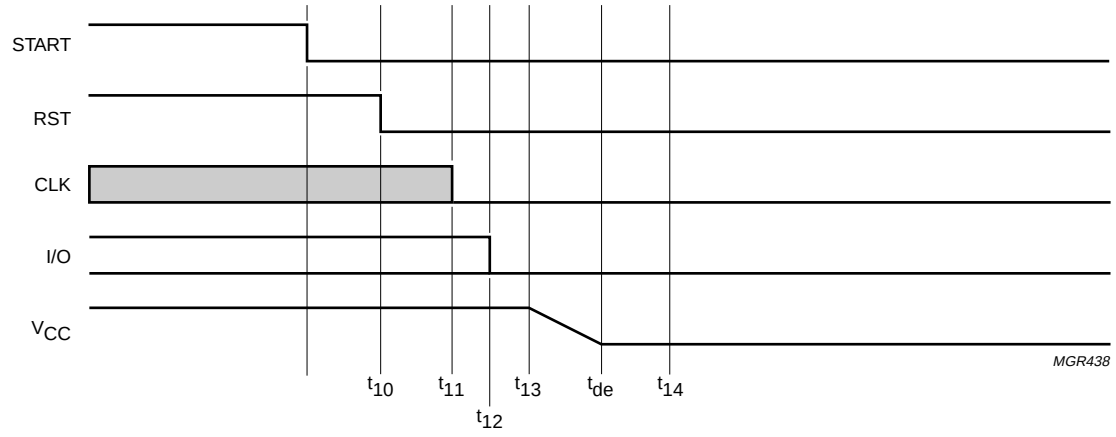


Fig.5 Deactivation sequence.

8.8 Protection

Two hardware fault conditions are monitored by the circuit:

- Short-circuits between V_{CC} and other contacts
- Supply drop-out.

When one of these problems is detected during a card session, the security logic block initiates an automatic deactivation of the contacts (see Fig.6).

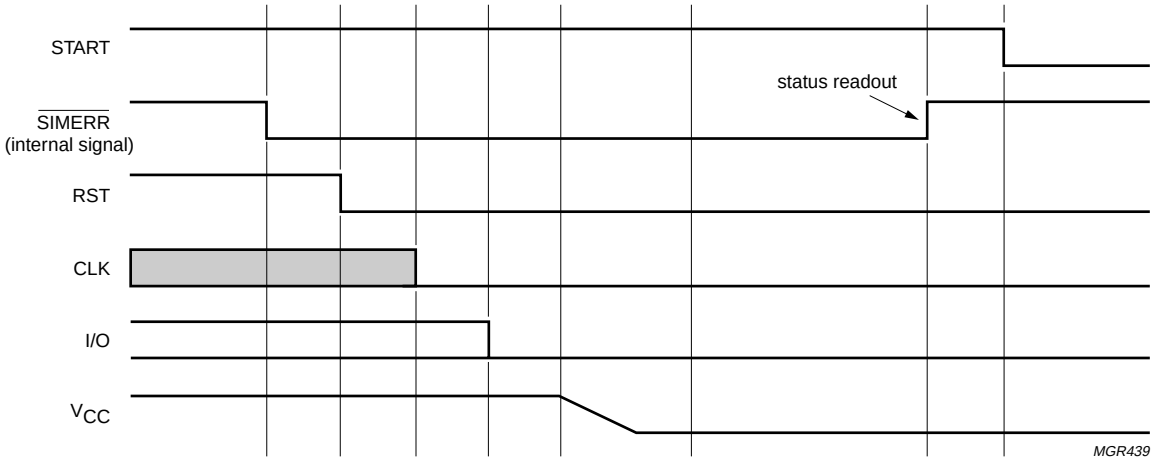


Fig.6 Emergency deactivation.

8.9 I/O circuitry

The Idle state is realized by both I/O and SIMI/O being pulled HIGH (via a 10 kΩ pull-up resistor from I/O to V_{CC} and via a 20 kΩ pull-up resistor from SIMI/O to V_{DDI}).

I/O is referenced to V_{CC} and SIMI/O to V_{DDI}, thus allowing operation with $V_{CC} \neq V_{DD} \neq V_{DDI}$.

When configuration bit I/OEN is logic 0, then I/O and SIMI/O are independent.

When bit I/OEN is logic 1, then the data transmission between I/O and SIMI/O is enabled.

The first side on which a falling edge occurs becomes the master. An anti-latch circuit disables the detection of falling edges on the other side, which becomes a slave.

After a delay time (t_d) of <500 ns on the falling edge, the N transistor on the slave side is turned on, thus transmitting the logic 0 present on the master side.

When the master goes back to logic 1, the P transistor on the slave side is turned on during t_d, and then both sides return to their Idle states.

The maximum frequency on these lines is 1 MHz.

9 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDP}	power supply voltage		–0.5	+6.5	V
V_{DDS}	signal supply voltage		–0.5	+6.5	V
V_{DDI}	interface signal supply voltage		–0.5	+6.5	V
$V_{i(n)}$	input voltage				
	pins 1, 2 and 17		–0.5	+6.5	V
	pin 16		–0.5	V_{DDS} + 0.5	V
	pins 19 and 20		–0.5	+6.5	V
	pins 10, 12 and 14		–0.5	V_{CC} + 0.5	V
	pin 13		–0.5	+6.5	V
	pin 9		–0.5	+7.5	V
	pins 3, 5, 7 and 8		–0.5	V_{VUP} + 0.5	V
P_{tot}	continuous total power dissipation	T_{amb} = –40 to +85 °C	–	230	mW
T_j	operating junction temperature		–	125	°C
T_{stg}	IC storage temperature		–55	+150	°C
$V_{esd(n)}$	electrostatic discharge voltage				
	on pins 10, 12, 13 and 14		–6	+6	kV
	on any other pin		–2	+2	kV

10 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handle Metal Oxide Semiconductor (MOS) devices.

11 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	35	K/W

12 CHARACTERISTICS

V_{DD} = 3 V; V_{DDI} = 1.5 V; f_{SIMCLK} = 13 MHz; f_{CLK} = 3.25 MHz; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage on pins V_{DDS} and V_{DDP}		2.5	–	6.0	V
I_{DD}	supply current on pins V_{DDS} and V_{DDP}	Off mode	–	–	5	µA
		inactive mode	–	–	50	µA
		Power-down mode; V_{CC} = 5 V; I_{CC} = 100 µA; SIMCLK connected to SGND or V_{DDI}; CLK is stopped	–	–	500	µA
		active mode; V_{CC} = 3 V; I_{CC} = 6 mA	–	–	18	mA
		active mode; V_{CC} = 5 V; I_{CC} = 10 mA	–	–	50	mA
		active mode; V_{DD} = 5 V; V_{CC} = 3 V; I_{CC} = 6 mA	–	–	10	mA
		active mode; V_{DD} = 5 V; V_{CC} = 5 V; I_{CC} = 10 mA	–	–	30	mA
V_{DDI}	interface signal supply voltage		1.5	–	6	V
I_{DDI}	interface signals supply current	SIMCLK connected to PGND or V_{DDI}	–	–	3	µA
		f_{SIMCLK} = 13 MHz; V_{DDI} = 1.5 V	–	–	120	µA
		f_{SIMCLK} = 13 MHz; V_{DDI} = 6 V	–	–	1.2	mA
$V_{th(VDD)}$	threshold voltage on V_{DD}	falling edge	2	–	2.3	V
$V_{hys(VDD)}$	hysteresis voltage on V_{DD}		40	–	200	mV
$V_{th(DEL)}$	threshold voltage on pin DEL		–	1.38	–	V
V_{DEL}	voltage on pin DEL		–	–	V_{DD}	V
$I_{ch(DEL)}$	charge current on pin DEL		–0.5	–1	–2.5	µA
$I_{dch(DEL)}$	discharge current on pin DEL	V_{DEL} = V_{DD}	0.5	–	–	mA
t_W	alarm pulse width	C_{DEL} = 10 nF	15	–	25	ms
Pin SIMCLK						
$f_{i(SIMCLK)}$	clock input frequency		0	–	20	MHz
t_f	fall time		–	–	1	µs
t_r	rise time		–	–	1	µs
V_{IL}	LOW-level input voltage		0	–	$0.3V_{DDI}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DDI}$	–	V_{DDI} + 0.3	V
I_L	leakage current		–	–	±3	µA
DC-to-DC converter						
$\frac{1}{2}f_{osc}$	oscillator frequency		1	–	1.6	MHz
V_{VUP}	voltage on pin VUP	5 V card	–	6.0	–	V
		3 V card	–	4.5	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pin SDA (open-drain)						
V_{IL}	LOW-level input voltage		–0.3	–	$+0.3V_{DDI}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DDI}$	–	6	V
I_{LH}	HIGH-level leakage current		–	–	1	µA
I_{IL}	LOW-level input current	depends on the pull-up resistor	–	–	–	µA
V_{OL}	LOW-level output voltage	I_{OL} = 3 mA	–	–	0.3	V
Pin SCL (open-drain)						
V_{IL}	LOW-level input voltage		–0.3	–	$+0.3V_{DDI}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DDI}$	–	6	V
I_{LI}	input leakage current		–	–	1	µA
Pin $\overline{\text{PWROFF}}$						
V_{IL}	LOW-level input voltage		0	–	$0.3V_{DDI}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DDI}$	–	V_{DDI} + 0.3	V
I_{LI}	input leakage current		–	–	±1	µA
Pin RST						
V_O	output voltage	inactive mode; I_O = 1 mA	–0.3	–	+0.3	V
I_O	output current	inactive mode; pin RST grounded	–	–	–1	mA
V_{OL}	LOW-level output voltage	I_{OL} = 200 µA	–0.2	–	+0.3	V
V_{OH}	HIGH-level output voltage	I_{OH} < –200 µA	V_{CC} – 0.5	–	V_{CC} + 0.2	V
t_f	fall time	C_L = 30 pF	–	–	0.5	µs
t_r	rise time	C_L = 30 pF	–	–	0.5	µs
Pin CLK						
V_O	output voltage	inactive mode; I_O = 1 mA	–0.3	–	+0.3	V
I_O	output current	inactive mode; pin CLK grounded	–	–	–1	mA
V_{OL}	LOW-level output voltage	I_{OL} = 200 µA	–0.2	–	+0.3	V
V_{OH}	HIGH-level output voltage	I_{OH} = –200 µA	V_{CC} – 0.5	–	V_{CC} + 0.2	V
t_f	fall time	C_L = 30 pF	–	–	8	ns
t_r	rise time	C_L = 30 pF	–	–	8	ns
f_{clk}	clock frequency	1 MHz power-down configuration	1	–	1.6	MHz
		regular activity	0	–	10	MHz
δ	duty factor	C_L = 30 pF	45	–	55	%
Pin V_{CC} (with 200 nF capacitor)						
V_O	output voltage	inactive mode; I_O = 1 mA	–	–	0.3	V
		active mode; 5 V card; no load	4.85	5.10	5.40	V
		active mode; 3 V card; no load	2.8	3.05	3.25	V
		5 V card; PDOWN = 1; I_{CC} < 5 mA	4.6	–	5.4	V
		3 V card; PDOWN = 1; I_{CC} < 5 mA	2.75	–	3.25	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_O	output voltage	active mode;				
		5 V card; with static load	4.60	–	5.40	V
		3 V card; with static load	2.75	–	3.25	V
		5 V card; 40 nAs pulses; note 1	4.60	–	5.40	V
		3 V card; 12 nAs pulses; note 2	2.75	–	3.25	V
I_O	output current	inactive mode; pin V_{CC} grounded	–	–	–	mA
		V_{CC} = 5V; V_{DD} < 3.7 V	–	–	15	mA
		V_{CC} = 5V; V_{DD} > 3.7 V	–	–	20	mA
		V_{CC} = 3 V; V_{DD} < 3.7 V	–	–	10	mA
		V_{CC} = 3 V; V_{DD} > 3.7 V	–	–	15	mA
SR	slew rate on V_{CC} (rise and fall)	$C_{L(max)}$ = 300 nF	0.05	0.17	0.25	V/µs
Pin I/O (internal pull-up resistor to V_{CC})						
V_O	output voltage	inactive mode; I_O = 1 mA	–	–	0.3	V
I_O	output current	inactive mode; pin I/O grounded	–	–	–1	mA
V_{OL}	LOW-level output voltage	I_{OL} = 1 mA	–0.2	–	+0.3	V
V_{OH}	HIGH-level output voltage	+25 µA< I_{OH} < –25 µA	$0.8V_{CC}$	–	V_{CC} + 0.2	V
V_{IL}	LOW-level input voltage		–0.3	–	+0.8	V
V_{IH}	HIGH-level input voltage		1.5	–	V_{CC} + 0.3	V
I_{LIH}	HIGH-level input leakage current		–	–	10	µA
I_{IL}	LOW-level input current		–	–	–600	µA
$t_{t(DI)}$	data input transition time	C_L = 30 pF	–	–	1.2	µs
$t_{t(DO)}$	data output transition time	C_L = 30 pF	–	–	0.5	µs
t_d	delay time on falling edge		–	–	500	ns
$R_{pu(int)}$	internal pull-up resistance between pins I/O and V_{CC}		13	–	20	kΩ
Pin SIMI/O (internal pull-up resistor to V_{DDI})						
V_{OL}	LOW-level output voltage	I_{OL} = 1 mA	–0.2	–	+0.3	V
V_{OH}	HIGH-level output voltage	with internal 20 kΩ pull-up resistor to V_{DDI}; I_O = 10 µA	V_{DDI} – 0.3	–	V_{DDI} + 0.2	V
V_{IL}	LOW-level input voltage		–0.3	–	$+0.3V_{DDI}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DDI}$	–	V_{DDI} + 0.3	V
I_{LIH}	HIGH-level input leakage current		–	–	10	µA
I_{IL}	LOW-level input current	with internal 20 kΩ pull-up resistor to V_{DDI}; V_I = 0 V	–	–	$\frac{-V_{DDI}}{20\ k\Omega}$	µA
$t_{t(DI)}$	data input transition time	C_L = 30 pF	–	–	1.2	µs
$t_{t(DO)}$	data output transition time	C_L = 30 pF	–	–	0.5	µs
t_d	delay time on falling edge		–	–	500	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{pu(int)}$	internal pull-up resistance between pins SIMI/O and V_{DDI}		16	–	26	kΩ
Timing						
t_{act}	activation time		–	–	150	µs
t_{de}	deactivation time		–	–	120	µs

Notes

1. Current pulses applied on V_{CC} (5 V card):
   a) Continuous spikes; 20 mA amplitude; I_{DC} = 0; 100 ns duration; pause 100 ns (2 nAs; I_{av} = 10 mA; f = 5 MHz).
   b) Continuous spikes; 20 mA amplitude; I_{DC} = 0; 400 ns duration; pause 400 ns (8 nAs; I_{av} = 10 mA; f = 1.25 MHz).
   c) Continuous spikes; 15 mA amplitude; I_{DC} = 5 mA; 150 ns duration; pause 300 ns (2.25 nAs; I_{av} = 10 mA; f = 2.22 MHz).
   d) Random spikes; 200 mA amplitude; I_{DC} = 5 mA; 200 ns duration; pause between 0.1 and 500 ms (40 nAs) (see Fig.7).
   e) Random spikes; 100 mA amplitude; I_{DC} = 0; 400 ns duration; pause between 0.1 and 500 ms (40 nAs).
   f) Random spikes; 195 mA amplitude; I_{DC} = 5 mA; 200 ns duration; pause between 0.1 and 500 ms (39 nAs).
2. Current pulses applied on V_{CC} (3 V card):
   a) Continuous spikes; 12 mA amplitude; I_{DC} = 0; 100 ns duration; pause 100 ns (1.2 nAs; I_{av} = 6 mA; f = 5 MHz).
   b) Continuous spikes; 12 mA amplitude; I_{DC} = 0; 400 ns duration; pause 400 ns (4.8 nAs; I_{av} = 6 mA; f = 1.25 MHz).
   c) Continuous spikes; 9 mA amplitude; I_{DC} = 3 mA; 150 ns duration; pause 300 ns (2.25 nAs; I_{av} = 6 mA; f = 2.22 MHz).
   d) Random spikes; 60 mA amplitude; I_{DC} = 5 mA; 200 ns duration; pause between 0.1 and 500 ms (12 nAs).
   e) Random spikes; 30 mA amplitude; I_{DC} = 0; 400 ns duration; pause between 0.1 and 500 ms (12 nAs).
   f) Random spikes; 57 mA amplitude; I_{DC} = 3 mA; 200 ns duration; pause between 0.1 and 500 ms (11.4 nAs).

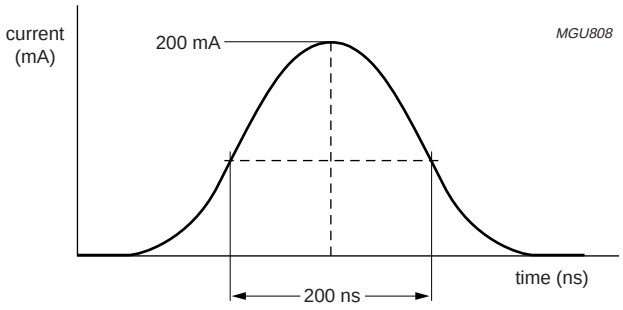
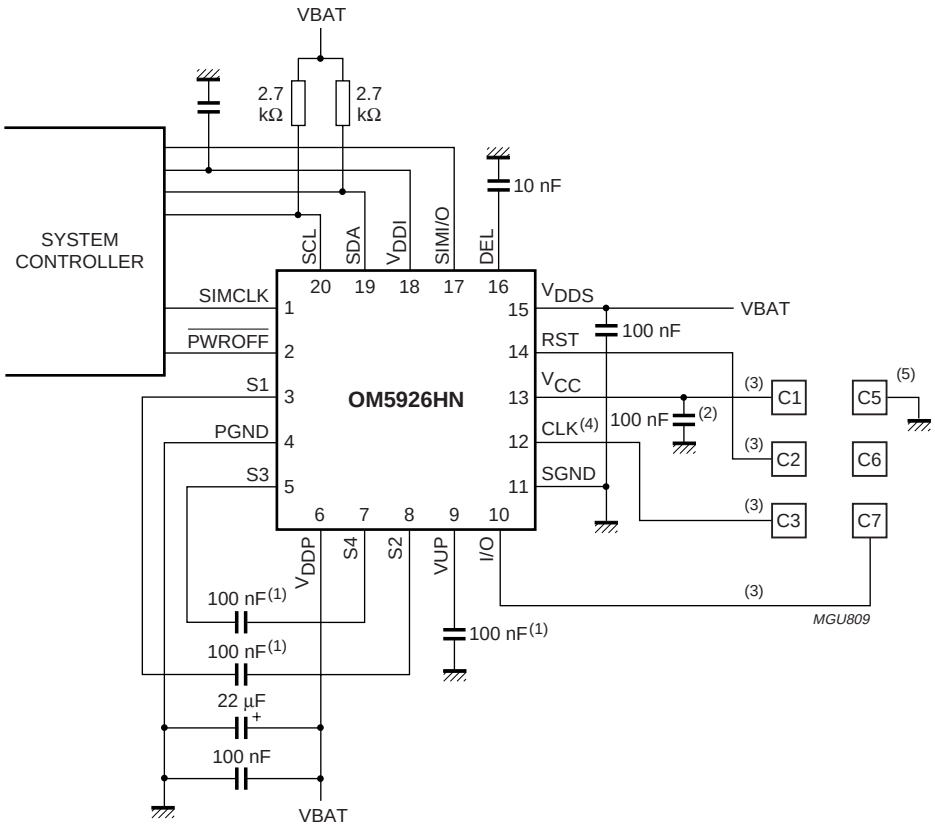


Fig.7 Example of 200 mA and 200 ns current pulse.

13 APPLICATION INFORMATION



(1) Capacitors on the DC-to-DC converter must have ESR less than 100 mΩ and must be placed close to the chip (some mm).

(2) Capacitor on V_{CC} must have ESR less than 100 mΩ.

(3) Tracks from the chip to the smart card connector must be as short as possible. If V_{CC} track exceeds 2 cm, then 2 capacitors have to be used: one near the chip, the second near the contact.

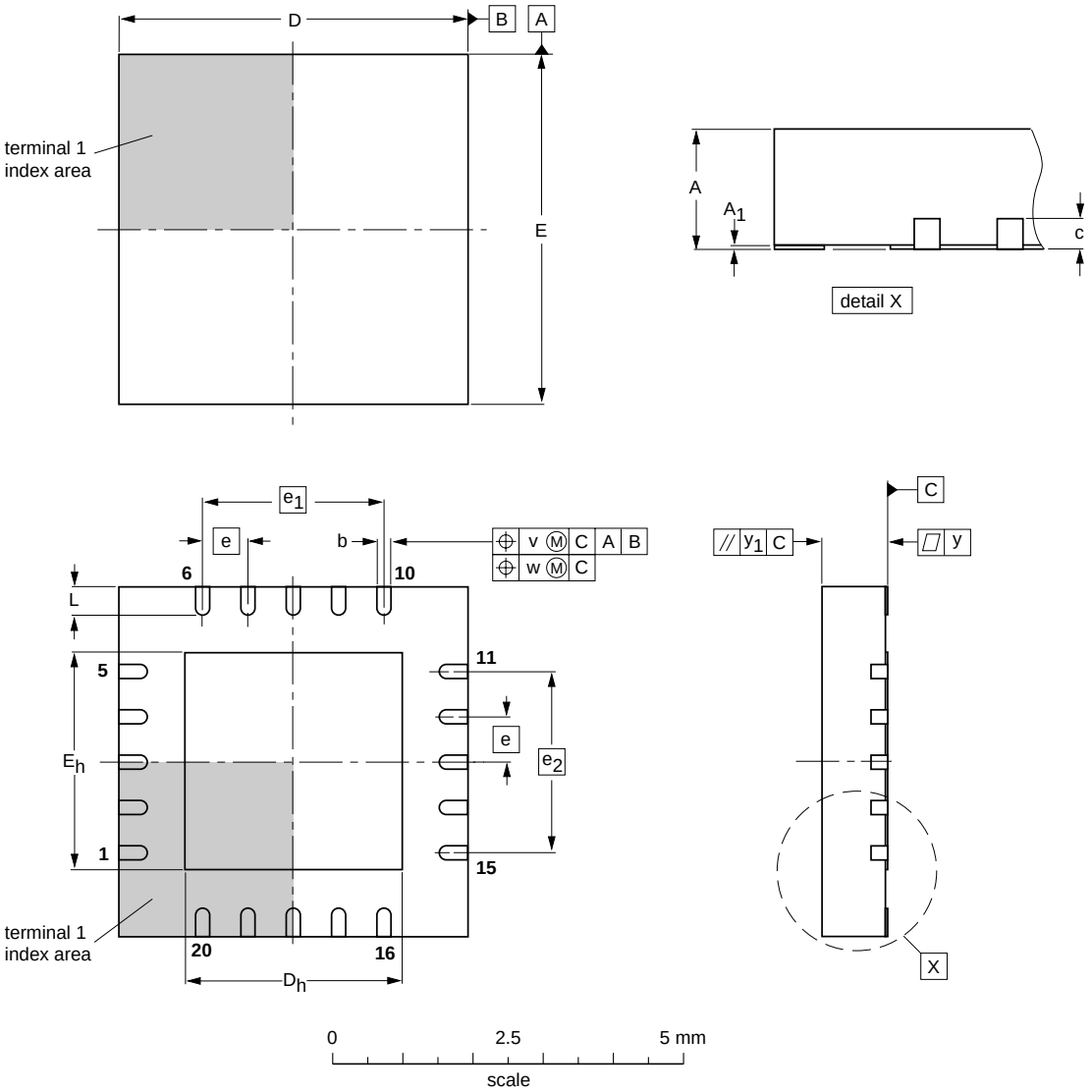
(4) CLK signal has to be routed far from I/O and RST.

(5) C5 must be electrically linked to chips GND without ground loop.

Fig.8 Application information.

14 PACKAGE OUTLINE

HVQFN20: plastic thermal enhanced very thin quad flat package; no leads; 20 terminals; body 5 x 5 x 0.85 mm **SOT662-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.38 0.23	0.2	5.1 4.9	3.25 2.95	5.1 4.9	3.25 2.95	0.65	2.6	2.6	0.75 0.50	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT662-1	- - -	MO-220	- - -			~~01-08-08~~ 02-10-22

15 SOLDERING

15.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

15.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferably be kept:

- below 220 °C for all the BGA packages and packages with a thickness ≥ 2.5mm and packages with a thickness <2.5 mm and a volume ≥350 mm^3 so called thick/large packages
- below 235 °C for packages with a thickness <2.5 mm and a volume <350 mm^3 so called small/thin packages.

15.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

15.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

15.5 Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE(1)	SOLDERING METHOD	
	WAVE	REFLOW(2)
BGA, LBGA, LFBGA, SQFP, TFBGA, VFBGA	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable(3)	suitable
PLCC(4), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(4)(5)	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended(6)	suitable

Notes

1. For more detailed information on the BGA packages refer to the *"(LF)BGA Application Note*" (AN01026); order a copy from your Philips Semiconductors sales office.
2. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
3. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
4. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
5. Wave soldering is suitable for LQFP, TQFP and QFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
6. Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

16 DATA SHEET STATUS

LEVEL	DATA SHEET STATUS(1)	PRODUCT STATUS(2)(3)	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

17 DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

18 DISCLAIMERS

Life support applications — These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

Right to make changes — Philips Semiconductors reserves the right to make changes in the products - including circuits, standard cells, and/or software - described or contained herein in order to improve design and/or performance. When the product is in full production (status ‘Production’), relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN). Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no licence or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

19 PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

NOTES

NOTES

NOTES

Philips Semiconductors – a worldwide company

Contact information

For additional information please visit **http://www.semiconductors.philips.com**. Fax: **+31 40 27 24825**
For sales offices addresses send e-mail to: **sales.addresses@www.semiconductors.philips.com**.

SCA75

Printed in The Netherlands 613502/01/pp28 Date of release: 2003 Feb 19 Document order number: 9397 750 10124

Let's make things better.

Philips Semiconductors

PHILIPS