UNIVERSAL SEMICONDUCTOR, INC.

USC1850/1852

8 BIT, 85 MCPS VIDEO DAC

FEATURES

- **8 Bit Resolution**
- **85 MSPS Min. Update Rate**
- **Single +5 V Supply**
- **TTL / CMOS Compatible**
- **Low Glitch Energy**
- **Adjustable Current Source**
- **Normal or Complement Data**
- **Independent Adjustable Output Levels**
  - **Composite Sync**
  - **Composite Blank**
  - **10% Bright**
- **Low Power CMOS (100 mW typical)**
- **Control Pins for Setting:**
  - **Reference White**
  - **Reference Black**

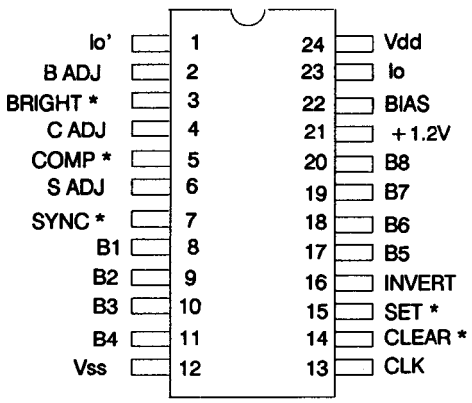
DESCRIPTION

The model USC1850 is a monolithic high speed, 8 bit DAC designed for video applications. The output of this silicon gate CMOS integrated circuit is a current source whose full scale value is set by an external resistor. The USC1850 has composite sync, composite blank, and 10 percent bright signals. It is able to drive 75 ohm or 37.5 ohm loads while operating at a minimum conversion rate of 85 MSPS. The input code is straight binary with the capability of accepting inverted incoming data. The USC1850 requires only a single +5 volt power supply and it will accept either TTL or CMOS inputs.

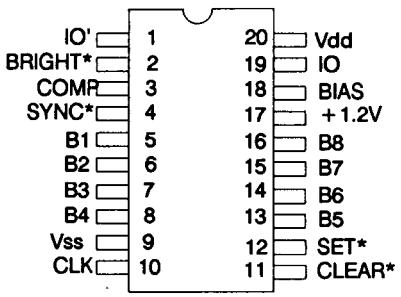
The USC1852 utilizes the USC1850 die for low cost 8 bit conversion in a 20 pin package. USC1850 and USC1852 are available in several package types with accuracy ranging from 1 LSB to 6 LSB.

PIN CONFIGURATION

USC1850



USC 1852



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ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNITS
Supply Voltage (V_{DD})	6	V
Supply Current (I_{DD})	60	mA
Full Scale Output Current (I_O)	30	mA
Drive Current into any pin	+/–10	mA
I_O or I_O' Output Voltage Range	+2.5 to –10	V
Logic Input Voltage Min	VGND –0.3	V
Logic Input Voltage Max	V_{DD} +0.3	V

MAXIMUM SWITCHING CHARACTERISTICS

V_{DD} = 5V ; T_A = 25°C ; 75 ohm load, 1 volt full scale output

PARAMETER	RATING	UNITS
Minimum Conversion Rate	85	MSPS
Settling Time to 0.2% *	20	ns
Output Transient Energy	100	pv-sec
Output Transient Amplitude	20	mV
Delay Time **	30	ns

* Typical time from beginning of output current change to final settling at 1/2 LSB ; Setup time 20ns max

** Max time from negative edge of clock to beginning of output current change

DIGITAL CHARACTERISTICS

V_{DD} = 5V ; T_A = 25°C

PARAMETER	RATING	UNITS
Compatibility	TTL ; CMOS	
Input Code	Binary	
Sync	40 1/2	IRE units
Brightness	10	IRE units
Blanking	7 1/2	IRE units
Video	92	IRE units
Logic 0 Input Voltage Max	0.8	V
Logic 1 Input Voltage Min	2.0	V

ELECTRICAL CHARACTERISTICS

V_{DD} = 5V ; T_A = 25°C ; I_O = 6 to 20mA

	PRODUCT GRADE				
PARAMETER	**B**	**C**	**D**	**E**	**UNITS**
Output Current Max (@ 1.2v)*	33	33	33	33	mA
Output Voltage Max	1.5	1.5	1.5	1.5	V
Resolution	8	8	8	8	Bits
Linearity Error Max	1	2	3	6	LSB
Diff. Linearity Error Max	1	2	3	6	LSB
Voltage Reference Min	1.17	1.15	1.15	1.15	V
Voltage Reference Max	1.29	1.31	1.31	1.31	V
Power Supply Rejection Ratio	35	35	35	35	db
Offset Current Max **	1	1	1	1	uA

* $I_O + I_O'$

** All current sources off

DEVICE OPERATION

The output of the USC1850 video DAC is a current source whose full scale value is set by an external resistor. This resistor is connected to an internal reference (1.23V nominal), and the current through the resistor represents 6 LSBs of output current. Thus, for a full scale current of 255 LSBs, I_O = 1.23 / R x 255 / 6 = 52 / R, where I_O = full scale output current, R = current setting resistor (ohms).

There is a separate pin (I_O) for the composite video signal. The output currents for composite sync, composite blank, and 10% bright are summed and appear at this pin (1). The three video signals have the following weighted values:

- Composite Sync 112 LSB (40 1/2 IRE)
- Composite Blank 21 LSB (7 1/2 IRE)
- 10% Bright 28 LSB (10 IRE)

Note that these currents are ratioed to the 8 bit DAC full scale current (255 LSBs). The video control pins operate as follows:

COMPOSITE SYNC (SYNC*): A logic "0" shuts off this current source and clears the DAC (00000000).

COMPOSITE BLANK (COMP*): A logic "0" shuts off this current source and clears the DAC (00000000).

10% BRIGHT (BRIGHT*): A logic "0" turns on this current source.

SET*: Sets 8 bit DAC to full scale (11111111). This is an asynchronous control, and it overrides all other controls when it is at a logic "0".

Clear*: This is a control pin that is synchronized with the clock. If CLEAR* is pulled low, then the input latches will be set to zero when the clock goes high. When the clock then goes low, the zeros are transferred to the output latches and this sets the DAC output current to zero. This line must be kept low to override data, but SET* will override CLEAR*.

INVERT: Complements bits B1 – B8 if pulled high (Logic 1).

SADJ, CADJ, and BADJ: Current can be injected (or removed) from these pins to add (subtract) from the set values of current for comp. sync (40 1/2 IRE) blank (7 1/2 IRE) and 10% bright (10 IRE). This allows adjustments of these current sources about their nominal set value (not available on the USC1852).

CLOCK: Loads data from B1 through B8 into the input latch while clock is high (Logic 1). Transfers data to output latch on falling edge of clock.

B1 – B8: These are the input data lines. B1 is the LSB and B8 is the MSB.

BIAS: Sets the current for the current sources. This line is driven by an internal amplifier. It can also be easily driven by an external source if desired. This line should be bypassed to VDD with a 0.01uF capacitor.

+1.2V: This line is held at a nominal voltage of +1.23V. A resistor is usually connected from it to ground to set up the full scale current of the DAC.

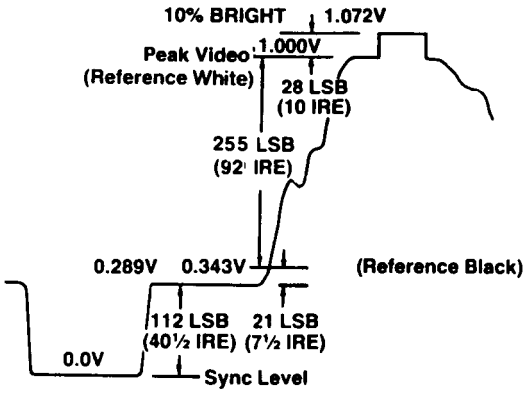


FIG. 1 A COMPOSITE VIDEO OUTPUT

Figure 1 shows the amplitudes of various parts of a video signal. These are expressed in volts, LSBs, and IRE units. Full scale signal (peak video) is nominally +1.00V which is equivalent to 140 IRE units (by definition). There are 416 current sources in the USC1850, and each represents 1 LSB. The active video is represented by 255 LSBs (8 bit DAC) which also represents 92 IRE units or .657V. The 10% bright signal is an optional feature, and it isn't necessary for normal video. It adds an extra 28 LSBs (10 IRE or 72mV) to the output signal.

A typical video application is shown in Figure 2 (Fig. 2A is 24 pin USC1850 ; Fig. 2B is 20 pin USC1852). The components marked with an asterisk are used to adjust the values of composite sync, composite blank, and 10% bright currents. Normally, these components aren't used since the composite video signals have been preset to their nominal values. The output load is a 75 ohm resistor. If this connects to a 75 ohm terminated cable, then the actual output load is 37.5 ohms, and, to achieve a 1.0V output, the resistors connected to the +1.2V reference pin should be half the values shown.

The BIAS Pin should be bypassed to V_{DD} as shown. V_{DD} should be bypassed to ground. The INVERT line is normally grounded. It is pulled high only if the input data is in complement form (logic 1 < 0.8V, logic 0 > 2.0V).

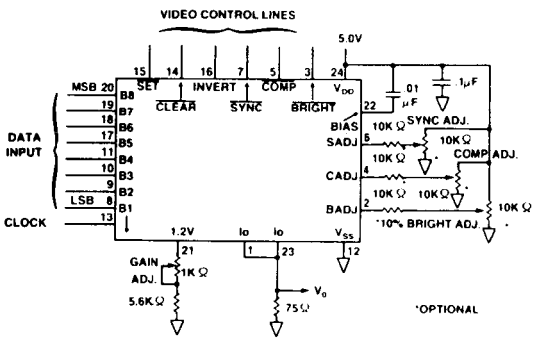


FIG. 2A TYPICAL USC1850 VIDEO APPLICATION

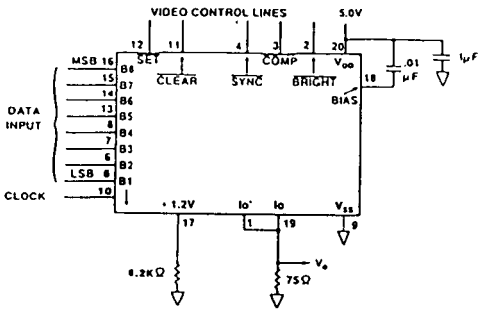


FIG. 2B TYPICAL USC1852 VIDEO APPLICATION

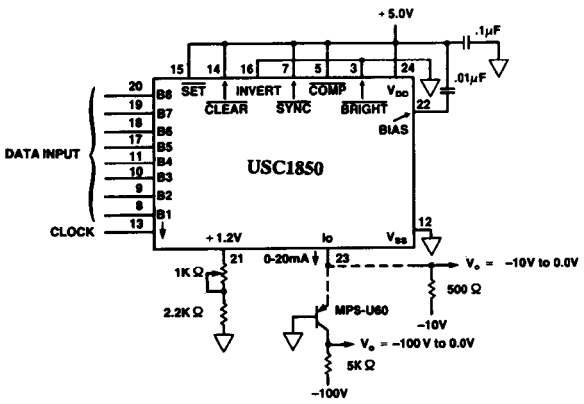


FIG. 3 NON-VIDEO APPLICATION (10V or100V)

Figure 3 shows the USC1850 used as an 8 bit DAC in a non-video application. By pulling SYNC* and COMP* high, BRIGHT* low, and leaving Io' unconnected (floating), the current consumption of the USC1850 is reduced since the composite sync, composite blank, and 10% bright currents are shut off. The output current, Io, can drive a 50 ohm resistor connected to ground to give a 0 to 1.0V output, or one can tie a 500 ohm resistor to –10V to get a 10V swing. For high voltage outputs, one can add a transistor and resistor as shown, as an easy way to get a 100V swing.

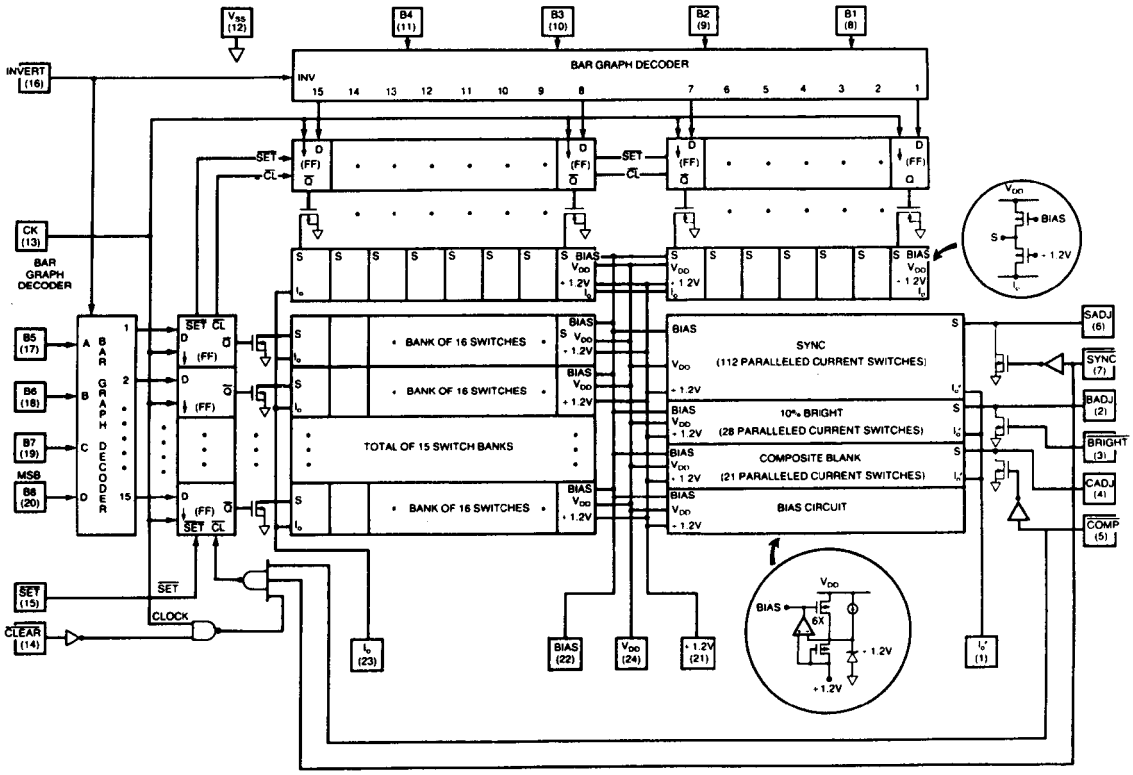
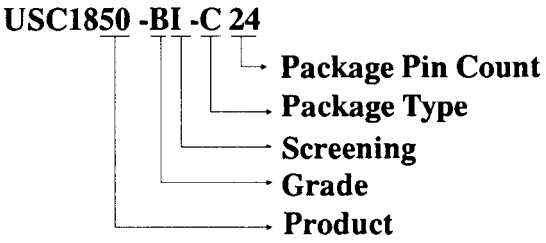


FIG. 4 USC1850 VIDEO

ORDERING INFORMATION



USC1850		USC1852	
CERDIP		CERDIP	
USC1850–BI–C24	+/– 1 LSB	USC1852–BI–C20	+/– 1 LSB
USC1850–CI–C24	+/– 2 LSB	USC1852–CI–C20	+/– 2 LSB
USC1850–DI–C24	+/– 3 LSB	USC1852–BM–C20	+/– 1 LSB
USC1850–EI–C24	+/– 6 LSB	USC1852–CM–C20	+/– 2 LSB
USC1850–BM–C24	+/– 1 LSB	USC1852–BX–C20	+/– 1 LSB
USC1850–CM–C24	+/– 2 LSB	USC1852–CX–C20	+/– 2 LSB
USC1850–BX–C24	+/– 1 LSB	PLASTIC DIP	
USC1850–CX–C24	+/– 2 LSB	USC1852–BI–P20	+/– 1 LSB
LEADLESS CHIP CARRIER		USC1852–CI–P20	+/– 2 LSB
USC1850–AM–L24	+/– 1/2 LSB	USC1852–DI–P20	+/– 3 LSB
USC1850–BM–L24	+/– 1 LSB	USC1852–EI–P20	+/– 6 LSB
USC1850–AX–L24	+/– 1/2 LSB	SOIC	
USC1850–BX–L24	+/– 1 LSB	USC1852–BI–Z20	+/– 1 LSB
DIE		USC1852–CI–Z20	+/– 2 LSB
USC1850–BI–DIE	+/– 1 LSB	USC1852–DI–Z20	+/– 3 LSB
USC1850–CI–DIE	+/– 2 LSB	USC1852–EI–Z20	+/– 6 LSB

SCREENING:

I = INDUSTRIAL TEMP RANGE (–25°C to +85°C)

M = MILITARY TEMP RANGE (–55°C to +125°C)