ON-SCREEN TUNING SCALE AND BAND DISPLAY

- DIGITAL TUNING BAR DISPLAY WITH MINIMUM EXTERNAL PRESETS
- ON-SCREEN DISPLAY OF THE BAND
- VERTICAL POSITION ON THE SCREEN EXTERNALLY ADJUSTABLE
- AUTOMATIC DISPLAY AT SEARCH COMMAND
- DESIGNED FOR USE WITH THE M193 ELECTRONIC PROGRAM MEMORY
- M191: STANDARD VERSION
- M091: FOR AUTOMATIC SEARCH IN FRENCH STANDARD APPLICATIONS

The M091 and M191 are monolithic integrated circuits designed to display on the screen of the television receiver a variable length strip corresponding to the voltage applied to the varicap tuner.
A variable number of rectangles symbolizing the selected band can also be displayed.
The circuits operate in conjunction with the M193 (Electronic Program Memory), from which they take the voltage and band information in a digital serial mode.
The 7 most significant digits of voltage information coming from the M193 are digitally converted into a 64 step variable pulse width giving either positive and negative polarity outputs for easy and versatile interfacing.
The variable length strip is displayed over 11 lines of a half frame picture with nine vertical graduations of 31 lines.
The vertical position of the strip can be adjusted with an external potentiometer over the whole screen.
The 2 digits of band information determine the number of rectangles appearing on the screen under the tuning strip. The rectangles are displayed over 11 lines of a half frame picture.
Automatic display is provided when the Electronic Program Memory is in the Search Mode; display on manual command is also possible.
The M191 is the standard version. The M091 is alternatively for displaying the tuning voltage when the automatic search is made by scanning the band in a reverse way (i.e. from 30 to 0V) as is required by the French standard.
The M091 displays 30V (maximum length of the strip) when the M193 Electronic Program Memory transmits information corresponding to 0V. It displays 0V when the M193 transmits information corresponding to 30V.
It displays 0V when the M193 transmits information corresponding to 30V.
The M091 and M191 are constructed in N-channel silicon gate technology and are available in a 16 pin dual in-line plastic package.

ABSOLUTE MAXIMUM RATINGS*

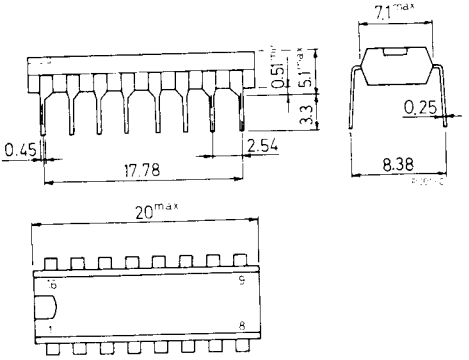
V_{DD} **	Supply voltage	-0.3 to 20	V
V_I	Input voltage	-0.3 to 20	V
I_I	Input current	-5	mA
$V_{O(off)}$	Off-state output voltage	20	V
I_O	Output current (except pins 12-13)	5	mA
	(pins 12-13)	15	mA
P_{tot}	Total package power dissipation	500	mW
T_{stg}	Storage temperature	-65 to 150	°C
T_{op}	Operating temperature	0 to 70	°C

* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

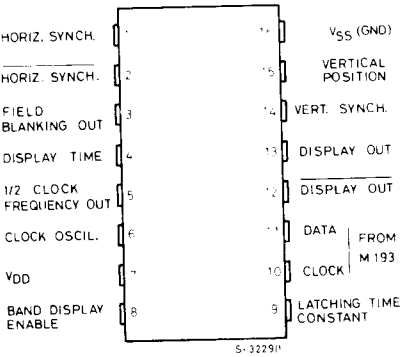
** All voltages are with respect to V_{SS} (GND).

ORDERING NUMBERS: M191 B1
M091 B1

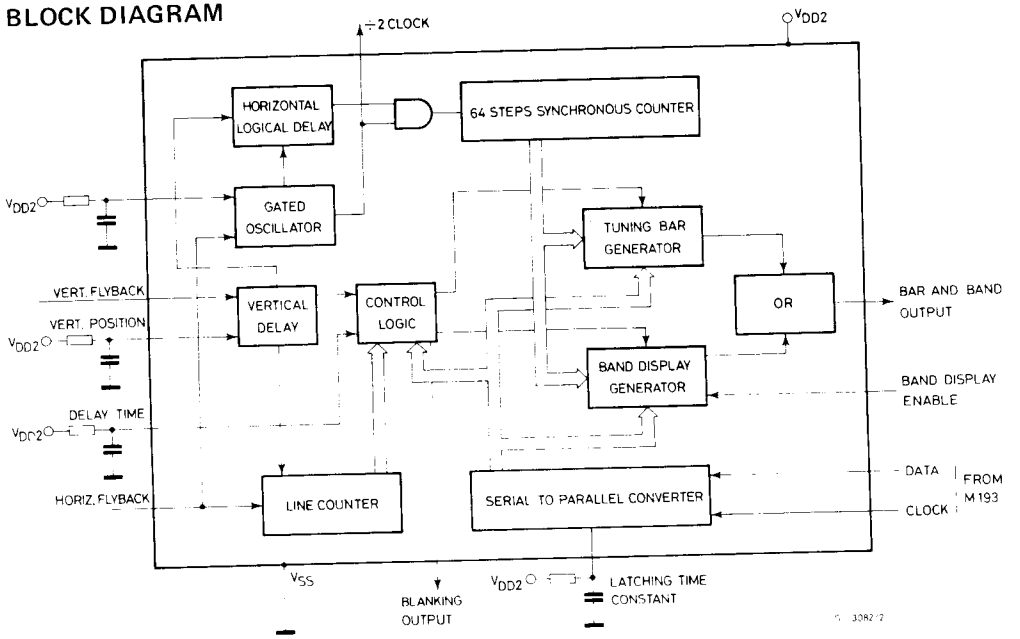
MECHANICAL DATA (dimensions in mm)



PIN CONNECTIONS



BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS

	Parameter	Min.	Typ.	Max.	
V_{DD}	Supply voltage	11.5	13	14.5	V
V_I	Input voltage			14.5	V
$V_{O\,(off)}$	Off-state output voltage			14.5	V
I_O	Output current - all pins except 4-6-12-13*			1	mA
	- pin 6			3	mA
	- pins 12-13			10	mA
f	Clock frequency		1.8	2.2	MHz
T_{op}	Operating temperature	0		70	°C
P_{tot}	Total package power dissipation			500	mW
C_9	Capacitance at pin 9		330	390	pF
C_6	Capacitance at pin 6		68	100	pF
C_{15}	Capacitance at pin 15		270	330	nF
C_4	Capacitance at pin 4**		10	12	μF
$R_{4,15}$	Resistance at pins 4-15		220	270	KΩ

* I_{O4} The output current of pin 4 is internally limited.
** C_4 Values up to 100 μF are allowed using a 1KΩ resistor in series with pin 4.

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions).

Typical values are at T_{amb} = 25°C, V_{DD} = 13V.

	Parameter	Test conditions	Pins	Values			Unit
				Min.	Typ.	Max.	
V_{IL}	Low level input voltage	V_{DD} = 11.5 to 14.5V	1-2-10-11-14			0.8	V
V_{IH}	High level input voltage	V_{DD} = 11.5 to 14.5V	1-2-10-11-14	3.5			V
V_{OL}	Low level output voltage	V_{DD} = 11.5V, I_{OL} = 10 mA	12-13			1	V
		V_{DD} = 11.5V, I_{OL} = 1 mA	3			1	V
V_T	Threshold voltage	V_{DD} = 11.5 to 14.5V	6-9-15		4		V
			4-8		2		
I_I	Input current	V_I = 14.5V				10	μA
$I_{O\,(off)}$	Off-state output current	V_{DD} = 14.5V	3-4-5-9-15			20	μA
			12-13			100	
I_{DD}	Supply current	V_{DD} = 14.5V				25	mA

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C)

Parameter		Test conditions	Values			Unit
			Min.	Typ.	Max.	
t_{TLH}, t_{THL}	Transition time	Pins 12-13 See fig. 3		80		ns
t_D	Delay time			50		ns

TYPICAL APPLICATION

Fig. 1

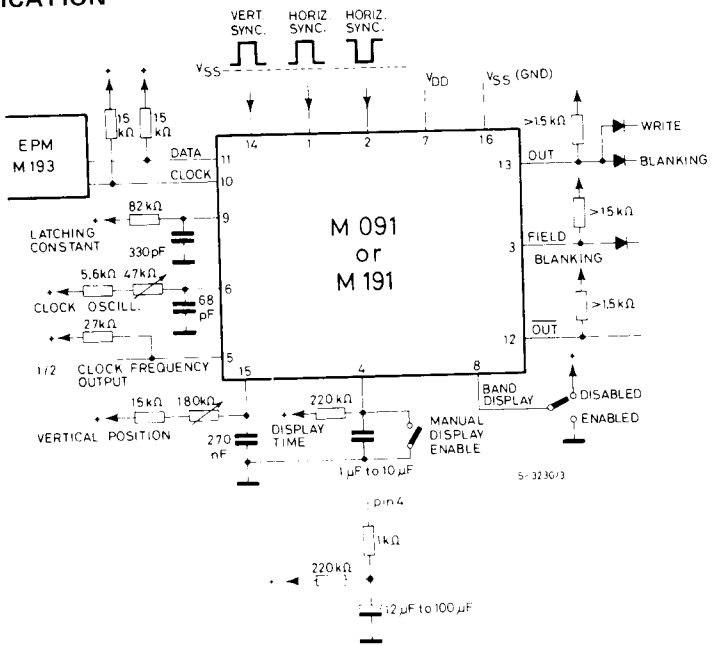
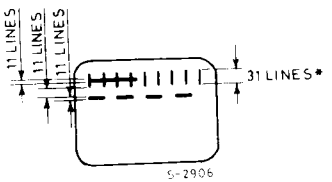
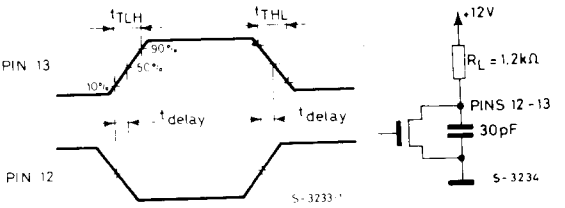


Fig. 2



* THE LINES CORRESPOND TO A HALF FRAME

Fig. 3

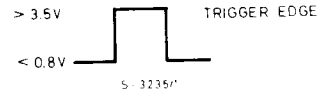


DESCRIPTION

Pins 1, 2 - Horizontal synchronization

Two Horizontal sync inputs are provided to allow for positive or negative pulses from the TV receiver.
Pin 1 is designed to accept a positive pulse derived from the line flyback through an interface.
The circuit is triggered on the negative edge of the incoming pulse.

Fig. 4 - Pin 1



The negative flyback pulses must be applied to pin 2. In this case the circuit is triggered on the positive edge of the pulse.

Fig. 5 - Pin 2

The display is delayed for a time corresponding to 32 clock periods after the triggering.
With a clock frequency of 1.8 MHz the delay is 9 μsec.
When pin 1 is used, pin 2 must be connected to V_{SS} (GND); when using pin 2, pin 1 must be at V_{DD}.

Pin 3 - Field blanking output

An open drain transistor is disabled during the lines which correspond to the display of the tuning scale and band information. This makes it possible to write the tuning scale and the band identification rectangles on a dark or alternative colour area. The signal is present for the full line period.

Pin 4 - Display time input

The display is automatically enabled when the M193 (Electronic Program Memory) is in the Search mode.
The RC network applied to pin 4 determines the time the display will last after a station is found.
When identification occurs the capacitor is unclamped and allowed to be charged by the external resistor.
The display is disabled when an internal threshold is reached.
The display is also enabled if the capacitor is discharged by connecting this pin to V_{SS} (GND) with an external clamp.
If a capacitor $> 10\ \mu F$ is used a 1 KΩ resistor must be placed in series with pin 4.

Pin 5 - 1/2 frequency clock output

The clock frequency divided by two is present on this pin for measurement purposes. To allow this, connect temporarily pin 1 to V_{SS} and pin 2 to V_{DD}. The output is open drain and an external pull-up resistor is needed.
If the output is not used it must be connected to V_{SS}.

DESCRIPTION (continued)

Pin 6 - Clock oscillator input

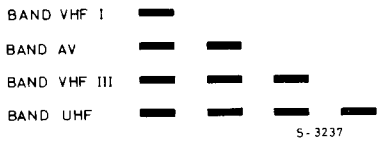
This pin is connected to a RC network as shown in fig. 1.
The clock frequency determines the horizontal width on the screen of the tuning scale, of the rectangles and the distance of the display from the left edge of the screen.
Fine adjustment of the clock frequency is obtained by the trimming resistor. Typical clock frequency is 1.8 MHz.

Pin 7 - V_{DD}

Pin 8 - Band display enable

When this pin is connected to V_{SS} (GND) a band display with the following format is enabled, on command, together with the tuning voltage display.

Fig. 6

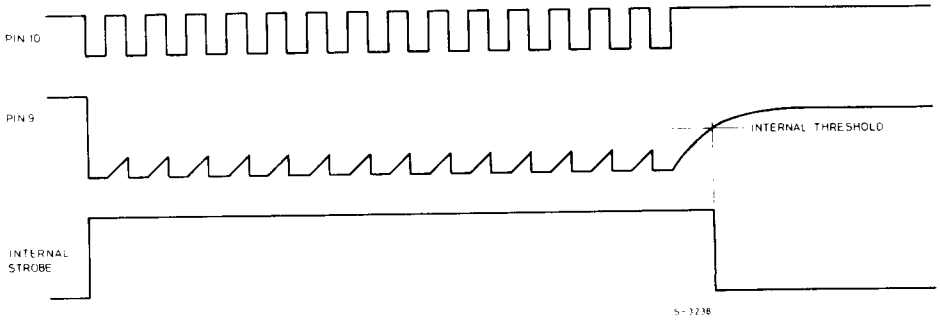


If this pin is connected to V_{DD} only the tuning voltage will be displayed.

Pin 9 - Latching time constant

An RC time constant must be applied to this pin to generate the internal latching signal.
The content of the internal shift register is transferred to the internal decoding circuit only at the end of the clock burst to avoid noise on the display during data transfer.
This is made by integrating the incoming clock burst with the RC time constant connected to pin 9 as shown in fig. 7.

Fig. 7

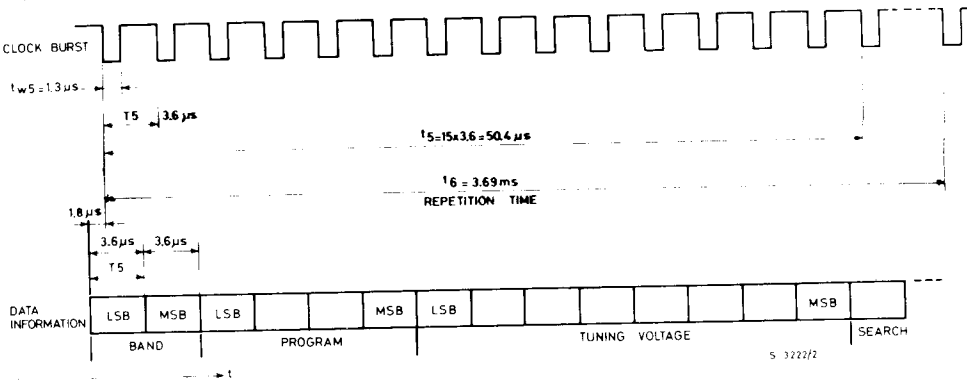


DESCRIPTION (continued)

Pin 10 - Clock input

This pin accepts the burst containing the 15 clock pulses available from the M193. The burst is used to load the serial Data on pin 11 into the internal 15 bit shift register (see fig. 8).

Fig. 8



Pin 11 - Data input

This pin accepts the 15 bit serial Data information available from the M193 EPM.
The burst contains 2 bits for band information, 4 bits for program, 8 bits for tuning voltage and 1 bit which indicates if the system is in the Search mode.

Pin 12 - Inverted video signal output

The signals of pin 13 are inverted and presented on this pin to allow easy interfacing in some chroma kits. The output is open drain.

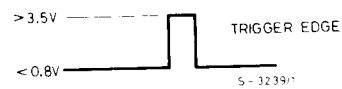
Pin 13 - Video signal output

The tuning scale and band information video signal is available on this pin, a load resistor is connected between the open drain output transistor and V_{DD}. White level corresponds to disable of the internal transistor.

Pin 14 - Vertical synchronization

The frame flyback pulse must be applied to this pin by means of an interface. The signal must be positive. The circuit is triggered by the negative edge of the pulse.

Fig. 9



DESCRIPTION (continued)

Pin 15 - Vertical position input

An internal monostable is triggered by the frame pulse applied on pin 14.
The display is allowed at the end of the cycle of the monostable. The RC network applied to this pin gives the time constant of the monostable determining the position of the display on the screen.

Pin 16 - V_{SS} (GND)

All voltages quoted are referred to Pin 16.