

1. INTRODUCTION

The ST7636R is a driver & controller LSI for 65K color graphic dot-matrix liquid crystal display systems. It generates 396 Segment and 132 Common driver circuits. This chip is connected directly to a microprocessor, accepts Serial Peripheral Interface (SPI) or 8-bit/16-bit parallel display data and stores in an on-chip display data RAM. It performs display data RAM read/write operation with no external operating clock to minimize power consumption. In addition, because it contains power supply circuits necessary to drive liquid crystal, it is possible to make a display system with the fewest components.

2. FEATURES

Driver Output Circuits

- ◆ 396 segment outputs / 132 common outputs

Applicable Duty Ratios

- ◆ Various partial display
- ◆ Partial window moving & data scrolling

Gray-Scale Display

- ◆ 4FRC & 31 PWM function circuit to display
- ◆ 64 gray-scale display.

On-chip Display Data RAM

- ◆ Capacity: 132 x 132 x 16 =278,784bits
- ◆ 4K colors (RGB)=(444) mode
- ◆ 65K colors (RGB)=(565) mode
- ◆ Truncated 262K colors (RGB)=(666) mode
- ◆ Truncated 16M colors (RGB)=(888) mode

Microprocessor Interface

- ◆ 8/16-bit parallel bi-directional interface with 6800-series or 8080-series
- ◆ 4-line serial interface (4-line-SIF)
- ◆ 3-line serial interface (3-line-SIF)

On-chip Low Power Analog Circuit

- ◆ On-chip oscillator circuit
- ◆ Voltage converter (x2, x3, x4, x5, x6, x7, x8)

- ◆ Voltage regulator (temperature gradient -0.15%/)
- ◆ On-chip electronic contrast control function (406 steps)
- ◆ Voltage follower (LCD bias: 1/5 to 1/12)

Operating Voltage Range

- ◆ Supply voltage (VDD, VDD1): 1.8 to 3.3V
(VDD2, VDD3, VDD4, VDD5): 2.4 to 3.3V
- ◆ LCD driving voltage (VOP = V0 - VSS): 3.76 to 18.0 V
- ◆ The suggested value of V0 is 12~15 V under bias =1/11 or 1/12

LCD Driving Voltage (EEPROM)

- ◆ To store contrast adjustment value for better display
- ◆ To store adjustment value for best crosstalk performance


EEPROM Adjustment Voltage

- ◆ When writing value to EEPROM, VDD2~VDD5 must follow as:
When Booster x6: VDD2~VDD5 =3.3V
When Booster x7: VDD2~VDD5 =2.8V~3.0V
and Booster:ON, Regulator: OFF, Follower: OFF, Display OFF (refer EEPROM flow, page.43 , page.105)

Package Type

- ◆ Application for COG

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ST7636R	6800 , 8080 ,4-Line , 3-Line interface	
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4. Pad Center Coordinates

PAD No.	PIN Name		X	Y
	CSEL=0	CSEL=1		
001	COM[44]	COM[88]	7227.3	598.0
002	COM[45]	COM[90]	7196.3	598.0
003	COM[46]	COM[92]	7165.3	598.0
004	COM[47]	COM[94]	7134.3	598.0
005	COM[48]	COM[96]	7103.3	598.0
006	COM[49]	COM[98]	7072.3	598.0
007	COM[50]	COM[100]	7041.3	598.0
008	COM[51]	COM[102]	7010.3	598.0
009	COM[52]	COM[104]	6979.3	598.0
010	COM[53]	COM[106]	6948.3	598.0
011	COM[54]	COM[108]	6917.3	598.0
012	COM[55]	COM[110]	6886.3	598.0
013	COM[56]	COM[112]	6855.3	598.0
014	COM[57]	COM[114]	6824.3	598.0
015	COM[58]	COM[116]	6793.3	598.0
016	COM[59]	COM[118]	6762.3	598.0
017	COM[60]	COM[120]	6731.3	598.0
018	COM[61]	COM[122]	6700.3	598.0
019	COM[62]	COM[124]	6669.3	598.0
020	COM[63]	COM[126]	6638.3	598.0
021	COM[64]	COM[128]	6607.3	598.0
022	COM[65]	COM[130]	6576.3	598.0
023	SEG[395]		6122.5	598.0
024	SEG[394]		6091.5	598.0
025	SEG[393]		6060.5	598.0
026	SEG[392]		6029.5	598.0
027	SEG[391]		5998.5	598.0
028	SEG[390]		5967.5	598.0
029	SEG[389]		5936.5	598.0
030	SEG[388]		5905.5	598.0
031	SEG[387]		5874.5	598.0
032	SEG[386]		5843.5	598.0
033	SEG[385]		5812.5	598.0
034	SEG[384]		5781.5	598.0

PAD No.	PIN Name		X	Y
	CSEL=0	CSEL=1		
035	SEG[383]		5750.5	598.0
036	SEG[382]		5719.5	598.0
037	SEG[381]		5688.5	598.0
038	SEG[380]		5657.5	598.0
039	SEG[379]		5626.5	598.0
040	SEG[378]		5595.5	598.0
041	SEG[377]		5564.5	598.0
042	SEG[376]		5533.5	598.0
043	SEG[375]		5502.5	598.0
044	SEG[374]		5471.5	598.0
045	SEG[373]		5440.5	598.0
046	SEG[372]		5409.5	598.0
047	SEG[371]		5378.5	598.0
048	SEG[370]		5347.5	598.0
049	SEG[369]		5316.5	598.0
050	SEG[368]		5285.5	598.0
051	SEG[367]		5254.5	598.0
052	SEG[366]		5223.5	598.0
053	SEG[365]		5192.5	598.0
054	SEG[364]		5161.5	598.0
055	SEG[363]		5130.5	598.0
056	SEG[362]		5099.5	598.0
057	SEG[361]		5068.5	598.0
058	SEG[360]		5037.5	598.0
059	SEG[359]		5006.5	598.0
060	SEG[358]		4975.5	598.0
061	SEG[357]		4944.5	598.0
062	SEG[356]		4913.5	598.0
063	SEG[355]		4882.5	598.0
064	SEG[354]		4851.5	598.0
065	SEG[353]		4820.5	598.0
066	SEG[352]		4789.5	598.0
067	SEG[351]		4758.5	598.0
068	SEG[350]		4727.5	598.0

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PAD No.	PIN Name		X	Y	PAD No.	PIN Name		X	Y
	CSEL=0	CSEL=1				CSEL=0	CSEL=1		
069	SEG[349]		4696.5	598.0	104	SEG[314]		3611.5	598.0
070	SEG[348]		4665.5	598.0	105	SEG[313]		3580.5	598.0
071	SEG[347]		4634.5	598.0	106	SEG[312]		3549.5	598.0
072	SEG[346]		4603.5	598.0	107	SEG[311]		3518.5	598.0
073	SEG[345]		4572.5	598.0	108	SEG[310]		3487.5	598.0
074	SEG[344]		4541.5	598.0	109	SEG[309]		3456.5	598.0
075	SEG[343]		4510.5	598.0	110	SEG[308]		3425.5	598.0
076	SEG[342]		4479.5	598.0	111	SEG[307]		3394.5	598.0
077	SEG[341]		4448.5	598.0	112	SEG[306]		3363.5	598.0
078	SEG[340]		4417.5	598.0	113	SEG[305]		3332.5	598.0
079	SEG[339]		4386.5	598.0	114	SEG[304]		3301.5	598.0
080	SEG[338]		4355.5	598.0	115	SEG[303]		3270.5	598.0
081	SEG[337]		4324.5	598.0	116	SEG[302]		3239.5	598.0
082	SEG[336]		4293.5	598.0	117	SEG[301]		3208.5	598.0
083	SEG[335]		4262.5	598.0	118	SEG[300]		3177.5	598.0
084	SEG[334]		4231.5	598.0	119	SEG[299]		3146.5	598.0
085	SEG[333]		4200.5	598.0	120	SEG[298]		3115.5	598.0
086	SEG[332]		4169.5	598.0	121	SEG[297]		3084.5	598.0
087	SEG[331]		4138.5	598.0	122	SEG[296]		3053.5	598.0
088	SEG[330]		4107.5	598.0	123	SEG[295]		3022.5	598.0
089	SEG[329]		4076.5	598.0	124	SEG[294]		2991.5	598.0
090	SEG[328]		4045.5	598.0	125	SEG[293]		2960.5	598.0
091	SEG[327]		4014.5	598.0	126	SEG[292]		2929.5	598.0
092	SEG[326]		3983.5	598.0	127	SEG[291]		2898.5	598.0
093	SEG[325]		3952.5	598.0	128	SEG[290]		2867.5	598.0
094	SEG[324]		3921.5	598.0	129	SEG[289]		2836.5	598.0
095	SEG[323]		3890.5	598.0	130	SEG[288]		2805.5	598.0
096	SEG[322]		3859.5	598.0	131	SEG[287]		2774.5	598.0
097	SEG[321]		3828.5	598.0	132	SEG[286]		2743.5	598.0
098	SEG[320]		3797.5	598.0	133	SEG[285]		2712.5	598.0
099	SEG[319]		3766.5	598.0	134	SEG[284]		2681.5	598.0
100	SEG[318]		3735.5	598.0	135	SEG[283]		2650.5	598.0
101	SEG[317]		3704.5	598.0	136	SEG[282]		2619.5	598.0
102	SEG[316]		3673.5	598.0	137	SEG[281]		2588.5	598.0
103	SEG[315]		3642.5	598.0	138	SEG[280]		2557.5	598.0

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PAD No.	PIN Name		X	Y	PAD No.	PIN Name		X	Y
	CSEL=0	CSEL=1				CSEL=0	CSEL=1		
139	SEG[279]		2526.5	598.0	174	SEG[244]		1441.5	598.0
140	SEG[278]		2495.5	598.0	175	SEG[243]		1410.5	598.0
141	SEG[277]		2464.5	598.0	176	SEG[242]		1379.5	598.0
142	SEG[276]		2433.5	598.0	177	SEG[241]		1348.5	598.0
143	SEG[275]		2402.5	598.0	178	SEG[240]		1317.5	598.0
144	SEG[274]		2371.5	598.0	179	SEG[239]		1286.5	598.0
145	SEG[273]		2340.5	598.0	180	SEG[238]		1255.5	598.0
146	SEG[272]		2309.5	598.0	181	SEG[237]		1224.5	598.0
147	SEG[271]		2278.5	598.0	182	SEG[236]		1193.5	598.0
148	SEG[270]		2247.5	598.0	183	SEG[235]		1162.5	598.0
149	SEG[269]		2216.5	598.0	184	SEG[234]		1131.5	598.0
150	SEG[268]		2185.5	598.0	185	SEG[233]		1100.5	598.0
151	SEG[267]		2154.5	598.0	186	SEG[232]		1069.5	598.0
152	SEG[266]		2123.5	598.0	187	SEG[231]		1038.5	598.0
153	SEG[265]		2092.5	598.0	188	SEG[230]		1007.5	598.0
154	SEG[264]		2061.5	598.0	189	SEG[229]		976.5	598.0
155	SEG[263]		2030.5	598.0	190	SEG[228]		945.5	598.0
156	SEG[262]		1999.5	598.0	191	SEG[227]		914.5	598.0
157	SEG[261]		1968.5	598.0	192	SEG[226]		883.5	598.0
158	SEG[260]		1937.5	598.0	193	SEG[225]		852.5	598.0
159	SEG[259]		1906.5	598.0	194	SEG[224]		821.5	598.0
160	SEG[258]		1875.5	598.0	195	SEG[223]		790.5	598.0
161	SEG[257]		1844.5	598.0	196	SEG[222]		759.5	598.0
162	SEG[256]		1813.5	598.0	197	SEG[221]		728.5	598.0
163	SEG[255]		1782.5	598.0	198	SEG[220]		697.5	598.0
164	SEG[254]		1751.5	598.0	199	SEG[219]		666.5	598.0
165	SEG[253]		1720.5	598.0	200	SEG[218]		635.5	598.0
166	SEG[252]		1689.5	598.0	201	SEG[217]		604.5	598.0
167	SEG[251]		1658.5	598.0	202	SEG[216]		573.5	598.0
168	SEG[250]		1627.5	598.0	203	SEG[215]		542.5	598.0
169	SEG[249]		1596.5	598.0	204	SEG[214]		511.5	598.0
170	SEG[248]		1565.5	598.0	205	SEG[213]		480.5	598.0
171	SEG[247]		1534.5	598.0	206	SEG[212]		449.5	598.0
172	SEG[246]		1503.5	598.0	207	SEG[211]		418.5	598.0
173	SEG[245]		1472.5	598.0	208	SEG[210]		387.5	598.0

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PAD No.	PIN Name		X	Y	PAD No.	PIN Name		X	Y
	CSEL=0	CSEL=1				CSEL=0	CSEL=1		
209	SEG[209]		356.5	598.0	244	SEG[174]		-728.5	598.0
210	SEG[208]		325.5	598.0	245	SEG[173]		-759.5	598.0
211	SEG[207]		294.5	598.0	246	SEG[172]		-790.5	598.0
212	SEG[206]		263.5	598.0	247	SEG[171]		-821.5	598.0
213	SEG[205]		232.5	598.0	248	SEG[170]		-852.5	598.0
214	SEG[204]		201.5	598.0	249	SEG[169]		-883.5	598.0
215	SEG[203]		170.5	598.0	250	SEG[168]		-914.5	598.0
216	SEG[202]		139.5	598.0	251	SEG[167]		-945.5	598.0
217	SEG[201]		108.5	598.0	252	SEG[166]		-976.5	598.0
218	SEG[200]		77.5	598.0	253	SEG[165]		-1007.5	598.0
219	SEG[199]		46.5	598.0	254	SEG[164]		-1038.5	598.0
220	SEG[198]		15.5	598.0	255	SEG[163]		-1069.5	598.0
221	SEG[197]		-15.5	598.0	256	SEG[162]		-1100.5	598.0
222	SEG[196]		-46.5	598.0	257	SEG[161]		-1131.5	598.0
223	SEG[195]		-77.5	598.0	258	SEG[160]		-1162.5	598.0
224	SEG[194]		-108.5	598.0	259	SEG[159]		-1193.5	598.0
225	SEG[193]		-139.5	598.0	260	SEG[158]		-1224.5	598.0
226	SEG[192]		-170.5	598.0	261	SEG[157]		-1255.5	598.0
227	SEG[191]		-201.5	598.0	262	SEG[156]		-1286.5	598.0
228	SEG[190]		-232.5	598.0	263	SEG[155]		-1317.5	598.0
229	SEG[189]		-263.5	598.0	264	SEG[154]		-1348.5	598.0
230	SEG[188]		-294.5	598.0	265	SEG[153]		-1379.5	598.0
231	SEG[187]		-325.5	598.0	266	SEG[152]		-1410.5	598.0
232	SEG[186]		-356.5	598.0	267	SEG[151]		-1441.5	598.0
233	SEG[185]		-387.5	598.0	268	SEG[150]		-1472.5	598.0
234	SEG[184]		-418.5	598.0	269	SEG[149]		-1503.5	598.0
235	SEG[183]		-449.5	598.0	270	SEG[148]		-1534.5	598.0
236	SEG[182]		-480.5	598.0	271	SEG[147]		-1565.5	598.0
237	SEG[181]		-511.5	598.0	272	SEG[146]		-1596.5	598.0
238	SEG[180]		-542.5	598.0	273	SEG[145]		-1627.5	598.0
239	SEG[179]		-573.5	598.0	274	SEG[144]		-1658.5	598.0
240	SEG[178]		-604.5	598.0	275	SEG[143]		-1689.5	598.0
241	SEG[177]		-635.5	598.0	276	SEG[142]		-1720.5	598.0
242	SEG[176]		-666.5	598.0	277	SEG[141]		-1751.5	598.0
243	SEG[175]		-697.5	598.0	278	SEG[140]		-1782.5	598.0

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PAD No.	PIN Name		X	Y	PAD No.	PIN Name		X	Y
	CSEL=0	CSEL=1				CSEL=0	CSEL=1		
279	SEG[139]		-1813.5	598.0	314	SEG[104]		-2898.5	598.0
280	SEG[138]		-1844.5	598.0	315	SEG[103]		-2929.5	598.0
281	SEG[137]		-1875.5	598.0	316	SEG[102]		-2960.5	598.0
282	SEG[136]		-1906.5	598.0	317	SEG[101]		-2991.5	598.0
283	SEG[135]		-1937.5	598.0	318	SEG[100]		-3022.5	598.0
284	SEG[134]		-1968.5	598.0	319	SEG[99]		-3053.5	598.0
285	SEG[133]		-1999.5	598.0	320	SEG[98]		-3084.5	598.0
286	SEG[132]		-2030.5	598.0	321	SEG[97]		-3115.5	598.0
287	SEG[131]		-2061.5	598.0	322	SEG[96]		-3146.5	598.0
288	SEG[130]		-2092.5	598.0	323	SEG[95]		-3177.5	598.0
289	SEG[129]		-2123.5	598.0	324	SEG[94]		-3208.5	598.0
290	SEG[128]		-2154.5	598.0	325	SEG[93]		-3239.5	598.0
291	SEG[127]		-2185.5	598.0	326	SEG[92]		-3270.5	598.0
292	SEG[126]		-2216.5	598.0	327	SEG[91]		-3301.5	598.0
293	SEG[125]		-2247.5	598.0	328	SEG[90]		-3332.5	598.0
294	SEG[124]		-2278.5	598.0	329	SEG[89]		-3363.5	598.0
295	SEG[123]		-2309.5	598.0	330	SEG[88]		-3394.5	598.0
296	SEG[122]		-2340.5	598.0	331	SEG[87]		-3425.5	598.0
297	SEG[121]		-2371.5	598.0	332	SEG[86]		-3456.5	598.0
298	SEG[120]		-2402.5	598.0	333	SEG[85]		-3487.5	598.0
299	SEG[119]		-2433.5	598.0	334	SEG[84]		-3518.5	598.0
300	SEG[118]		-2464.5	598.0	335	SEG[83]		-3549.5	598.0
301	SEG[117]		-2495.5	598.0	336	SEG[82]		-3580.5	598.0
302	SEG[116]		-2526.5	598.0	337	SEG[81]		-3611.5	598.0
303	SEG[115]		-2557.5	598.0	338	SEG[80]		-3642.5	598.0
304	SEG[114]		-2588.5	598.0	339	SEG[79]		-3673.5	598.0
305	SEG[113]		-2619.5	598.0	340	SEG[78]		-3704.5	598.0
306	SEG[112]		-2650.5	598.0	341	SEG[77]		-3735.5	598.0
307	SEG[111]		-2681.5	598.0	342	SEG[76]		-3766.5	598.0
308	SEG[110]		-2712.5	598.0	343	SEG[75]		-3797.5	598.0
309	SEG[109]		-2743.5	598.0	344	SEG[74]		-3828.5	598.0
310	SEG[108]		-2774.5	598.0	345	SEG[73]		-3859.5	598.0
311	SEG[107]		-2805.5	598.0	346	SEG[72]		-3890.5	598.0
312	SEG[106]		-2836.5	598.0	347	SEG[71]		-3921.5	598.0
313	SEG[105]		-2867.5	598.0	348	SEG[70]		-3952.5	598.0

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PAD No.	PIN Name		X	Y	PAD No.	PIN Name		X	Y
	CSEL=0	CSEL=1				CSEL=0	CSEL=1		
349	SEG[69]		-3983.5	598.0	384	SEG[34]		-5068.5	598.0
350	SEG[68]		-4014.5	598.0	385	SEG[33]		-5099.5	598.0
351	SEG[67]		-4045.5	598.0	386	SEG[32]		-5130.5	598.0
352	SEG[66]		-4076.5	598.0	387	SEG[31]		-5161.5	598.0
353	SEG[65]		-4107.5	598.0	388	SEG[30]		-5192.5	598.0
354	SEG[64]		-4138.5	598.0	389	SEG[29]		-5223.5	598.0
355	SEG[63]		-4169.5	598.0	390	SEG[28]		-5254.5	598.0
356	SEG[62]		-4200.5	598.0	391	SEG[27]		-5285.5	598.0
357	SEG[61]		-4231.5	598.0	392	SEG[26]		-5316.5	598.0
358	SEG[60]		-4262.5	598.0	393	SEG[25]		-5347.5	598.0
359	SEG[59]		-4293.5	598.0	394	SEG[24]		-5378.5	598.0
360	SEG[58]		-4324.5	598.0	395	SEG[23]		-5409.5	598.0
361	SEG[57]		-4355.5	598.0	396	SEG[22]		-5440.5	598.0
362	SEG[56]		-4386.5	598.0	397	SEG[21]		-5471.5	598.0
363	SEG[55]		-4417.5	598.0	398	SEG[20]		-5502.5	598.0
364	SEG[54]		-4448.5	598.0	399	SEG[19]		-5533.5	598.0
365	SEG[53]		-4479.5	598.0	400	SEG[18]		-5564.5	598.0
366	SEG[52]		-4510.5	598.0	401	SEG[17]		-5595.5	598.0
367	SEG[51]		-4541.5	598.0	402	SEG[16]		-5626.5	598.0
368	SEG[50]		-4572.5	598.0	403	SEG[15]		-5657.5	598.0
369	SEG[49]		-4603.5	598.0	404	SEG[14]		-5688.5	598.0
370	SEG[48]		-4634.5	598.0	405	SEG[13]		-5719.5	598.0
371	SEG[47]		-4665.5	598.0	406	SEG[12]		-5750.5	598.0
372	SEG[46]		-4696.5	598.0	407	SEG[11]		-5781.5	598.0
373	SEG[45]		-4727.5	598.0	408	SEG[10]		-5812.5	598.0
374	SEG[44]		-4758.5	598.0	409	SEG[9]		-5843.5	598.0
375	SEG[43]		-4789.5	598.0	410	SEG[8]		-5874.5	598.0
376	SEG[42]		-4820.5	598.0	411	SEG[7]		-5905.5	598.0
377	SEG[41]		-4851.5	598.0	412	SEG[6]		-5936.5	598.0
378	SEG[40]		-4882.5	598.0	413	SEG[5]		-5967.5	598.0
379	SEG[39]		-4913.5	598.0	414	SEG[4]		-5998.5	598.0
380	SEG[38]		-4944.5	598.0	415	SEG[3]		-6029.5	598.0
381	SEG[37]		-4975.5	598.0	416	SEG[2]		-6060.5	598.0
382	SEG[36]		-5006.5	598.0	417	SEG[1]		-6091.5	598.0
383	SEG[35]		-5037.5	598.0	418	SEG[0]		-6122.5	598.0

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PAD No.	PIN Name		X	Y	PAD No.	PIN Name		X	Y
	CSEL=0	CSEL=1				CSEL=0	CSEL=1		
419	COM[66]	COM[131]	-6576.3	598.0	454	COM[101]	COM[61]	-7438.0	160.5
420	COM[67]	COM[129]	-6607.3	598.0	455	COM[102]	COM[59]	-7438.0	129.5
421	COM[68]	COM[127]	-6638.3	598.0	456	COM[103]	COM[57]	-7438.0	98.5
422	COM[69]	COM[125]	-6669.3	598.0	457	COM[104]	COM[55]	-7438.0	67.5
423	COM[70]	COM[123]	-6700.3	598.0	458	COM[105]	COM[53]	-7438.0	36.5
424	COM[71]	COM[121]	-6731.3	598.0	459	COM[106]	COM[51]	-7438.0	5.5
425	COM[72]	COM[119]	-6762.3	598.0	460	COM[107]	COM[49]	-7438.0	-25.5
426	COM[73]	COM[117]	-6793.3	598.0	461	COM[108]	COM[47]	-7438.0	-56.5
427	COM[74]	COM[115]	-6824.3	598.0	462	COM[109]	COM[45]	-7438.0	-87.5
428	COM[75]	COM[113]	-6855.3	598.0	463	COM[110]	COM[43]	-7438.0	-118.5
429	COM[76]	COM[111]	-6886.3	598.0	464	COM[111]	COM[41]	-7438.0	-149.5
430	COM[77]	COM[109]	-6917.3	598.0	465	COM[112]	COM[39]	-7438.0	-180.5
431	COM[78]	COM[107]	-6948.3	598.0	466	COM[113]	COM[37]	-7438.0	-211.5
432	COM[79]	COM[105]	-6979.3	598.0	467	COM[114]	COM[35]	-7438.0	-242.5
433	COM[80]	COM[103]	-7010.3	598.0	468	COM[115]	COM[33]	-7438.0	-273.5
434	COM[81]	COM[101]	-7041.3	598.0	469	COM[116]	COM[31]	-7438.0	-304.5
435	COM[82]	COM[99]	-7072.3	598.0	470	COM[117]	COM[29]	-7438.0	-335.5
436	COM[83]	COM[97]	-7103.3	598.0	471	COM[118]	COM[27]	-7438.0	-366.5
437	COM[84]	COM[95]	-7134.3	598.0	472	COM[119]	COM[25]	-7438.0	-397.5
438	COM[85]	COM[93]	-7165.3	598.0	473	COM[120]	COM[23]	-7438.0	-428.5
439	COM[86]	COM[91]	-7196.3	598.0	474	COM[121]	COM[21]	-7438.0	-459.5
440	COM[87]	COM[89]	-7227.3	598.0	475	COM[122]	COM[19]	-7438.0	-490.5
441	COM[88]	COM[87]	-7438.0	563.5	476	COM[123]	COM[17]	-7438.0	-521.5
442	COM[89]	COM[85]	-7438.0	532.5	477	COM[124]	COM[15]	-7438.0	-552.5
443	COM[90]	COM[83]	-7438.0	501.5	478	COM[125]	COM[13]	-7438.0	-583.5
444	COM[91]	COM[81]	-7438.0	470.5	479	COM[126]	COM[11]	-7227.3	-598.0
445	COM[92]	COM[79]	-7438.0	439.5	480	COM[127]	COM[9]	-7196.3	-598.0
446	COM[93]	COM[77]	-7438.0	408.5	481	COM[128]	COM[7]	-7165.3	-598.0
447	COM[94]	COM[75]	-7438.0	377.5	482	COM[129]	COM[5]	-7134.3	-598.0
448	COM[95]	COM[73]	-7438.0	346.5	483	COM[130]	COM[3]	-7103.3	-598.0
449	COM[96]	COM[71]	-7438.0	315.5	484	COM[131]	COM[1]	-7072.3	-598.0
450	COM[97]	COM[69]	-7438.0	284.5	485	VDD		-6100.1	-634.0
451	COM[98]	COM[67]	-7438.0	253.5	486	CL		-5990.1	-634.0
452	COM[99]	COM[65]	-7438.0	222.5	487	CLS		-5880.1	-634.0
453	COM[100]	COM[63]	-7438.0	191.5	488	VSS		-5770.1	-634.0

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PAD No.	PIN Name		X	Y	PAD No.	PIN Name		X	Y
	CSEL=0	CSEL=1				CSEL=0	CSEL=1		
489	VDD		-5660.1	-634.0	524	VDD		-1810.1	-634.0
490	A0		-5550.1	-634.0	525	SI		-1700.1	-634.0
491	RW_WR		-5440.1	-634.0	526	SCL		-1590.1	-634.0
492	VSS		-5330.1	-634.0	527	XCS		-1480.1	-634.0
493	VDD		-5220.1	-634.0	528	VDD		-1370.1	-634.0
494	D0		-5110.1	-634.0	529	VDD		-1260.1	-634.0
495	D1		-5000.1	-634.0	530	VDD		-1150.1	-634.0
496	D2		-4890.1	-634.0	531	VDD		-1040.1	-634.0
497	D3		-4780.1	-634.0	532	VDD1		-930.1	-634.0
498	D4		-4670.1	-634.0	533	VDD1		-820.1	-634.0
499	D5		-4560.1	-634.0	534	VSS1		-710.1	-634.0
500	D6		-4450.1	-634.0	535	VSS1		-600.1	-634.0
501	D7		-4340.1	-634.0	536	VSS		-490.1	-634.0
502	VSS		-4230.1	-634.0	537	VSS		-380.1	-634.0
503	VDD		-4120.1	-634.0	538	VSS		-270.1	-634.0
504	D8		-4010.1	-634.0	539	VSS		-160.1	-634.0
505	D9		-3900.1	-634.0	540	VSS		-50.1	-634.0
506	D10		-3790.1	-634.0	541	VSS		59.9	-634.0
507	D11		-3680.1	-634.0	542	VSS2		169.9	-634.0
508	D12		-3570.1	-634.0	543	VSS2		279.9	-634.0
509	D13		-3460.1	-634.0	544	VSS2		389.9	-634.0
510	D14		-3350.1	-634.0	545	VSS2		499.9	-634.0
511	D15		-3240.1	-634.0	546	VSS2		609.9	-634.0
512	VSS		-3130.1	-634.0	547	VSS2		719.9	-634.0
513	VDD		-3020.1	-634.0	548	VSS2		829.9	-634.0
514	E_RD		-2910.1	-634.0	549	VSS2		939.9	-634.0
515	RST		-2800.1	-634.0	550	VSS2		1049.9	-634.0
516	VSS		-2690.1	-634.0	551	VSS4		1159.9	-634.0
517	VDD		-2580.1	-634.0	552	VSS4		1269.9	-634.0
518	CSEL		-2470.1	-634.0	553	VDD4		1379.9	-634.0
519	INTRS		-2360.1	-634.0	554	VDD4		1489.9	-634.0
520	IF1		-2250.1	-634.0	555	VDD3		1599.9	-634.0
521	IF2		-2140.1	-634.0	556	VDD3		1709.9	-634.0
522	IF3		-2030.1	-634.0	557	VDD2		1819.9	-634.0
523	VSS		-1920.1	-634.0	558	VDD2		1929.9	-634.0

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PAD No.	PIN Name		X	Y	PAD No.	PIN Name		X	Y
	CSEL=0	CSEL=1				CSEL=0	CSEL=1		
559	VDD2		2039.9	-634.0	594	V3		5889.9	-634.0
560	VDD2		2149.9	-634.0	595	V2		5999.9	-634.0
561	VDD2		2259.9	-634.0	596	V1		6109.9	-634.0
562	VDD2		2369.9	-634.0	597	V0OUT		6219.9	-634.0
563	VDD2		2479.9	-634.0	598	V0OUT		6329.9	-634.0
564	VDD2		2589.9	-634.0	599	V0OUT		6439.9	-634.0
565	VDD5		2699.9	-634.0	600	V0OUT		6549.9	-634.0
566	VDD5		2809.9	-634.0	601	V0IN		6659.9	-634.0
567	VDD5		2919.9	-634.0	602	V0IN		6769.9	-634.0
568	VDD5		3029.9	-634.0	603	V0IN		6879.9	-634.0
569	TCAP		3139.9	-634.0	604	V0IN		6989.9	-634.0
570	C2P		3249.9	-634.0	605	COM[0]	COM[0]	7072.3	-598.0
571	C2N		3359.9	-634.0	606	COM[1]	COM[2]	7103.3	-598.0
572	C6P		3469.9	-634.0	607	COM[2]	COM[4]	7134.3	-598.0
573	C2N		3579.9	-634.0	608	COM[3]	COM[6]	7165.3	-598.0
574	C4P		3689.9	-634.0	609	COM[4]	COM[8]	7196.3	-598.0
575	C7P		3799.9	-634.0	610	COM[5]	COM[10]	7227.3	-598.0
576	C1N		3909.9	-634.0	611	COM[6]	COM[12]	7438.0	-583.5
577	C5P		4019.9	-634.0	612	COM[7]	COM[14]	7438.0	-552.5
578	C3P		4129.9	-634.0	613	COM[8]	COM[16]	7438.0	-521.5
579	C1N		4239.9	-634.0	614	COM[9]	COM[18]	7438.0	-490.5
580	C1P		4349.9	-634.0	615	COM[10]	COM[20]	7438.0	-459.5
581	VLCDIN		4459.9	-634.0	616	COM[11]	COM[22]	7438.0	-428.5
582	VLCDIN		4569.9	-634.0	617	COM[12]	COM[24]	7438.0	-397.5
583	VLCDIN		4679.9	-634.0	618	COM[13]	COM[26]	7438.0	-366.5
584	VLCDIN		4789.9	-634.0	619	COM[14]	COM[28]	7438.0	-335.5
585	VLCDIN		4899.9	-634.0	620	COM[15]	COM[30]	7438.0	-304.5
586	VLCDIN		5009.9	-634.0	621	COM[16]	COM[32]	7438.0	-273.5
587	VLCDOUT		5119.9	-634.0	622	COM[17]	COM[34]	7438.0	-242.5
588	VLCDOUT		5229.9	-634.0	623	COM[18]	COM[36]	7438.0	-211.5
589	VLCDOUT		5339.9	-634.0	624	COM[19]	COM[38]	7438.0	-180.5
590	VLCDOUT		5449.9	-634.0	625	COM[20]	COM[40]	7438.0	-149.5
591	VREF		5559.9	-634.0	626	COM[21]	COM[42]	7438.0	-118.5
592	VR		5669.9	-634.0	627	COM[22]	COM[44]	7438.0	-87.5
593	V4		5779.9	-634.0	628	COM[23]	COM[46]	7438.0	-56.5

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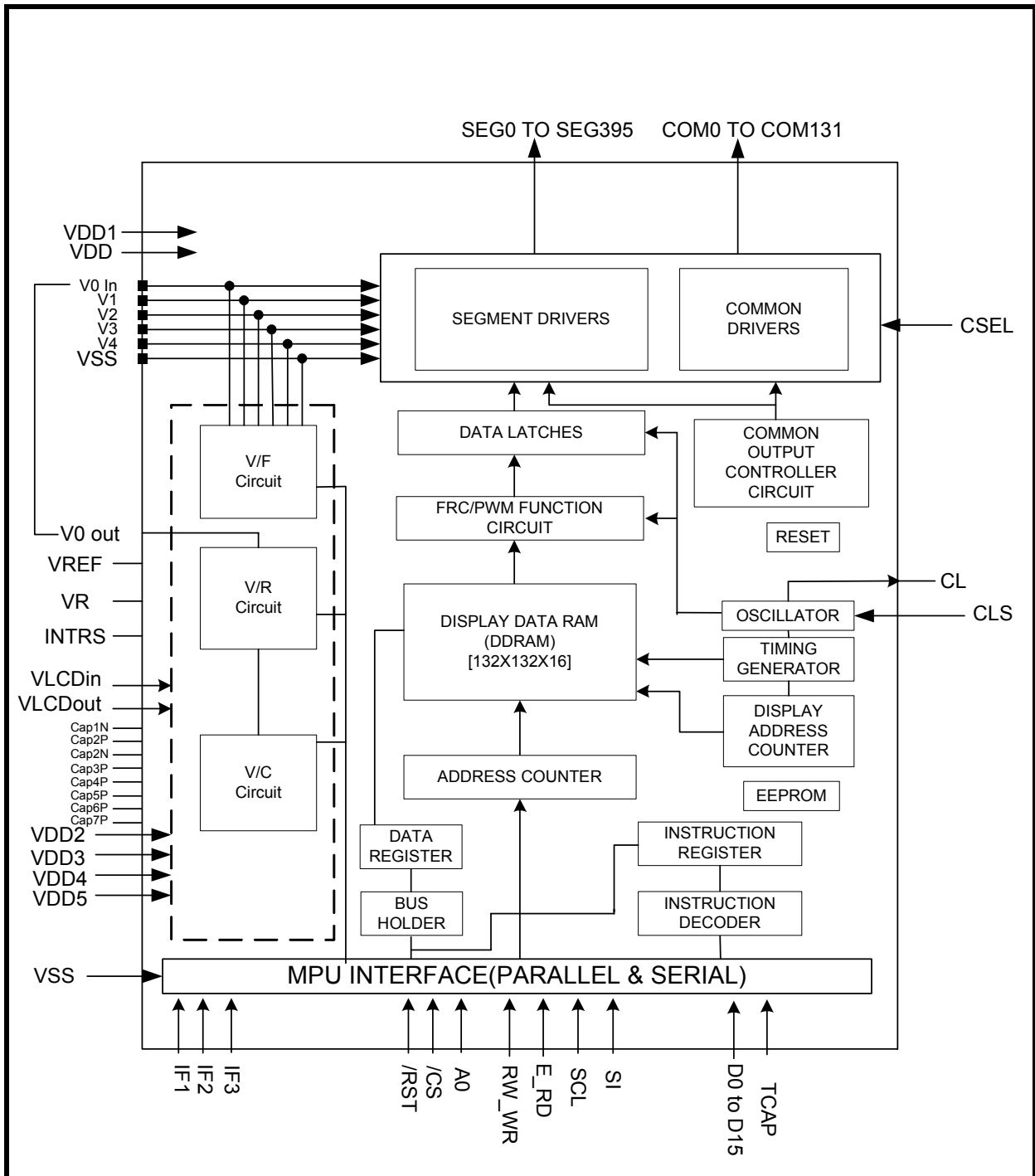
PAD No.	PIN Name		X	Y
	CSEL=0	CSEL=1		
629	COM[24]	COM[48]	7438.0	-25.5
630	COM[25]	COM[50]	7438.0	5.5
631	COM[26]	COM[52]	7438.0	36.5
632	COM[27]	COM[54]	7438.0	67.5
633	COM[28]	COM[56]	7438.0	98.5
634	COM[29]	COM[58]	7438.0	129.5
635	COM[30]	COM[60]	7438.0	160.5
636	COM[31]	COM[62]	7438.0	191.5
637	COM[32]	COM[64]	7438.0	222.5
638	COM[33]	COM[66]	7438.0	253.5

PAD No.	PIN Name		X	Y
	CSEL=0	CSEL=1		
639	COM[34]	COM[68]	7438.0	284.5
640	COM[35]	COM[70]	7438.0	315.5
641	COM[36]	COM[72]	7438.0	346.5
642	COM[37]	COM[74]	7438.0	377.5
643	COM[38]	COM[76]	7438.0	408.5
644	COM[39]	COM[78]	7438.0	439.5
645	COM[40]	COM[80]	7438.0	470.5
646	COM[41]	COM[82]	7438.0	501.5
647	COM[42]	COM[84]	7438.0	532.5
648	COM[43]	COM[86]	7438.0	563.5

Dummy Pad

PAD No.	X	Y
dummy1	-6980.1	-634.0
dummy2	-6870.1	-634.0
dummy3	-6760.1	-634.0
dummy4	-6650.1	-634.0
dummy5	-6540.1	-634.0
dummy6	-6430.1	-634.0
dummy7	-6320.1	-634.0
dummy8	-6210.1	-634.0

5. BLOCK DIAGRAM



6. PIN DESCRIPTION

6.1 POWER SUPPLY

Name	I/O	Description										
VDD	Supply	Power supply for logic circuit										
VDD1	Supply	Power supply for OSC circuit										
VDD2	Supply	Power supply for Booster Circuit										
VDD3	Supply	Power supply for LCD.										
VDD4	Supply	Power supply for LCD.										
VDD5	Supply	Power supply for LCD.										
VSS	Supply	Ground for logic circuit. Ground system should be connected together.										
VSS1	Supply	Ground for OSC circuit. Ground system should be connected together.										
VSS2	Supply	Ground for Booster Circuit. Ground system should be connected together.										
VSS4	Supply	Ground for LCD. Ground system should be connected together.										
VLCD _{OUT}	Supply	If the internal voltage generator is used, the VLCD _{IN} & VLCD _{OUT} must be connected together. If an external supply is used, this pin must be left open.										
VLCD _{IN}	Supply	An external LCD supply voltage can be supplied using the VLCD _{IN} pad. In this case, VLCD _{OUT} has to be left open, and the internal voltage generator has to be programmed to zero. (SET register VC=0)										
V0in V0out V1 V2 V3 V4	I/O	<p>LCD driver supply voltages</p> <p>V0in & V0out should be connected together.</p> <p>Voltages should have the following relationship;</p> <p>$V0 (V0in) \geq V1 \geq V2 \geq V3 \geq V4 \geq VSS, V4 < 2.3V$</p> <p>When the internal power circuit is active, these voltages are generated as following table according to the state of LCD bias.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>LCD bias</th> <th>V1</th> <th>V2</th> <th>V3</th> <th>V4</th> </tr> </thead> <tbody> <tr> <td>1/N bias</td> <td>$(N-1) / N \times V0$</td> <td>$(N-2) / N \times V0$</td> <td>$(2/N) \times V0$</td> <td>$(1/N) \times V0$</td> </tr> </tbody> </table> <p>NOTE: N = 5 to 12</p>	LCD bias	V1	V2	V3	V4	1/N bias	$(N-1) / N \times V0$	$(N-2) / N \times V0$	$(2/N) \times V0$	$(1/N) \times V0$
LCD bias	V1	V2	V3	V4								
1/N bias	$(N-1) / N \times V0$	$(N-2) / N \times V0$	$(2/N) \times V0$	$(1/N) \times V0$								

6.2 LCD Power Supply Pins

Pin Name	I/O	Function
CAP1N	O	DC/DC voltage converter. Connect capacitors between this terminal and the CAP1P, CAP3P, CAP5P, CAP7P terminal.
CAP2N	O	DC/DC voltage converter. Connect capacitors between this terminal and the CAP2P, CAP4P, CAP6P terminal.
CAP1P	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1N terminal.
CAP2P	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2N terminal.
CAP3P	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1N terminal.
CAP4P	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2N terminal.

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CAP5P	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1N terminal.
CAP6P	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2N terminal.
CAP7P	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1N terminal.
VREF	O	Reference voltage output for monitor only. Left it opened.
VR	I	Reference voltage output for monitor only. Left it opened.

6.3 SYSTEM CONTROL

Name	I/O	Description
CLS	I	When using internal clock oscillator, connect CLS to VDD. When using external clock oscillator, connect CLS to VSS.
CL	I/O	When using internal clock oscillator, it's oscillator output. When using external clock oscillator, it's clock input.
INTRS	I	This terminal selects the resistors for the V0 voltage level adjustment. This pin should be fixed to High.
CSEL	I	Select Common output direction. CSEL="L", COM0~COM65 is in one side, COM66~COM131 is in the opposite side. CSEL="H", COM2n(even number) is in the one side, COM2n+1 (odd number) is in the opposite side.
TCAP	I/O	Test pin. Left it opened.

6.4 MICROPROCESSOR INTERFACE

Name	I/O	Description																												
RST	I	Reset input pin When RESETB is "L", initialization is executed.																												
IF[3:1]	I	Parallel / Serial data input select input <table border="1" data-bbox="432 1473 1005 1821"> <thead> <tr> <th>IF1</th> <th>IF2</th> <th>IF3</th> <th>MPU interface type</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>H</td> <td>H</td> <td>80 series 16-bit parallel</td> </tr> <tr> <td>H</td> <td>H</td> <td>L</td> <td>80 series 8-bit parallel</td> </tr> <tr> <td>H</td> <td>L</td> <td>L</td> <td>68 series 16-bit parallel</td> </tr> <tr> <td>L</td> <td>H</td> <td>H</td> <td>68 series 8-bit parallel</td> </tr> <tr> <td>L</td> <td>L</td> <td>H</td> <td>9-bit serial (3 line)</td> </tr> <tr> <td>L</td> <td>L</td> <td>L</td> <td>8-bit serial (4 line)</td> </tr> </tbody> </table>	IF1	IF2	IF3	MPU interface type	H	H	H	80 series 16-bit parallel	H	H	L	80 series 8-bit parallel	H	L	L	68 series 16-bit parallel	L	H	H	68 series 8-bit parallel	L	L	H	9-bit serial (3 line)	L	L	L	8-bit serial (4 line)
IF1	IF2	IF3	MPU interface type																											
H	H	H	80 series 16-bit parallel																											
H	H	L	80 series 8-bit parallel																											
H	L	L	68 series 16-bit parallel																											
L	H	H	68 series 8-bit parallel																											
L	L	H	9-bit serial (3 line)																											
L	L	L	8-bit serial (4 line)																											
/CS	I	Chip select input pins Data / Instruction I/O is enabled only when /CS is "L". When chip select is non-active, D0 to D15 become high impedance.																												
A0	I	Register select input pin																												

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		<p>A0 = "H": D0 to D15 or SI are display data A0 = "L": D0 to D15 or SI are control data In 3-line or 2-line interface not let it floating, contact it to VSS or VDD.</p>									
RW_WR	I	<p>Read / Write execution control pin</p> <table border="1"> <thead> <tr> <th>MPU type</th> <th>RW_WR</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>6800-series</td> <td>RW</td> <td>Read / Write control input pin RW = "H" : read RW = "L" : write</td> </tr> <tr> <td>8080-series</td> <td>/WR</td> <td>Write enable clock input pin The data on D0 to D15 are latched at the rising edge of the /WR signal.</td> </tr> </tbody> </table> <p>When in the serial interface, contact it to VSS or VDD.</p>	MPU type	RW_WR	Description	6800-series	RW	Read / Write control input pin RW = "H" : read RW = "L" : write	8080-series	/WR	Write enable clock input pin The data on D0 to D15 are latched at the rising edge of the /WR signal.
MPU type	RW_WR	Description									
6800-series	RW	Read / Write control input pin RW = "H" : read RW = "L" : write									
8080-series	/WR	Write enable clock input pin The data on D0 to D15 are latched at the rising edge of the /WR signal.									
E_RD	I	<p>Read / Write execution control pin</p> <table border="1"> <thead> <tr> <th>MPU Type</th> <th>E_RD</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>6800-series</td> <td>E</td> <td>Read / Write control input pin RW = "H": When E is "H", D0 to D15 are in an output status. RW = "L": The data on D0 to D15 are latched at the falling edge of the E signal.</td> </tr> <tr> <td>8080-series</td> <td>/RD</td> <td>Read enable clock input pin When /RD is "L", D0 to D15 are in an output status.</td> </tr> </tbody> </table> <p>When in the serial interface, contact it to VSS or VDD.</p>	MPU Type	E_RD	Description	6800-series	E	Read / Write control input pin RW = "H": When E is "H", D0 to D15 are in an output status. RW = "L": The data on D0 to D15 are latched at the falling edge of the E signal.	8080-series	/RD	Read enable clock input pin When /RD is "L", D0 to D15 are in an output status.
MPU Type	E_RD	Description									
6800-series	E	Read / Write control input pin RW = "H": When E is "H", D0 to D15 are in an output status. RW = "L": The data on D0 to D15 are latched at the falling edge of the E signal.									
8080-series	/RD	Read enable clock input pin When /RD is "L", D0 to D15 are in an output status.									
D15 to D0	I/O	<p>They connect to the standard 8-bit or 16 bit MPU bus via the 8/16 –bit bi-directional bus. When the following interface is selected and the /CS pin is high, the following pins become high impedance.</p> <ol style="list-style-type: none"> In 8-bit parallel: D15-D8 are in the state of high impedance, should contact to "H" level or "L" level. In Serial interface: D15-D0 are in the state of high impedance, should contact to "H" level or "L" level. 									
SI	I	<p>This pin is used to input serial data when the serial interface is selected.(3 line and 4 line) When not use contact it to VDD (high level).</p>									
SCL	I	<p>This pin is used to input serial clock when the serial interface is selected. The data is converted in the rising edge. (3 line and 4 line) When not use contact it to VDD (high level).</p>									

NOTE:

Microprocessor interface pins should not be floating in any operation mode.

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6.5 LCD DRIVER OUTPUTS

Name	I/O	Description																										
SEG0 to SEG395	O	LCD segment driver outputs The display data and the M signal control the output voltage of segment driver.																										
		<table border="1"> <thead> <tr> <th rowspan="2">Display data</th> <th rowspan="2">M (Internal)</th> <th colspan="2">Segment driver output voltage</th> </tr> <tr> <th>Normal display</th> <th>Reverse display</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>H</td> <td>V0</td> <td>V2</td> </tr> <tr> <td>H</td> <td>L</td> <td>VSS</td> <td>V3</td> </tr> <tr> <td>L</td> <td>H</td> <td>V2</td> <td>V0</td> </tr> <tr> <td>L</td> <td>L</td> <td>V3</td> <td>VSS</td> </tr> <tr> <td colspan="2">Sleep in mode</td> <td>VSS</td> <td>VSS</td> </tr> </tbody> </table>	Display data	M (Internal)	Segment driver output voltage		Normal display	Reverse display	H	H	V0	V2	H	L	VSS	V3	L	H	V2	V0	L	L	V3	VSS	Sleep in mode		VSS	VSS
		Display data			M (Internal)	Segment driver output voltage																						
			Normal display	Reverse display																								
		H	H	V0	V2																							
		H	L	VSS	V3																							
L	H	V2	V0																									
L	L	V3	VSS																									
Sleep in mode		VSS	VSS																									
COM0 to COM131	O	LCD common driver outputs The internal scanning data and M signal control the output voltage of common driver.																										
		<table border="1"> <thead> <tr> <th>Scan data</th> <th>M (Internal)</th> <th>Common driver output voltage</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>H</td> <td>VSS</td> </tr> <tr> <td>H</td> <td>L</td> <td>V0</td> </tr> <tr> <td>L</td> <td>H</td> <td>V1</td> </tr> <tr> <td>L</td> <td>L</td> <td>V4</td> </tr> <tr> <td colspan="2">Sleep in mode</td> <td>VSS</td> </tr> </tbody> </table>	Scan data	M (Internal)	Common driver output voltage	H	H	VSS	H	L	V0	L	H	V1	L	L	V4	Sleep in mode		VSS								
		Scan data	M (Internal)	Common driver output voltage																								
		H	H	VSS																								
		H	L	V0																								
		L	H	V1																								
L	L	V4																										
Sleep in mode		VSS																										
Sleep in mode		VSS																										

ST7636R I/O PIN ITO Resister Limitation

Pin Name	ITO Resister
VREF, TCAP, CL, VR	Floating
IF[3:1],CLS,CSEL,INTRS	No Limitation
VDD, VDD1~VDD5, VSS, CAP1N, CAP2N, VLCD _{IN} , VLCD _{OUT}	<100Ω
V0in, V0out, V1, V2, V3, V4, CAP1P~7P	<100Ω
A0, E_RD, RW_WR, /CS, D0 ...D15, SCL, SI	<1KΩ
RST	<10KΩ

NOTE:

- (1) Make sure the ITO resistance of COM0 ~ COM131 is equal, and so is it of SEG0 ~ SEG395.
- (2) All the resistance values in above table are under digital power supply is 2.8V condition.

7. FUNCTIONAL DESCRIPTION

7.1 MICROPROCESSOR INTERFACE

Chip Select Input

/CS pin is for chip selection. The ST7636R can function with an MPU when /CS is "L". In case of serial interface, the internal shift register and the counter are reset.

7.1.1 Selecting Parallel / Serial Interface

ST7636R has seven types of interface with an MPU, which are two serial and four parallel interfaces. This parallel or serial interface is determined by IF pin as shown in table 7.1.1.

Table 7.1.1 Parallel / Serial Interface Mode

I/F Mode			I/F Description	Pin Assignment							
IF1	IF2	IF3		/CS	A0	E_RD	RW_WR	D15 to D8	D7 to D0	SI	SCL
H	H	H	80 serial 16-bit parallel	/CS	A0	/RD	/WR	D15 ~ D8	D7 ~ D0	--	--
H	H	L	80 serial 8-bit parallel	/CS	A0	/RD	/WR	--	D7 ~ D0	--	--
H	L	L	68 serial 16-bit parallel	/CS	A0	E	R/W	D15 ~ D8	D7 ~ D0	--	--
L	H	H	68 serial 8-bit parallel	/CS	A0	E	R/W	--	D7 ~ D0	--	--
L	L	L	8-bit SPI mode (4 line)	/CS	A0	--	--	--	--	SI	SCL
L	L	H	9-bit SPI mode (3 line)	/CS	--	--	--	--	--	SI	SCL

NOTE: When these pins are set to any other combination, A0, E_RD and RW_WR inputs are disabled and D0 to D15 are to be high impedance.

7.1.2 8-bit or 16-bit Parallel Interface

The ST7636R identifies the type of the data bus signals according to the combination of A0, /RD (E) and /WR (W/R) signals, as shown in table 7.1.2.

Table 7.1.2 Parallel Data Transfer

Common	6800-series		8080-series		Description
	A0	R/W	E	/RD	
H	H	H	L	H	Display data read out
H	L	H	H	L	Display data write
L	H	H	L	H	Register status read
L	L	H	H	L	Writes to internal register (instruction)

Relation between Data Bus and Gradation Data

ST7636R offers 4096 color display, 65K color display, truncated 262K color, and truncated 16M color.

When using 4096, 65K, 262K, and 16M color, you can specify color for each of R, G, B using the palette function.

Use the command for switching between these modes.

(1) 4096-color display

www. (1-1) Type A 4096 color display

1. 8-bit mode

D7, D6, D5, D4, D3, D2, D1, D0: RRRRGGGG 1st write

D7, D6, D5, D4, D3, D2, D1, D0: BBBBRRRR 2nd write

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D7, D6, D5, D4, D3, D2, D1, D0: GGGGBBBB 3rd write

2 pixels of data are read after the third write operation as shown, and it is written in the display RAM.

2. 16-bit mode

D15, D14, D13, D12, D11, D10, D9, D8, D7, D6, D5, D4, D3, D2, D1, D0: RRRRGGGGBBBBXXXX

Data is acquired through signal write operation and then written to the display RAM.

“XXXX” are dummy bits, and they are ignored for display.

(1-2) Type B 4096 color display

1. 8-bit mode

D7, D6, D5, D4, D3, D2, D1, D0: XXXXRRRR 1st write

D7, D6, D5, D4, D3, D2, D1, D0: GGGGBBBB 2nd write

A single pixel of data is read after the second write operation as shown, and it is written in the display RAM.

2. 16-bit mode

D15, D14, D13, D12, D11, D10, D9, D8, D7, D6, D5, D4, D3, D2, D1, D0: XXXXRRRRGGGGBBBB

A single pixel of data is read and written in the display RAM in a single write operation.

“XXXX” are dummy bits, and they are ignored for display.

(2) 65K color input mode

1. 8-bit mode

D7, D6, D5, D4, D3, D2, D1, D0: RRRRRGGG 1st write

D7, D6, D5, D4, D3, D2, D1, D0: GGGBBBBB 2nd write

A single pixel of data is read after the second write operation as shown, and it is written in the display RAM.

2. 16-bit mode

D15, D14, D13, D12, D11, D10, D9, D8, D7, D6, D5, D4, D3, D2, D1, D0: RRRRRGGGGGBBBBBB (16 bits)

Data is acquired through signal write operation and then written to the display RAM.

(3) truncated 262K color input mode

1. 8-bit mode

D7, D6, D5, D4, D3, D2, D1, D0: RRRRRRXX 1st write

D7, D6, D5, D4, D3, D2, D1, D0: GGGGGGXX 2nd write

D7, D6, D5, D4, D3, D2, D1, D0: BBBBXX 3rd write

www.DataSheet4U.com A single pixel of data is read after the third write operation as shown, and it is written in the display RAM.

“X” is dummy bit, and it is ignored for display.

2. 16 bit mode

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D15, D14, D13, D12, D11, D10, D9, D8, D7, D6, D5, D4, D3, D2, D1, D0: RRRRRRXXGGGGGGXX 1st write

D15, D14, D13, D12, D11, D10, D9, D8, D7, D6, D5, D4, D3, D2, D1, D0: BBBBXXXXXXXXXXXXXXXX 2nd write

A single pixel of data is read after the second write operation as shown, and it is written in the display RAM.

(4) truncated 16M color input mode

1. 8-bit mode

D7, D6, D5, D4, D3, D2, D1, D0: RRRRRRRR 1st write

D7, D6, D5, D4, D3, D2, D1, D0: GGGGGGGG 2nd write

D7, D6, D5, D4, D3, D2, D1, D0: BBBBBBBB 3rd write

A single pixel of data is read after the third write operation as shown, and it is written in the display RAM.

2. 16 bit mode

D15, D14, D13, D12, D11, D10, D9, D8, D7, D6, D5, D4, D3, D2, D1, D0: RRRRRRRRGGGGGGGG 1st write

D15, D14, D13, D12, D11, D10, D9, D8, D7, D6, D5, D4, D3, D2, D1, D0: BBBBBBBBXXXXXXXX 2nd write

A single pixel of data is read after the second write operation as shown, and it is written in the display RAM.

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7.1.3 8- and 9-bit Serial Interface

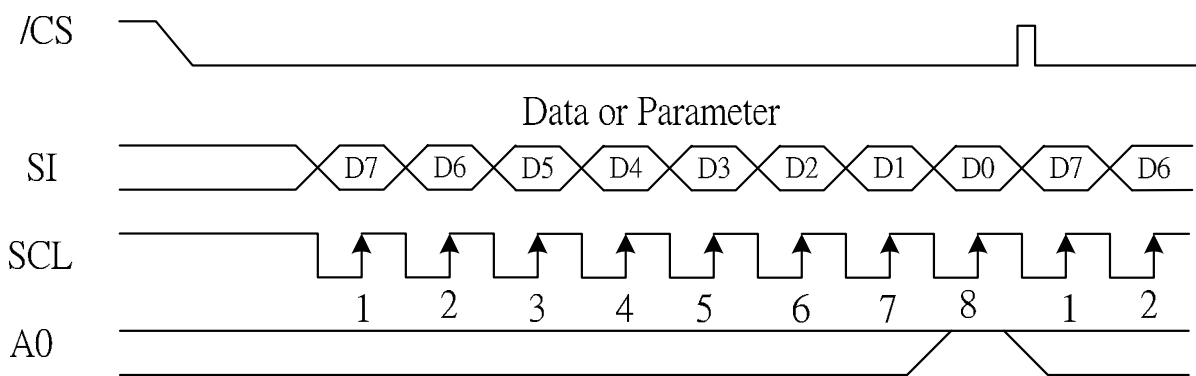
The 8-bit serial interface uses four pins /CS, SI, SCL, and A0 to enter commands and data. Meanwhile, the 9-bit serial interface uses three pins /CS, SI and SCL for the same purpose.

Data read is not available in the serial interface. Data entered must be 8 bits. Refer to the following chart for entering commands, parameters or gray-scale data.

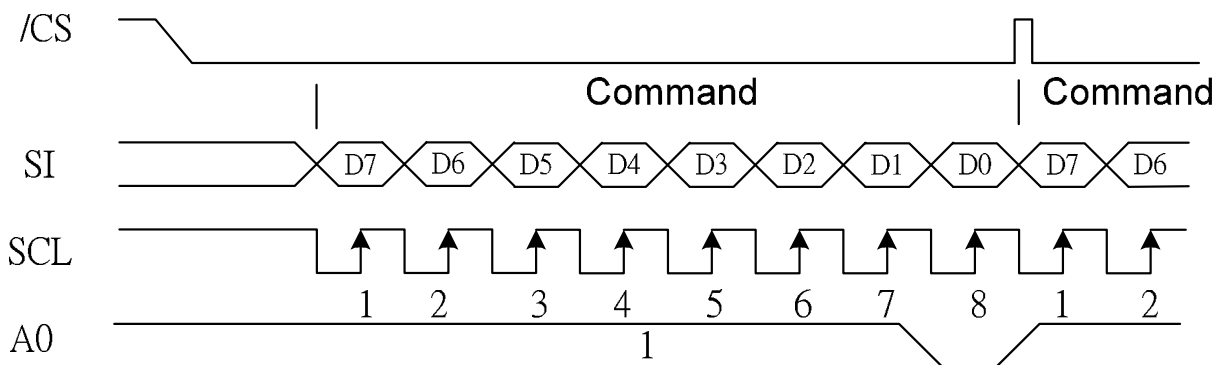
The relation between gray-scale data and data bus in the serial input is the same as that in the 8-bit parallel interface mode at every gradation.

(1) 8-bit serial interface (4 line)

When entering data (parameters): A0= HIGH at the rising edge of the 8th SCL.



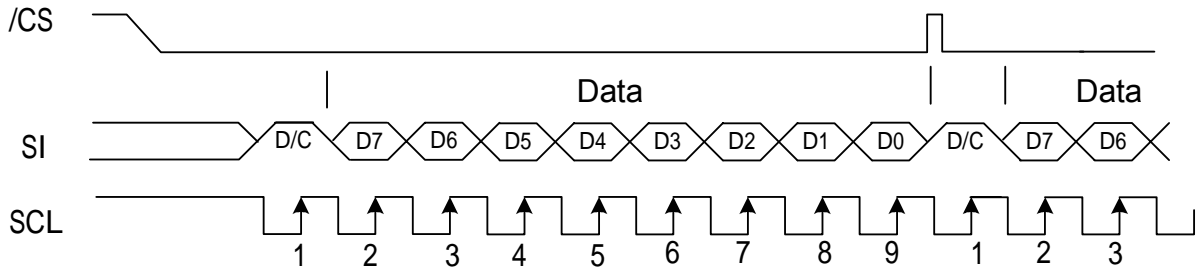
When entering command: A0= LOW at the rising edge of the 8th SCL



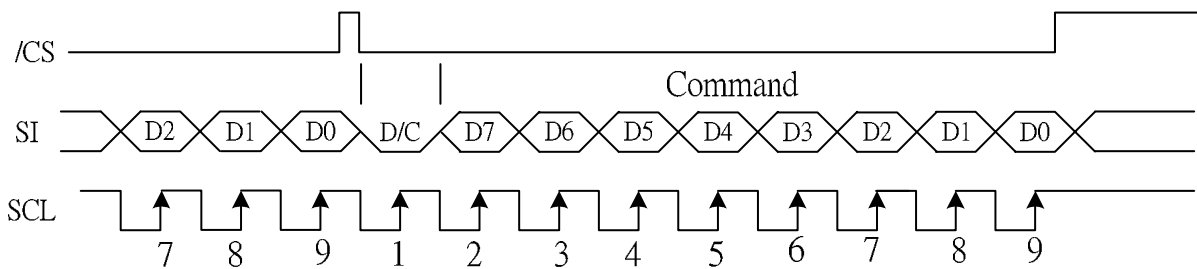
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(2) 9-bit serial interface (3 line)

When entering data (parameters): SI= HIGH at the rising edge of the 1st SCL.



When entering command: SI= LOW at the rising edge of the 1st SCL.



- If /CS is set to HIGH while the 8 bits from D7 to D0 are entered, the data concerned is invalidated. Before entering succeeding sets of data, you must correctly input the data concerned again.
- In order to avoid data transfer error due to incoming noise, it is recommended to set /CS at HIGH on byte basis to initialize the serial-to-parallel conversion counter and the register.
- When executing the command RAMWR, set /CS to HIGH after writing the last address (after starting the 9th pulse in case of 9-bit serial input or after starting the 8th pulse in case of 8-bit serial input).

7.2 ACCESS TO DDRAM AND INTERNAL REGISTERS

ST7636R realizes high-speed data transfer because the access from MPU is a sort of pipeline processing done via the bus holder attached to the internal, requiring the cycle time alone without needing the wait time.

For example, when MPU writes data to the DDRAM, the data is once held by the bus holder and then written to the DDRAM before the succeeding write cycle is started. When MPU reads data from the DDRAM, the first read cycle is dummy and the bus holder holds the data read in the dummy cycle, and then it read from the bus holder to the system bus in the succeeding read cycle. Figure 7.2.1 illustrates these relations.

In 80-series interface mode:

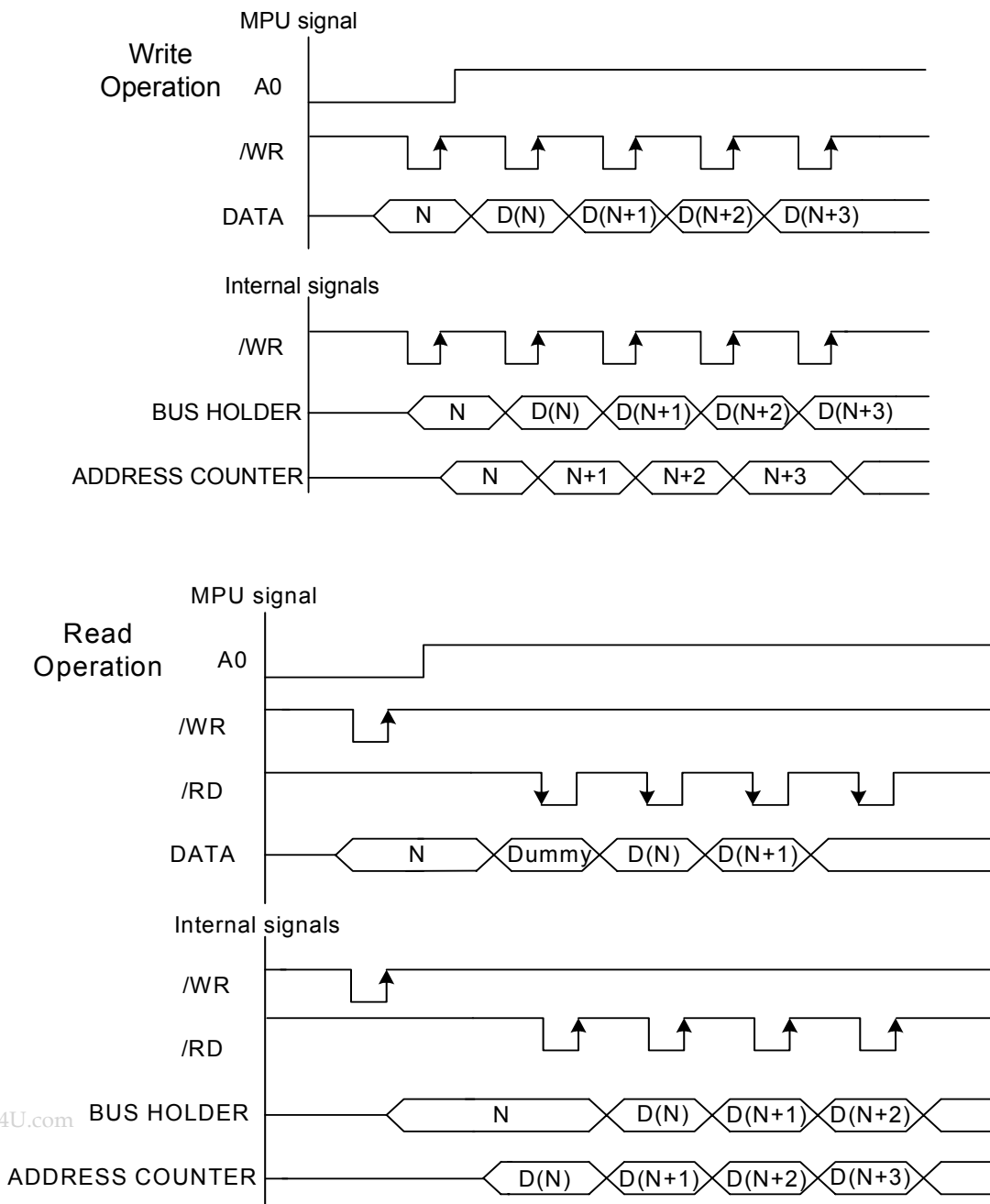


Figure 7.2.1

7.3 DISPLAY DATA RAM (DDRAM)

7.3.1 DDRAM

It is 132 X 132 X 16 bits capacity RAM prepared for storing dot data. You can access a desired bit by specifying the page address and column address. Since display data from MCU D7 to D0 and D15 to D8 correspond to one or two pixels of RGB, data transfer related restrictions are reduced, realizing the display flexing.

The RAM on ST7636R is separated to a block per 4 lines to allow the display system to process data on the block basis. MPU's read and write operations to and from the RAM are performed via the I/O buffer circuit; Reading of the RAM for the liquid crystal drive is controlled from another separate circuit. Refer to the following memory map for the RAM configuration.

Memory Map (When using the Type A 4096 color. 8-bit mode,)

RGB alignment (Command of Data Control Parameter2 = 000)														
direction Column scan	P11:0	0			1			131						
	→													
	P11:1	131			130			0						
	←													
Color		R	G	B	R	G	B		R	G	B			
Example: Data/Scan format		D0_7	D0_3	D1_7	D1_3	D2_7	D2_3		D196_3	D197_7	D197_3			
→		D0_6	D0_2	D1_6	D1_2	D2_6	D2_2		D196_2	D197_6	D197_2			
↘		D0_5	D0_1	D1_5	D1_1	D2_5	D2_1		D196_1	D197_5	D197_1			
↙		D0_4	D0_0	D1_4	D1_0	D2_4	D2_0		D196_0	D197_4	D197_0			
→														
BLOCK	Page scan		Memory Map											
	P10:0	P10:1												
0	0	131	↑	↓										
	1	130												
	2	129												
	3	128												
1	4	127												
	5	126												
	6	125												
	7	124												
31	124	7												
	125	6												
	126	5												
	127	4												
32	128	3												
	129	2												
	130	1												
	131	0												
SEGout			0	1	2	3	4	5	393	394	395			

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Memory Map (When using the Type A 4096 color. 16-bit mode.)

RGB alignment (Command of Data Control Parameter2 = 000)											
direction	Column scan	P11:0	0			1			131		
		P11:1	131			130			0		
Color		R	G	B	R	G	B	R	G	B	
Example: Data/Scan format		D0_15	D0_11	D0_7	D1_15	D1_11	D1_7	D131_15	D131_11	D131_7	
		D0_14	D0_10	D0_6	D1_14	D1_10	D1_6	D131_14	D131_10	D131_6	
		D0_13	D0_9	D0_5	D1_13	D1_9	D1_5	D131_13	D131_9	D131_5	
		D0_12	D0_8	D0_4	D1_12	D1_8	D1_4	D131_12	D131_8	D131_4	
BLOCK	Page scan		Memory Map								
	P10:0	P10:1									
0	0	131	↓	↑	0	1	2	3	4	5	
	1	130									
	2	129									
	3	128									
1	4	127	↓	↑	0	1	2	3	4	5	
	5	126									
	6	125									
	7	124									
31	124	7	↓	↑	0	1	2	3	4	5	
	125	6									
	126	5									
	127	4									
32	128	3	↓	↑	0	1	2	3	4	5	
	129	2									
	130	1									
	131	0									
SEGout			0	1	2	3	4	5	393	394	395

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Memory Map (When using the Type B 4096 color. 8-bit mode,)

RGB alignment (Command of Data Control Parameter2 = 000)												
direction	Column scan	P11:0	0			1			131			
		P11:1	131			130			0			
Color		R	G	B	R	G	B	R	G	B		
Example: Data/Scan format		D0_3	D1_7	D1_3	D2_3	D3_7	D3_3	D262_3	D263_7	D263_3		
		D0_2	D1_6	D1_2	D2_2	D3_6	D3_2	D262_2	D263_6	D263_2		
		D0_1	D1_5	D1_1	D2_1	D3_5	D3_1	D262_1	D263_5	D263_1		
		D0_0	D1_4	D1_0	D2_0	D3_4	D3_0	D262_0	D263_4	D263_0		
BLOCK	Page scan		Memory Map									
	P10:0	P10:1										
0	0	131										
	1	130										
	2	129										
	3	128										
1	4	127										
	5	126										
	6	125										
	7	124										
31	124	7										
	125	6										
	126	5										
	127	4										
32	128	3										
	129	2										
	130	1										
	131	0										
SEGout			0	1	2	3	4	5	393	394	395	

You can change position of R and B with DATACTL command.

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Memory Map (When using the Type B 4096 color. 16-bit mode.)

RGB alignment (Command of Data Control Parameter2 = 000)											
direction	Column scan	P11:0	0			1			131		
		P11:1	131			130			0		
Color		R	G	B	R	G	B	R	G	B	
Example: Data/Scan format		D0_11	D0_7	D0_3	D1_11	D1_7	D1_3	D131_11	D131_7	D131_3	
		D0_10	D0_6	D0_2	D1_10	D1_6	D1_2	D131_10	D131_6	D131_2	
		D0_9	D0_5	D0_1	D1_9	D1_5	D1_1	D131_9	D131_5	D131_1	
		D0_8	D0_4	D0_0	D1_8	D1_4	D1_0	D131_8	D131_4	D131_0	
BLOCK	Page scan		Memory Map								
	P10:0	P10:1									
0	0	131	↓	↑	R	G	B	R	G	B	
	1	130									
	2	129									
	3	128									
1	4	127									
	5	126									
	6	125									
31	124	7									
	125	6									
	126	5									
32	127	4									
	128	3									
	129	2									
	130	1									
	131	0									
SEGout			0	1	2	3	4	5	393	394	395

You can change position of R and B with DATACTL command.

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Memory Map (When using the 65Kcolor. 8-bit mode,)

RGB alignment (Command of Data Control Parameter2 = 000)														
Column scan direction	P11:0	0			1			131						
	P11:1	131			130			0						
	Color	R	G	B	R	G	B	R	G	B				
	Example: Data/Scan format	D0_7	D0_2	D1_4	D2_7	D2_2	D3_4	D262_7	D262_2	D263_4				
	D0_6	D0_1	D1_3	D2_6	D2_1	D3_3	D262_6	D262_1	D263_3					
	D0_5	D0_0	D1_2	D2_5	D2_0	D3_2	D262_5	D262_0	D263_2					
	D0_4	D1_7	D1_1	D2_4	D3_7	D3_1	D262_4	D263_7	D263_1					
	D0_3	D1_6	D1_0	D2_3	D3_6	D3_0	D262_3	D263_6	D263_0					
		D1_5		D3_5			D263_5							
BLOCK	Page scan		Memory Map											
	P10:0	P10:1												
0	0	131	↑	↓	0	1	2	3	4	5	393	394	395	
	1	130												
	2	129												
	3	128												
1	4	127												
	5	126												
	6	125												
7	124													
31	124	7												
	125	6												
	126	5												
	127	4												
32	128	3												
	129	2												
	130	1												
	131	0												
SEGout			0	1	2	3	4	5	393	394	395			

You can change position of R and B with DATACTL command.

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Memory Map (When using the 65K color. 16-bit mode)

RGB alignment (Command of Data Control Parameter2 = 000)												
direction Column scan	P11:0	0			1			131				
	→											
	P11:1	131			130			0				
	←											
Color		R	G	B	R	G	B		R	G	B	
Example: Data/Scan format		D0_15	D0_10	D0_4	D1_15	D1_10	D1_4		D131_15	D131_10	D131_4	
→		D0_14	D0_9	D0_3	D1_14	D1_9	D1_3		D131_14	D131_9	D131_3	
↘		D0_13	D0_8	D0_2	D1_13	D1_8	D1_2		D131_13	D131_8	D131_2	
↙		D0_12	D0_7	D0_1	D1_12	D1_7	D1_1		D131_12	D131_7	D131_1	
→		D0_11	D0_6	D0_0	D1_11	D1_6	D1_0		D131_11	D131_6	D131_0	
			D0_5			D1_5				D131_5		
BLOCK	Page scan		Memory Map									
	P10:0	P10:1										
0	0	131										
	1	130										
	2	129										
	3	128										
1	4	127										
	5	126										
	6	125										
	7	124										
31	124	7										
	125	6										
	126	5										
	127	4										
32	128	3										
	129	2										
	130	1										
	131	0										
SEGout			0	1	2	3	4	5		393	394	395

You can change position of R and B with DATACTL command.

ST7636R

Memory Map (When using the 262K/16Mcolor. 8-bit mode,)

RGB alignment (Command of Data Control Parameter2 = 000)												
Column scan direction	P11:0		0			1			131			
	P11:1		131			130			0			
	Color		R	G	B	R	G	B	R	G	B	
	Example: Data/Scan format		D0_7	D1_7	D2_7	D3_7	D4_7	D5_7	D393_7	D394_7	D395_7	
		D0_6	D1_6	D2_6	D3_6	D4_6	D5_6	D393_6	D394_6	D395_6		
		D0_5	D1_5	D2_5	D3_5	D4_5	D5_5	D393_5	D394_5	D395_5		
		D0_4	D1_4	D2_4	D3_4	D4_4	D5_4	D393_4	D394_4	D395_4		
		D0_3	D1_3	D2_3	D3_3	D4_3	D5_3	D393_3	D394_3	D395_3		
		D0_2	D1_2	D2_2	D3_2	D4_2	D5_2	D393_2	D394_2	D395_2		
		D0_1	D1_1	D2_1	D3_1	D4_1	D5_1	D393_1	D394_1	D395_1		
		D0_0	D1_0	D2_0	D3_0	D4_0	D5_0	D393_0	D394_0	D395_0		
BLOCK	Page scan		Memory Map									
	P10:0	P10:1										
0	0	131										
	1	130										
	2	129										
	3	128										
1	4	127										
	5	126										
	6	125										
	7	124										
31	124	7										
	125	6										
	126	5										
	127	4										
32	128	3										
	129	2										
	130	1										
	131	0										
SEGout			0	1	2	3	4	5	393	394	395	

You can change position of R and B with DATACTL command.

ST7636R

Memory Map (When using the 16 gray-scale, 262K/16M color. 16-bit mode)

RGB alignment (Command of Data Control Parameter2 = 000)																														
Column scan direction	P11:0	0	1		131																									
		→																												
	P11:1	131	130		0																									
		←																												
Color		R	G	B	R	G	B		R	G	B																			
Example: Data/Scan format		D0_15	D0_7	D1_15	D1_7	D2_7	D2_7		D176_7	D177_7	D177_7																			
		D0_14	D0_6	D1_14	D1_6	D2_6	D2_6		D176_6	D177_6	D177_6																			
		D0_13	D0_5	D1_13	D1_5	D2_5	D2_5		D176_5	D177_5	D177_5																			
		D0_12	D0_4	D1_12	D1_4	D2_4	D2_4		D176_4	D177_4	D177_4																			
		D0_11	D0_3	D1_11	D1_3	D2_3	D2_3		D176_3	D177_3	D177_3																			
		D0_10	D0_2	D1_10	D1_2	D2_2	D2_2		D176_2	D177_2	D177_2																			
		D0_9	D0_1	D1_9	D1_1	D2_1	D2_1		D176_1	D177_1	D177_1																			
		D0_8	D0_0	D1_8	D1_0	D2_0	D2_0		D176_0	D177_0	D177_0																			
BLOCK	Page scan		Memory Map																											
	P10:0	P10:1																												
0	0	131																												
	1	130																												
	2	129																												
	3	128																												
1	4	127																												
	5	126																												
	6	125																												
	7	124																												
31	124	7																												
	125	6																												
	126	5																												
	127	4																												
32	128	3																												
	129	2																												
	130	1																												
	131	0																												
SEGout			0	1	2	3	4	5		393	394																			

You can change position of R and B with DATACTL command.

ST7636R

Memory Map (When using the 16 gray-scale, 262K/16M color. 16-bit mode)

RGB alignment (Command of Data Control Parameter2 = 000)													
Column scan direction	P11:0	0	1		131								
		→											
	P11:1	131	130		0								
		←											
Color		R	G	B	R	G	B		R	G	B		
Example: Data/Scan format		D0_15	D0_7	D1_15	D1_7	D2_7	D2_7		D176_7	D177_7	D177_7		
		D0_14	D0_6	D1_14	D1_6	D2_6	D2_6		D176_6	D177_6	D177_6		
		D0_13	D0_5	D1_13	D1_5	D2_5	D2_5		D176_5	D177_5	D177_5		
		D0_12	D0_4	D1_12	D1_4	D2_4	D2_4		D176_4	D177_4	D177_4		
		D0_11	D0_3	D1_11	D1_3	D2_3	D2_3		D176_3	D177_3	D177_3		
		D0_10	D0_2	D1_10	D1_2	D2_2	D2_2		D176_2	D177_2	D177_2		
		D0_9	D0_1	D1_9	D1_1	D2_1	D2_1		D176_1	D177_1	D177_1		
		D0_8	D0_0	D1_8	D1_0	D2_0	D2_0		D176_0	D177_0	D177_0		
BLOCK	Page scan		Memory Map										
	P10:0	P10:1											
0	0	131	↓	↑									
	1	130											
	2	129											
	3	128											
1	4	127											
	5	126											
	6	125											
	7	124											
31	124	7											
	125	6											
	126	5											
	127	4											
32	128	3											
	129	2											
	130	1											
	131	0											
SEGout			0	1	2	3	4	5	393	394	395		

You can change position of R and B with DATACTL command.

7.3.2 Page Address Control Circuit

This circuit is used to control the address in the page direction when MPU accesses the DDRAM or when reading the DDRAM to display image on the LCD.

You can specify a scope of the page address with page address set command. When the page-direction scan is specified with DATACTL command and the address are incremented from the start up to the end page, the column address is incremented by 1 and the page address returns to start page.

The DDRAM supports up to 132 lines, and thus the total page becomes 132.

In the read operation, as the end page is reached, the column address is automatically incremented by 1 and the page address is returned to start page.

Using the address normal/inverse parameter of DATACTL command allows you to inverse the correspondence between the DDRAM address and command output.

7.3.3 Column Address Control Circuit

This circuit is used to control the address in the column direction when MPU accesses the DDRAM. You can specify a scope of the column address using column address set command. When the column-direction scan is specified with DATACTL command and the address are incremented from the start up to the end page, the page address is incremented by 1 and the column address returns to start column.

In the read operation, too, the column address is automatically incremented by 1 and returned to start page as the end column is reached.

Just like the page address control circuit, using the column address normal/inverse parameter of DATACTL command enables to inverse the correspondence between the DDRAM column address and segment output. This arrangement relaxes restrictions in the chip layout on the LCD module.

7.3.4 I/O Buffer Circuit

It is the bi-directional buffer used when MPU reads or writes the DDRAM. Since MPU's read or write of DDRAM is performed independently from data output to the display data latch circuit, asynchronous access to the DDRAM when the LCD is turned on does not cause troubles such as flicking of the display images.

7.3.5 Block Address Circuit

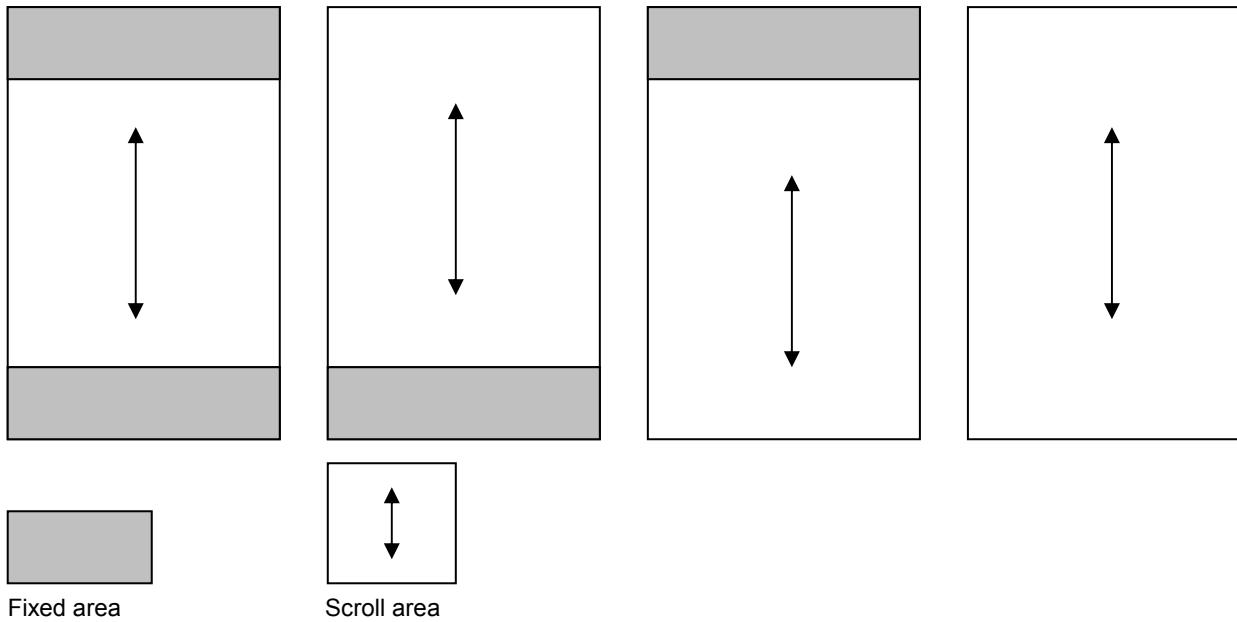
The circuit associates pages on DDRAM with COM output. ST7636R processes signals for the liquid crystal display on 4-page basis. Thus, when specifying a specific area in the area scroll display or partial display, you must designate it in block.

7.3.6 Display data Latch Circuit

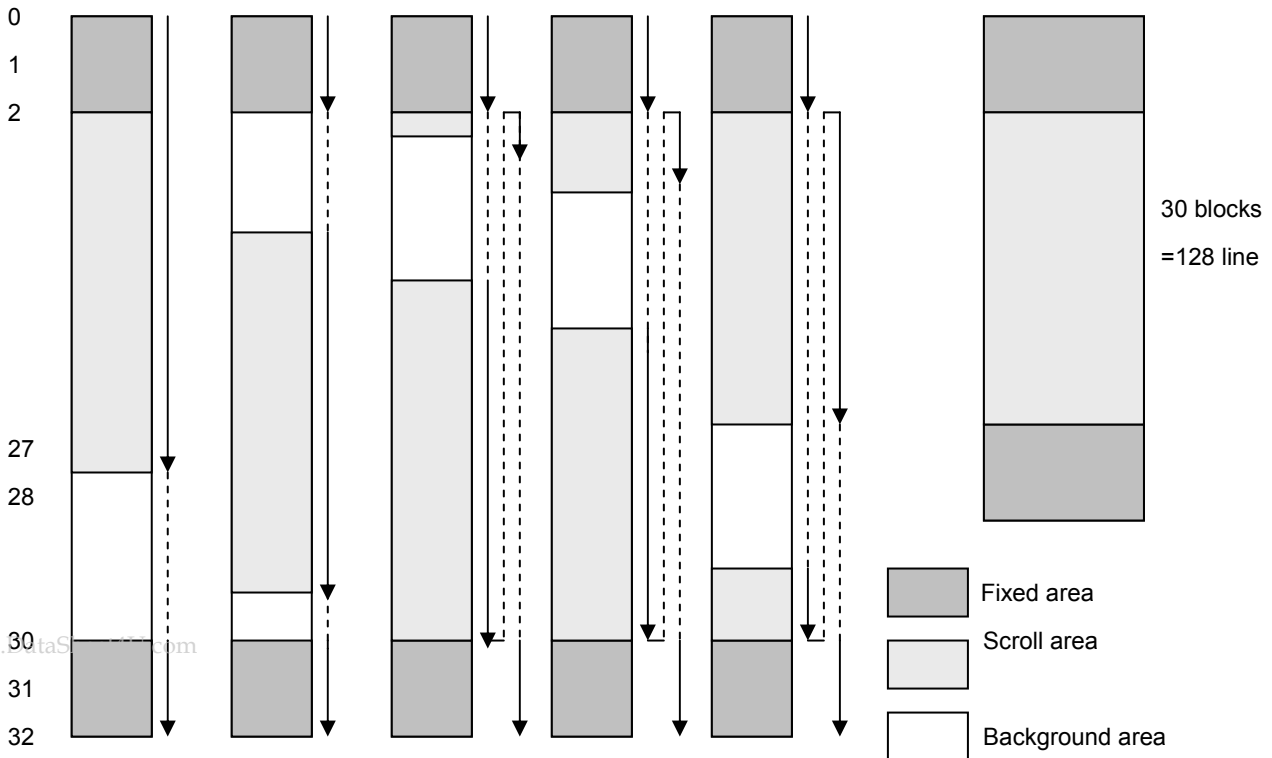
www. This circuit is used to temporarily hold display data to be output from the DDRAM to the SEG decoder circuit. Since display normal/inverse and display on/off commands are used to control data in the latch circuit alone, they do not modify data in the DDRAM.

7.4 Area Scroll Display

Using area scroll set and scroll start set commands allows you to scroll the display screen partially. You can select any one of the following four scroll patterns.

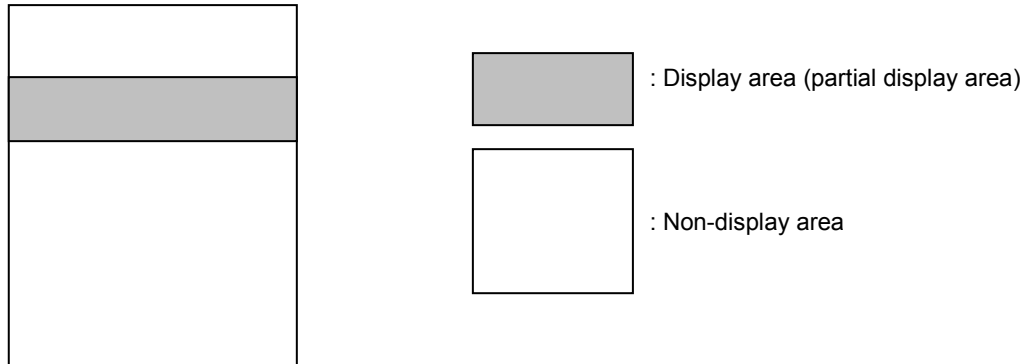


DDRAM



7.5 Partial Display

Using partial in command allows you turn on the partial display (division by line) of the screen. This mode requires less current consumption than the whole screen display, making it suitable for the equipment in the standby state.



If the partial display region is out of the Max. Display range, it would be no operation

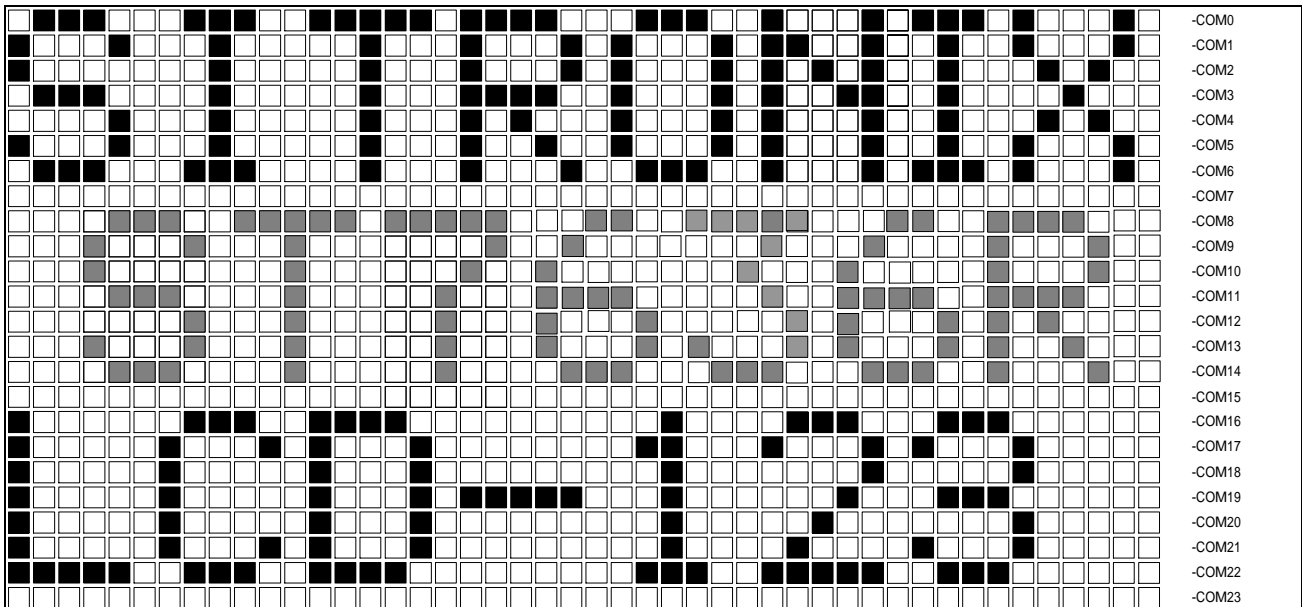


Figure 7.5.1 Reference Example for Partial Display

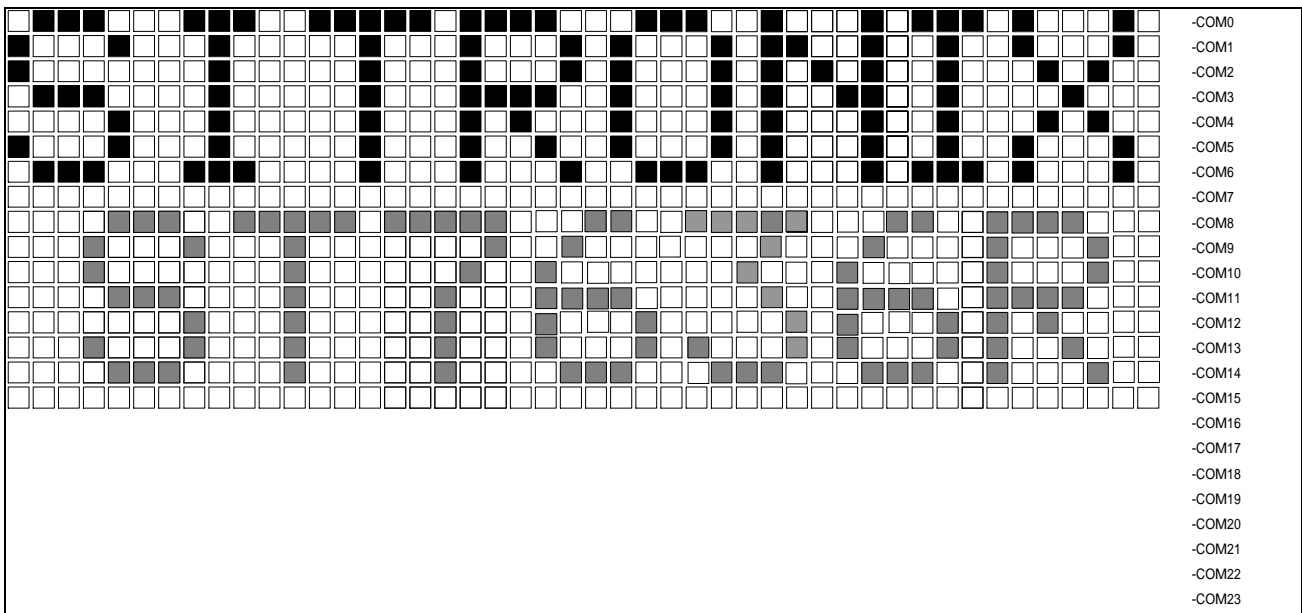


Figure 7.5.2 Partial Display (Partial Display Duty=16,initial COM0=0)

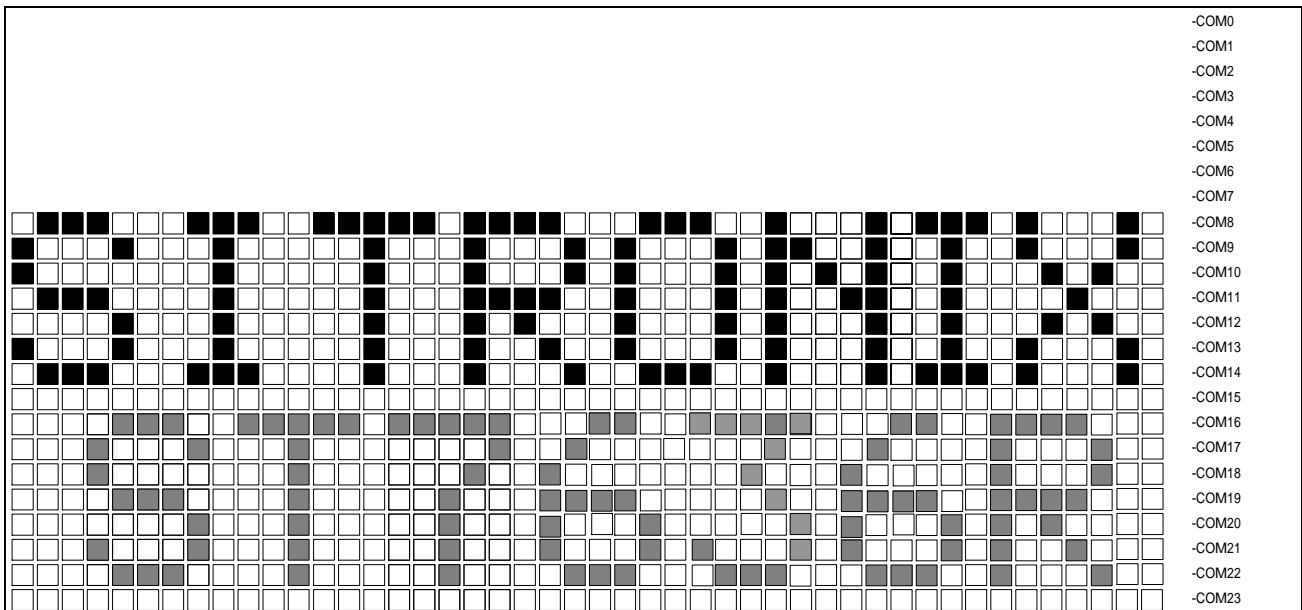


Figure 7.5.3 Moving Display (Partial Display Duty=16,Initial COM0=8)

7.6 Gary-Scale Display

ST7636R incorporates a 4FRC & 31 PWM function circuit to display a 64 gray-scale display.

7.7 Oscillation circuit

This is on-chip Oscillator without external resistor. When the internal oscillator is used, CLS must connect to VDD; when the external oscillator is used, CL could be input pin. This oscillator signal is used in the voltage converter and display timing generation circuit.

7.8 Display Timing Generator Circuit

This circuit generates some signals to be used for displaying LCD. The display clock, CL (internal), generated by oscillation clock, generates the clock for the line counter and the signal for the display data latch. The line address of on-chip RAM is generated in synchronization with the display clock and the display data latch circuit latches the 132-bit display data in synchronization with the display clock. The display data, which is read to the LCD driver, is completely independent of the access to the display data RAM from the microprocessor. The display clock generates an LCD AC signal (M), which enables the LCD driver to make an AC drive waveform, and also generates an internal common timing signal and start signal to the common driver. The frame signal or the line signal changes the M by setting internal instruction. Driving waveform and internal timing signal are shown in Figure 7.8.1.

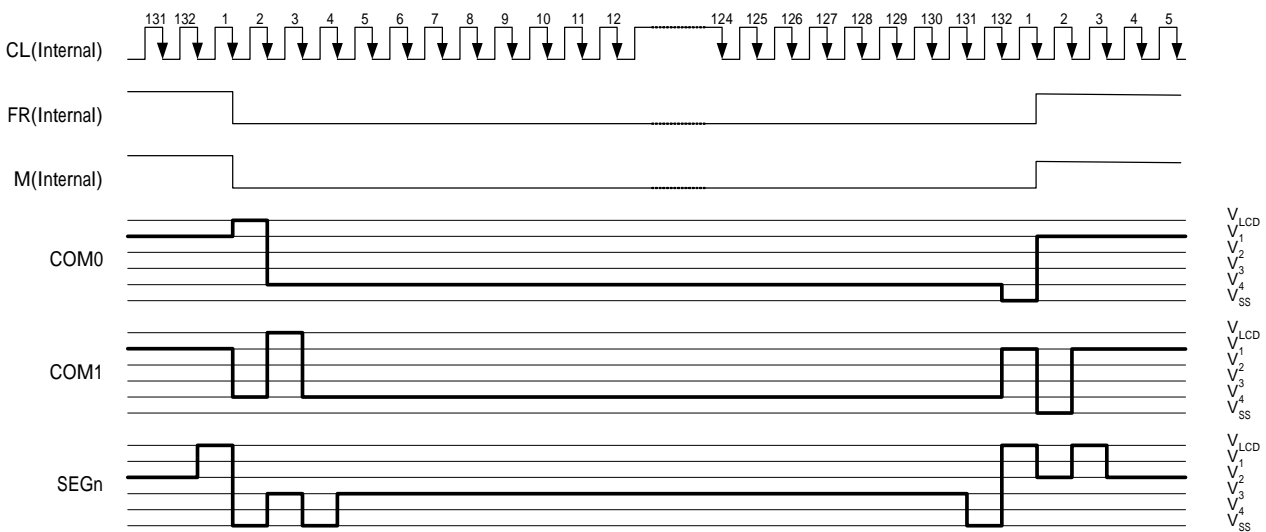


Figure 7.8.1 2-frame AC Driving Waveform (Duty Ratio: 1/132)

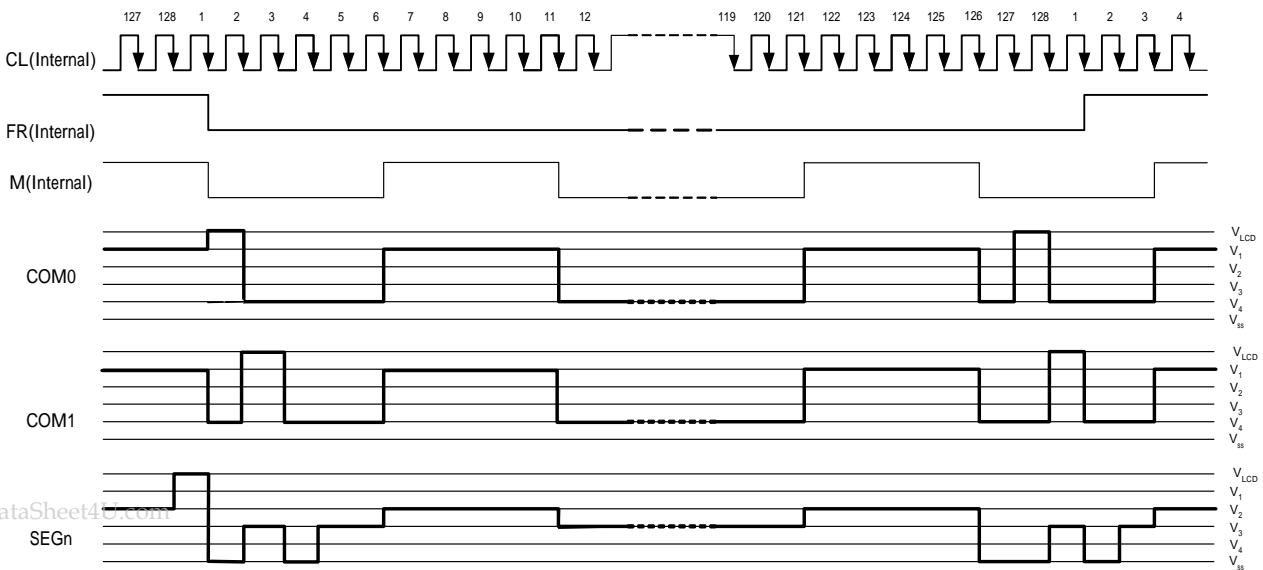
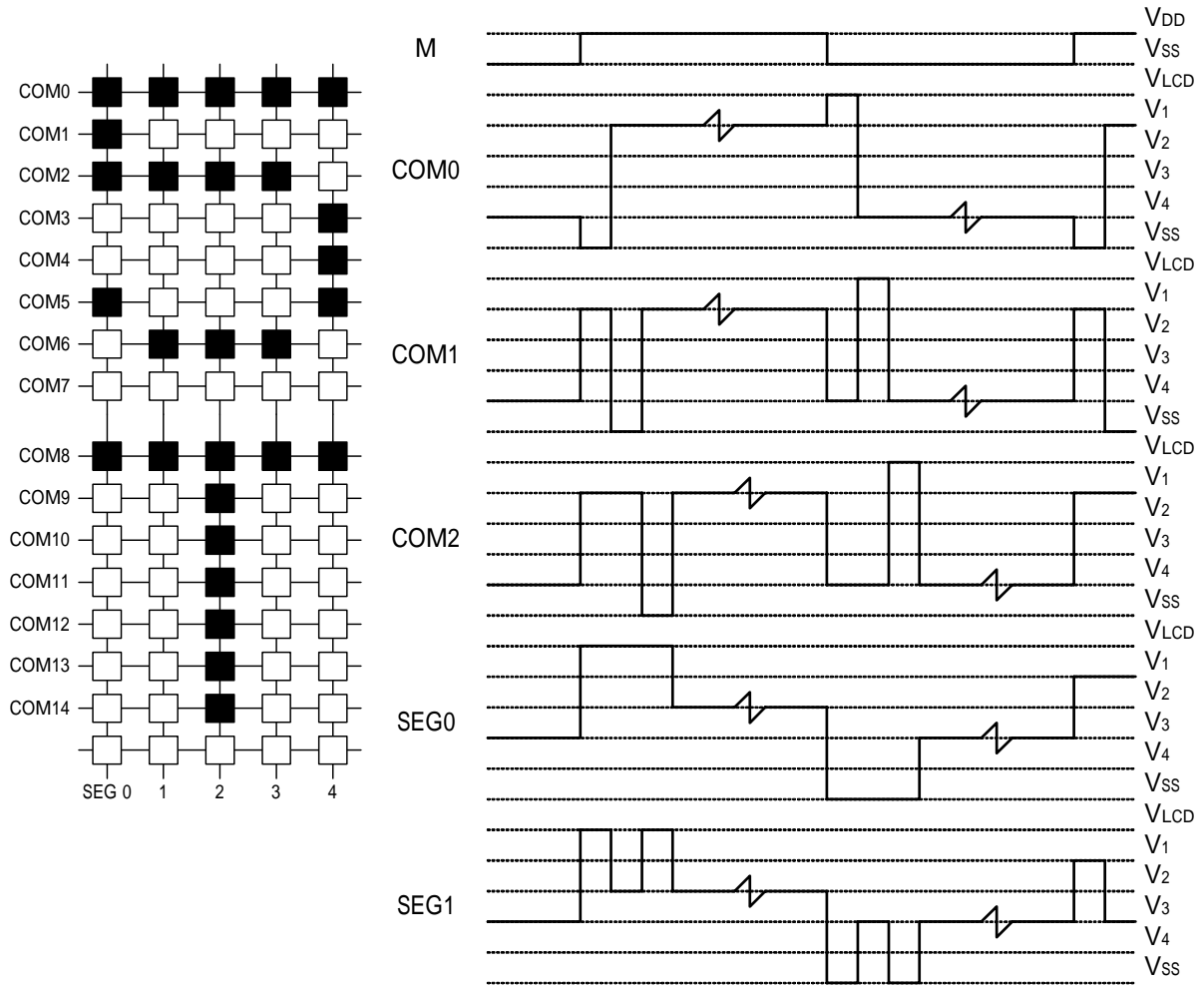


Figure 7.8.2 N-Line Inversion Driving Waveform (N=5, Duty Ratio=1/128)

7.9 Liquid Crystal drive Circuit

This driver circuit is configured by 132-channel common drivers and 396-channel segment drivers. This LCD panel driver voltage depends on the combination of display data and M signal.



7.10 Liquid Crystal Driver Power Circuit

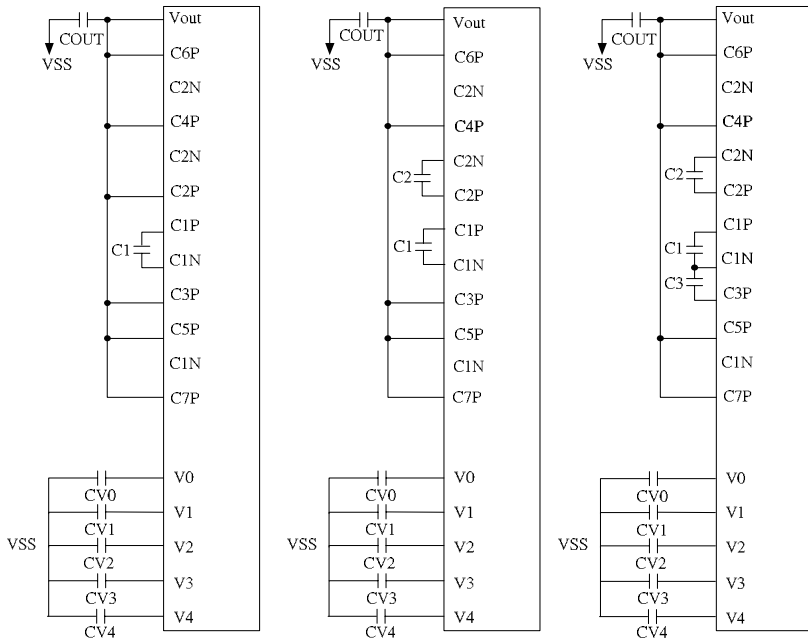
The Power Supply circuits generate the voltage levels necessary to drive liquid crystal driver circuits with low power consumption and the fewest components. There are voltage converter circuits, voltage regulator circuits, and voltage follower circuits. They are controlled by power control instruction. For details, refers to "Instruction Description". Table 7.10.1 shows the referenced combinations in using Power Supply circuits.

Table 7.10.1 Recommended Power Supply Combinations

User setup	Power control (VC VR VF)	V/C circuits	V/R circuits	V/F circuits	VLCD	V0	V1 to V4
Only the internal power supply circuits are used	1 1 1	ON	ON	ON	To series a capacitor to GND	To series a capacitor to GND	To series a capacitor to GND
Only the voltage regulator circuits and voltage follower circuits are used	0 1 1	OFF	ON	ON	External input	To series a capacitor to GND	To series a capacitor to GND
Only the voltage follower circuits are used	0 0 1	OFF	OFF	ON	Open	External input	To series a capacitor to GND
Only the external power supply circuits are used	0 0 0	OFF	OFF	OFF	Open	External input	External input

7.10.1 Voltage Converter Circuits

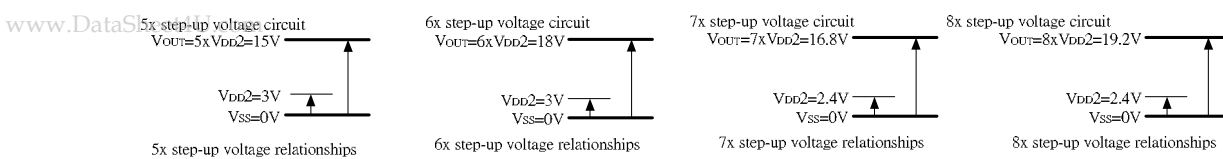
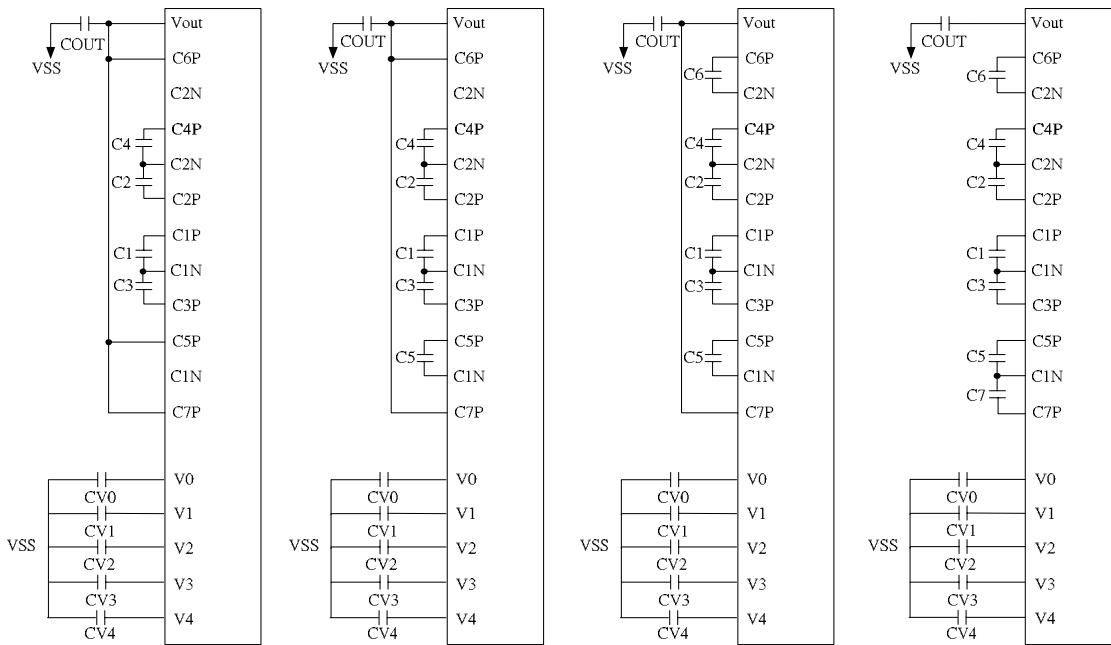
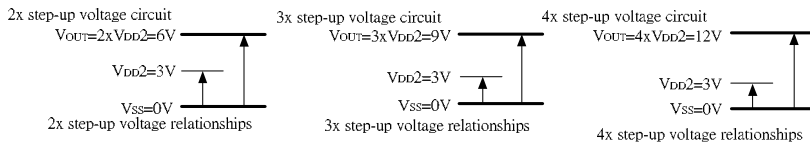
The Step-up Voltage Circuits



The critical operating voltage of capacitor is determined by following calculations.

- Booster capacitors:
- $C1 > VDD2 \times 1$
 - $C2 > VDD2 \times 2$
 - $C3 > VDD2 \times 3$
 - $C4 > VDD2 \times 4$
 - $C5 > VDD2 \times 5$
 - $C6 > VDD2 \times 6$
 - $C7 > VDD2 \times 7$
 - $COUT > VDD2 \times \text{Booster Step}$

- Follower output capacitors:
- $CV0 > V0$
 - $CV1 > V0 \times [(N-1)/N]$
 - $CV2 > V0 \times [(N-2)/N]$
 - $CV3 > V0 \times [2/N]$
 - $CV4 > V0 \times [1/N]$
 - note: $N = \text{VLCID Bias}$



7.10.2 Voltage Regulator Circuits

SET VOP (SETVOP)

The set VOP function is used to program the optimum LCD supply voltage V0.

SETVOP

Reset state of Vop[8:0] is 257DEC = 13.88V.

The VOP value is programmed via the Vop[8:0] register.

$$V0 = a + (Vop[8:6]Vop[5:0]) \cdot b$$

Ex: Vop[5:0]=000001, Vop[8:6]=100

→ Vop [8:0]=100000001

→ $3.6 + 257 \times 0.04 = 13.88$

- a is a fixed constant value (see table 7.10.2).
- b is a fixed constant value (see table 7.10.2).
- Vop[8:0] is the programmed VOP value. The programming range for Vop[8:0] is 5 to 410 (19Ahex).
- Vop[5:0] is the set contrast value which can be set via the command SETVOP and EEPROM.(See command VOLUP & VOLDOWN)
-

Table 7.10.2

SYMBOL	VALUE	UNIT
a	3.6	V
b	0.04	V

The Vop[8:0] value must be in the VOP programming range as given in Figure 7.10.2. Evaluating equation (1), values outside the programming range indicated in Figure 7.10.2 may result. Calculated values below 4 will be mapped to Vop[8:0] = 4, resulting Vop[8:0] values higher than 410 will be mapped to Vop[8:0] = 410. (Sitronix suggests that the Vop range is equal 4.5V to 18V.

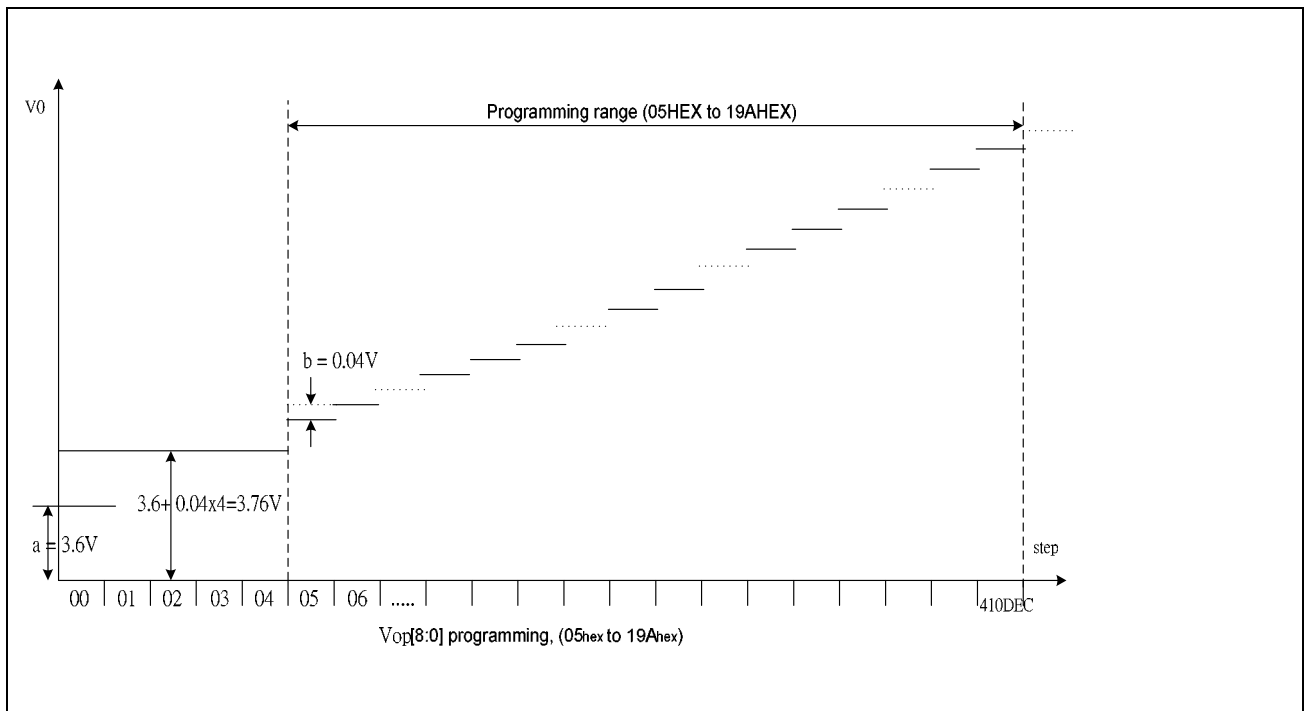


Figure 7.10.2 VOP programming range

As the programming range for internal generated V_0 voltage allows itself value above the max voltage (18V). So users have to ensure, under all conditions, like setting the VPR register and the temperature compensation, the V_0 voltage must remain below 18V including all tolerances.

7.10.3 EEPROM Setting Flow

EEPROM Setting Flow

(Detail flow chart and its application programs, refer page.104)

The ST7636R provide the Write and Read function to write the Electronic Control value and Built-in resistance ratio into and read them from the built-in EEPROM. Using the Write and Read functions, you can store these values appropriate to each LCD panel. This function is very convenient for user in setting from some different panel's voltage. But using this function must attend the setting procedure. Please see the following diagram.

Note1: This setting flow is used for LCM assembler.

Note2: When writing value to EEPROM, the voltage of VDD2~VDD5 (Analog power) = 2.8V~3.0V when Booster x7, and VDD2~VDD5 (Analog power) = 3.3V when Booster x6.

Note3: When writing value to EEPROM, the Booster must turn ON, Regulator and Follower must turn OFF, and Display also must turn OFF.

Note4: When writing value to EEPROM, the voltage of VLCD must be more than 18V (Booster efficiency must be concerned).

Note5: To avoid some errors during IC operation, EEPROM shouldn't be written without preceding loading correctly register values from EEPROM.

Note6: If the EEPROM is exposed to a high temperature for hours, data in the memory cell may probably be lost before the data retention guarantee period. To retain data in the memory cell, keep the mamory cell below 90 . The data retention guarantee period is specified including the retention period.

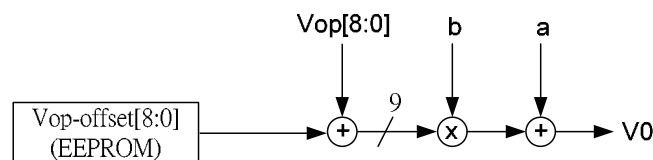


Figure 7.10.5 EC value control for different modules by loading EEPROM offset

7.11 RESET CIRCUIT

When Power is Turned On

Input power (VDD1~VDD5)



Be sure to apply POWER-ON RESET (RESET=LOW)



< Display Setting 1 >

Display control (DISCTL)

Setting clock dividing ratio :

Duty setting :

Setting reverse rotation number of line :

Common scan direction (COMSCN)

Setting scan direction :

Oscillation on (OSCON) :



Sleep-out (SLIPOUT) :



< Power Supply Setting >

Electronic volume control (VOLCTR)

Setting volume value :

Setting built-in resistance value :

Power control (PWRCTR)

Setting operation of power supply circuit :



< Display Setting 2 >

Normal rotation of display (DISNOR) / inversion of display (DISINV) :

Partial-in (PTLIN) / Partial-out (PLOUT)

Setting fix area :

Area scroll set (ASCSET)

Setting area scroll region :

Setting area scroll type :

Scroll start set (SCSTART)

Setting scroll start address :



< Display Setting 3 >

Data control (DATCTL)

Setting normal radiation / inversion of page address :

Setting normal radiation / inversion of column address :

<< State after reset >>

2 divisions

1/4

11H reverse rotations

COM0→COM65, COM66→COM131

Oscillation off

Sleep-in

<< State after reset >>

0

0 (3.76)

ALL OFF

<< State after reset >>

Normal rotation of display

Partial-out

0

Full-screen scroll

0

<< State after reset >>

Normal rotation

Normal rotation

ST7636R

Setting direction of address scanner :

Setting RGB arrangement : Column direction

Setting gradation : RGB

65K-color position set (RGBSET8) 65K

Setting color position at 65K-color :



All 0

< RAM Setting >

Page address set (PASET)

<< State after reset >>

Setting start page address :

Setting end page address :

0

Column address set (PASET)

0

Setting start column address :

Setting end column address :

0



0

< RAM Write >

Memory write command (RAMWR)

<< State after reset >>

Writing displayed data : repeat as many as the number needed and exit by entering other command.



< Waiting (approximately 100ms) >

Wait until the power supply voltage has stabilized.

Enter the power supply control command first, then wait at least 100ms before entering the Display ON command when the built-in power supply circuit operates. If you do not wait, an unwanted display may appear on the liquid crystal panel.



Display on (DISON) :

Display off

Note:

1. If changes are unnecessary after reset, command input is unnecessary.
2. Detail initial program please refer page.70

8. COMMANDS

8.1 Command table

Ext=0																
Command	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function	Hex	Parameter	Index	
DISON	0	1	0	1	0	1	0	1	1	1	1	Display On	AF	None	1	
DISOFF	0	1	0	1	0	1	0	1	1	1	0	Display Off	AE	None	2	
DISNOR	0	1	0	1	0	1	0	0	1	1	0	Normal Display	A6	None	3	
DISINV	0	1	0	1	0	1	0	0	1	1	1	Inverse Display	A7	None	4	
COMSCN	0	1	0	1	0	1	1	1	0	1	1	Com Scan Direction	BB	1 byte	5	
DISCTR1	0	1	0	1	1	0	0	1	0	1	0	Display Control_1	CA	3 byte	6	
SLPP	0	1	0	0	0	0	0	0	1	0	0	Sleep In/Out Preparation	04	1 byte	7	
SLPIN	0	1	0	1	0	0	1	0	1	0	1	Sleep In	95	None	8	
SLPOUT	0	1	0	1	0	0	1	0	1	0	0	Sleep Out	94	None	9	
PASET	0	1	0	0	1	1	1	0	1	0	1	Page Address Set	75	2 byte	10	
CASET	0	1	0	0	0	0	1	0	1	0	1	Column Address Set	15	2 byte	11	
DATCTL	0	1	0	1	0	1	1	1	1	0	0	Data Scan Direction	BC	3 byte	12	
RAMWR	0	1	0	0	1	0	1	1	1	0	0	Writing to Memory	5C	Data	13	
RAMRD	0	1	0	0	1	0	1	1	1	0	1	Reading from Memory	5D	Data	14	
PLTIN	0	1	0	1	0	1	0	1	0	0	0	Partial display in	A8	2 byte	15	
PLTOUT	0	1	0	1	0	1	0	1	0	0	1	Partial display out	A9	None	16	
RMWIN	0	1	0	1	1	1	0	0	0	0	0	Read Modify Write In	E0	None	17	
RMWOUT	0	1	0	1	1	1	0	1	1	1	0	Read Modify Write Out	EE	None	18	
ASCSET	0	1	0	1	0	1	0	1	0	1	0	Area Scroll Set	AA	4 byte	19	
SCSTART	0	1	0	1	0	1	0	1	0	1	1	Scroll Start Set	AB	1 byte	20	
OSCON	0	1	0	1	1	0	1	0	0	0	1	Internal OSC on	D1	None	21	
OSCOFF	0	1	0	1	1	0	1	0	0	1	0	Internal OSC off	D2	None	22	
PWRCTL	0	1	0	0	0	1	0	0	0	0	0	Power Control	20	1 byte	23	
VOLCTR	0	1	0	1	0	0	0	0	0	0	1	EC control	81	2 byte	24	
VOLUP	0	1	0	1	1	0	1	0	1	1	0	EC increase 1	D6	None	25	
VOLDOWN	0	1	0	1	1	0	1	0	1	1	1	EC decrease 1	D7	None	26	
STREAD	0	0	1	Status Read								Status Read			27	
EPSRRD1	0	1	0	0	1	1	1	1	1	0	0	READ Register1	7C	None	28	
EPSRRD2	0	1	0	0	1	1	1	1	1	0	1	READ Register2	7D	None	29	
NOP	0	1	0	0	0	1	0	0	1	0	1	NOP Instruction	25	None	30	
EEOK	0	1	0	0	0	0	0	0	1	1	1	EEPROM Function Start	07	1 byte	31	
RESERVED	0	1	0	1	0	0	0	0	0	1	0	Do not Use	82		32	
AUSAM	0	1	0	0	1	1	0	0	0	0	0	Auto-sampling	60	1 byte	33	

Ext=1																
Command	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function	Hex	Parameter	Index	
Frame1 Set	0	1	0	0	0	1	0	0	0	0	0	FRAME 1 PWM Set	20	16 byte	1	
Frame2 Set	0	1	0	0	0	1	0	0	0	0	1	FRAME 2 PWM Set	21	16 byte	2	
Frame3 Set	0	1	0	0	0	1	0	0	0	1	0	FRAME 3 PWM Set	22	16 byte	3	
Frame4 Set	0	1	0	0	0	1	0	0	0	1	1	FRAME 4 PWM Set	23	16 byte	4	
ANASET	0	1	0	0	0	1	1	0	0	1	0	Analog Set	32	3 byte	5	
EPCTIN	0	1	0	1	1	0	0	1	1	0	1	Control EEPROM	CD	1 byte	6	
EPCOUT	0	1	0	1	1	0	0	1	1	0	0	Cancel EEPROM	CC	None	7	
EPMWR	0	1	0	1	1	1	1	1	1	0	0	Write to EEPROM	FC	None	8	
EPMRD	0	1	0	1	1	1	1	1	1	0	1	Read from EEPROM	FD	None	9	
DISCTR2	0	1	0	1	1	1	1	0	0	1	1	Display Control_2	F3	1 byte	10	
DISPADJ	0	1	0	1	1	1	1	1	0	1	0	Display Performance Adjustment	FA	1 byte	11	
IIPP	0	1	0	1	1	1	1	0	1	0	0	Internal Initialize Preparation	F4	1 byte	12	

Ext=1 or Ext=0																
Command	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function	Hex	Parameter	Index	
Ext In	0	1	0	0	0	1	1	0	0	0	0	Ext=0 Set	30	None	--	
Ext Out	0	1	0	0	0	1	1	0	0	0	1	Ext=1 Set	31	None	--	

8.2 EXT="0" Function Description

(1) Display ON (DISON) Command: 1; Parameter: None (AFH)

It is used to turn the display on. When the display is turned on, segment outputs and common outputs are generated at the level corresponding to the display data and display timing. You can't turn on the display as long as the sleep mode is selected. Thus, whenever using this command, you must cancel the sleep mode first.

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	0	1	0	1	1	1	1

(2) Display OFF (DISOFF) Command: 1; Parameter: None (AEH)

It is used to forcibly turn the display off. As long as the display is turned off, every on segment and common outputs are forced to VSS level.

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	0	1	0	1	1	1	0

(3) Normal display (DISNOR) Command: 1; Parameter: None (A6H)

It is used to normally highlight the display area without modifying contents of the display data RAM.

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	0	1	0	0	1	1	0

(4) Inverse display (DISINV) Command: 1; Parameter: None (A7)

It is used to inversely highlight the display area without modifying contents of the display data RAM. This command does not invert non-display areas in case of using partial display.

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	0	1	0	0	1	1	1

(5) Common scan (COMSCAN) Command: 1; Parameter: 1 (BBH)

It is used to specify the common output direction in the pin of CSEL = L. This command helps increasing degrees of freedom of wiring on the LCD panel.

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	1	0	1	1	1	0	1	1	-
Parameter1 (P1)	1	1	0	*	*	*	*	*	P12	P11	P10	Command Scan direction

When CSEL=0 configuration is selected, pins and common outputs are scanned in the order shown below.

P12	P11	P10	Common scan direction					
			COM0 pin	COM65 pin	COM66 pin	COM131 pin		
0	0	0	0	→	65	66	→	131
0	0	1	0	→	65	131	→	66
0	1	0	65	→	0	66	→	131
0	1	1	65	→	0	131	→	66

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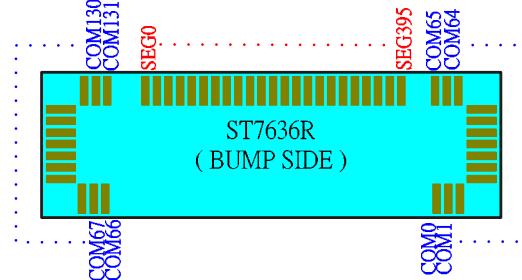
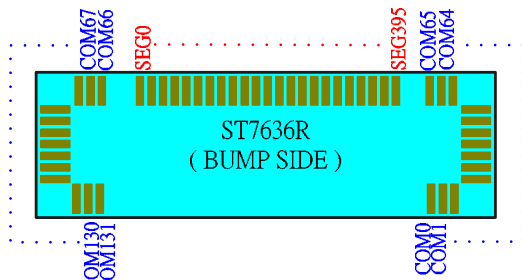
Common scan direction

Original graphic :



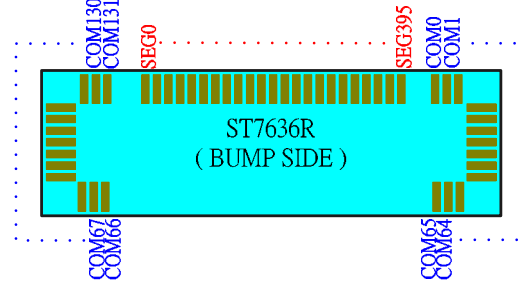
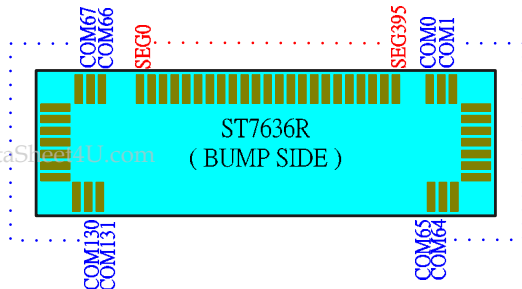
P12:P11:P10:0:0 (0→65,66→131)

P12:P11:P10:0:1 (0→65, 131→66)



P12:P11:P10:0:1:0 (65→0, 66→131)

P12:P11:P10:0:1:1 (65→0, 131→66)



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Figure 8.2.1 Common scan direction configuration when CSEL=0

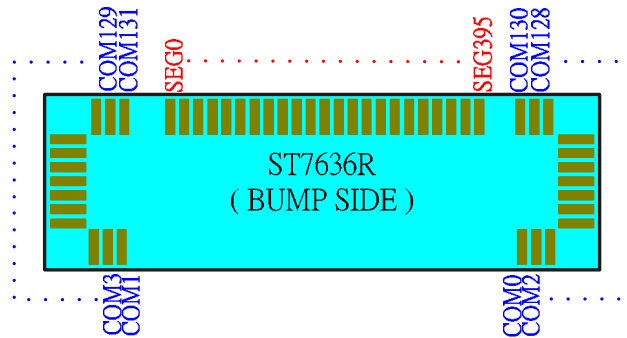


Figure 8.2.2 Common scan direction configuration when CSEL=1
Note : under CSEL=1 configuration, command #BBH will have no effect upon IC operation.
The common scan direction is fixed.

(6) Display control_1 (DISCTR1) Command: 1; Parameter: 3 (CAH)

This command and succeeding parameters are used to perform the display timing-related setups. This command must be selected before using SLPOUT. Don't change this command while the display is turned on.

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	1	1	0	0	1	0	1	0	-
Parameter1(P1)	1	1	0	*	*	*	P14	P13	P12	*	*	CL dividing ratio, F1 and F2 drive pattern.
Parameter2(P2)	1	1	0	*	*	P25	P24	P23	P22	P21	P20	Drive duty
Parameter3(P3)	1	1	0	*	*	*	P34	P33	P32	P31	P30	FR inverse-set value 1 (value 2 is in EXT="1" mode)

P1: it is used to specify the CL dividing ratio.

P14, P13, P12: CL dividing ratio. They are used to change number of dividing stages of external or internal clock.

P14	P13	P12	CL dividing ratio
0	0	0	Not divide
0	0	1	2 divisions
0	1	0	4 divisions
0	1	1	8 divisions

P2: It is used to specify the duty of the module on block basis.

Duty	*	*	P25	P24	P23	P22	P21	P20	(Numbers of display lines)/4-1
Example: 1/128 duty	0	0	0	1	1	1	1	1	128/4-1=31

This will output driving voltage waveforms from com0 to com127.

P3: It is used to specify the number of lines to be inversely highlighted on LCD panel from P34 to P30

(Lines can be inversely highlighted in the range of 2 to 128 and P12 to P11 could be set in EXT="1" mode)

Define example	EXT=1 (command= F3H)			EXT=0 (command= CAH)					
	P12	P11	P10	P34	P33	P32	P31	P30	
Inversely highlighted line	P12	P11	P10	P34	P33	P32	P31	P30	Inversely highlighted lines-1
Example: 0AH	0	0	0	0	1	0	1	0	11-1=10
Example: 8CH	1	0	0	0	1	1	0	0	77-1=76

In the default, 0 inverse highlight lines are selected.

P34="0": Inversion occurs every frame. P34="1": Independent from frames.

(7) Sleep In/Out Preparation (SLPP) Command: 1; Parameter: 1 (04H)

Using this command to setup ready status for sleep-in or sleep out.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	0	0	0	0	1	0	0	-
Parameter(P1)	1	1	0	0	0	1	1	1	1	1	P10	Sleep in/out ready

P10 = "1": Ready for sleep in. P10 = "0": Ready for sleep out.

Parameter 3FH is used to initialize sleep-in sequencing, and parameter 3EH is used to initialize sleep-out sequencing.

(8) Sleep in (SPLIN) Command: 1; Parameter: None (95H)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	0	0	1	0	1	0	1

(9) Sleep out (SLPOUT) Command: 1; Parameter: None (94H)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	0	0	1	0	1	0	0

(10) Page address set (PASET) Command: 1; Parameter: 2 (75H)

When MPU makes access to the display data RAM, this command and succeeding parameters are used to specify the page address area. As the addresses are incremented from the start to the end page in the page-direction scan, the column address is incremented by 1 and the page address is returned to the start page.

Note: that the start and end page must be specified as a pair. Also, the relation "start page < end page" must be maintained.

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	1	1	1	0	1	0	1	-
Parameter1(P1)	1	1	0	P17	P16	P15	P14	P13	P12	P11	P10	Start page
Parameter2(P2)	1	1	0	P27	P26	P25	P24	P23	P22	P21	P20	End page

(11) Column address set (CASET) Command: 1; Parameter: 2 (15H)

When MPU makes access to the display data RAM, this command and succeeding parameters are used to specify the column address area. As the addresses are incremented from the start to the end column in the column-direction scan, the page address is incremented by 1 and the column address is returned to the start column.

Note: that the start and end column must be specified as a pair. Also, the relation “start column < end column” must be maintained.

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	0	0	1	0	1	0	1	-
Parameter1(P1)	1	1	0	P17	P16	P15	P14	P13	P12	P11	P10	Start address
Parameter2(P2)	1	1	0	P27	P26	P25	P24	P23	P22	P21	P20	End address

(12) Data control (DATCTL) Command: 1;Parameter: 3 (BCH)

This command and succeeding parameters are used to perform various setups needed when MPU operates display data stored on the built-in RAM.

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	1	0	1	1	1	1	0	0	-
Parameter1(P1)	1	1	0	*	*	*	*	*	P12	P11	P10	Normal/inverse display of page / column address and address scan direction.
Parameter2(P2)	1	1	0	*	*	*	*	*	*	*	P20	RGB arrangement
Parameter3(P3)	1	1	0	*	*	*	*	*	P32	P31	P30	Gray-scale setup

P1: It is used to specify the normal or inverse display of the page / column address and also to specify the address scanning direction.

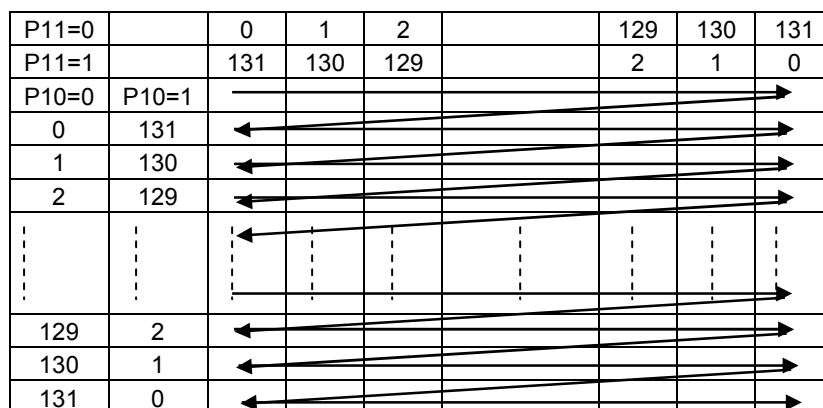
P10: Normal/inverse display of the page address. P10=0: Normal and P10=1: Inverse

P11: Normal/reverse turn of column address. P11=0: Normal rotation and P11=1: Reverse rotation.

P12: Address-scan direction. P12=0: In the column direction and P12=1: In the page direction.

Page address and page-address scan direction

P12=0 Column direction



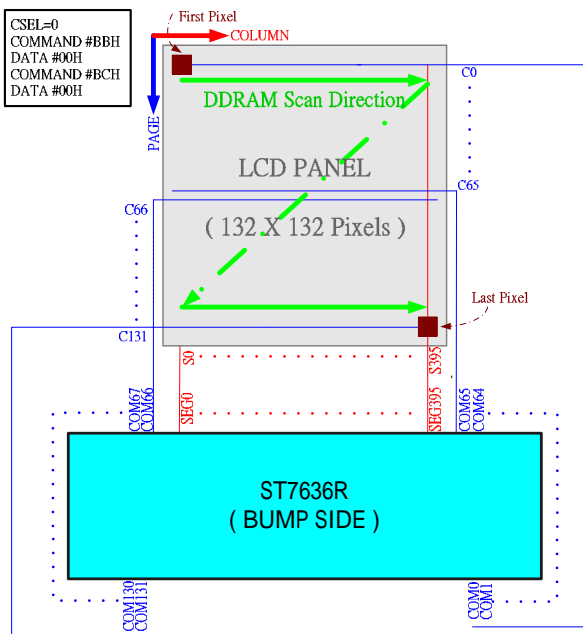
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P12=1 Page direction

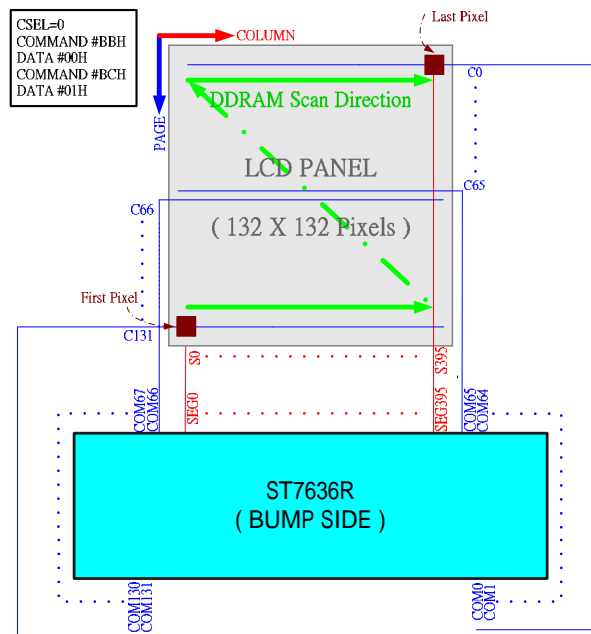
P11=0		0	1	2		129	130	131
P11=1		131	130	129		2	1	0
P10=0	P10=1							
0	131							
1	130							
2	129							
⋮	⋮							
129	2							
130	1							
131	0							

P2: RGB arrangement. This parameter allows you to change RGB arrangement of data which is going to be written into RAM, and therefore causes the inverse RGB rotation of the segment output of ST7636R. You can fit RGB arrangement on the LCD panel according to this parameter setting.

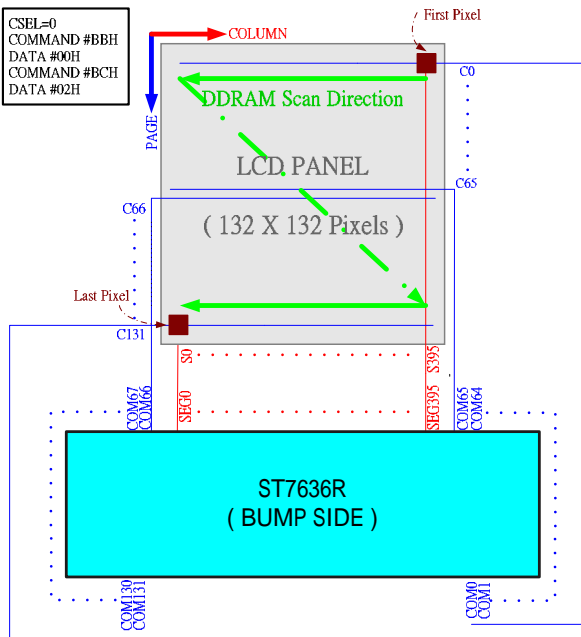
P20	SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	...	SEG395
0	R	G	B	R	G	B	R	G	...	B
1	B	G	R	B	G	R	B	G	...	R



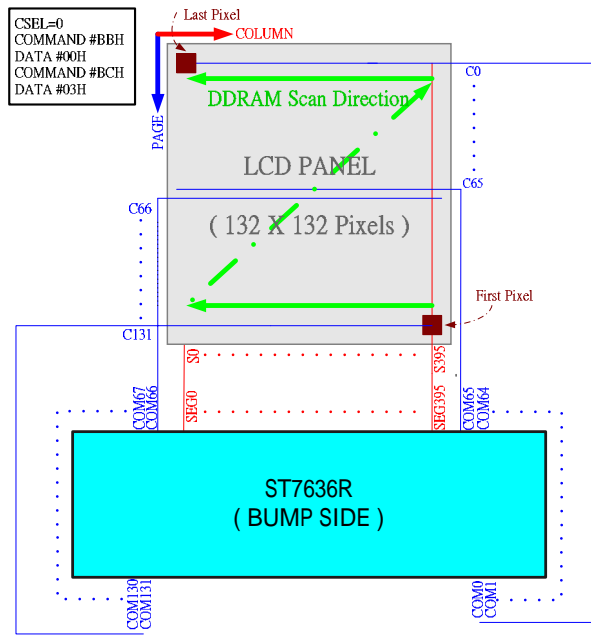
(a) COMMAND #BCH, DATA #00H



(b) COMMAND #BCH, DATA #01H



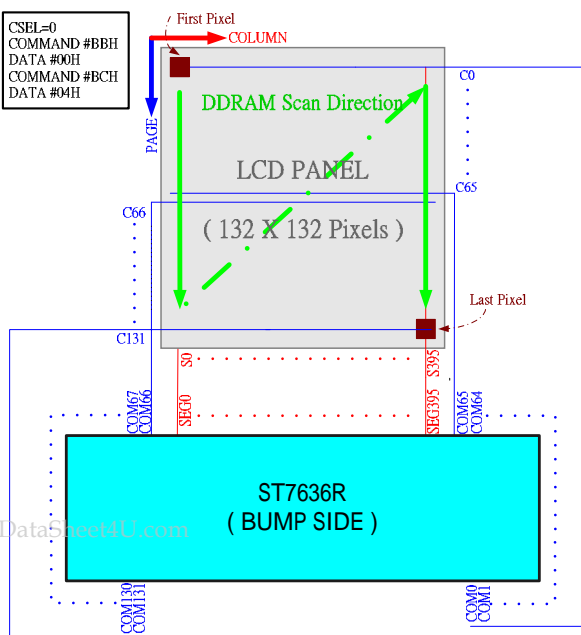
(c) COMMAND #BCH, DATA #02H



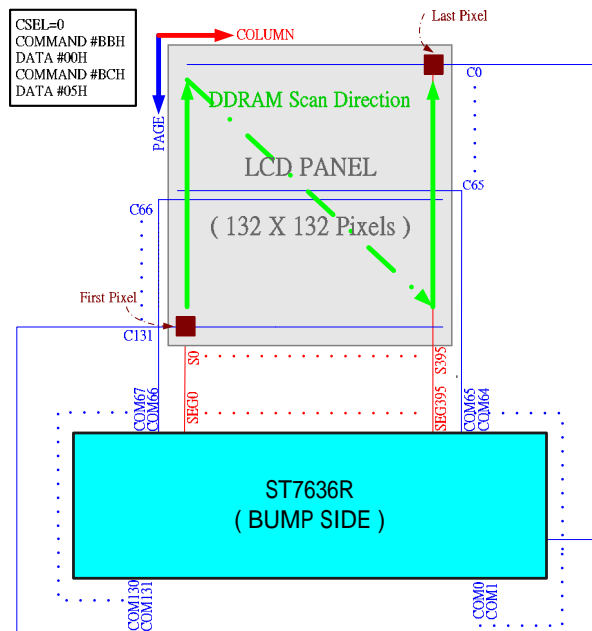
(d) COMMAND #BCH, DATA #03H

Figure 8.2.3 Different RAM accessing setup when CSEL=0 under COMMAND #BBH, DATA #00H

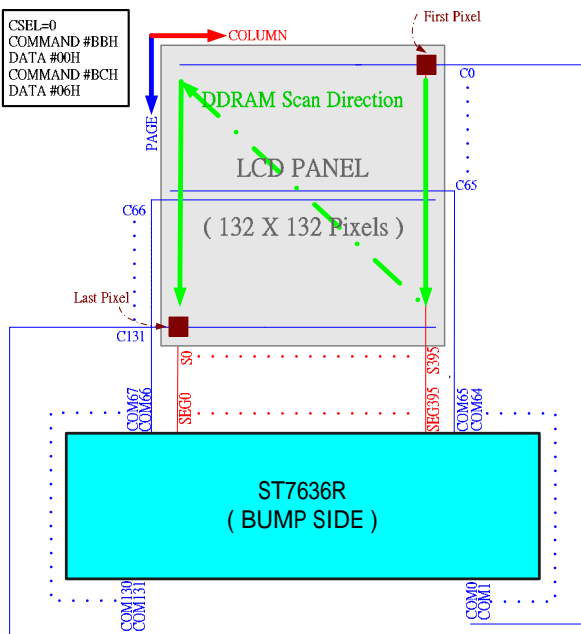
- (a) COMMAND #BCH, DATA #00H
- (b) COMMAND #BCH, DATA #01H
- (c) COMMAND #BCH, DATA #02H
- (d) COMMAND #BCH, DATA #03H



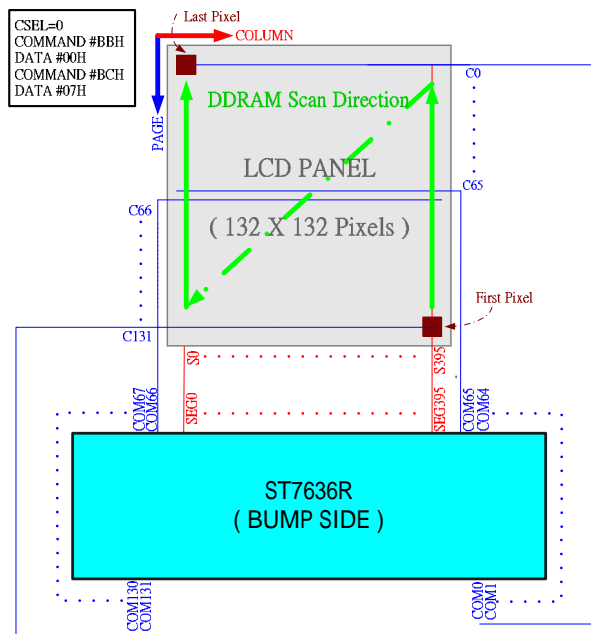
(e) COMMAND #BCH, DATA #04H



(f) COMMAND #BCH, DATA #05H



(g) COMMAND #BCH, DATA #06H



(h) COMMAND #BCH, DATA #07H

Figure 8.2.3 Different RAM accessing setup when CSEL=0 under COMMAND #BBH, DATA #00H (continue)

- (e) COMMAND #BCH, DATA #04H
- (f) COMMAND #BCH, DATA #05H
- (g) COMMAND #BCH, DATA #06H
- (h) COMMAND #BCH, DATA #07H

P3: Gray scale setup. Using this parameter, you can select the 4K, 65K, 262K, and 16M display mode depending on the difference in RGB data arrangement.

P32	P31	P30	Numbers of gray-scale
0	0	1	64-gray 65K
0	1	0	64-gray 262K
1	0	0	64-gray 16M
1	0	1	16-gray 4K Type A
1	1	0	16-gray 4K Type B

(13) Memory write (RAMWR) Command: 1; Parameter: Numbers of data written (5CH)

When MPU writes data to the display memory, this command turns on the data entry mode. Entering this command always sets the page and column address at the start address. You can rewrite contents of the display data RAM by entering data succeeding to this command. At the same time, this operation increments the page or column address as applicable. The write mode is automatically cancelled if any other command is entered.

1. 8-bit bus

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	1	0	1	1	1	0	0	-
Parameter	1	1	0	Data to be written							Data to be written	

2. 16-bit bus

	A0	RD	RW	D15	D14	...	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	*	*	...	*	*	0	1	0	1	1	1	0	0	Memory write
parameter	1	1	0	Data to be written												Write data	

(14) Memory read (RAMRD) Command: 1; Parameter: Numbers of data read (5DH)

When MPU read data from the display memory, this command turns on the data read mode. Entering this command always sets the page and column address at the start address. After entering this command, you can read contents of the display data RAM. At the same time, this operation increments the page or column address as applicable. The data read mode is automatically cancelled if any other command is entered.

1. 8-bit bus

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	1	0	1	1	1	0	1	-
Parameter	1	0	1	Data to be read							Data to be read	

2. 16-bit bus

	A0	RD	RW	D15	D14	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	*	*	*	*	*	0	1	0	1	1	1	0	1	Memory read
parameter	1	0	1	Data to be read												Read data	

(15) Partial in (PTLIN) Command: 1; Parameter: 2 (A8H)

This command and succeeding parameters specify the partial display area. This command is used to turn on partial display of the screen (dividing screen by lines) in order to save power. Since ST7636R processes the liquid crystal display signal on 4-line basis (block basis), the display and non-display areas are also specified on 4-bit line (block basis).

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	1	0	1	0	1	0	0	0	-
Parameter(P1)	1	1	0	*	*	P15	P14	P13	P12	P11	P10	Start block address
Parameter(P2)	1	1	0	*	*	P25	P24	P23	P22	P21	P20	End block address

A block address that can be specified for the partial display must be the display one (don't try to specify an address not to be displayed when scrolled).

(16) Partial out (PTLOUT) Command: 1; Parameter: 0 (A9H)

This command is used to exit from the partial display mode.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	0	1	0	1	0	0	1

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(17) Read modify write in (RMWIN) Command: 1; Parameter: 0 (E0H)

This command is used along with the column address set command, page address set command and read modify write out command. This function is used when frequently modifying data to specify a specific display area such as blinking cursor. First set a specific display area using the column and page address commands. Then, enter this command to set the column and page addresses at the start address of the specific area. When this operation is complete, the column (page) address won't be modified by the display data read command. It is incremented only when the display data write command is used. You can cancel this mode by entering the read modify write out or any other command.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	1	1	0	0	0	0	0

(18) Read modify write out (RMWOUT) Command: 1; Parameter: 0 (EEH)

Enter this command cancels the read modify write mode

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	1	1	0	1	1	1	0

(19) Area scroll set (ASCSET) Command: 1; Parameter: 4 (AAH)

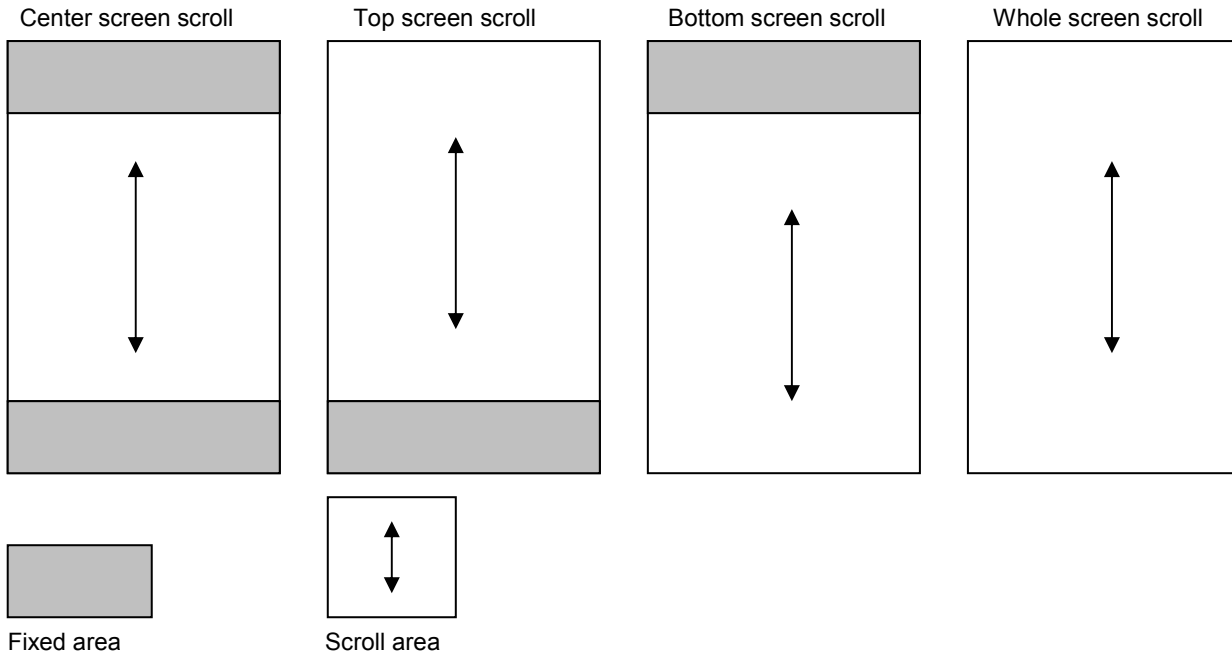
It is used when scrolling only the specified portion of the screen (dividing the screen by lines). This command and succeeding parameters specify the type of area scroll, fix area and scroll area.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	1	0	1	0	1	0	1	0	-
Parameter(P1)	1	1	0	*	*	P15	P14	P13	P12	P11	P10	Top block address
Parameter(P2)	1	1	0	*	*	P25	P24	P23	P22	P21	P20	Bottom block address
Parameter(P3)	1	1	0	*	*	P35	P34	P33	P32	P31	P30	Number of specified blocks
Parameter(P4)	1	1	0	*	*	*	*	*	*	P41	P40	Area scroll mode

P4: It is used to specify an area scroll mode.

P41	P40	Type of area scroll
0	0	Center screen scroll
0	1	Top screen scroll
1	0	Bottom screen scroll
1	1	Whole screen scroll

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Since ST7636R processes the liquid crystal display signals on the four-line basis (block basis), FIX and scroll areas are also specified on the four-line basis (block basis).

DDRAM address corresponding to the top FIX area is set in the block address incrementing direction starting with 0 block. DDRAM address corresponding to the bottom FIX area is set in the block address decreasing direction starting with 32st block. Other DDRAM blocks excluding the top and bottom FIX areas are assigned to the scroll + background areas.

P1: It is used to specify the top block address of the scroll + background areas. Specify the 0th block for the top screen scroll or whole screen scroll.

P2: It specifies the bottom address of the scroll+ background areas. Specify the 32th block for the bottom or whole screen scroll.

Required relation between the start and end blocks (top block address < bottom block address) must be maintained.

P3: It specifies a specific number of blocks {Numbers of (Top FIX area + Scroll area) block-1}. When the bottom scroll or whole screen scroll, the value is identical with P2.

You can turn on the area scroll function by executing the area scroll set command first and then specifying the display start block of the scroll area with the scroll start set command.

[Area Scroll Setup Example]

In the center screen scroll of 1/120 duty (display range: 120 lines=30 blocks), if 8 lines=2 blocks and 8 lines=2 blocks are specified for the top and bottom FIX areas, 104 lines =26 blocks is specified for the scroll areas, respectively, 12 lines = 3 blocks on the DDRAM are usable as the background-area. Value of each parameter at this time is as shown below.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0	
P1	1	1	0	*	*	0	0	0	0	1	0	Top block address = 2
P2	1	1	0	*	*	0	1	1	1	1	0	Bottom block address = 30

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P3	1	1	0	*	*	0	1	1	1	1	0	Number of specific blocks = 30
P4	1	1	0	*	*	*	*	*	*	0	0	Area scroll mode = center

(20) Scroll start address set (SCSTART) Command:1 Parameter: 1 (ABH)

This command and succeeding parameters are used to specify the start block address of the scroll area.

Note: that you must execute this command after executing the area scroll set command. Scroll becomes available by dynamically changing the start block address.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	1	0	1	0	1	0	1	1	-
Parameter(P1)	1	1	0	*	*	P15	P14	P13	P12	P11	P10	Start block address

(21) Internal oscillation on (OSCON) Command: 1; Parameter: 0 (D1H)

This command turns on the internal oscillation circuit. It is valid only when the internal oscillation circuit of CLS = HIGH is used.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	1	0	1	0	0	0	1

(22) Internal oscillation off (OSOFF) Command: 1; Parameter: 0 (D2H)

It turns off the internal oscillation circuit. This circuit is turned off in the reset mode.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	1	0	1	0	0	1	0

(23) Power control set (PWRCTR) Command: 1; Parameter: 1 (20H)

This command is used to turn on or off the Booster circuit, follower voltage, and voltage regulator circuit.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	1	0	0	1	0	0	0	0	0	-
Parameter(P1)	1	1	0	*	*	*	0	P13	0	P11	P10	LCD drive power

P10: It turns on or off the voltage regulator voltage.

P10 = "1": ON. P10 = "0": OFF

P11: It turns on or off the follower circuit.

P11 = "1": ON. P11 = "0": OFF

P13: It turns on or off the Booster.

P13 = "1": ON. P13 = "0": OFF

(24) Electronic volume control (VOLCTR) Command: 1; Parameter: 2 (81H)

The command is used to program the optimum LCD supply voltage VOP (V0) Reference to 7.10.2

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	1	0	0	0	0	0	0	1	-

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Parameter(P1)	1	1	0	*	*	P15	P14	P13	P12	P11	P10	Set Vop[5:0]
Parameter(P2)	1	1	0	*	*	*	*	*	P18	P17	P16	Set Vop[8:6]

(25) Increment electronic control (VOLUP) Command: 1; Parameter: 0 (D6H)

With the VOLUP and VOLDDOWN command the VOP voltage and therewith the contrast of the LCD can be adjusted.

This command increments electronic control value Vop[5:0] of voltage regulator circuit by 1.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	1	0	1	0	1	1	0

If you set the electronic control value to 111111, the control value is set to 000000 after this command has been executed.

(26) Decrement electronic control (VOLDDOWN) Command: 1; Parameter: 0 (D7H)

With the VOLUP and VOLDDOWN command the VOP voltage and therewith the contrast of the LCD can be adjusted.

This command decrements electronic control value Vop[5:0] of voltage regulator circuit by 1.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	1	0	1	0	1	1	1

If you set the electronic control value to 000000, the control value is set to 111111 after this command has been executed.

Table 8.1.1 Possible Vop[5:0] values

Electronic Control Value	Decimal Equivalent	VOP Offset
111111	31	+1240 mV
111110	30	+1200 mV
111101	29	+1160 mV
...
000010	2	+80 mV
000001	1	+40 mV
000000	0	0 mV
111111	-1	-40 mV
111110	-2	-80 mV
...
100010	-30	-1200 mV
100001	-31	-1240 mV
100000	-32	-1280mV

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(27) Status read (STREAD) Command: 1; Parameter: None

It is the command for reading the internal condition of the IC.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	0	1	(8) Status data							

Issue STREAD (Status Read) command only to read the internal condition of the IC. One status data can be displayed depending on the setting. Issue the NOP command after the STREAD (Status Read) command.

The Status data will be composed of 8 bits below:

D7: Area scroll mode	Refer to P41 (ASCSET)	
D6: Area scroll mode	Refer to P40 (ASCSET)	
D5: RMW on/off	0 : Out	1 : In
D4: Scan direction	0 : Column	1 : Page
D3: Display ON/OFF	0 : OFF	1 : ON
D2: EEPROM access	0: OutAccess	1: InAccess
D1: Display normal/inverse	0 : Normal	1 : Inverse
D0: Partial display	0 : OFF	1 : ON

(28) Read Register 1 (EPSRRD1) Command: 1; Parameter: 0 (7CH)

It is the command for reading the Electronic Control values.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	0	1	1	1	1	1	0	0

Issue the EPSRRD1 and then STREAD (Status Read) commands in succession to read the Electronic Control values. One status data can be displayed depending on the setting. Also, always issue the NOP command after the STREAD (Status Read) command.

The Status data will be composed of 8 bits below:

D7: 0	
D6: 0	
D[5:0]: Vop[5:0]	Refer to electronic volume control values Vop[5:0]

(29) Read Register 2 (EPSRRD2) Command: 1 ;Parameter: 0 (7DH)

It is the command for reading ID codes of the ST7636R and the built-in resistance ratio.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	0	1	1	1	1	1	0	1

Issue the EPSRRD2 and then STREAD (Status Read) commands in succession to read IC's ID and the built-in resistance ratio. One status data can be displayed depending on the setting. Also, always issue the NOP command after the STREAD (Status Read) command.

The Status data will be composed of 8 bits below:

D[7:3]: ST7636R ID codes	00001
D[2:0]: Vop[8:6]	Refer to the built-in resistance ratio Vop[8:6]

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(30) Non-operating (NOP) Command: 1; Parameter: 0 (25H)

This command does not affect the operation.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	0	0	1	0	0	1	0	1

This command, however, has the function of canceling the IC test mode. Thus, it is recommended to enter it periodically to prevent malfunctioning due to noise and such.

(31) EEPROM Function Start (EEOK) Command:1;Parameter:1(07H)

In the OTP read/write flow, EEPROM is ready after issuing this command. Its parameter is set to 19H.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	0	0	0	0	1	1	1	-
Parameter(P1)	1	1	0	0	0	0	1	1	0	0	1	19H

(32) Reserved (82H)

Do not use this command.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	0	0	0	0	0	1	0

(33) Auto-sampling (AUSAM) Command: 1; Parameter: None (60H)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	0	1	1	0	0	0	0	0

8.3 EXT="1" Function Description

(1) Set Frame1 value (Frame1 set) Command: 1; Parameter: 16 (20H)

Command	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Frame1 Set	0	1	0	0	0	1	0	0	0	0	0	FRAME 1 PWM Set

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Parameter1(P1)	1	1	0	*	*	*	P14	P13	P12	P11	P10	Set RGB level 0 of 1st frame
Parameter2(P2)	1	1	0	*	*	*	P24	P23	P22	P21	P20	Set RGB level 1 of 1st frame
Parameter15(P15)	1	1	0	*	*	*	P154	P153	P152	P151	P150	Set RGB level 14 of 1st frame
Parameter16(P16)	1	1	0	*	*	*	P164	P163	P162	P161	P160	Set RGB level 15 of 1st frame

(2)Set Frame2 value (Frame2 set) Command: 1; Parameter: 16 (21H)

Command	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
---------	----	----	----	----	----	----	----	----	----	----	----	----------

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Frame2 Set	0	1	0	0	0	1	0	0	0	0	1	FRAME 2 PWM Set
------------	---	---	---	---	---	---	---	---	---	---	---	-----------------

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Parameter1(P1)	1	1	0	*	*	*	P14	P13	P12	P11	P10	Set RGB level 0 of 2nd frame
Parameter2(P2)	1	1	0	*	*	*	P24	P23	P22	P21	P20	Set RGB level 1 of 2nd frame
Parameter15(P15)	1	1	0	*	*	*	P154	P153	P152	P151	P150	Set RGB level 14 of 2nd frame
Parameter16(P16)	1	1	0	*	*	*	P164	P163	P162	P161	P160	Set RGB level 15 of 2nd frame

(3) Set Frame3 value (Frame3 set) Command: 1; Parameter: 16 (22H)

Command	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Frame3 Set	0	1	0	0	0	1	0	0	0	1	0	FRAME 3 PWM Set

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Parameter1(P1)	1	1	0	*	*	*	P14	P13	P12	P11	P10	Set RGB level 0 of 3rd frame
Parameter2(P2)	1	1	0	*	*	*	P24	P23	P22	P21	P20	Set RGB level 1 of 3rd frame
Parameter15(P15)	1	1	0	*	*	*	P154	P153	P152	P151	P150	Set RGB level 14 of 3rd frame
Parameter16(P16)	1	1	0	*	*	*	P164	P163	P162	P161	P160	Set RGB level 15 of 3rd frame

(4) Set Frame4 value (Frame4 set) Command: 1; Parameter: 16 (23H)

Command	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Frame4 Set	0	1	0	0	0	1	0	0	0	1	1	FRAME 4 PWM Set

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Parameter1(P1)	1	1	0	*	*	*	P14	P13	P12	P11	P10	Set RGB level 0 of 4th frame
Parameter2(P2)	1	1	0	*	*	*	P24	P23	P22	P21	P20	Set RGB level 1 of 4th frame
Parameter15(P15)	1	1	0	*	*	*	P154	P153	P152	P151	P150	Set RGB level 14 of 4th frame
Parameter16(P16)	1	1	0	*	*	*	P164	P163	P162	P161	P160	Set RGB level 15 of 4th frame

The default value of RGB level set

	FRAM1 SET	FRAM2 SET	FRAM3 SET	FRAME4 SET
RGB level0	00	00	00	00
RGB level1	02	02	02	02
RGB level2	05	05	05	05
RGB level3	07	07	07	08

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RGB level4	0A	0A	0A	0B
RGB level5	0D	0D	0D	0C
RGB level6	0F	10	0F	10
RGB level7	11	12	11	12
RGB level8	13	14	13	14
RGB level9	16	16	16	15
RGB level10	18	18	18	17
RGB level11	19	19	19	1A
RGB level12	1B	1B	1B	1A
RGB level13	1C	1C	1C	1D
RGB level14	1D	1D	1D	1E
RGB level15	1E	1E	1E	1E

All the modulation range of each level for each frame is from 00'H to 1F'H.

Example : Paint setup

```
void LoadPaint( void )
```

```
{
    Write( COMMAND, 0x0031 );           // Ext = 1

    Write( COMMAND, 0x0020 );           // Palette FRC1 Setup
    Write( DATA, 0x0000 );             // RGB Level0 Setup
    Write( DATA, 0x0002 );             // RGB Level1 Setup
    Write( DATA, 0x0005 );             // RGB Level2 Setup
    .....
    .....
    Write( DATA, 0x001E );             // RGB Level15 Setup

    Write( COMMAND, 0x0021 );           // Palette FRC2 Setup
    Write( DATA, 0x0000 );             // RGB Level0 Setup
    Write( DATA, 0x0002 );             // RGB Level1 Setup
    Write( DATA, 0x0005 );             // RGB Level2 Setup
    .....
    .....
    Write( DATA, 0x001E );             // RGB Level15 Setup

    Write( COMMAND, 0x0022 );           // Palette FRC3 Setup
    Write( DATA, 0x0000 );             // RGB Level0 Setup
    Write( DATA, 0x0002 );             // RGB Level1 Setup
    Write( DATA, 0x0005 );             // RGB Level2 Setup
    .....
    .....
    Write( DATA, 0x001E );             // RGB Level15 Setup

    Write( COMMAND, 0x0023 );           // Palette FRC4 Setup
    Write( DATA, 0x0000 );             // RGB Level0 Setup
    Write( DATA, 0x0002 );             // RGB Level1 Setup
    Write( DATA, 0x0005 );             // RGB Level2 Setup
    .....
    .....
}
```


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```

Write( DATA, 0x001E );           // RGB Level15 Setup

Write( COMMAND, 0x0030 );        // Ext = 0
}

```

(5) Analog set (ANASET) Command 1; Parameter: 3 (32H)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	0	1	1	0	0	1	0	-
Parameter1(P1)	1	1	0	*	*	*	*	*	P12	P11	P10	OSC frequency Adjustment
Parameter2(P2)	1	1	0	*	*	*	*	*	*	P21	P20	Booster Efficiency Set
Parameter3(P3)	1	1	0	*	*	*	*	*	P32	P31	P30	Bias setting

P1: OSC frequency adjustment

P12	P11	P10	CL pin frequency (KHz) : CL dividing ratio setting = 00H (No division)	CL pin frequency (KHz) : CL dividing ratio setting = 04H (Divided by 2)
0	0	0	10.46	5.23
0	0	1	10.82	5.41
0	1	0	11.67	5.84
0	1	1	12.74	6.37
1	0	0	14.03	7.02
1	0	1	15.63	7.82
1	1	0	17.61	8.81
1	1	1	20.32	10.16

OSC frequency can be adjusted by P1 setting and command CAH, see page 51.

The default OSC frequency (CL pin frequency) is 10.46 KHz.

And the frame frequency is from OSC frequency and duty setting, as the formula shown below:

$$\text{Frame frequency} = \text{OSC frequency} / (\text{Duty}+1)$$

Example:

- duty=132, P1 setting=[000], frame frequency=10.46KHz/133~78.64Hz
- duty=128, P1 setting=[101], frame frequency=15.63KHz/129~121.16Hz

P2: Booster Efficiency set

P21	P20	Frequency (Hz)
0	0	Level 1
0	1	Level 2
1	0	Level 3

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1	1	Level 4
---	---	---------

By Booster Stages (2X, 3X, 4X, 5X, 6X, 7X, 8X) and Booster Efficiency (Level1~4) commands, we could easily set the best Booster performance with suitable current consumption. If the Booster Efficiency is set to higher level (level4 is higher than level1). The Boost Efficiency is better than lower level, and it just need few more power consumption current.

P3: Select LCD bias ratio of the voltage required for driving the LCD.

P32	P31	P30	LCD bias
0	0	0	1/12
0	0	1	1/11
0	1	0	1/10
0	1	1	1/9
1	0	0	1/8
1	0	1	1/7
1	1	0	1/6
1	1	1	1/5

(6) Control EEPROM: 1; Parameter: 1 (CDH)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	1	0	0	1	1	0	1
Parameter1(P1)	1	1	0	*	*	P15	*	*	*	*	*

P15: when setting "1" → The Write Enable of EEPROM will be opened.

P15: when setting "0" → The Read Enable of EEPROM will be opened.

(7) Cancel EEPROM Command: 1;Parameter: None (CCH)

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	1	0	0	1	1	0	0

(8) Write data to EEPROM (EPMWR) Command: 1; Parameter: None (FCH)

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	1	1	1	1	1	0	0

(9) Read data from EEPROM (EPMWR) Command: 1; Parameter: None (FDH)

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	1	1	1	1	1	0	1

(10) Display control_2 (DISCTR2) Command: 1; Parameter: 1 (F3H)

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This command is used to extend the higher byte of inversing lines highlighted on LCD panel from P12 to P10 and P33 to P30 (lines can be inversely highlighted in the range of 2 to 128)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	1	1	1	1	0	0	1	1	-
Parameter1(P1)	1	1	0	*	*	*	*	*	P12	P11	P10	FR inverse-set value 2

Define example	EXT=1 (command= F3H)			EXT=0 (command= CAH)					
	P12	P11	P10	P34	P33	P32	P31	P30	
Inversely highlighted line	P12	P11	P10	P34	P33	P32	P31	P30	Inversely highlighted lines-1
Example: 0AH	0	0	0	0	1	0	1	0	11-1=10
Example: 8CH	1	0	0	0	1	1	0	0	77-1=76

In the default, 0 inverse highlight lines are selected.

P34="0": Inversion occurs every frame. P34="1": Independent from frames.

(11) Display performance adjustment (DISPADJ) Command: 1; Parameter: 1 (FAH)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	1	1	1	1	1	0	1	0	Display performance adjustment
Parameter1(P1)	1	1	0	*	*	*	P14	P13	P12	P11	P10	Fine tuning level set

ST7636R provide the function of 32 levels fine tuning to adjust best crosstalk performance for each module. Just like Vop offset for different modules, the fine tuning level value can also be stored in EEPROM, and therefore each module can have its individual setup for best display performance.

Due to IC and module process variation, it's hard for all modules to have same display performance. By using this command, different modules can adjust to the best performance by having different parameters of DISPADJ. When loading EEPROM, this individual parameter can be loaded into IC and best display performance can be achieved. Detail using method please refer ST7636R EEPROM User Manual guide.

(12) Internal Initialize Preparation (IIPP) Command: 1; Parameter: 1 (F4H)

Use this command to set internal initializing for ready status.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	1	1	1	1	0	1	0	0	-
Parameter(P1)	1	1	0	0	1	0	1	1	0	0	0	Internal initialize sequencing

8.4 EXT="0" or "1" Function Description

(1) Extension instruction disable (EXT IN) Command:1 Parameter: None (30H)

Use the "Ext=0" command table

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	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	0	0	1	1	0	0	0	0

(2) Extension instruction enable (EXT OUT) Command:1 Parameter: None (31H)

Use the extended command table (EXT="1")

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	0	0	1	1	0	0	0	1

8.5 Referential Instruction Setup Flow

8.5.1 Initializing with the Built-in Power Supply Circuits

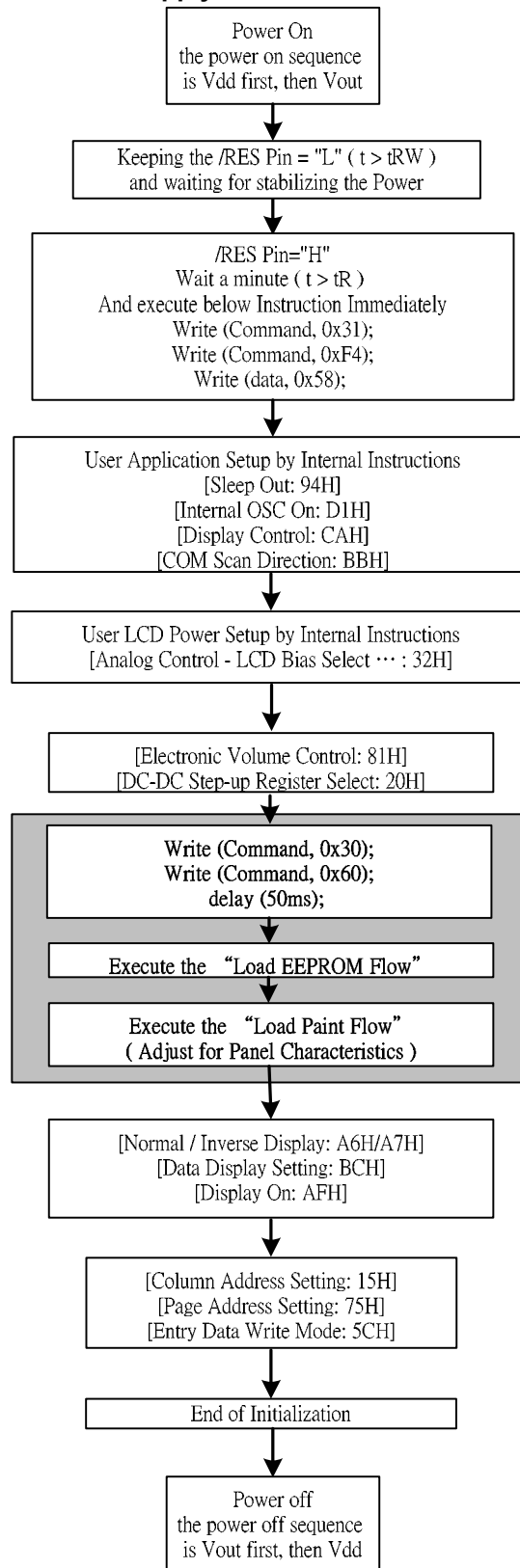


Figure 8.5.1.1 Initializing with the Built-in Power Supply Circuits

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Example : Initial code for 128X128

```
void ST7636R_Init( void )
{
    Write( COMMAND, 0x30 );           // Ext = 0
    Write( COMMAND, 0x04 );           // Sleep In/Out Preparation
    Write( DATA, 0x3e );             // Sleep In/Out Sequencing

    Write( COMMAND, 0x31 );           // Ext = 1
    Write( COMMAND, 0xf4 );           // Internal Initialize Preparation
    Write( DATA, 0x58 );             // Internal Initialize Sequencing

    Write( COMMAND, 0x30 );           // Ext = 0
    Write( COMMAND, 0x94 );           // Sleep Out
    Write( COMMAND, 0xd1 );           // Internal OSC on
    Write( COMMAND, 0xca );           // Display Control
    Write( DATA, 0x00 );             // CL divisions Ratio
    Write( DATA, 0x1f );             // Duty Setting (= 128)
    Write( DATA, 0x00 );             // N-Line Inverse-set value

    Write( COMMAND, 0x31 );           // Ext = 1
    Write( COMMAND, 0x32 );           // Analog Setting
    Write( DATA, 0x00 );             // OSC Frequency adjustment
    Write( DATA, 0x01 );             // Booster Efficiency Setting
    Write( DATA, 0x00 );             // Bias Setting (=1/12)

    Write( COMMAND, 0x30 );           // Ext = 0
    Write( COMMAND, 0x81 );           // Electronic Volume Control
    Write( DATA, 0x1B );             // EV:Vop[5:0]_6bit
    Write( DATA, 0x04 );             // EV:Vop[8:6]_3bit
                                        // Vop is 14.92V under this condition for example

    Write( COMMAND, 0x20 );           // Power Control
    Write( DATA, 0x0b );             // B/F/R = On/On/On

    Write( COMMAND, 0x30 );           // Ext = 0
    Write( COMMAND, 0x60 );           // Auto-sampling
    delay(50000);                     // Delay 50ms
    LoadEEPROM();                     // Load EEPROM (refer page 71)
    LoadPaint();                      // Load Gamma Table Parameter (refer page 64)

    Write( COMMAND, 0x30 );           // Ext = 0
    Write( COMMAND, 0xa7 );           // Inverse Display
    Write( COMMAND, 0xbb );           // Com Scan Direction
    Write( DATA, 0x01 );             // 0~65 / 131~66
    Write( COMMAND, 0xbc );           // Data Scan Direction
    Write( DATA, 0x00 );             // Page / Column Address Setting
    Write( DATA, 0x00 );             // RGB arrangement (0:RGB 1:BGR)
    Write( DATA, 0x01 );             // Gray-scale setup ( 64-gray: 01H)

    Write( COMMAND, 0x75 );           // Page address set
    Write( DATA, 0x00 );             // From page address 0
    Write( DATA, 0x7f );             // to page address 127
    Write( COMMAND, 0x15 );           // Column address set
    Write( DATA, 0x00 );             // From column address 0
    Write( DATA, 0x7f );             // to column address 127

    Write( COMMAND, 0xaf );           // Display On
    Write( COMMAND, 0x30 );           // Ext = 0
}
```

}

Example : Load EEPROM

```
void LoadEEPROM( void )
```

```
{
```

Write(COMMAND, 0x31);	// Ext = 1
Write(COMMAND, 0xcd);	// Enable EEPROM
Write(DATA, 0x00);	//
delay(50000);	// Delay 50ms
Write(COMMAND, 0xfd);	// Load EEPROM
delay(50000);	// Delay 50ms
Write(COMMAND, 0xcc);	// Disable EEPROM
Write(COMMAND, 0x30);	// Ext = 0

```
}
```

8.5.2 Data Displaying

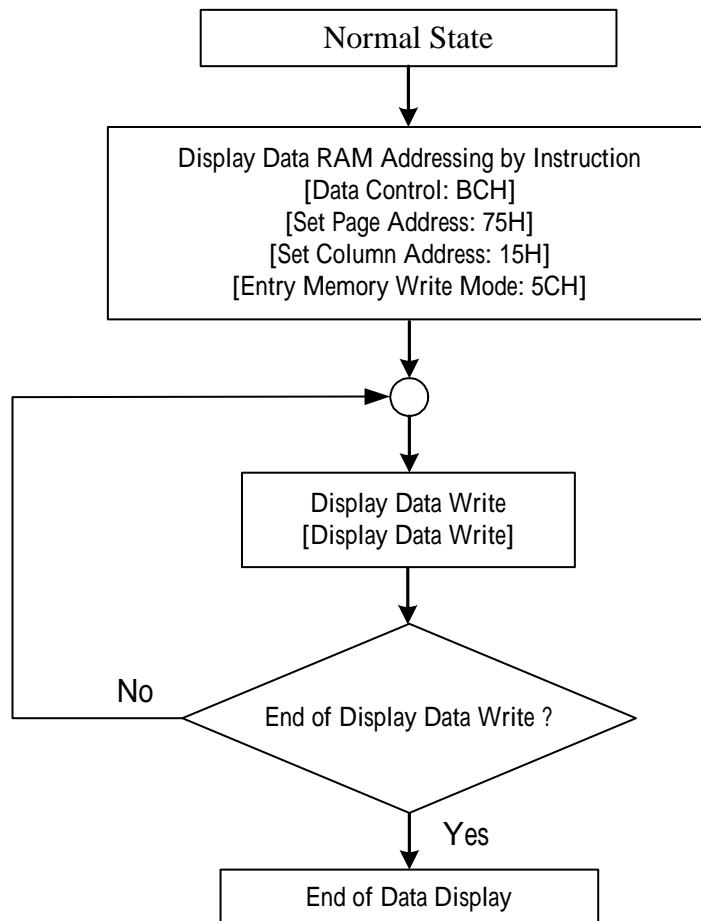


Figure 8.5.2.1 Data Displaying

Example : Display for 128X128

```

void Display( char *pattern )
{
    unsigned char i, j;

    Write( COMMAND, 0x30 );           // Ext = 0
    Write( COMMAND, 0x15 );          // Column address set
    Write( DATA, 0 );                // From column address 0 to 127
    Write( DATA, 127 );
    Write( COMMAND, 0x75 );          // Page address set
    Write( DATA, 0 );                // From page address 0 to 127
    Write( DATA, 127 );
    Write( COMMAND, 0x5c );          // Entry Memory Write Mode
    for( j = 0; j < 127; j++ )
        for( i = 0; i < 127; i++ )
            Write( DATA, pattern[j*128+i] ); // Display Data Write
}

```

8.5.3 Partial Display In/Out

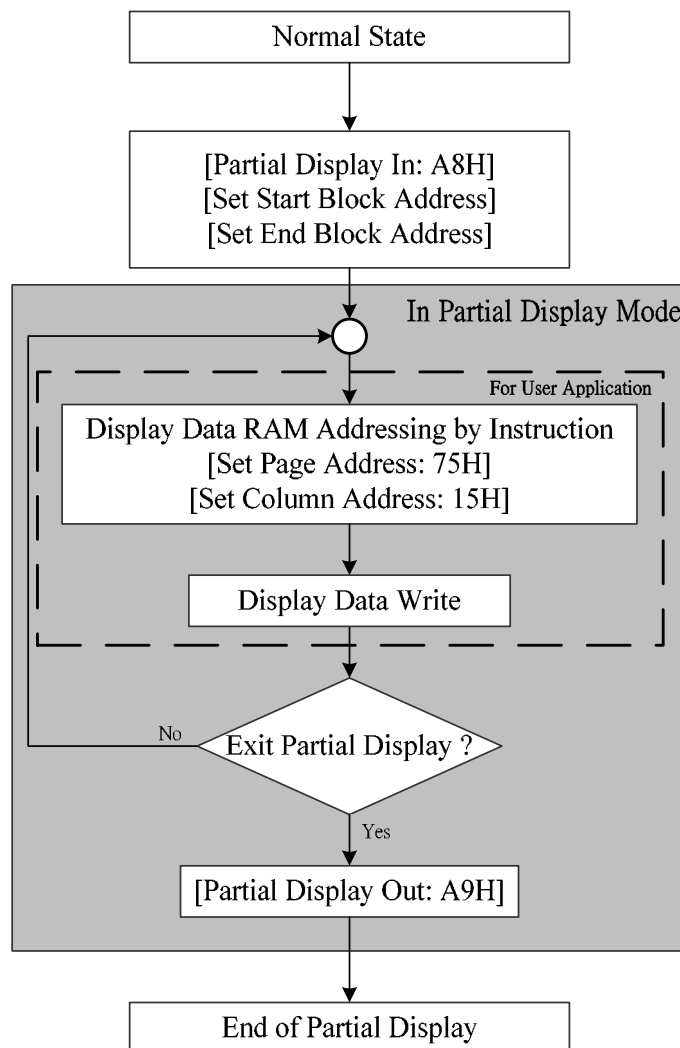


Figure 8.5.3.1 Partial Display In/Out

Example : Partial Display In Operation

```
void PartailIn( unsigned char start_block, unsigned char end_block )
{
    Write( COMMAND, 0x30 );           // Ext = 0
    Write( COMMAND, 0xA8);           // Partial Display In Function
    Write( DATA, start_block );     // Start Block
    Write( DATA, end_block );       // End Block
}

void PartailOut( void )
{
    Write( COMMAND, 0x30 );           // Ext = 0
    Write( COMMAND, 0xA9 );          // Partial Display Out Function
}

extern unsigned char *display_pattern;
void main()
{
    PartailIn( 11, 18 );              // entry partial display mode

    Windowing( 0, 11*4, 131, 18*4 ); // set the page and column range
    PartialDisplay( display_pattern ); // Fill the data into partial display area
    .
    .
    .
    PartailOut();                     // Out of partial display mode
}
```

8.5.4 Scroll Display

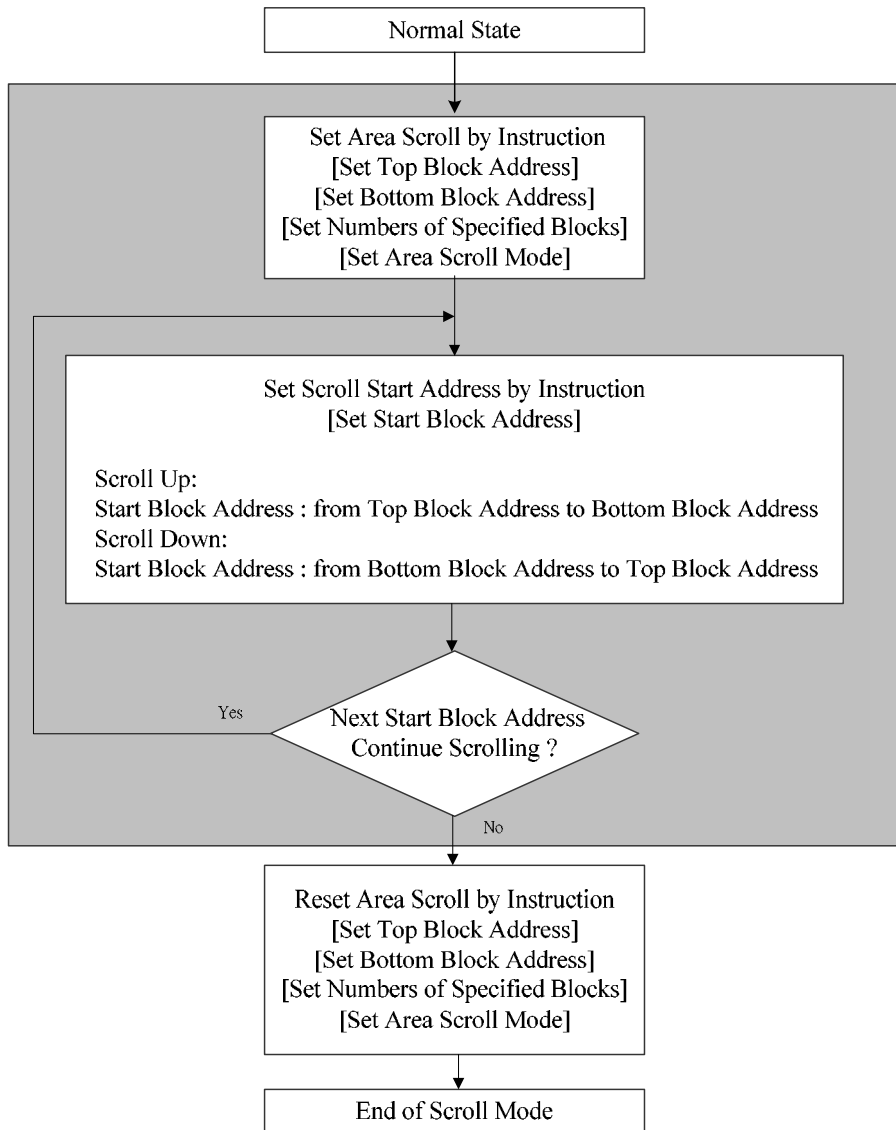


Figure 8.5.4.1 Scroll Display

Example : Screen Scroll Operation

```

void CenterScreenScroll( void )
{
    Write( COMMAND, 0x30 );           // Ext = 0
    Write( COMMAND, 0xAA);           // Partial Display In Function
    Write( DATA, 0x0a );             // Top_Block=10
    Write( DATA, 0x14 );             // Bottom_Block=20
    Write( DATA, 0x14 );             // Number of Specified Blocks=Bottom_Block=20
    Write( DATA, 0x00 );             // Area Scroll Type=Center Screen Scroll

    ScrollUp() or ScrollDown();       // Scroll Up or Scroll Down
}
  
```

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```
void TopScreenScroll( void )
{
    Write( COMMAND, 0x30 );           // Ext = 0
    Write( COMMAND, 0xAA);           // Partial Display In Function
    Write( DATA, 0x00 );           // Top_Block=0
    Write( DATA, 0x14 );           // Bottom_Block=20
    Write( DATA, 0x14 );           // Number of Specified Blocks=Bottom_Block=20
    Write( DATA, 0x01 );           // Area Scroll Type=Top Screen Scroll

    ScrollUp() or ScrollDown();     // Scroll Up or Scroll Down
}
```

```
void BottomScreenScroll( void )
{
    Write( COMMAND, 0x30 );           // Ext = 0
    Write( COMMAND, 0xAA);           // Partial Display In Function
    Write( DATA, 0x0a );           // Top_Block=10
    Write( DATA, 0x20 );           // Bottom_Block=32
    Write( DATA, 0x20 );           // Number of Specified Blocks=Bottom_Block=32
    Write( DATA, 0x02 );           // Area Scroll Type=Bottom Screen Scroll

    ScrollUp() or ScrollDown();     // Scroll Up or Scroll Down
}
```

```
void WholeScreenScroll( void )
{
    Write( COMMAND, 0x30 );           // Ext = 0
    Write( COMMAND, 0xAA);           // Partial Display In Function
    Write( DATA, 0x00 );           // Top_Block=0
    Write( DATA, 0x20 );           // Bottom_Block=32
    Write( DATA, 0x20 );           // Number of Specified Blocks=Bottom_Block=32
    Write( DATA, 0x03 );           // Area Scroll Type=Whole Screen Scroll

    ScrollUp() or ScrollDown();     // Scroll Up or Scroll Down
}
```

```
void ScrollUp( void )
{
    Write( COMMAND, 0x30 );           // Ext = 0
    Write( COMMAND, 0xAB);           // Scroll Start Set
    Write( DATA, Top_Block);        // Start Block Address=Top_Block
    Delay();                          // Delay

    Write( COMMAND, 0x00AB);         // Scroll Start Set
    Write( DATA, Top_Block + 1 );    // Start Block Address= Top_Block+1
    Delay();                          // Delay

    Write( COMMAND, 0x00AB);         // Scroll Start Set
    Write( DATA, Top_Block + 2 );    // Start Block Address= Top_Block +2
    Delay();                          // Delay
    .....
}
```

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```
.....
Write( COMMAND, 0x00AB);           // Scroll Start Set
Write( DATA, Bottom_Block );     // Start Block Address= Bottom_Block
Delay();                           // Delay
}

void ScrollDown( void )
{

    Write( COMMAND, 0x30 );         // Ext = 0
    Write( COMMAND, 0x00AB);       // Scroll Start Set
    Write( DATA, Bottom_Block);   // Start Block Address= Bottom_Block
    Delay();                       // Delay

    Write( COMMAND, 0x00AB);       // Scroll Start Set
    Write( DATA, Bottom_Block -1 ); // Start Block Address= Bottom_Block -1
    Delay();                       // Delay

    Write( COMMAND, 0x00AB);       // Scroll Start Set
    Write( DATA, Bottom_Block -2 ); // Start Block Address= Bottom_Block -2
    Delay();                       // Delay

    .....
    .....
    Write( COMMAND, 0x00AB);       // Scroll Start Set
    Write( DATA, Top_Block );     // Start Block Address= Top_Block
    Delay();                       // Delay
}
```

8.5.5 Read-Modify-Write Cycle

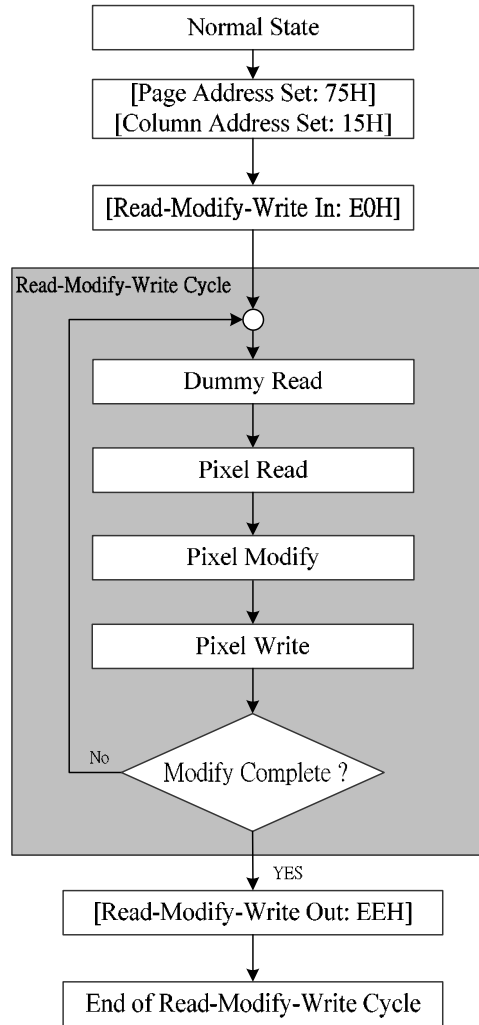


Figure 8.5.5.1 Read-Write-Modify Cycle

Example : Read-Write-Modify Cycle

```

void ReadModifyWriteIn( void )
{
    Write( COMMAND, 0x30 );    // Ext = 0
    Write( COMMAND, 0xE0 );    // Entry the Read-Modify-Write mode
}

void ReadModifyWriteOut( void )
{
    Write( COMMAND, 0x30 );    // Ext = 0
    Write( COMMAND, 0xEE );    // Out of partial display mode
}

extern unsigned char *display_pattern;
void main()
{
    unsigned pixel, i;

    Windowing( 11, 31, 80, 50 );    // set the page and column range
    ReadModifyWriteIn();            // entry the Read-Modify-Write mode
  
```

```

for( i = 0 ; i < 1400 ; i++ )
{
  Read( DATA );           // For dummy read
  pixel = Read( DATA );  // Pixel read
  pixel = pixel & 0x07ff; // Pixel modify: red filter
  Write( DATA, pixel );
}

ReadModifyWriteOut();    // Out of Read-Modify-Write mode
}

```

8.5.6 Power OFF

Power OFF

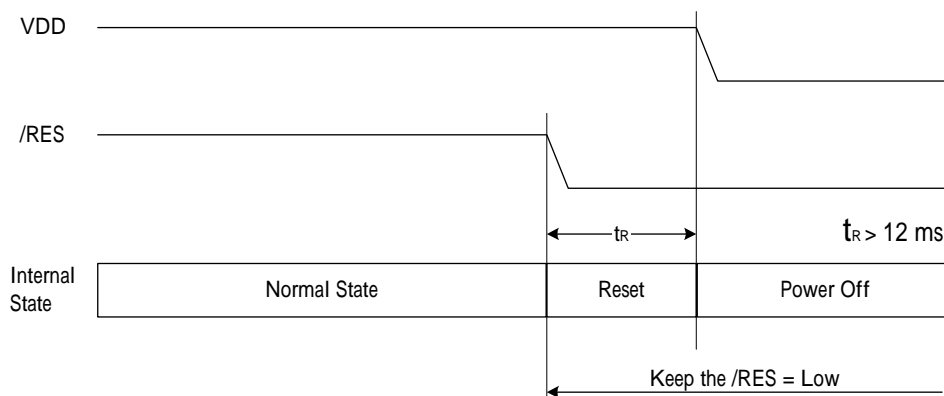
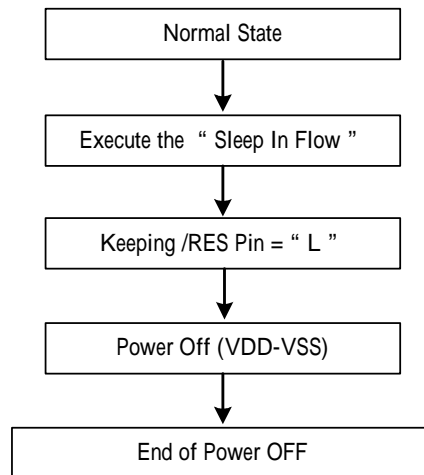


Figure 8.5.6.1 Power off

8.5.7 Sleep In/Out

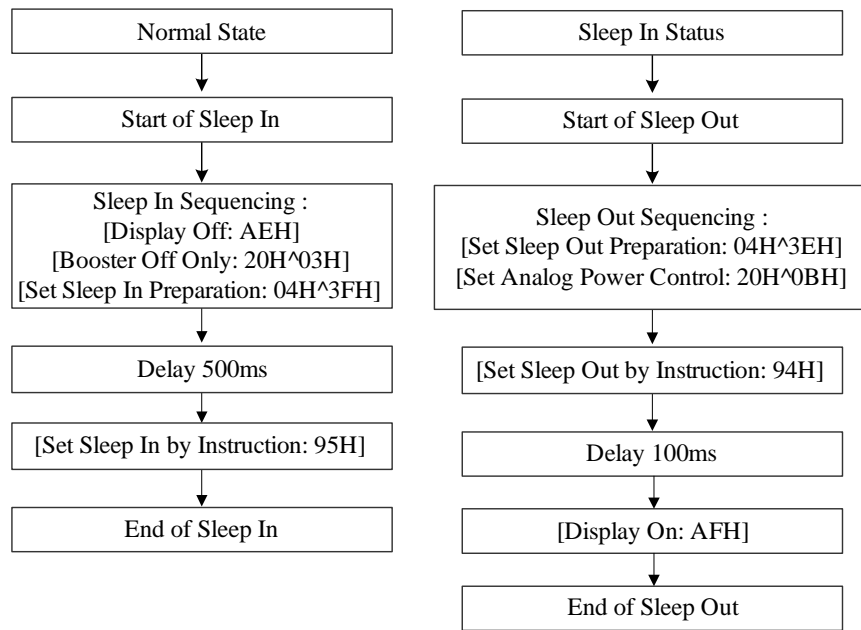


Fig 8.5.7.1 Sleep In/Out Flow

Example : Sleep In Operation

```
void SleepIn( void )
```

```
{
  Write( COMMAND, 0x30 ); // Ext = 0
  Write( COMMAND, 0xae ); // Display Off
  Write( COMMAND, 0x20 ); // Power Control
  Write( DATA, 0x03 ); // B/F/R = Off/On/On
  Write( COMMAND, 0x04 ); // Sleep In Preparation
  Write( DATA, 0x3f ); // Sleep In Sequencing
  Delay( 500ms ); // Delay 500ms
  Write( COMMAND, 0x95 ); // Sleep In
}
```

Example : Sleep Out Operation

```
void SleepOut( void )
```

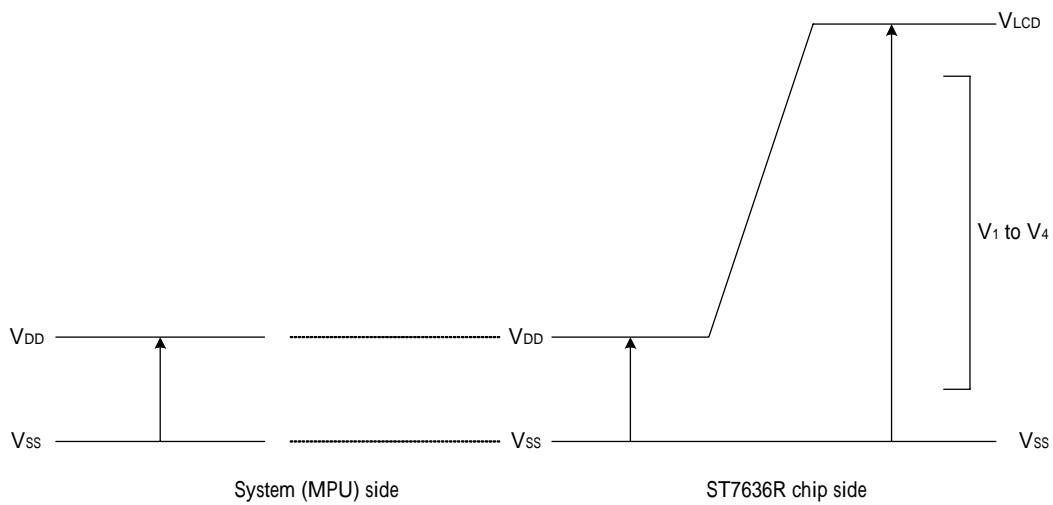
```
{
  Write( COMMAND, 0x30 ); // Ext = 0
  Write( COMMAND, 0x04 ); // Sleep Out Preparation
  Write( DATA, 0x3e ); // Sleep Out Sequencing
  Write( COMMAND, 0x20 ); // Power Control
  Write( DATA, 0x0b ); // B/F/R = On/On/On
  Write( COMMAND, 0x94 ); // Sleep Out
  Delay( 100ms ); // Delay 100ms
  Write( COMMAND, 0xaf ); // Display On
}
```

9. LIMITING VALUES

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In accordance with the Absolute Maximum Rating System; see notes 1 and 2.

Parameter	Symbol	Conditions	Unit
Power supply voltage	VDD, VDD1~VDD5	-0.5 ~ +3.6	V
Power supply voltage	VLCD _{IN}	-0.5 ~ +20	V
Power supply voltage	V1, V2, V3, V4	0.3 to VLCD _{IN}	V
Input voltage	V _{IN}	-0.5 to VDD+0.5	V
Output voltage	V _O	-0.5 to VDD+0.5	V
Operating temperature (Die)	TOPR	-30 to +85	°C
Storage temperature (Die)	TSTR	-40 to +125	°C



Notes

1. Stresses above those listed under Limiting Values may cause permanent damage to the device.
2. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.
3. Insure that the voltage levels of V1, V2, V3, and V4 are always such as below:

$$VLCD_{IN} \quad V_0 \quad V_1 \quad V_2 \quad V_3 \quad V_4 \quad V_{SS}, V_4 < 2.3V$$

10. HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see "Handling MOS devices").

11. DC CHARACTERISTICS

$V_{DD} = 1.8\text{ V to }3.3\text{V (VDD, VDD1)}, V_{DD} = 2.4\text{ V to }3.3\text{V (VDD2, VDD3, VDD4, VDD5)}$

; $V_{SS} = 0\text{ V}; V_{LCD} = 3.76\text{ to }18.0\text{V}; T_{amb} = -30\text{ to }+85$; unless otherwise specified.

Item	Symbol	Condition	Rating			Units	Applicable Pin	
			Min.	Typ.	Max.			
High-level Input Voltage	VIHC		$0.7 \times VDD$	—	VDD	V	*1	
Low-level Input Voltage	VILC		VSS	—	$0.3 \times VDD$	V	*1	
High-level Output Voltage	VOHC		$0.7 \times VDD$	—	VDD	V	*2	
Low-level Output Voltage	VOLC		VSS	—	$0.3 \times VDD$	V	*2	
Input leakage current	ILI	$V_{IN} = VDD\text{ or }VSS$	-1.0	—	1.0	μA	*3	
Output leakage current	ILO	$V_{IN} = VDD\text{ or }VSS$	-3.0	—	3.0	μA	*4	
Liquid Crystal Driver ON Resistance	RON	$T_a = 25^\circ\text{C}$ (Relative To VSS) $V_{OIN} = 14.7\text{ V}$	—	1	10	K Ω	SEGN COMn *5	
Oscillator Frequency	Internal Oscillator	fOSC	1/132 duty $T_a = 25^\circ\text{C}$ 31 PWM	—	10.42	20.83	kHz	*6
	External Input	fCL		—	323.02	645.73		
	Frame frequency	fFRAME		Internal OSC: $f_{FRAME} = f_{OSC} / (\text{Duty} + 1)$ External OSC: $f_{FRAME} = f_{CL} / [31 * (\text{Duty} + 1)]$				Hz

Item	Symbol	Condition	Rating			Units	Applicable Pin	
			Min.	Typ.	Max.			
Internal Power	Operating Voltage (1)	VDD VDD1	(Relative to VSS)	1.8	—	3.3	V	VSS*7
	Operating Voltage (2)	VDD2 VDD3 VDD4 VDD5	(Relative to VSS)	2.4	—	3.3	V	VSS
	Supply Step-up output voltage Circuit	VLCD _{OUT}	(Relative To VSS)	—	—	20	V	VLCD _{OUT}

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	Voltage regulator Circuit Operating Voltage	VLCD _{IN}	(Relative To VSS)	—	—	20	V	VLCD _{IN}
--	---	--------------------	-------------------	---	---	----	---	--------------------

Dynamic Consumption Current: During Display, with the Internal Power Supply OFF Current consumed by total ICs when an external power supply is used.

Test pattern	Symbol	Condition	Rating			Units	Notes
			Min.	Typ.	Max.		
Display Pattern Normal	ISS	VDD = 2.8 V, Booster x 7 V0 – VSS (Vop) = 13.84 V @ 1/12 bias, 1/132 duty	—	500	—	μA	*8
Power Down	ISS	Ta = 25°C	—	—	10	μA	die

Notes to the DC characteristics

1. The maximum possible VLCD voltage that may be generated is depend on voltage, temperature, loading (display pattern), and internal clock rate.
2. Power-down mode is meaning that during power down state, all static currents are switched off.
3. If external VLCD, the display load current is not transmitted to I_{DD}.
4. External VLCD voltage is applied to VLCD_{IN} pin; VLCD_{IN} is disconnected from VLCD_{OUT}.

References for items market with *

- *1 The A0, D0 to D5, D6 (SI), D7 (SCL), /RD (E), /WR, /(R/W), /CS, IMS, OSC, P/S, /DOF, RESB terminals.
- *2 The D0 to D7.
- *3 The A0, /RD (E), /WR, /(R/W), /CS, and RES terminals.
- *4 Applies when the D0 to D5, D6 (SI), D7 (SCL) terminals are in a high impedance state.
- *5 These are the resistance values for when a 0.2 x V0 voltage is applied between the output terminal SEGn or COMn and the various power supply terminals (V1, V2, V3, and V4). These are specified for the operating voltage range.
RON = 0.2 V0/ΔI (Where ΔI is the current that flows when 0.2 V0 is applied while the power supply is ON.)
- *6 The relationship between the oscillator frequency and the frame rate frequency under CL dividing ratio setting = 00H.
- *7 While a broad range of operating voltages is guaranteed, performance cannot be guaranteed if there are sudden fluctuations to the voltage while the MPU is being accessed.
- *8 It indicates the current consumed on ICs alone when the internal oscillator circuit and display are turned on.

12. TIMING CHARACTERISTICS

System Bus Read/Write Characteristics 1 (For the 8080 Series MPU)

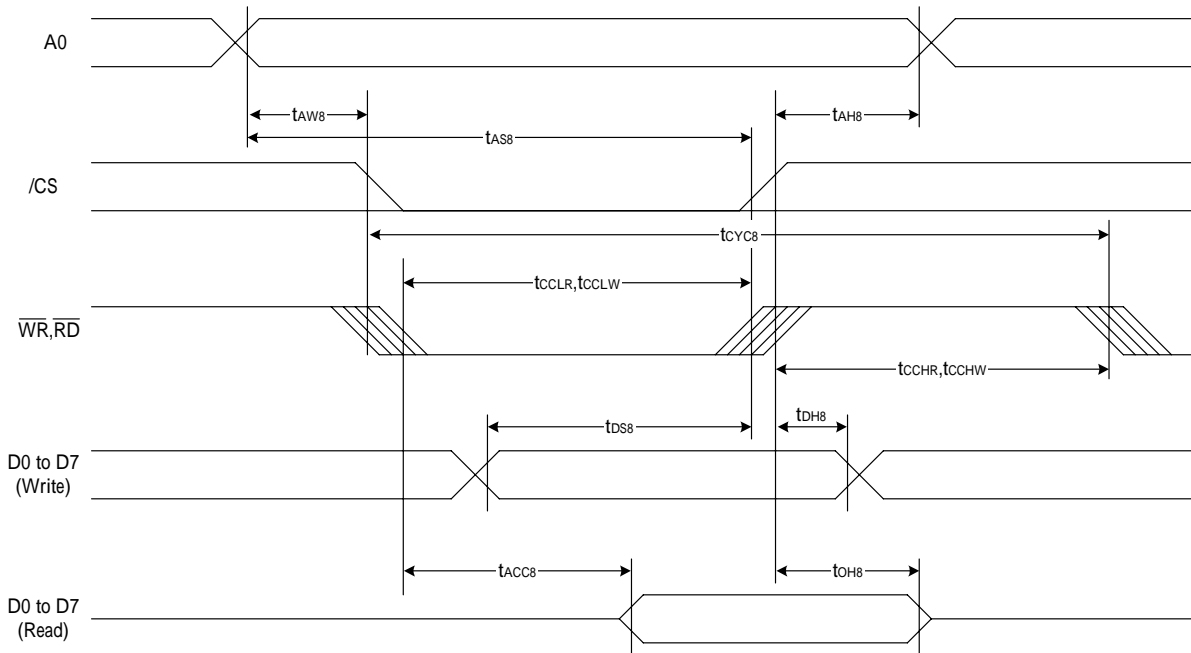


Figure 12.1

($V_{DD}=3.3V$, $T_a = -30^{\circ}C$ to $85^{\circ}C$, die)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH8		10	—	ns
Address setup time		tAS8		40	—	
Address setup time		tAW8		0	—	
System cycle time (WRITE)	WR	tCYC8		170	—	ns
/WR L pulse width (WRITE)		tCCLW		50	—	
/WR H pulse width (WRITE)		tCCHW		130	—	
System cycle time (READ)	RD	tCYC8		160	—	
/RD L pulse width (READ)		tCCLR		80	—	
/RD H pulse width (READ)		tCCHR		80	—	
WRITE data setup time	D0 to D7	tDS8		50	—	
WRITE data hold time		tDH8		10	—	
READ access time		tACC8	CL = 100 pF	—	70	
READ Output disable time		tOH8	CL = 100 pF	—	60	

(V_{DD}=2.8V, Ta= -30°C to 85°C, die)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH8		10	—	ns
Address setup time		tAS8		50	—	
Address setup time		tAW8		0	—	
System cycle time (WRITE)	WR	tCYC8		180	—	ns
/WR L pulse width (WRITE)		tCCLW		55	—	
/WR H pulse width (WRITE)		tCCHW		140	—	
System cycle time (READ)	RD	tCYC8		180	—	
/RD L pulse width (READ)		tCCLR		90	—	
/RD H pulse width (READ)		tCCHR		90	—	
WRITE data setup time	D0 to D7	tDS8		55	—	
WRITE data hold time		tDH8		10	—	
READ access time		tACC8	CL = 100 pF	—	75	
READ Output disable time		tOH8	CL = 100 pF	—	65	

(V_{DD}=1.8V, Ta= -30°C to 85°C, die)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH8		10	—	ns
Address setup time		tAS8		80	—	
Address setup time		tAW8		0	—	
System cycle time (WRITE)	WR	tCYC8		400	—	ns
/WR L pulse width (WRITE)		tCCLW		70	—	
/WR H pulse width (WRITE)		tCCHW		300	—	
System cycle time (READ)	RD	tCYC8		400	—	
/RD L pulse width (READ)		tCCLR		200	—	
/RD H pulse width (READ)		tCCHR		200	—	
WRITE data setup time	D0 to D7	tDS8		90	—	
WRITE data hold time		tDH8		10	—	
READ access time		tACC8	CL = 100 pF	—	90	
READ Output disable time		tOH8	CL = 100 pF	—	80	

*1 The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr +tf) (tCYC8 – tCCLW – tCCHW) for (tr + tf) (tCYC8 – tCCLR – tCCHR) are specified.

*2 All timing is specified using 20% and 80% of V_{DD} as the reference.

*3 tCCLW and tCCLR are specified as the overlap between /CS being “L” and WR and RD being at the “L” level.

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System Bus Read/Write Characteristics 1 (For the 6800 Series MPU)

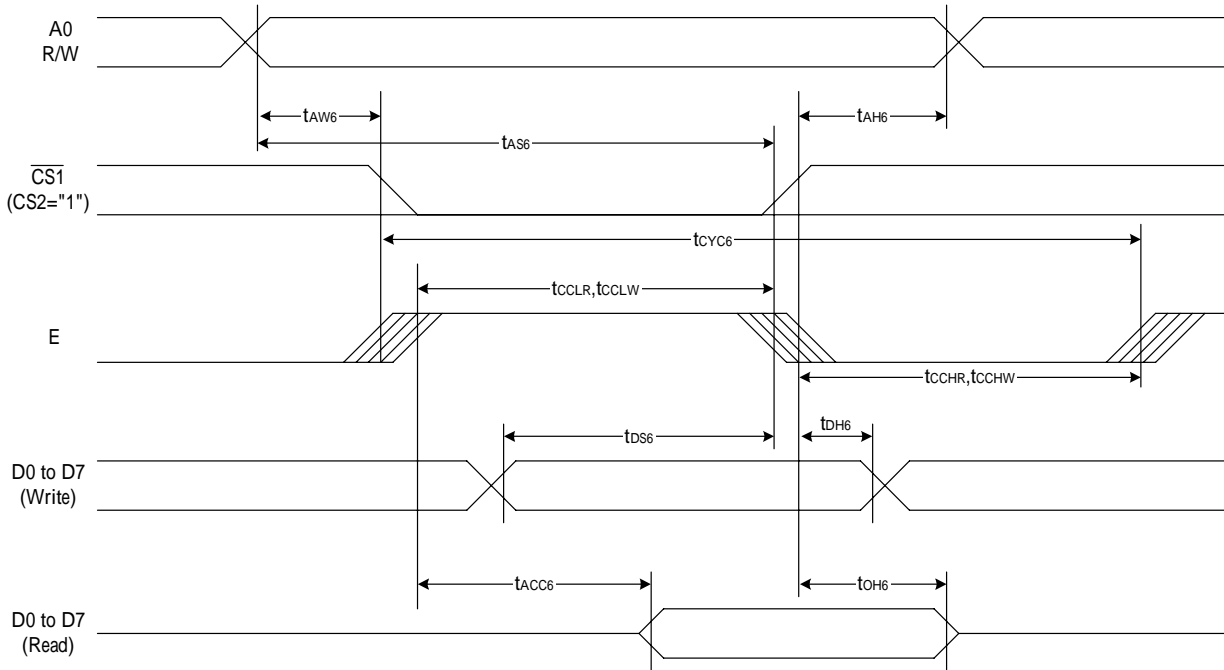


Figure 12.2

($V_{DD}=3.3V$, $T_a = -30^{\circ}C$ to $85^{\circ}C$, die)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH6		10	—	ns
Address setup time		tAS6		50	—	
Address setup time		tAW6		0	—	
System cycle time (WRITE)	WR	tCYC6		170	—	ns
Enable L pulse width (WRITE)		tCCLW		130	—	
Enable H pulse width (WRITE)		tCCHW		40	—	
System cycle time (READ)	RD	tCYC6		160	—	
Enable L pulse width (READ)		tCCLR		80	—	
Enable H pulse width (READ)		tCCHR		80	—	
WRITE data setup time	D0 to D7	tDS6		50	—	
WRITE data hold time		tDH6		10	—	
READ access time		tACC6	CL = 100 pF	—	70	
READ Output disable time		tOH6	CL = 100 pF	—	60	

(V_{DD}=2.8V, Ta= -30°C to 85°C, die)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH6		10	—	ns
Address setup time		tAS6		60	—	
Address setup time		tAW6		0	—	
System cycle time (WRITE)	WR	tCYC6		195	—	ns
Enable L pulse width (WRITE)		tCCLW		160	—	
Enable H pulse width (WRITE)		tCCHW		45	—	
System cycle time (READ)	RD	tCYC6		180	—	
Enable L pulse width (READ)		tCCLR		90	—	
Enable H pulse width (READ)		tCCHR		90	—	
WRITE data setup time	D0 to D7	tDS6		55	—	
WRITE data hold time		tDH6		10	—	
READ access time		tACC6	CL = 100 pF	—	75	
READ Output disable time		tOH6	CL = 100 pF	—	65	

(V_{DD}=1.8V, Ta= -30°C to 85°C, die)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH6		10	—	ns
Address setup time		tAS6		100	—	
Address setup time		tAW6		0	—	
System cycle time (WRITE)	WR	tCYC6		390	—	ns
Enable L pulse width (WRITE)		tCCLW		300	—	
Enable H pulse width (WRITE)		tCCHW		60	—	
System cycle time (READ)	RD	tCYC6		400	—	
Enable L pulse width (READ)		tCCLR		200	—	
Enable H pulse width (READ)		tCCHR		200	—	
WRITE data setup time	D0 to D7	tDS6		90	—	
WRITE data hold time		tDH6		10	—	
READ access time		tACC6	CL = 100 pF	—	90	
READ Output disable time		tOH6	CL = 100 pF	—	80	

*1 The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr +tf) (tCYC6 – tEWLW – tEWHW) for (tr + tf) (tCYC6 – tEWLR – tEWHR) are specified.

*2 All timing is specified using 20% and 80% of V_{DD} as the reference.

*3 tEWLW and tEWLR are specified as the overlap between /CS being “L” and E.

Serial Interface Characteristics (For 4-Line Interface)

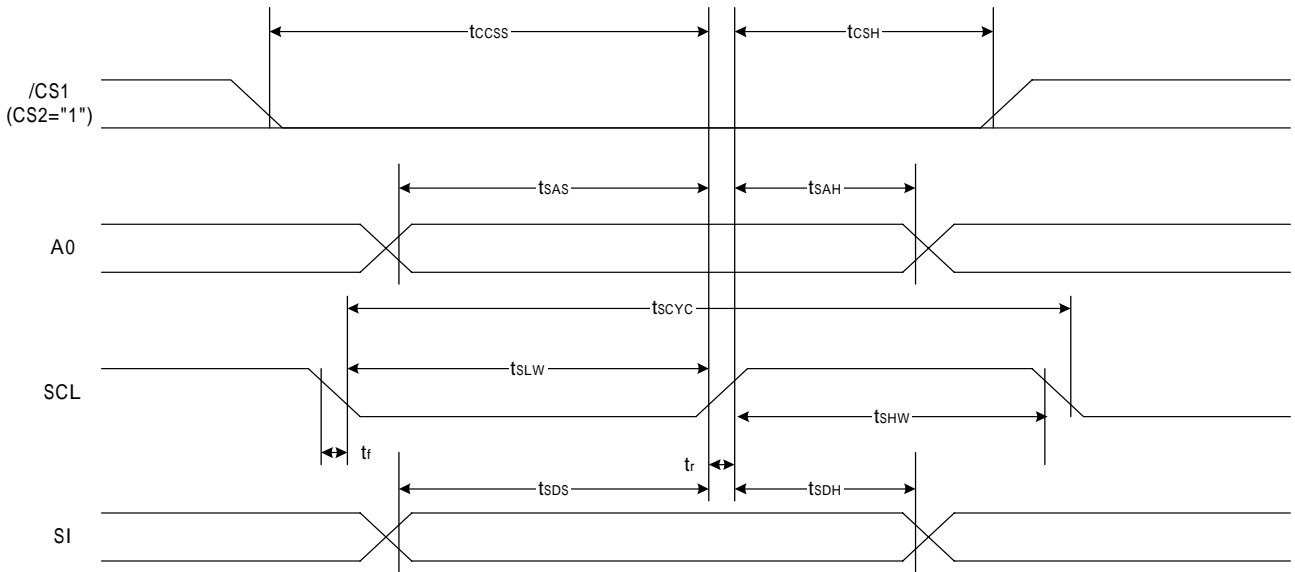


Fig 12.3

($V_{DD}=3.3V, T_a = -30^{\circ}C$ to $85^{\circ}C$, die)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial clock period	SCL	tSCYC		80	—	ns
SCL "H" pulse width		tSHW		40	—	
SCL "L" pulse width		tSLW		40	—	
Address setup time	A0	tSAS		10	—	
Address hold time		tSAH		30	—	
Data setup time	SI	tSDS		10	—	
Data hold time		tSDH		30	—	
CS-SCL time	/CS	tCSS		10	—	
CS-SCL time		tCSH		30	—	

(V_{DD}=2.8V, T_a= -30°C to 85°C, die)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial clock period	SCL	tSCYC		90	—	ns
SCL "H" pulse width		tSHW		45	—	
SCL "L" pulse width		tSLW		45	—	
Address setup time	A0	tSAS		10	—	
Address hold time		tSAH		35	—	
Data setup time	SI	tSDS		10	—	
Data hold time		tSDH		35	—	
CS-SCL time	/CS	tCSS		10	—	
CS-SCL time		tCSH		35	—	

(V_{DD}=1.8V, T_a= -30°C to 85°C, die)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial clock period	SCL	tSCYC		100	—	ns
SCL "H" pulse width		tSHW		50	—	
SCL "L" pulse width		tSLW		50	—	
Address setup time	A0	tSAS		10	—	
Address hold time		tSAH		40	—	
Data setup time	SI	tSDS		10	—	
Data hold time		tSDH		40	—	
CS-SCL time	/CS	tCSS		10	—	
CS-SCL time		tCSH		40	—	

*1 The input signal rise and fall time (tr, tf) are specified at 15 ns or less.

*2 All timing is specified using 20% and 80% of VDD as the standard.

Serial Interface Characteristics (For 3-Line Interface)

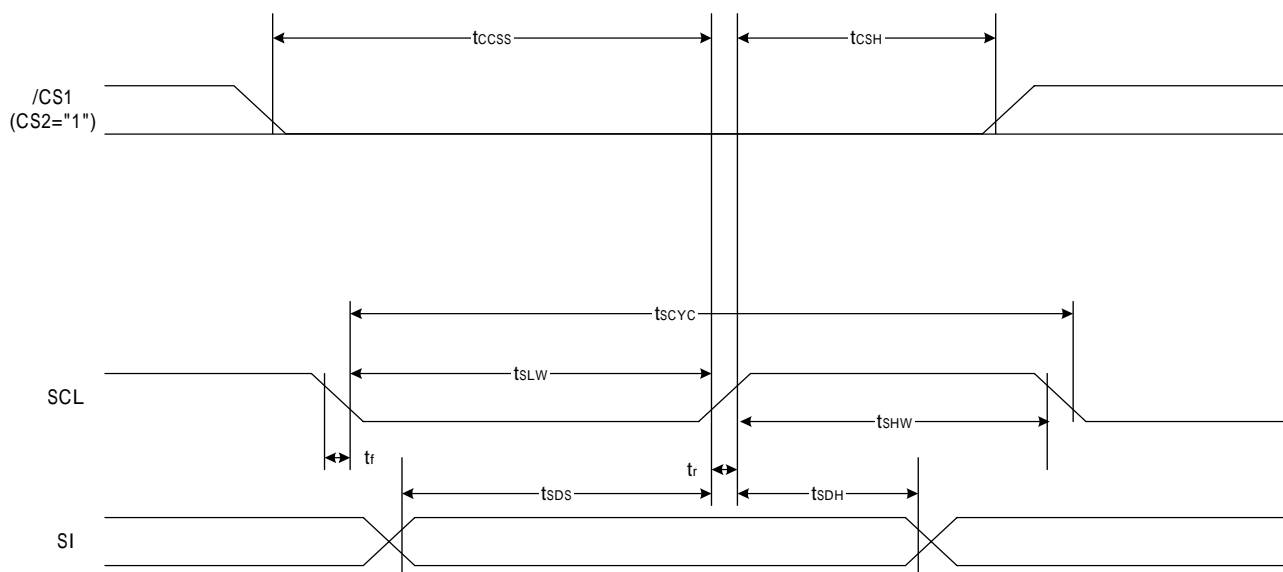


Fig 12.4

($V_{DD}=3.3V$, $T_a = -30^{\circ}C$ to $85^{\circ}C$, die)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial clock period	SCL	tSCYC		80	—	ns
SCL "H" pulse width		tSHW		40	—	
SCL "L" pulse width		tSLW		40	—	
Data setup time	SI	tSDS		10	—	
Data hold time		tSDH		30	—	
CS-SCL time	/CS	tCSS		10	—	
CS-SCL time		tCSH		30	—	

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(V_{DD}=2.8V, Ta= -30°C to 85°C, die)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial clock period	SCL	tSCYC		90	—	ns
SCL "H" pulse width		tSHW		45	—	
SCL "L" pulse width		tSLW		45	—	
Data setup time	SI	tSDS		10	—	
Data hold time		tSDH		35	—	
CS-SCL time	/CS	tCSS		10	—	
CS-SCL time		tCSH		35	—	

(V_{DD}=1.8V, Ta= -30°C to 85°C, die)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial clock period	SCL	tSCYC		100	—	ns
SCL "H" pulse width		tSHW		50	—	
SCL "L" pulse width		tSLW		50	—	
Data setup time	SI	tSDS		10	—	
Data hold time		tSDH		40	—	
CS-SCL time	/CS	tCSS		10	—	
CS-SCL time		tCSH		40	—	

*1 The input signal rise and fall time (tr, tf) are specified at 15 ns or less.

*2 All timing is specified using 20% and 80% of VDD as the standard.

13. RESET TIMING

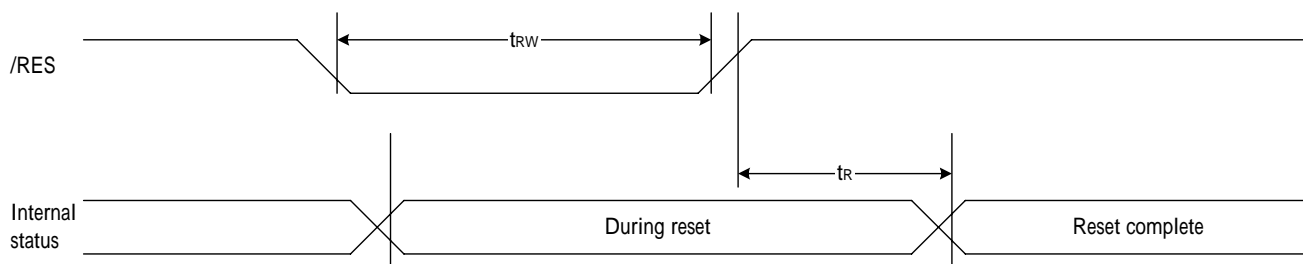


Fig 13.1

(VDD = 3.3V, Ta = -30°C to 85°C, die)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		tR		900	—	—	ns
Reset “L” pulse width	RESB	tRW		1200	—	—	ns

(VDD = 2.8V, Ta = -30°C to 85°C, die)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		tR		860	—	—	ns
Reset “L” pulse width	RESB	tRW		1300	—	—	ns

(VDD = 1.8V, Ta = -30°C to 85°C, die)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		tR		690	—	—	ns
Reset “L” pulse width	RESB	tRW		2040	—	—	ns

14. Display Application Examples between ST7636R and Panel

14.1 128 X 128 panel and CSEL=0 configuration

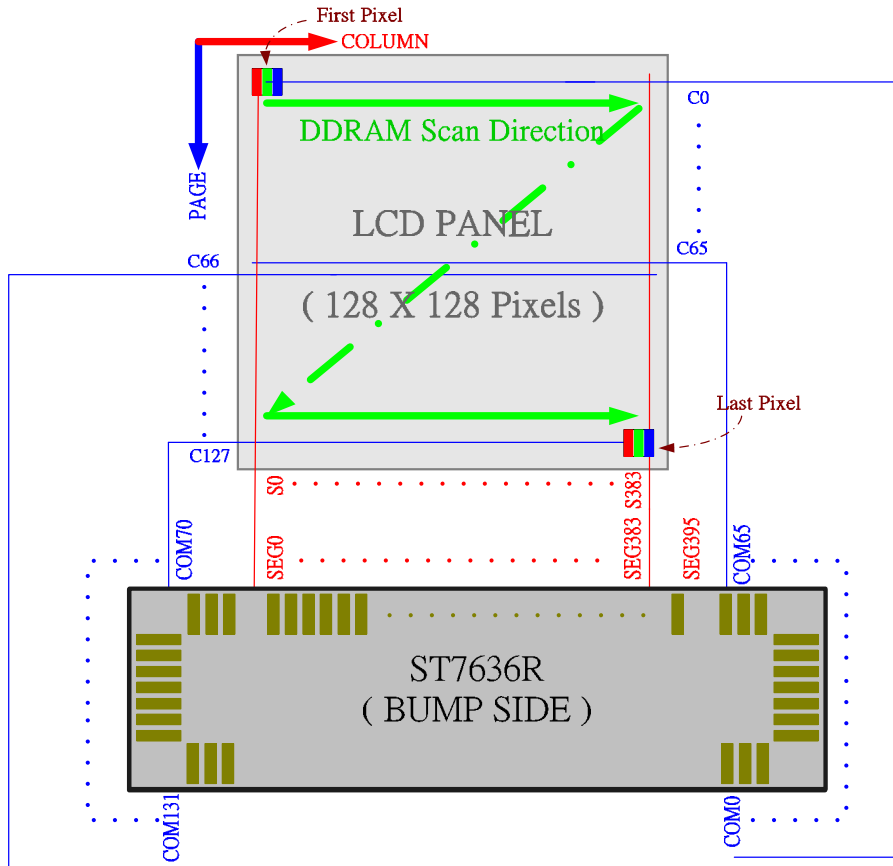


Figure 14.1 128 X 128 panel and CSEL=0 configuration

Initialize Setting :

Application Suggestion

VDD, VDD1 = 1.8 ~ 3.3 (V)
 VDD2 ~ VDD5 = 2.4 ~ 3.3 (V)
 Bias = 1 / 12
 Duty = 128

Option Pin Setting:

CSEL = 0

Register Setting:

COMMAND	PARAMETER	DESCRIPTION
BBH	P1 = 01H	Common scan direction
CAH	P2 = 31H	Duty = 128
75H	P1 = 0, P2 = 127	Page = 0 ~ 127
15H	P1 = 0, P2 = 127	Column = 0 ~ 127
BCH	P1 = 00H	Address scan direction
BCH	P2 = 00H	RGB arrangement

14.2 128 X 128 panel and CSEL=0 configuration

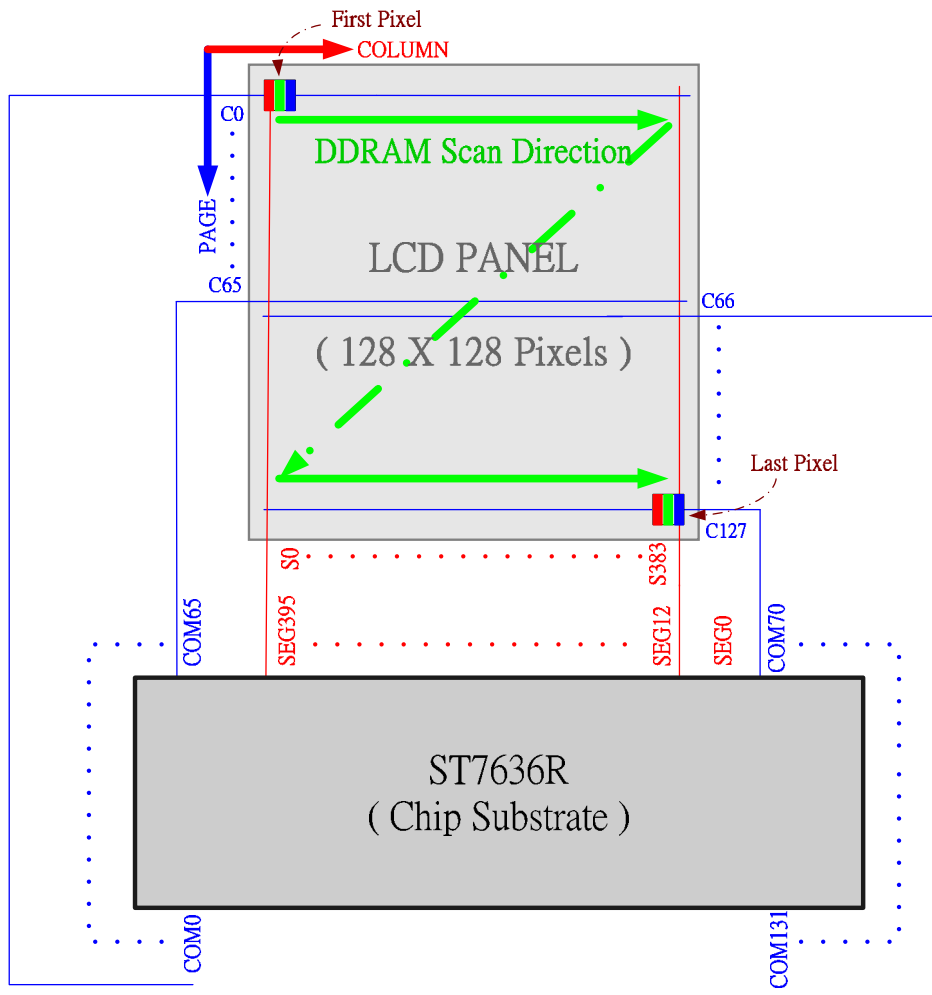


Figure 14.2 128 X 128 panel and CSEL=0 configuration

Initialize Setting :

Application Suggestion

VDD, VDD1 = 1.8 ~ 3.3 (V)
 VDD2 ~ VDD5 = 2.4 ~ 3.6 (V)
 Bias = 1 / 12
 Duty = 128

Option Pin Setting:

CSEL = 0

Register Setting:

COMMAND	PARAMETER	DESCRIPTION
BBH	P1 = 01H	Common scan direction
CAH	P2 = 31H	Duty = 128
75H	P1 = 0, P2 = 127	Page = 0 ~ 127
15H	P1 = 4, P2 = 131	Column = 4 ~ 131
BCH	P1 = 02H	Address scan direction
BCH	P2 = 01H	RGB arrangement

14.3 128 X 128 panel and CSEL=1 configuration

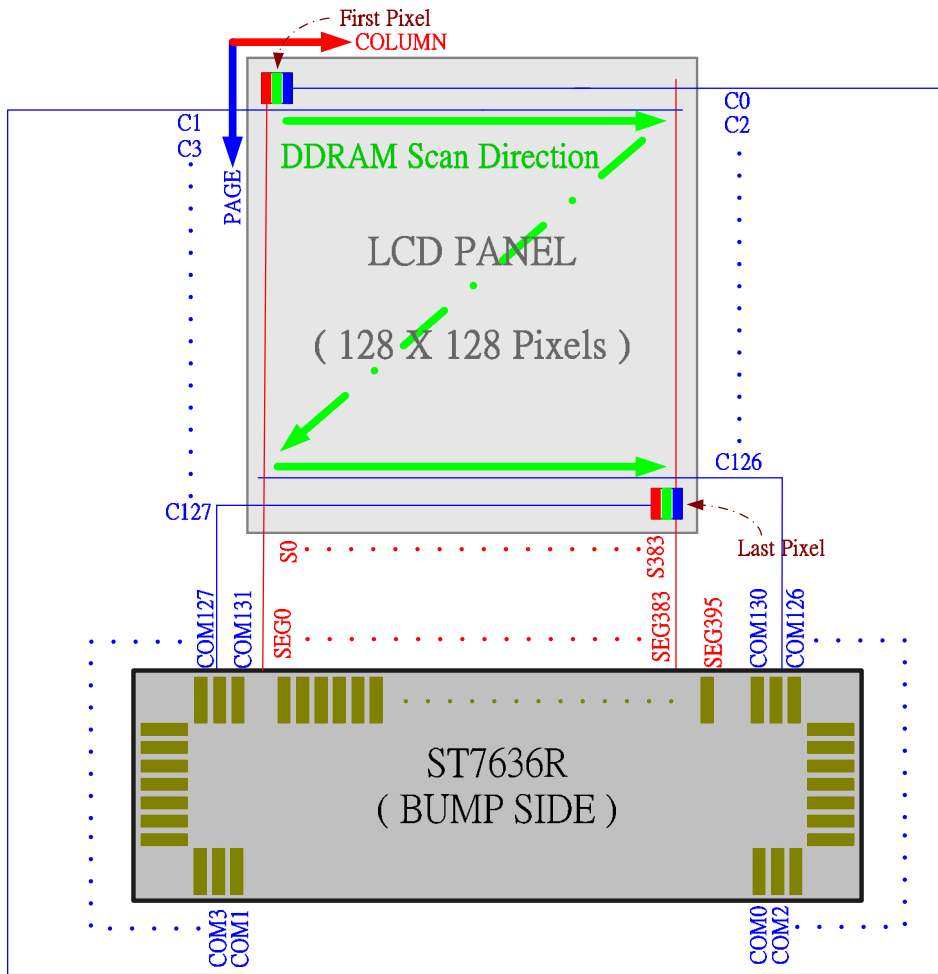


Figure 14.3 128 X 128 panel and CSEL=1 configuration

Initialize Setting :

Application Suggestion

VDD, VDD1 = 1.8 ~ 3.3 (V)
 VDD2 ~ VDD5 = 2.4 ~ 3.6 (V)
 Bias = 1/12
 Duty = 128

Option Pin Setting:

CSEL = 1

Register Setting:

COMMAND	PARAMETER	DESCRIPTION
CAH	P2 = 31H	Duty = 128
75H	P1 = 0, P2 = 127	Page = 0 ~ 127
15H	P1 = 0, P2 = 127	Column = 0 ~ 127
BCH	P1 = 00H	Address scan direction
BCH	P2 = 00H	RGB arrangement

14.4 128 X 128 panel and CSEL=1 configuration

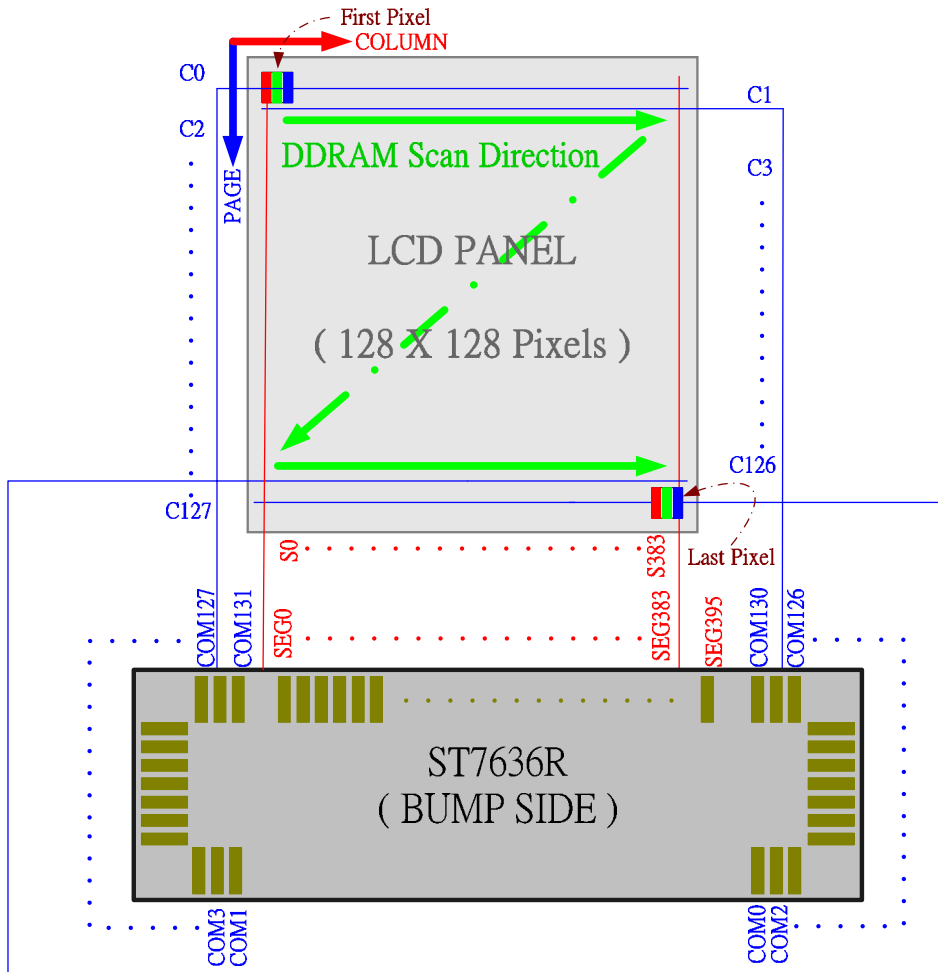


Figure 14.4 128 X 128 panel and CSEL=1 configuration

Initialize Setting :

Application Suggestion

VDD, VDD1 = 1.8 ~ 3.3 (V)
 VDD2 ~ VDD5 = 2.4 ~ 3.6 (V)
 Bias = 1/12
 Duty = 128

Option Pin Setting:

CSEL = 1

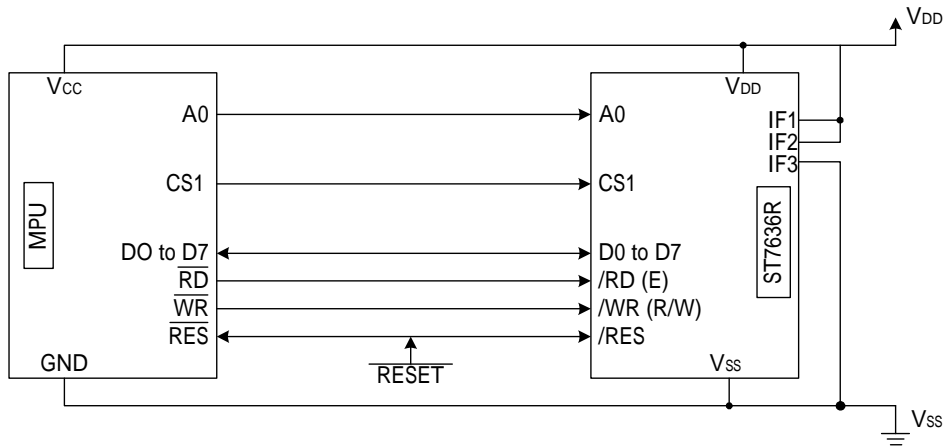
Register Setting:		
COMMAND	PARAMETER	DESCRIPTION
CAH	P2 = 31H	Duty = 128
75H	P1 = 0, P2 = 127	Page = 0 ~ 127
15H	P1 = 0, P2 = 127	Column = 0 ~ 127
BCH	P1 = 03H	Address scan direction
BCH	P2 = 00H	RGB arrangement

15. THE MPU INTERFACE (REFERENCE EXAMPLES)

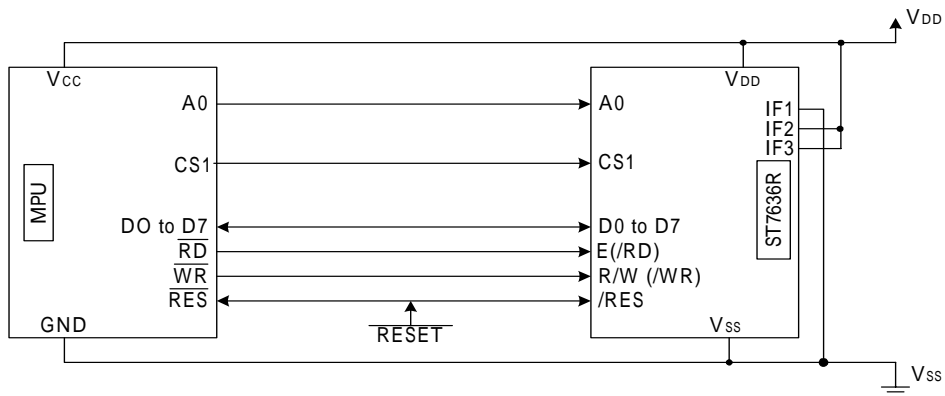
The ST7636R Series can be connected to either 8080 Series MPUs or to 6800 Series MPUs. Moreover, using the serial interface it is possible to operate the ST7636R series chips with fewer signal lines.

The display area can be enlarged by using multiple ST7636R Series chips. When this is done, the chip select signal can be used to select the individual lcs to access.

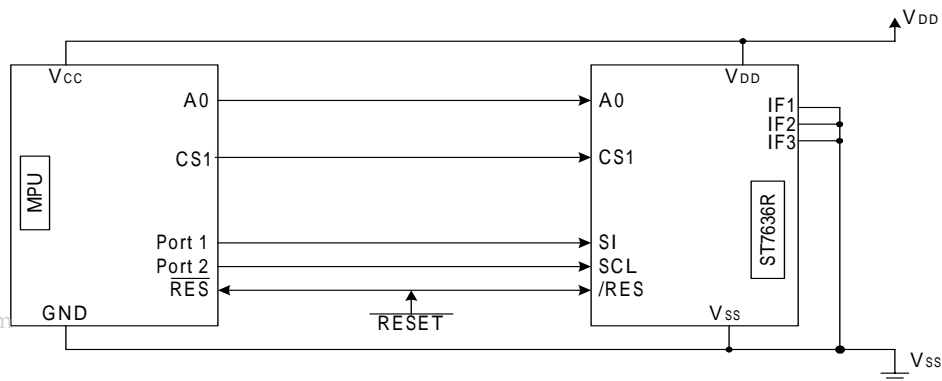
(1) 8080 Series MPUs



(2) 6800 Series MPUs

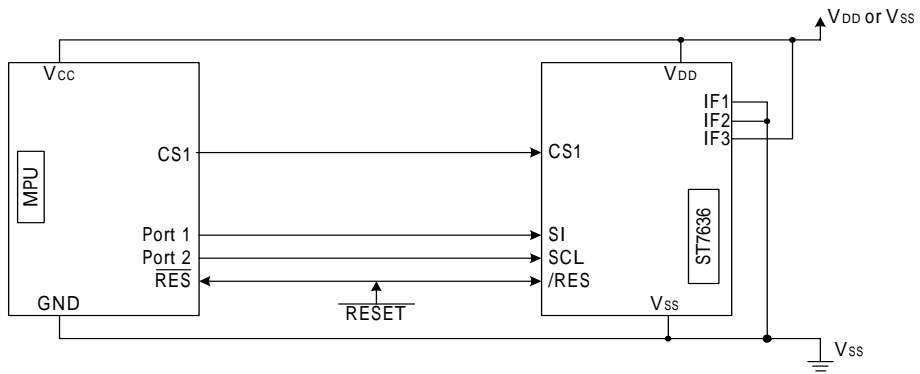


(3) Using the Serial Interface (4-line interface)



ST7636R

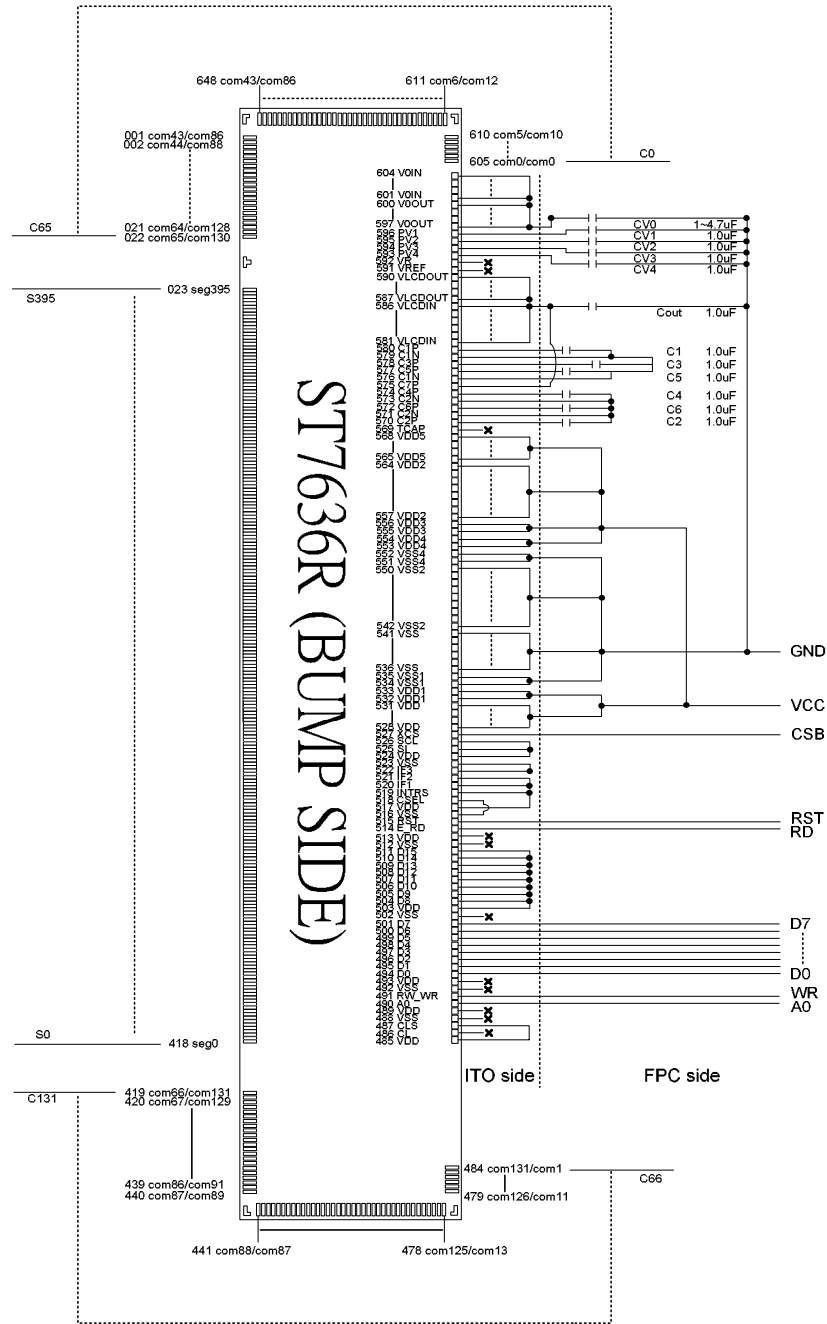
(4) Using the Serial Interface (3-line interface)



ST7636R

Application Circuits (Continue)

(B) 80 Series 8-bit Parallel Interface:



Interface: 80 series 8-bit Interface

www.Booster.cdn

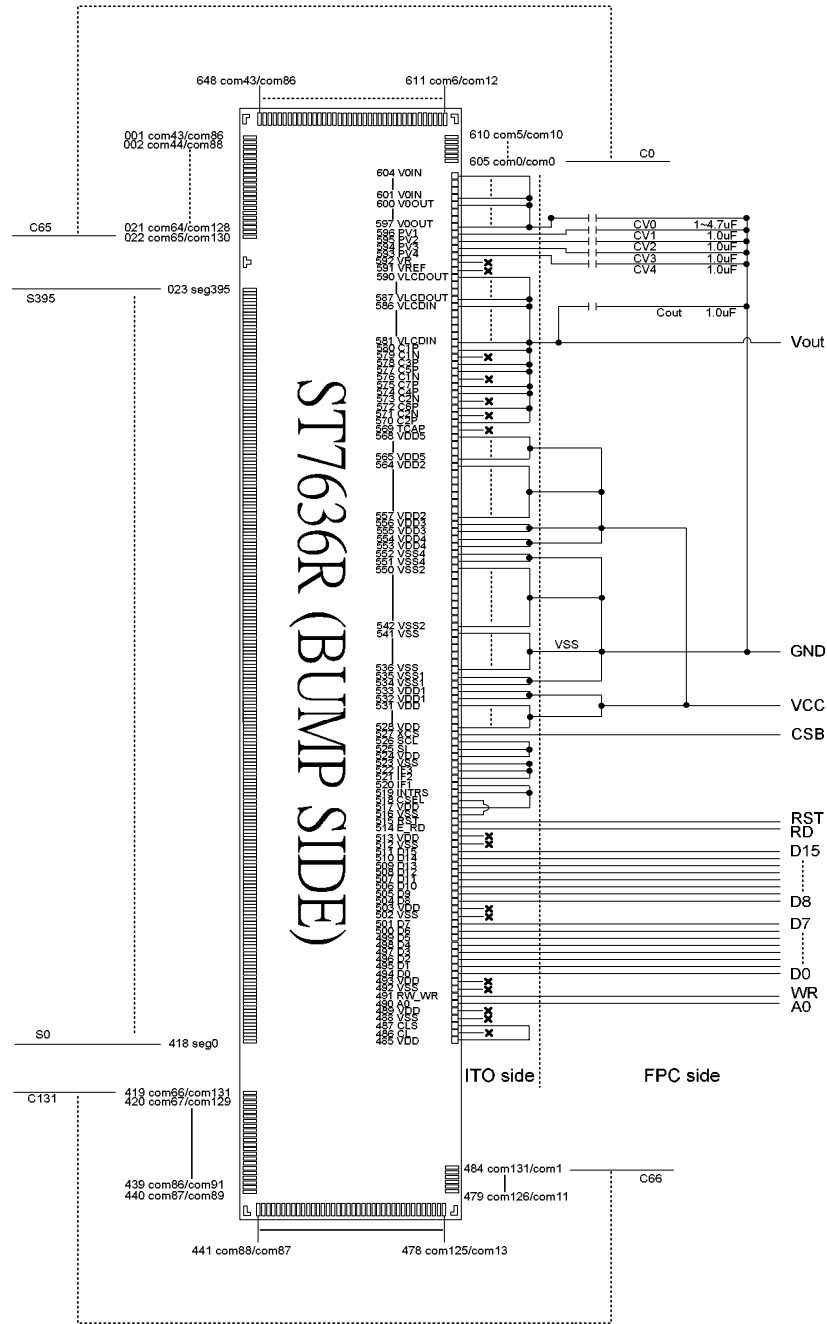
Use Internal Resistors

Capacitor: 1.0 uF / 25V

ST7636R

Application Circuits (Continue)

(C) 68 Series 16-bit Parallel Interface (with external power supply to VLCD):



Interface: 68 series 16-bit Interface

www. Booster: register VC = 0

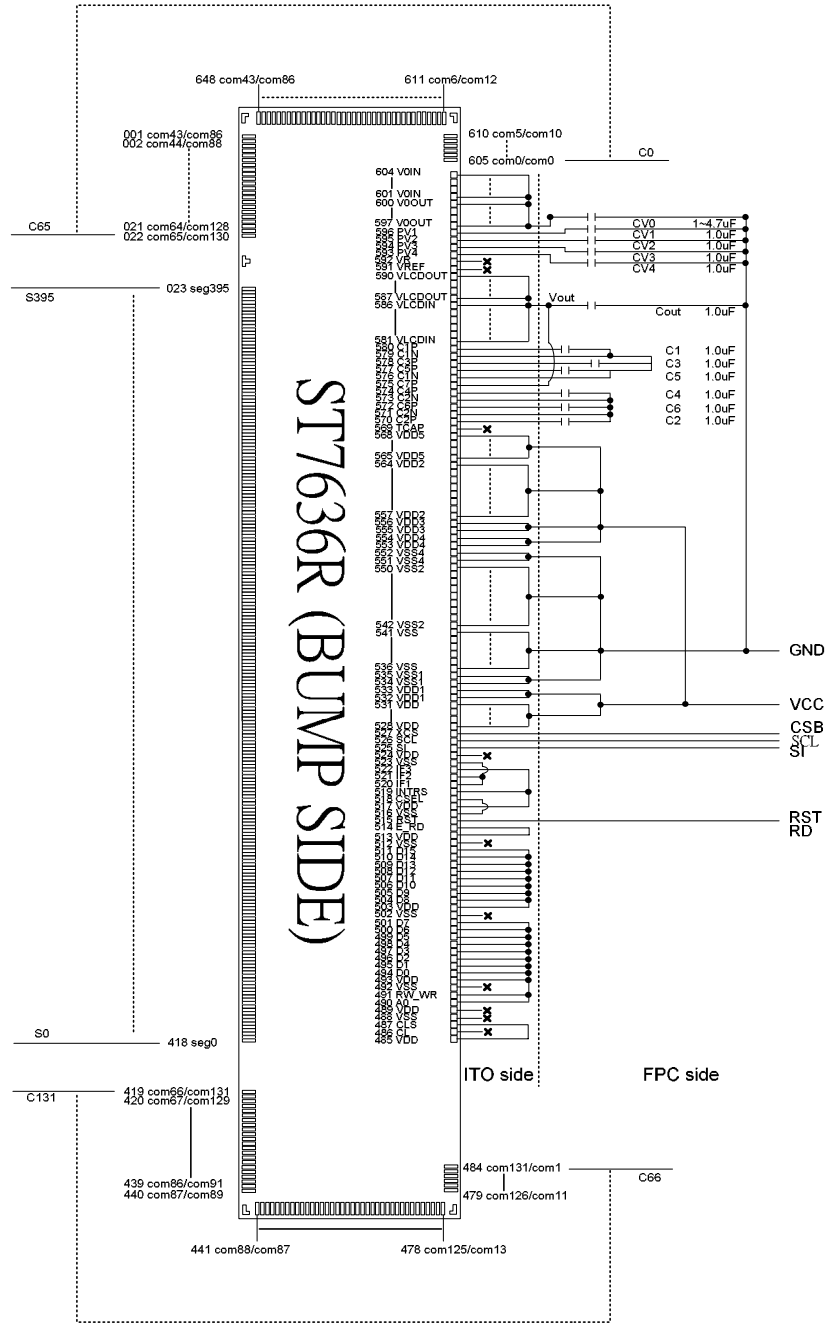
Use External Power Supply to VLCD

Capacitor: 1.0 uF / 25V

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Application Circuits (Continue)

(D) 3 Line Serial Peripheral Interface:



Interface: 3 Line Serial Peripheral Interface

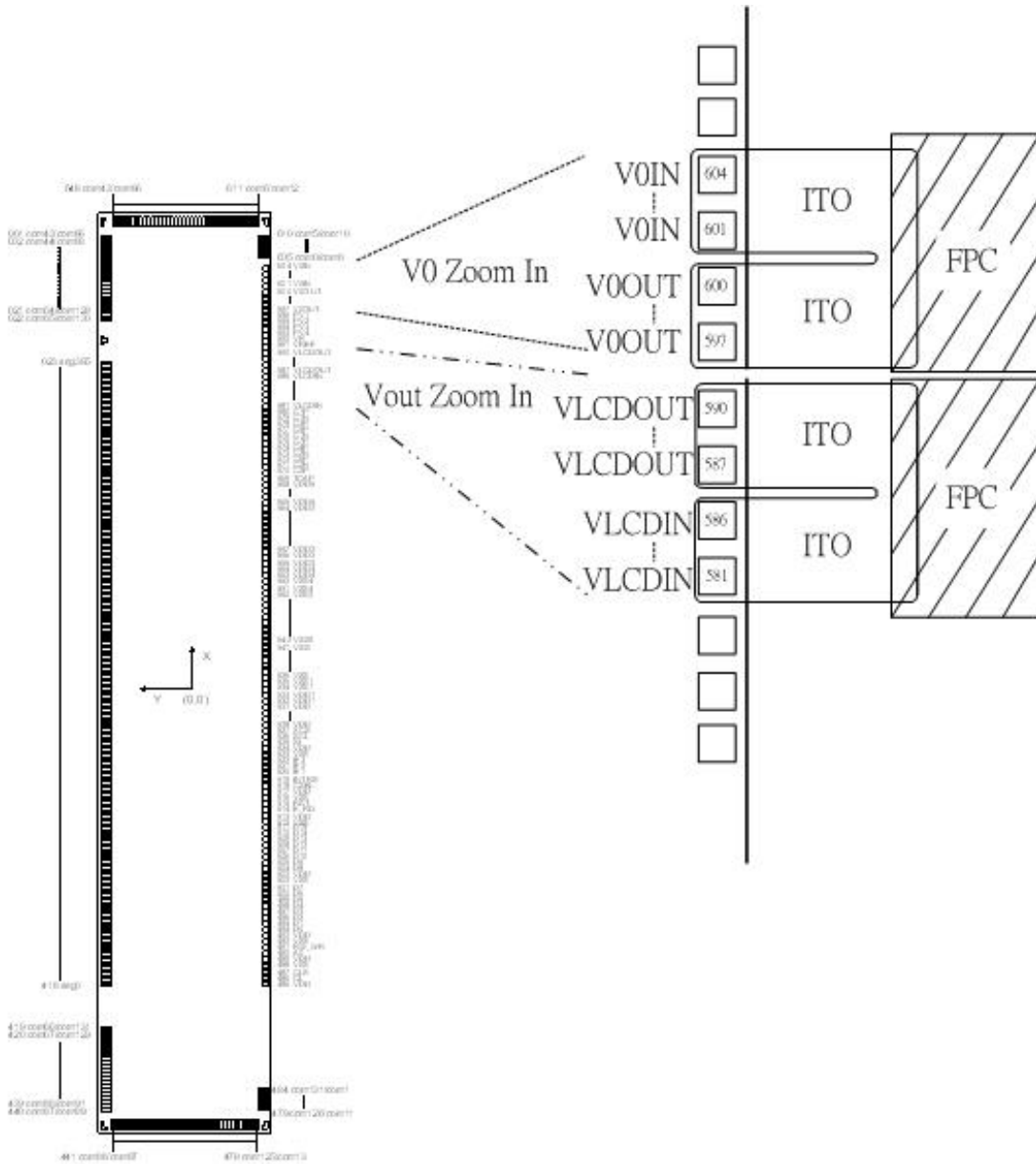
Booster: 7x

Use Internal Resistors

Capacitor: 1.0 uF / 25V

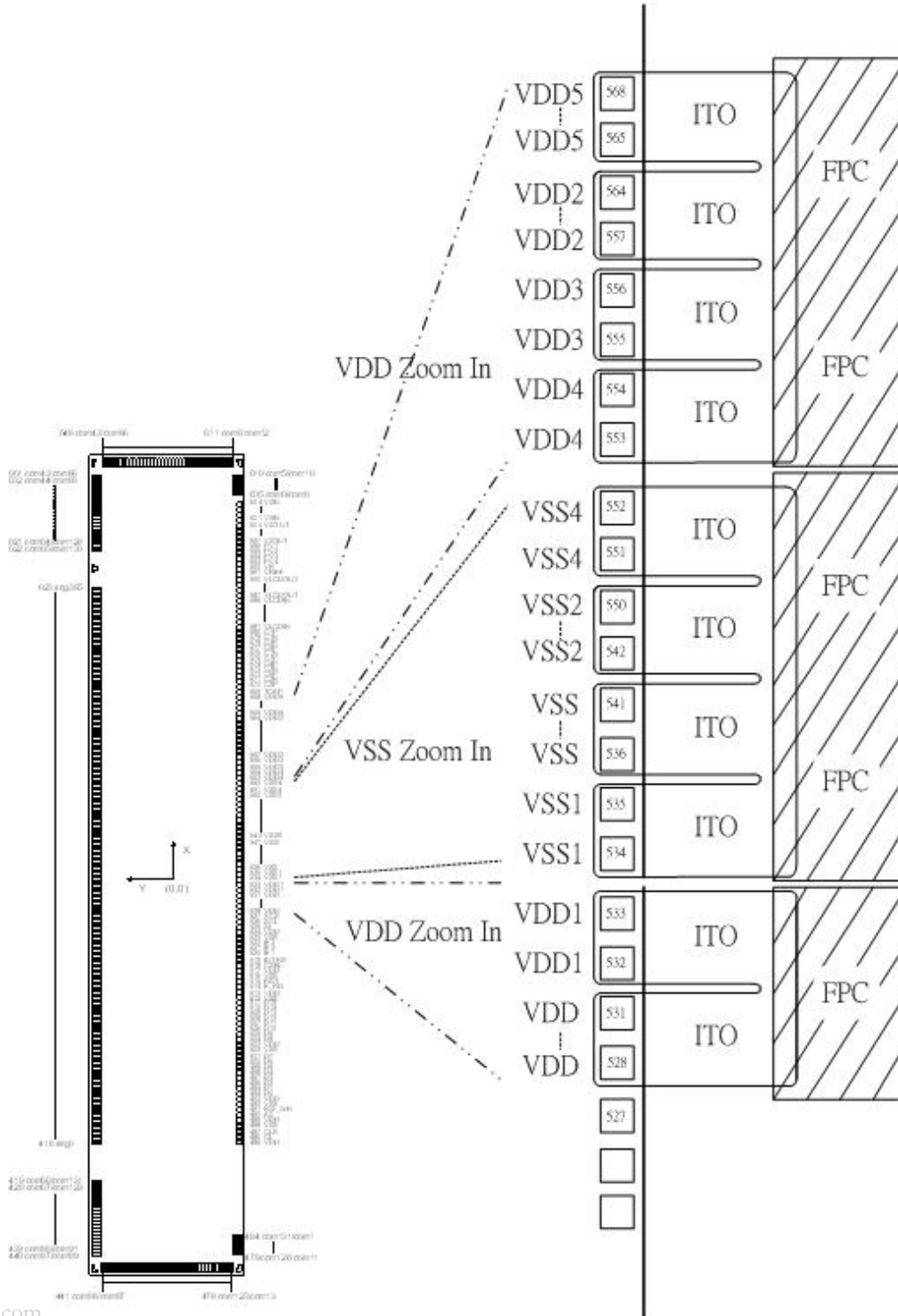
16. Application Note of VLCD and Vop (V0) ITO Layout

When using internal voltage generator, VLCDIN, VLCDOUT must be connected together. V0IN and V0OUT must be connected together too. In the following is the ITO layout for VLCDIN, VLCDOUT, V0IN and V0OUT individually. Please follow the way as below for these two LCD power voltages.



17. Application Note of VDD and VSS ITO Layout

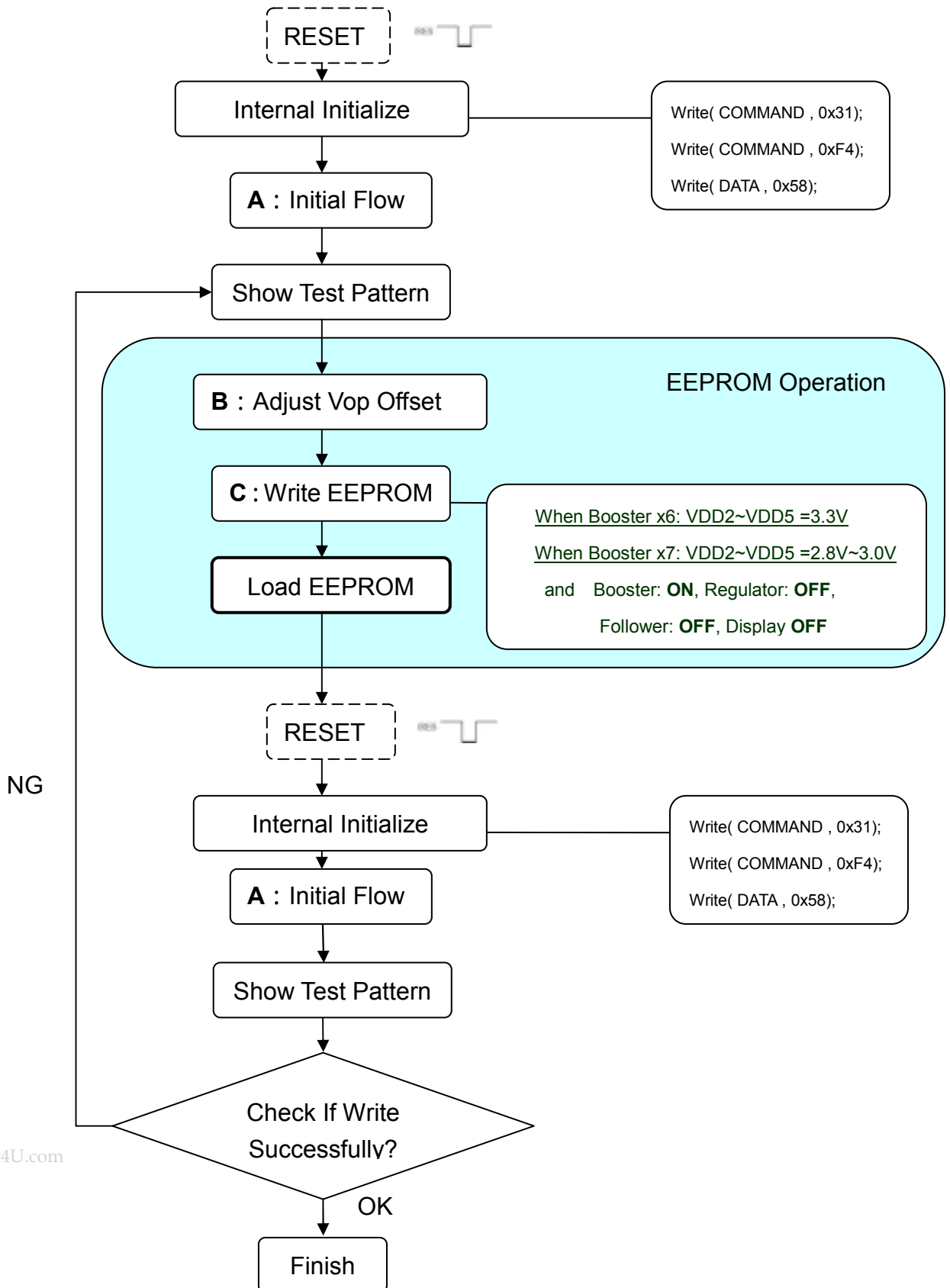
In the following is the ITO layout of power system (VDD and VSS). Please follow the way as below for VDD and VSS ITO layout.



18. Application Note of EEPROM Flow

In the following is EEPROM flow chart and its detail application programs.

● EEPROM Flow Chart



● Application Programs

A. Initial Flow

```
void ST7636R_Init( void )
```

```
{
```

Write(COMMAND, 0x30);	// Ext = 0
Write(COMMAND, 0x04);	// Sleep In/Out Preparation
Write(DATA, 0x3e);	// Sleep In/Out Sequencing
Write(COMMAND, 0x31);	// Ext = 1
Write(COMMAND, 0xf4);	// Internal Initialize Preparation
Write(DATA, 0x58);	// Internal Initialize Sequencing
Write(COMMAND, 0x30);	// Ext = 0
Write(COMMAND, 0x94);	// Sleep Out
Write(COMMAND, 0xd1);	// Internal OSC on
Write(COMMAND, 0xca);	// Display Control
Write(DATA, 0x00);	// CL divisions Ratio
Write(DATA, 0x1f);	// Duty Setting (= 128)
Write(DATA, 0x00);	// N-Line Inverse-set value
Write(COMMAND, 0x31);	// Ext = 1
Write(COMMAND, 0x32);	// Analog Setting
Write(DATA, 0x00);	// OSC Frequency adjustment
Write(DATA, 0x01);	// Booster Efficiency Setting
Write(DATA, 0x00);	// Bias Setting (=1/12)
Write(COMMAND, 0x30);	// Ext = 0
Write(COMMAND, 0x81);	// Electronic Volume Control
Write(DATA, 0x1B);	// EV:Vop[5:0]_6bit
Write(DATA, 0x04);	// EV:Vop[8:6]_3bit
	// Vop is 14.92V under this condition for example
Write(COMMAND, 0x20);	// Power Control
Write(DATA, 0x0b);	// B/F/R = On/On/On
Write(COMMAND, 0x30);	// Ext = 0
Write(COMMAND, 0x60);	// Auto-sampling
delay(50000);	// Delay 50ms
LoadEEPROM();	// Load EEPROM (refer page 71)
LoadPaint();	// Load Gamma Table Parameter (refer page 64)
Write(COMMAND, 0x30);	// Ext = 0
Write(COMMAND, 0xa7);	// Inverse Display
Write(COMMAND, 0xbb);	// Com Scan Direction
Write(DATA, 0x01);	// 0~65 / 131~66
Write(COMMAND, 0xbc);	// Data Scan Direction
Write(DATA, 0x00);	// Page / Column Address Setting
Write(DATA, 0x00);	// RGB arrangement (0:RGB 1:BGR)
Write(DATA, 0x01);	// Gray-scale setup (64-gray: 01H)
Write(COMMAND, 0x75);	// Page address set
Write(DATA, 0x00);	// From page address 0
Write(DATA, 0x7f);	// to page address 127
Write(COMMAND, 0x15);	// Column address set
Write(DATA, 0x00);	// From column address 0

Write(DATA, 0x7f);	// to column address 127
Write(COMMAND, 0xaf);	// Display On
Write(COMMAND, 0x30);	// Ext = 0
}	

B. Adjust Vop Offset

```
void adj_Vop_offset(void)
```

```
{
int i,j=1;
while(j)
{
if (KeyScan1==0)i=1; // Define KeyScan1 for "D6" use
if (KeyScan2==0)i=2; // Define KeyScan2 for "D7" use
if (KeyScan3==0)i=3; // Define KeyScan3 for "write" use
if (KeyScan1==1 & KeyScan2==1 & KeyScan3==1)i=4; // Jump to break
switch (i)
{
Case 1:
Write( COMMAND, 0xd6 ); // Vop Offset +1 step
break;
case 2:
Write( COMMAND, 0xd7 ); // Vop Offset -1 step
break;
case 3:
write_7636Reeprom(); // Write EEPROM Flow
j=0;
break;
default:
break;
}
}
}
```

C. Write EEPROM

```
void write_7636Reeprom(void)
```

```
{
Write( COMMAND, 0x30 ); // EXT=0
Write( COMMAND, 0xae ); // Display Off
Write( COMMAND, 0x20 ); // Power Control
Write( DATA, 0x08 ); // B/F/R = ON/OFF/OFF
Write( COMMAND, 0x8e ); // Enable EEPROM Write Mode
Write( COMMAND, 0x31 ); // EXT=1
Write( COMMAND, 0xeb ); // Select EEPROM
Write( DATA, 0x00 ); // EEPROM 1st byte
Write( COMMAND, 0x31 ); // EXT=1
Write( COMMAND, 0xcd ); // Control EEPROM ON
Write( DATA, 0x20 ); // Write EEPROM Mode
delay(50000); // Delay 50 ms
Write( COMMAND, 0xfc ); // Write Data to EEPROM
}
```

delay(50000);	// Delay 50ms
Write(COMMAND, 0xeb);	// Select EEPROM
Write(DATA, 0x01);	// EEPROM 2nd byte
Write(COMMAND, 0x31);	// EXT=1
Write(COMMAND, 0xcd);	// Control EEPROM ON
Write(DATA, 0x20);	// Write EEPROM Mode
delay(50000);	// Delay 50 ms
Write(COMMAND, 0xfc);	// Write Data to EEPROM
delay(50000);	// Delay 50ms
Write(COMMAND, 0xeb);	// Select EEPROM
Write(DATA, 0x02);	// EEPROM 3rd byte
Write(COMMAND, 0x31);	// EXT=1
Write(COMMAND, 0xcd);	// Control EEPROM ON
Write(DATA, 0x20);	// Write EEPROM Mode
delay(50000);	// Delay 50 ms
Write(COMMAND, 0xfc);	// Write Data to EEPROM
delay(50000);	// Delay 50ms
Write(COMMAND, 0xeb);	// Select EEPROM
Write(DATA, 0x03);	// EEPROM 4th byte
Write(COMMAND, 0x31);	// EXT=1
Write(COMMAND, 0xcd);	// Control EEPROM ON
Write(DATA, 0x20);	// Write EEPROM Mode
delay(50000);	// Delay 50 ms
Write(COMMAND, 0xfc);	// Write Data to EEPROM
delay(50000);	// Delay 50ms
Write(COMMAND, 0xeb);	// Select EEPROM
Write(DATA, 0x04);	// EEPROM 5th byte
Write(COMMAND, 0x31);	// EXT=1
Write(COMMAND, 0xcd);	// Control EEPROM ON
Write(DATA, 0x20);	// Write EEPROM Mode
delay(50000);	// Delay 50 ms
Write(COMMAND, 0xfc);	// Write Data to EEPROM
delay(50000);	// Delay 50ms
Write(COMMAND, 0x31);	// EXT=1
Write(COMMAND, 0xcc);	// Cancel EEPROM
delay(50000);	// Delay 50ms
Write(COMMAND, 0x30);	// EXT=0
Write(COMMAND, 0x8f);	// Disable EEPROM Write Mode
Write(COMMAND, 0x30);	// EXT=0
Write(COMMAND, 0x20);	// Power Control
Write(DATA, 0x0b);	// B/F/R = On/On/On
Write(COMMAND, 0xaf);	// Display On

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NOTE:

Microprocessor interface pins should not be floating in any operation mode.

