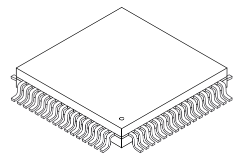
AutoBahn™ Spanceiver™
100MByte/s Version

MC100SX1451FI100

AUTOBAHN™
SPANCEIVER™



FI SUFFIX
CERAMIC QFP PACKAGE
CASE 963–02

The MC100SX1451FI100 AutoBahn chip is a high–speed serial–to–parallel, parallel–to–serial transceiver. The AutoBahn can be used to implement a high–speed, half–duplex, bi–directional serial data link with an effective data transfer rate of 100MByte/sec. A higher performance AutoBahn chip, with user selectable serial data transfer rates of 100 or 200MByte/s, is planned (see the MC100SX1451FI200 datasheet).This serial link can be used to establish multi–point or point–to–point connections. A unique differential cutoff driver switches from a standard PECL V_{OH} level to cutoff. In the cutoff state the outputs present a high impedance which is required to implement a true shared bus. The part features a 32–bit wide parallel TTL compatible I/O interface that can connect directly with standard memory or bus transceiver devices. The control pins are all TTL compatible to simplify interfacing requirements. The serial interface is PECL (Positive Emitter Coupled Logic) which provides excellent transmission line drive capability. Because the serial bus is implemented using differential ECL technology, the receiver circuitry exhibits excellent common mode noise rejection.

- 100MByte/s Serial Data Transfer Capability
- TTL Compatible Parallel Interface
- Supports 16– or 32–Bit Data Bus Interfaces
- Bus Driving Differential ECL Serial Outputs
- On–Board Clock Recovery and Data Synchronization
- 64–Pin Surface Mount CQFP Packaging
- Parallel Data Bus Handshake Control

An innovative data synchronizing architecture allows data to be transmitted in bursts without preamble bits. This allows instantaneous data acquisition without the inherent overhead of traditional PLL clock recovery. Thus, the data transfer is nearly overhead free with only one synchronization bit for every byte of data transmitted. Insertion and removal of synchronization bits are totally transparent to the user.

The AutoBahn supports variable data transfer rates. This is accomplished by combining the fixed burst transfer rates of 50 or 100MByte/s with a flexible method of allowing data to be written into the AutoBahn for transfer. If new data has not been written into the parallel data register prior to the completion of a serial data burst, the AutoBahn will insert a gap in the serial data stream. Therefore, the effective throughput of the serial bus is throttled by the speed of the parallel host interface which writes data to the chip.

With its very high block data transfer capability and instantaneous start up ability, the AutoBahn is ideally suited for multimedia graphics applications and parallel processing architectures requiring multi–processor communication links.

Motorola's state–of–the–art MOSAIC V™ process allows for the realization of 1.8GHz internal clock rates at power levels which are compatible with today's low profile surface mount packages. Furthermore, the design is implemented with a flow–through pinout architecture to simplify PCB layout and routing. The board space efficiency of the CQFP ensures that the AutoBahn device will prove valuable in the most demanding space conscious applications.

The AutoBahn chip works from a single +5.0V supply. Separate internal V_{CC} busses isolate the TTL outputs from the high speed PECL circuitry.

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'Spanceiver' has been formed as a contraction of Serial/Parallel Transceiver.

MOSAIC V is a trademark of Motorola, Inc.

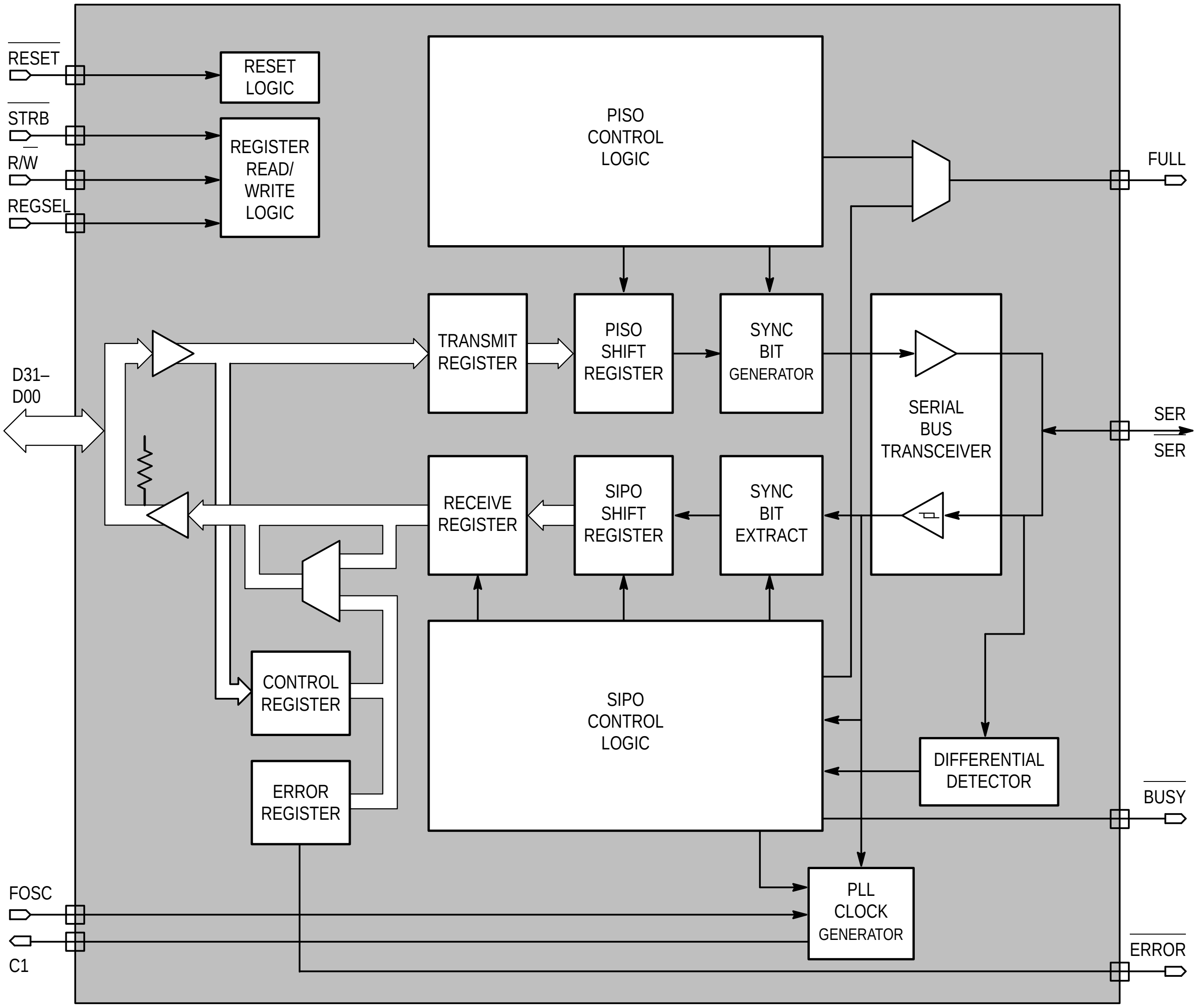


Figure 1. Simplified Block Diagram

PIN DESCRIPTIONS

Name	I/O	Description
TTL COMPATIBLE I/O		
$\overline{\text{RESET}}$	I	Asynchronous reset signal which places the AutoBahn into default state. In most applications, $\overline{\text{RESET}}$ should only have to be asserted on system startup.
R/$\overline{\text{W}}$	I	Read/Write control signal. Used to select between writing to or reading from the AutoBahn.
REGSEL	I	Control signal used to select between the Parallel Data Register and the Control and Error Register(s). A logic 'H' selects the data register while a logic 'L' selects the Control and Error Register(s).
D00 – D31	I/O	Bi–directional data inputs/outputs. These pins comprise the data bus to be used to interface to the user host interface. D00 is the least significant bit.
$\overline{\text{STRB}}$	I	Data strobe signal. During a write, it indicates that data is valid on the parallel bus. While in a read, it indicates that the AutoBahn can now place data on the parallel interface.
FULL	O	Signal which indicates that the transmitter or receiver presently contains data. In conjunction with the $\overline{\text{STRB}}$ signal, it is used to implement a two signal handshake for parallel data transfers.
$\overline{\text{BUSY}}$	O	Serial bus $\overline{\text{BUSY}}$ signal, used to indicate to the parallel interface that the AutoBahn bus is presently in use.
$\overline{\text{ERROR}}$	O	Control output which is used to indicate that the AutoBahn has identified a fault condition. The error condition can then be read out from the Error Register.
FOSC	I	25.00MHz clock source from a crystal oscillator reference.
PECL COMPATIBLE I/O		
SER/$\overline{\text{SER}}$	I/O	Differential serial data inputs/outputs which operate at modified PECL levels.

POWER, GROUND AND FILTER PINS

Name	Number	Description
C1	1	PLL Filter Capacitor Pin
V_{CCE}	1	Positive Supply for Internal PECL Logic Circuitry
V_{CCO}	1	Positive Supply for PECL Outputs
V_{EE}	1	Ground for PECL
V_{CCT}	7	Positive Supply for TTL Compatible Signals
V_{EET}	8	Ground for TTL Compatible Signals
V_{CCX}	1	Positive Supply for VCO
V_{EEX}	1	Ground for VCO

BLOCK DIAGRAM FUNCTIONAL DESCRIPTION

Reset Logic

The Reset Logic generates the internal reset signal used to set the device into a known state. The reset signal clears the Control and Error Registers and resets the SIPO and PISO Control Logic. The external reset signal is validated with the FOSC input clock to assure that a valid reset pulse has been applied to the chip. The external reset input pin (RESET) must be low for a minimum of 125 nsec after the FOSC input is stable. STRB assertion may occur no earlier than 500 nsec after RESET deassertion (reset recovery time).

Control Register

The Control Register is used to configure the operation of the AutoBahn. The register fields are described in detail in the section containing the Control and Error Register Bit Definition.

Register Read/Write Control Logic

This logic is utilized to access the Transmit Register, the Receive Register, and the Control and Error Registers from the parallel bus. The interface protocol utilizes two direction control signals (R/W and REGSEL). The actual handshake to read or write data from the chip is accomplished with the input STRB signal , combined with the output FULL signal.

Transmit Register

The transmit register is a 32–bit wide parallel–loadable register. This register interfaces to the bi–directional TTL compatible data bus. Access to this register is controlled via the Register Read/Write Logic.

PISO Shift Register

The PISO (Parallel In/Serial Out) Register accepts data from the Transmit Register and converts it into a serial bit stream. This register is under control of the PISO Control Logic. The shift register can be adjusted to handle 16–bit or 32–bit data traffic based on the state of the appropriate field in the Control Register.

PISO Control Logic

The PISO (Parallel In/Serial Out) Control Logic is responsible for controlling the transfer of data out from the AutoBahn to the serial bus. This logic interfaces to the PISO Shift Register and the SYNC Bit Generator. It is driven by the PLL Clock Generator.

SYNC Bit Generator

This circuitry inserts one bit of timing information into the data stream before every byte of data is sent to the Serial Bus Transceiver and transmitted. This timing information is used by the receiver to properly re–clock the incoming data stream. To support the maximum data rate of 100 MByte/sec, the actual serial shift rate is 900 MBit/s NRZ, rather than 800 MBit/s NRZ. The insertion and removal of SYNC bits is transparent to the end user.

Serial Bus Transceiver

The transceiver implements a two signal bi–directional differential bus. The transceiver circuitry consists of a highly sensitive differential receiver and a cutoff driver. The receiver accepts a differential signal from the serial bus. This differential signal is amplified and limited by the receiver before being routed to the clock generation circuitry for clock extraction and data re–timing.

The cutoff driver is used to transmit serial data on to the bus. The outputs switch between a normal HIGH level (V_{OH}) and a cutoff LOW signal – when low the output emitter follower is turned 'off', thus presenting a high impedance to the bus. If the cutoff driver is disabled, both outputs of the differential pair go to the cutoff state so the bus resource is available for use by other AutoBahn chips sharing the same bus.

Differential Detector

The differential detector is used to recognize when the serial bus goes out of the cutoff state and into a differential steady state condition. The differential detector is only utilized at the very start of a transmission. The detector informs the SIPO Control Logic that the serial bus is no longer in cutoff so that the bus BUSY signal can be asserted by the device.

PLL Clock Generator

The Clock Generator circuitry synthesizes a master timing clock from the frequency reference signal (FOSC) input. The clock generator provides timing signals used to support the transfer rate of 900 MBit/s. The clock is generated by a Phase Locked Loop (PLL) which requires a simple external capacitor to set the loop filter bandwidth. The value for C1 is 2700 pF. This circuitry is used to provide the master timing for the PISO and SIPO Control Logic blocks.

SYNC Bit Extractor

The SYNC Bit Extractor removes each SYNC bit from the incoming data stream. It is controlled by the SIPO Control Logic. If a SYNC bit is not detected at the proper bit time in the extraction process, a field will be set in the Error Register to indicate that a transmission error has occurred.

SIPO Shift Register

The SIPO (Serial In/Parallel Out) Register accepts data from the SYNC Bit Extractor and converts it into a parallel word that is then transferred to the Receive Register. The operation of this shift register is controlled by the SIPO Control Logic.

SIPO Control Logic

The SIPO (Serial In/Parallel Out) Control Logic is responsible for controlling the transfer of data into the AutoBahn. This circuitry performs all the critical control functions to allow the AutoBahn to accept and process the incoming serial data stream. The SIPO Control Logic has the ability to detect certain transmission related errors and set the appropriate field(s) in the Error Register.

Receive Register

The receive register is a 32–bit wide parallel load register. It accepts data from the SIPO (Serial In/Parallel Out) Shift Register. This register interfaces to the bi–directional TTL compatible data bus. Access to this register is controlled via the Register Read/Write Logic.

Error Register

The AutoBahn has the capability to detect certain transmission related error conditions. These errors are detected by the SIPO Control Logic which sets the appropriate error field in the Error Register. The register fields are described in detail in the section containing the Control and Error Register Bit Definition. The Error Register has additional logic that is used to generate the ERROR signal.

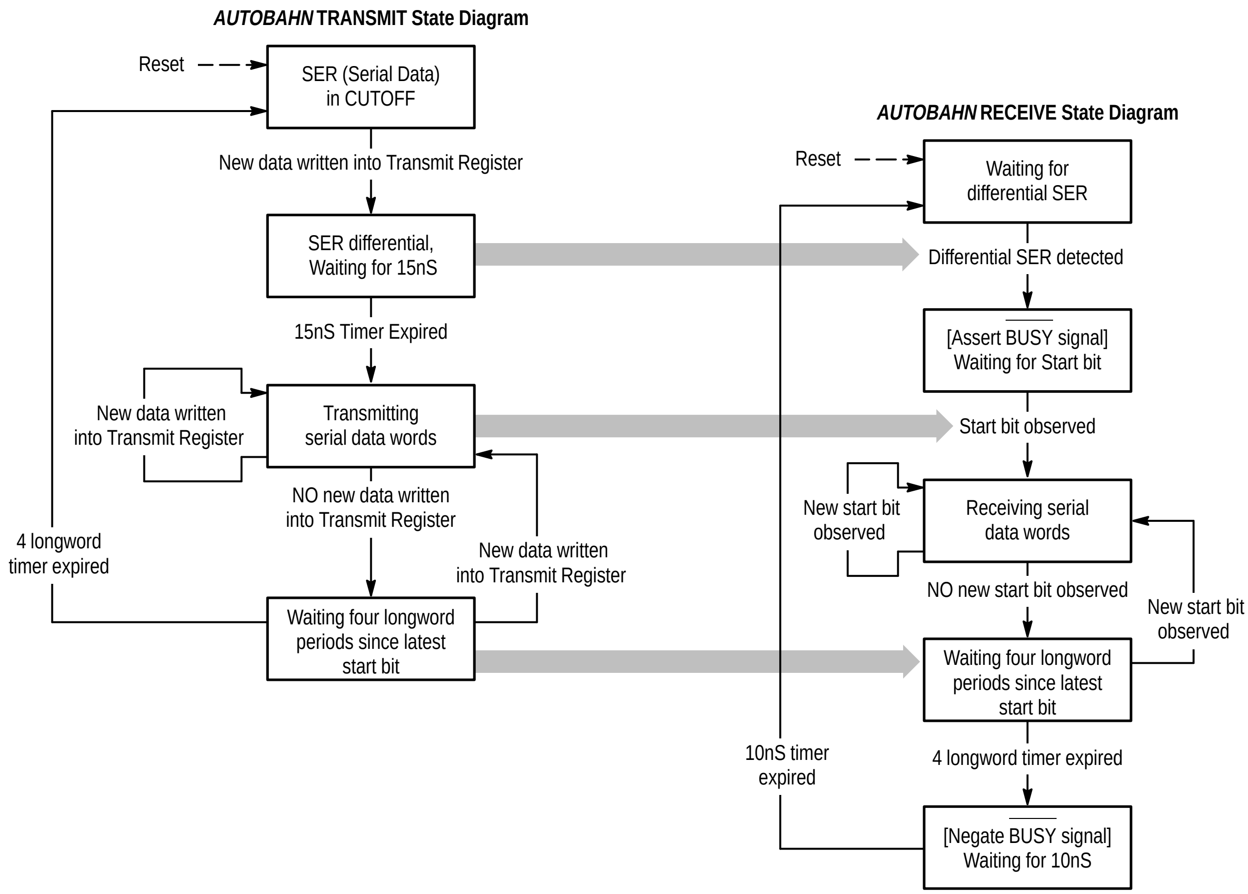


Figure 2. Transmit and Receive State Diagram

THEORY OF OPERATION AND TRANSMIT TIMING PRINCIPLE

The AutoBahn is a high speed data mover resource for use in parallel bus systems, such as the VMEbus. It is also suitable for proprietary bus architectures and point–to–point links. All necessary logic, such as multiplexing/de–multiplexing, control, and timing generation is incorporated on chip. External control signals and a frequency reference must be provided to the device. Arbitration is off loaded to the parallel bus system; thus, no collision detection or protocol overhead is required for the chip. The AutoBahn has three primary operating modes:

– Idle
– Transmit
– Receive

Figure 2 has been included to aid in understanding the operation of the device.

Idle Mode

After the device has been reset, the default operating mode is Idle. In the default condition the serial bus is cut off and the receiver is 'listening' to detect activity on the serial bus. The function of this mode is to detect serial bus activity and assert a $\overline{\text{BUSY}}$ signal. In a VME type application, this signal is used by the local controller to determine when to arbitrate for the serial bus resource.

Transmit Mode

To begin a transfer, data is written into the parallel data register. This event starts an internal timeout timer. The AutoBahn transfers the data to the serial transmit register, inserts timing information, and shifts the data out the serial bus. The timing information adds one additional bit into the data stream for every byte of data. Because the data is NRZ, a 900MBit/s data rate translates into a maximum frequency of 450MHz.

If a new word has been loaded into the parallel data register, the next transfer will begin. Otherwise, the differential output driver will hold the serial bus at the state of the last data bit transmitted. The bus will be held in this state until new data is loaded into the parallel data register or the timeout time expires.

The timeout timer runs for a period of four 32–bit transfer times. The transfer rate is selected through control register select bits. As an example, in 32–bit mode with a transfer rate of 100MByte/s, a new data word is transferred approximately every 40ns (32 data bits + 4 synchronization bits = 36 bits * 1.1ns/bit). For this case, the timeout timer runs for approximately 160ns. The timeout timer is re–started every time a new serial word transmission begins.

The transmit timeout timer serves two functions. It allows the termination of block data transfers without the need for explicit external control. After the last word in a data block is written into the device, the timeout timer will expire and the device will return to the idle state. More importantly, it allows the AutoBahn to support a broad range of data transfer rates. If a hardware design application only needs capacity to transfer data at 60MByte/s, the AutoBahn will automatically burst the data out at 100MByte/sec and insert pauses in the serial data stream to accommodate the slower parallel data transfer rate. This means the user can tailor the design of the parallel memory interface to meet the needs of the application, while still taking advantage of the performance of the AutoBahn.

Since the AutoBahn only has one level of elastic storage, the receiver memory interface must be able to support the same transfer rate as the transmitter.

Receive Mode

When the AutoBahn is operating in receive mode it strips off the timing information and clocks the data into the serial register. When the register is full, it transfers the data into the parallel data register and asserts the FULL signal pin to indicate the presence of data. The interface hardware detects the presence of new data and reads out the content of the data register. In receive mode, a timeout timer is also employed to handle the end of data transfer termination. The receive timeout timer operates in the same manner as the transmit timeout timer. Every time new data is received, the timeout timer is re–started. If no data is received, the timeout timer will expire and the part will return to the idle state. Typical data transmission waveforms are shown in Figure 3 and Figure 4.

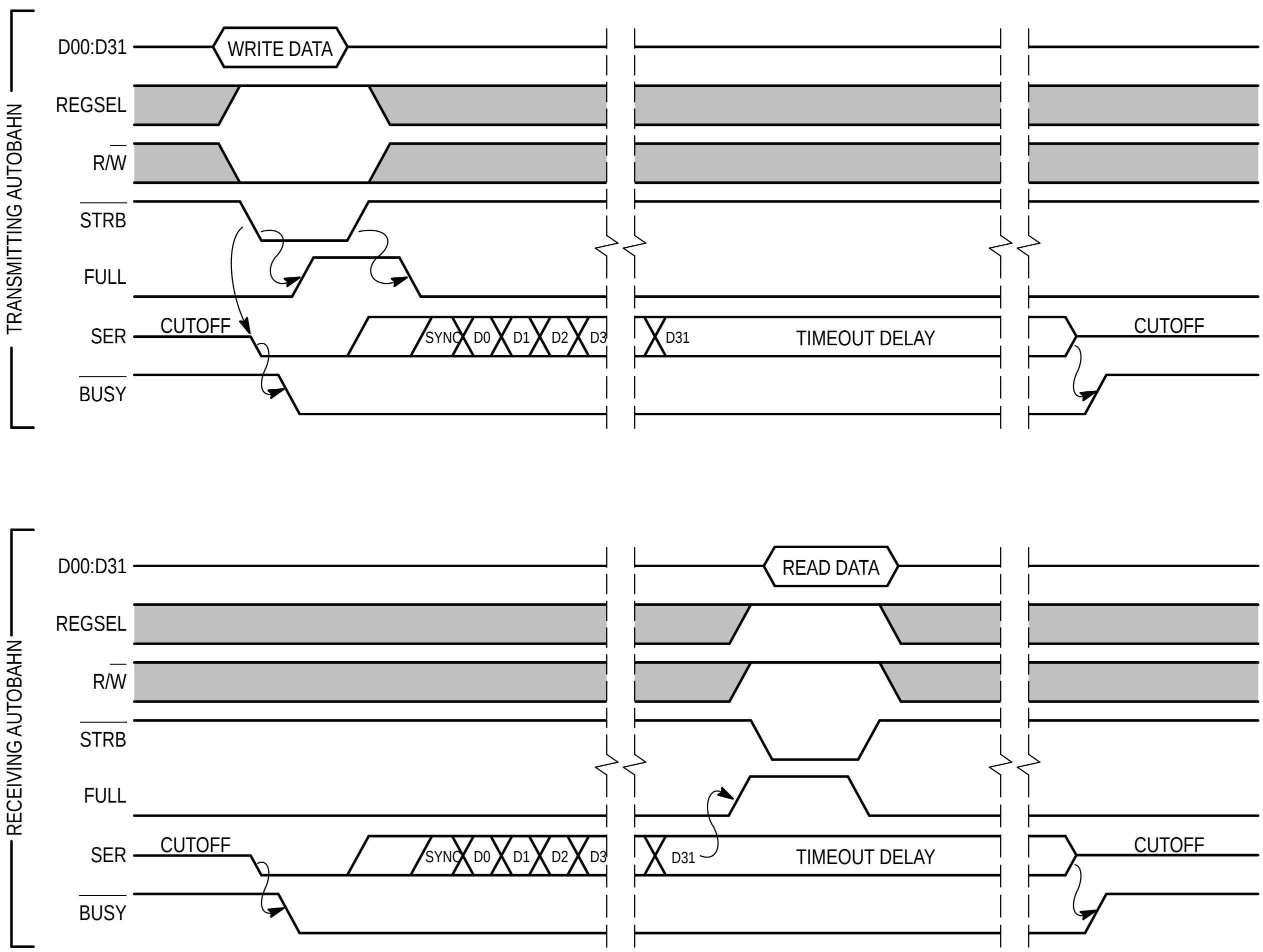


Figure 3. Transmit and Receive Timing for a Single 32–Bit Longword Transmissions

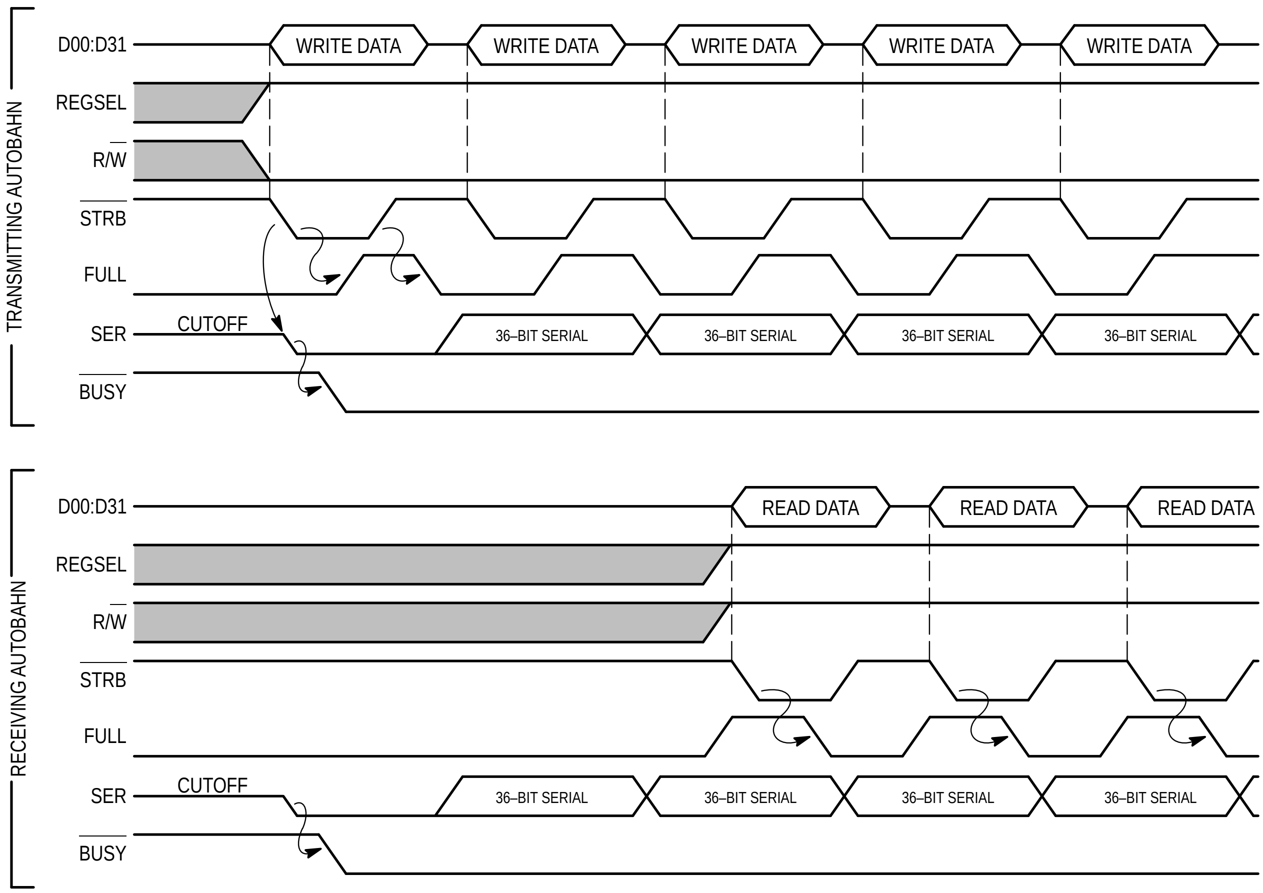


Figure 4. Transmit and Receive Timing for Burst Transmission

APPLICATION CIRCUIT AND POWER SUPPLY

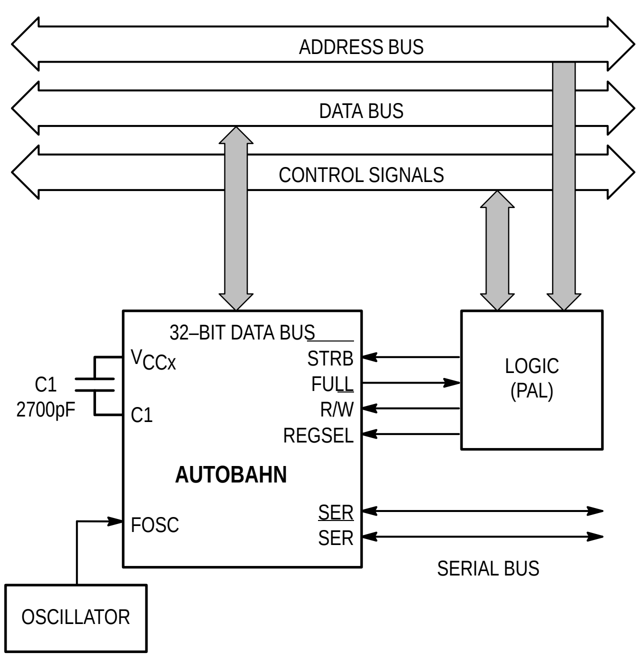
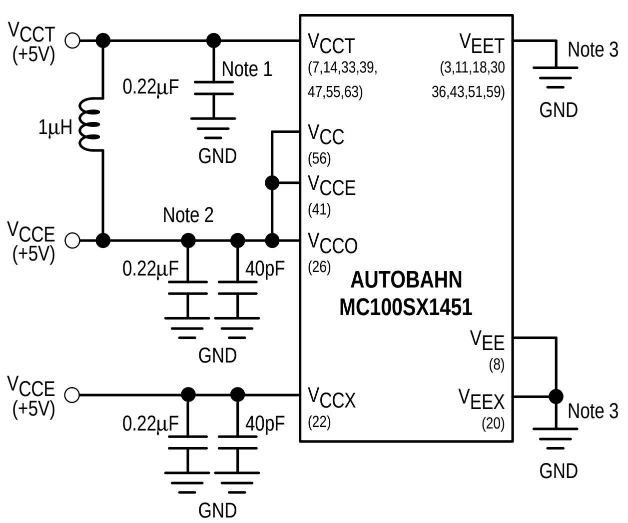


Figure 5. Simplified Application Circuit



Note 1: Capaitor located close to every pin.
Note 2: If separate supply planes for ECL and TTL are available, the inductor is not necessary.
Note 3: A common ground plane for TTL and ECL must be used.

Figure 6. Power Supply Filtering

PECL DESIGN CONSIDERATIONS

The differential serial bus is realized using PECL (Positive Emitter Coupled Logic). PECL is normal ECL with the V_{CC} and V_{EE} power supplies levels shifted from ground and –5.2V to +5.0V and ground respectively. This change simplifies the requirements of interfacing high speed ECL circuitry and TTL circuitry on the same chip and improves the user system architecture because only a single power supply is required.

The output driver circuitry is an open emitter, emitter follower which generates PECL levels when terminated by a pull down resistor to an appropriate reference voltage. The output emitter follower circuitry is optimized to drive transmission lines. To minimize line reflections, the transmission line should be terminated with the line characteristic impedance, in most cases 50Ω. The simplest and most robust method of realizing this termination in PECL is with a resistor divider network referenced to V_{CC}. This means the PECL output levels and the termination voltage will then be referenced to the same V_{CC} supply.

Figure 8 is the equivalent circuit for the serial bus. Resistors R1 and R2 are used to implement a simple voltage divider with the characteristic impedance of the transmission line. The following equations are used to solve for these values.

$$R1 = R2\ (\{V_{CC} - V_{TT}\}/\{V_{TT} - V_{EE}\})$$
$$R2 = Z_O\ (\{V_{CC} - V_{EE}\}/\{V_{CC} - V_{TT}\})$$
$$V_{TT} = V_{CC}\ (R2/\{R1 + R2\})$$

For the typical setup:

V_{CC} = 5.0V; V_{EE} = GND; V_{TT} = 3.0V; and Z_O = 50Ω

R2 = 50 ({5 – 0}/{5–3}) = 125Ω
R1 = 125 ({5–3}/{3–0}) = 83.3Ω

More detailed information about PECL and thevenin equivalent termination schemes can be found in Motorola Application Note AN1406/D – “Designing with PECL”.

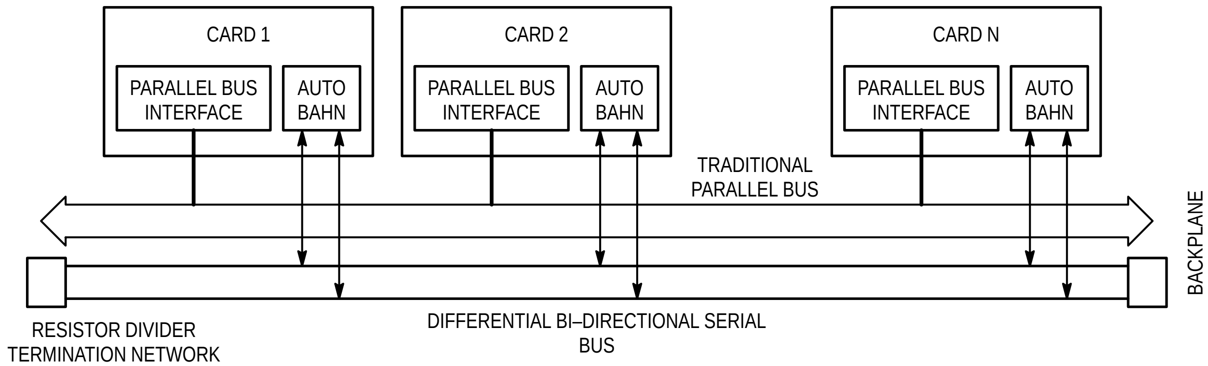


Figure 7. Typical Bus Application

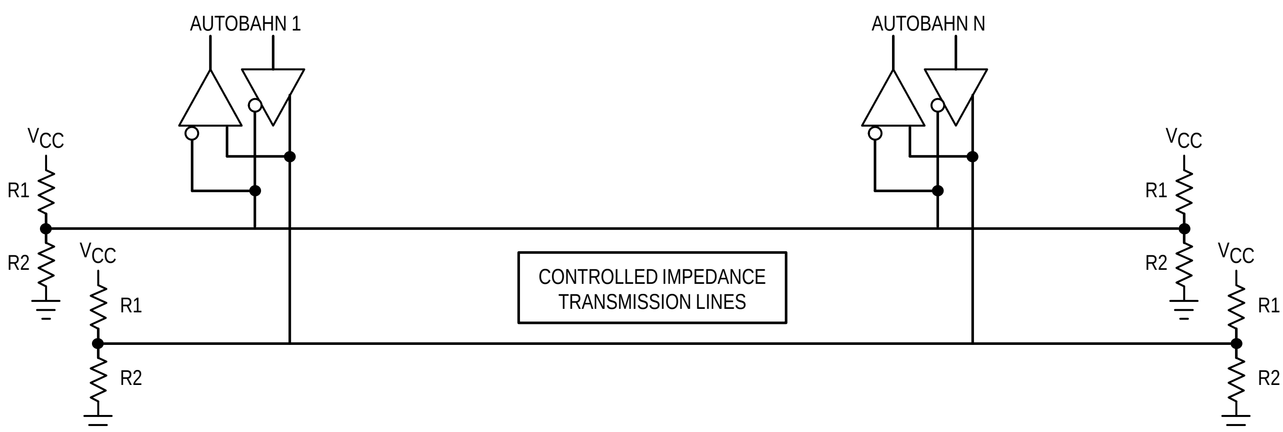


Figure 8. Equivalent Circuit for Serial Bus

CONTROL AND ERROR REGISTER BIT DEFINITIONS

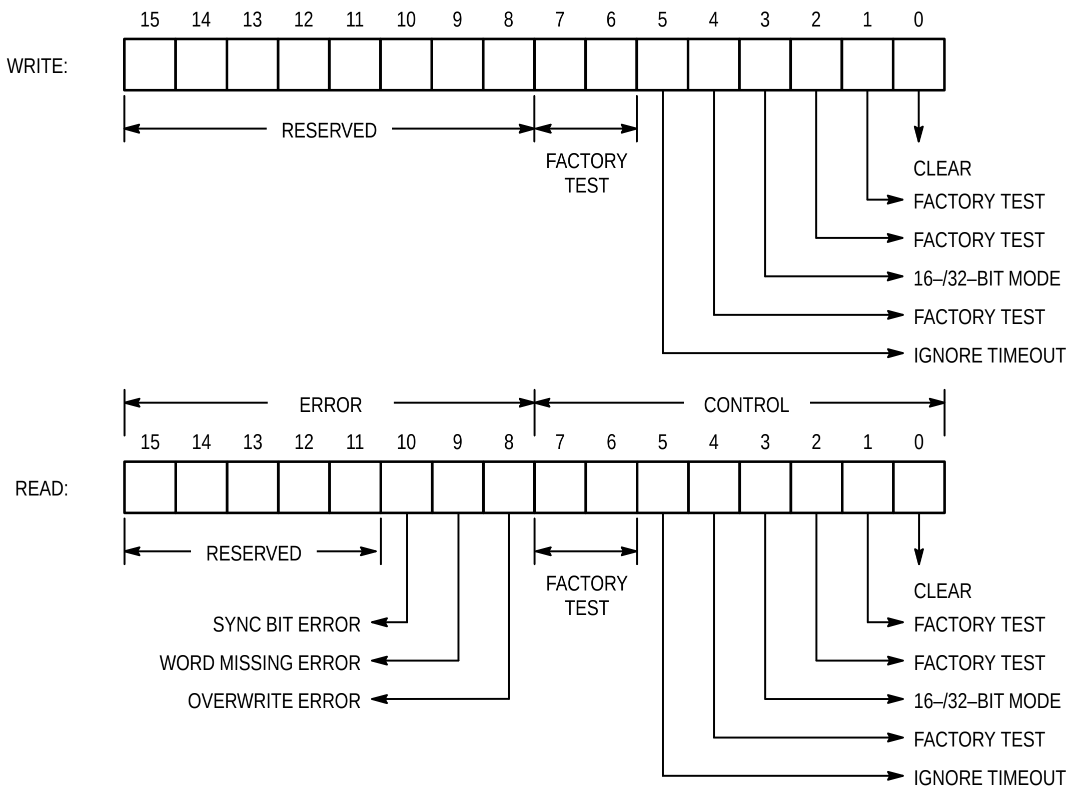


Figure 9. Control and Error Register Definitions

Clear

Asserting this bit clears the internal control logic and terminates any transmit or receive activity. To remove the Clear condition, this bit must be set to a logic 'H' which sets the chip into the Idle mode.

H Normal Operation
L Clear

16/32 Bit Mode

This bit defines the data width on the host interface. This feature allows the AutoBahn chip to be used in systems with either 16–bit or 32–bit data width without the need for additional interface hardware. In 16–bit mode, the data bus used is D00 – D15.

H 32–bit data width
L 16–bit data width

Factory Test

These bits are used by the manufacturer for testing the product. It must be set to a logic 'H' state for proper operation.

H Normal Operation

Ignore Timeout

This bit is used to disable the timeout timer for the transmitter. The purpose of this bit is to allow for the establishment of permanent or temporary dedicated links. When this bit is asserted, the timeout timer will be ignored by the PISO Control Logic. This bit only needs to be set in the transmitting AutoBahn chip. To exit this mode, the Control Register must be accessed, and the field must be de–asserted.

H Normal Operation
L Disable Timeout

Overwrite Error Flag

This bit will be set if the data in the parallel register is overwritten. This can occur in Receive mode if data is not read from the parallel register in a timely manner. The overwrite error does not occur in idle mode.

H Overwrite
L No Overwrite

Word Missing Error

This bit will be asserted if the second half of a 32–bit transfer is not completed before the time out timer expires. This can occur if the transmitter fails to complete the transfer. This field will be asserted only after the timeout timer expires.

H Word Missing Error
L No Error

SYNC Bit Missing Error

This bit will be asserted if the AutoBahn detects that a SYNC bit has not been received at the proper time by the PISO Control Logic. If this bit has been asserted then the data has been corrupted.

H SYNC Bit Missing Error
L No Error

Reserved Bits

All reserved bits are allocated for future enhancements. The user must write logic 'H' values into these bits. Reserved bits are read back as 'do not care'.

CRYSTAL OSCILLATOR REQUIREMENTS

The AutoBahn requires a high quality frequency source (FOSC) which is used as the reference for the PLL Clock Generator. The performance requirements were targeted to provide the AutoBahn chip appropriate design margin for the serial data transfer operation as well as to allow the user flexibility is selecting a commercially available low cost crystal oscillator. Below is a list of the key performance attributes of the crystal oscillator.

Parameter	Rating
Frequency	25.000MHz
Stability	±100ppm
Output Levels	TTL
Duty Cycle	45% / 55% at 1.5V
Rise/Fall Time	≤7nsec
Operating Range	0°C to 70°C
Startup Time	10msec

There are many suppliers of high quality crystal oscillator frequency sources which meet or exceed the above requirements. One such supplier is JVC. Their part numbers for 25MHz oscillators are as follows: VX4321–2500 (Metal Can) or SMC2500 (SMD).

THERMAL CONSIDERATIONS

As in any system, proper thermal management is essential to establish the appropriate trade–off between performance, density, reliability, and cost. In particular, the designer should be aware of the reliability implications of continuously operating semiconductor devices at high junction temperatures.

The increasing use of surface mount devices (SMD) is putting a greater emphasis on the need for better thermal system management. SMD devices require less board space than their through–hole equivalents; so, designs incorporating SMD technologies have a higher thermal density. To optimize the thermal management of the system, it is imperative that the user understand all the variables which contribute to the device junction temperature.

By proper package selection, the vendor can select the proper package and die attach method to decrease the thermal resistance and thus the junction temperature of the device. The user has the greatest control of additional variables which commonly impact the thermal performance of the device. Ambient temperatures, air flow, and related cooling techniques are obvious user–controlled variables; however, PCB substrate material, layout density, size of the air gap between the board and the package, amount of exposed copper interconnect, use of thermally conductive epoxies, and the number of boards in a chassis can all have significant impacts on the thermal performance of the system.

PCB substrates have different thermal characteristics which should be explored when considering alternatives. The user should also account for the different power dissipations of various components in the system and space them on the PCB accordingly. In this way the heat load is spread across a larger area and "hot spots" do not appear in the layout. Copper interconnect traces act as heat radiators; therefore, improved thermal dissipation can be achieved through the addition of interconnect traces on the top layer. Finally, thermally conductive epoxies can accelerate the transfer of heat from the device to the PCB where it can be more easily transferred to the ambient.

The following equation can be used to estimate the junction temperature of a device in a given environment:

$$T_J = T_A + P_D * \Theta_{JA}$$

T_J Junction Temperature
T_A Ambient Temperature
P_D Power Dissipation
Θ_{JA} Average Package Thermal Resistance (Junction – Ambient)

The power dissipation is comprised of two elements: the internal gate power and the power associated with the output signals. Essentially, the two contributors can be calculated separately, then added to give the total power dissipation for the device. The source of the output power distribution depends on whether the device is transmitting or receiving. In transmit mode, the PECL outputs are dissipating power, while in receive mode, the parallel outputs are dissipating dynamic power. The worst case condition, when the AutoBahn is in receive mode, is described below.

$$P_D = P_{static} + P_o\ (TTL)$$

where $Pstatic = I_{CC} * V_{CC}$

V_{CC} Operating voltage
I_{CC} Static DC Current

and $Po\ (TTL) = No * C_L * F_D * V_S\ \hat{}2$

C_L Capacitive load (in pF)
F_D Parallel Data Rate (0.5 * # MBits/sec)
V_S Output Swing
No Number of outputs (16 or 32)

For a typical application:

C_L	20 pF
F_D	0.5* 100 MBits/s
V_S	3.8 V
No	32 outputs
V_{CC}	5V
I_{CC}	700 mA

$P_D = 470 * 5 + 32 * 20pF * 25 MHz*3.8^2$

$P_D = 3.5 + 0.231W = 3.73W$

The ceramic quad flat package selected is manufactured from an Aluminum nitride (AlN) ceramic material for optimum thermal performance. A table of the average Θ_{JA} values for this package under various air flow conditions is listed below:

Air Flow (m/sec)	Θ_{JA} (°C/W)
0	40
1	32
2	23

With this information, the user can estimate the junction temperature of the device in their application.

MAXIMUM RATINGS*

Symbol	Parameter		Value	Unit
V_{CC}	Power Supply (V_{EE} = 0V)		–0.5 to 6.5	V
V_{IN}	Input Voltage (V_{EE} = 0V)		–0.5 to 6.5	V
I_{OUT}	PECL Output Current	Continuous Surge	50 100	mA
$I_{OUT–TTL}$	TTL Output Current		TBD	
T_A	Operating Temperature Range		0 to 70	°C
T_{STG}	Storage Temperature Range		–50 to +175	°C
T_J	Maximum Junction Temperature		175	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

TTL DC CHARACTERISTICS ($V_{CCT} = V_{CC} = V_{CCO}$ = 5.0V ±5%)

Symbol	Parameter	Min	Typ	Max	Unit	Condition
I_{IH}	Input HIGH Current			0.7	µA	$V_{IN} = V_{CC}$
I_{IL}	Input LOW Current			–0.6	mA	V_{IN} = GND
V_{OH}	Output HIGH Voltage	2.5			V	I_{OH} = –2mA
V_{OL}	Output LOW Voltage			0.5	V	I_{OL} = 5.0mA
V_{IH}	Input HIGH Voltage	2.0			V	
V_{IL}	Input LOW Voltage			0.8	V	
I_{OZ}	Tri–State Current			±15	µA	
I_{CC}	Device Current Drain		700	760	mA	

100E PECL DC CHARACTERISTICS ($V_{CCT} = V_{CC} = V_{CCO}$ = 5.0V ±5%)

Symbol	Parameter	Min	Max	Unit	Condition
I_{IH}	Input HIGH Current		200	µA	
I_{IL}	Input LOW Current	0.500		µA	
V_{OH}	Output HIGH Voltage	3.975	4.25	V	
V_{CUT}	Output CUTOFF Voltage	3.000	3.07	V	Note 1.
V_{IH}	Input HIGH Voltage	3.835	4.12	V	
V_{IL}	Input LOW Voltage	3.000	3.07	V	
V_{PP} (DC)	Input Sensitivity	150		mV	Note 2.

NOTE: PECL levels are referenced to V_{CC} and will vary 1:1 with power supply. The outputs are loaded with an equivalent 25Ω termination to +3.0V. The values shown are for $V_{CC} = V_{CCO} = V_{CCT}$ = 5.0V.

1. Valid when the equivalent termination voltage is 3.0V to assure proper operation.
2. V_{PP} is the minimum differential input voltage required to assure proper operation.

AC CHARACTERISTICS ($V_{CC} = V_{CCO} = V_{CCT}$ = 5.0V ±5%; $V_{EE} = V_{EEX} = V_{EET}$ = GND)

Symbol	Characteristic	Name	Wave–form	0°C			25°C			70°C			Unit	Condition
				Min	Typ*	Max	Min	Typ*	Max	Min	Typ*	Max		
t_s	Setup Time R/W→STRB REGSEL→STRB Data→STRB	T2	2	1.0			1.0			1.0			ns	
t_h	Hold Time STRB→R/W STRB→REGSEL	T3	2	3.0			3.0			3.0			ns	
t_{pd}	Propagation Delay STRB→FULL	T4	2	4.0	6.0	9.0	4.0	6.0	9.0	4.0	6.0	9.0	ns	
t_h	Hold Time STRB→Data	T5	2	3.0			3.0			3.0			ns	
t_{pd}	Propagation Delay SER→BUSY	T6	3	6.0	8.0	10.0	6.0	8.0	10.0	6.0	8.0	10.0	ns	
t_s	Setup Time R/W→STRB REGSEL→STRB	T7	4	2.0			2.0			2.0			ns	
t_h	Hold Time STRB→R/W STRB→REGSEL	T8	4	1.0			1.0			1.0			ns	
t_{pd}	Propagation Delay STRB→Data Valid	T9	4	7.0	8.5	18.0	7.0	8.5	18.0	7.0	8.5	18.0	ns	Note 1 on page 13
t_{pd}	Propagation Delay STRB→FULL	T10	4	5.5	8.0	10.0	5.5	8.0	10.0	5.5	8.0	10.0	ns	Note 1 on page 13
t_{pd}	Propagation Delay STRB→Data Invalid	T11	4	12.0	14.0	17.0	12.0	14.0	17.0	12.0	14.0	17.0	ns	Note 1 on page 13
t_s	Setup Time R/W→STRB REGSEL→STRB Data→STRB	T12	5	1.0			1.0			1.0			ns	
t_h	Hold Time STRB→R/W STRB→REGSEL	T13	5	3.0			3.0			3.0			ns	
t_h	Hold Time STRB→Data	T14	5	3.0			3.0			3.0			ns	
t_{pw}	Pulse Width STRB	T15	5	7.0		12.0	7.0		12.0	7.0		12.0	ns	
t_s	Setup Time R/W→STRB REGSEL→STRB	T16	6	2.0			2.0			2.0			ns	
t_h	Hold Time STRB→R/W STRB→REGSEL	T17	6	2.0			2.0			2.0			ns	
t_{pd}	Propagation Delay STRB→Data Valid	T18	6	7.0	8.5	18.0	7.0	8.5	18.0	7.0	8.5	18.0	ns	
t_{pw}	Pulse Width STRB	T19	6	7.0		12.0	7.0		12.0	7.0		12.0	ns	
t_{pd}	Propagation Delay STRB→Data Invalid	T20	6		14.0	17.0		14.0	17.0		14.0	17.0	ns	
t_r, t_f	TTL Rise/Fall Time	—	—		3.0			6.1 12.6			3.0		ns	10 – 90% 15pF Load
t_r, t_f	PECL Rise/Fall Time	—	—		200			770 930			200		ps	20 – 80%

* Values for 0°C and 70°C are target values. Typicals for 25°C are taken from a small measurement database. Min and Max values are derived from using 3 sigmas point of the data distribution and will be added when the data becomes available.

Note 1:
Propagation Delay T9

Becasue the typical use of the AutoBahn is in a shared bus system, the propagartion delay T9 (STRB –> data valid) is the time between the falling edge of STRB and OUTPUT ACTIVE of the receiver. The crosspoint of 1.5V is dependent on the bus environment. See Figure 10.

Propagation Delay T10

This value is taken with the high impedance active probe. With a higher load at the pin, this value will be higher up to 5%.

Propagation Delay T11

The definition of the propagation delay T11 corresponds to T9. In this case, T11 is the time between the rising edge of STRB and the HIGH IMPEDANCE of the receiver. That means, other talker of the common bus have to wait for T11 to send datas to the bus. See Figure 10.

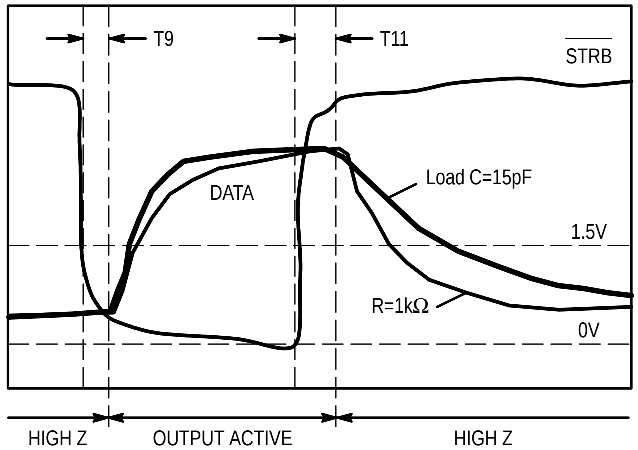
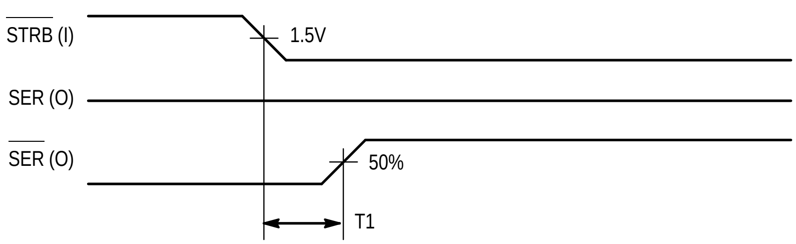


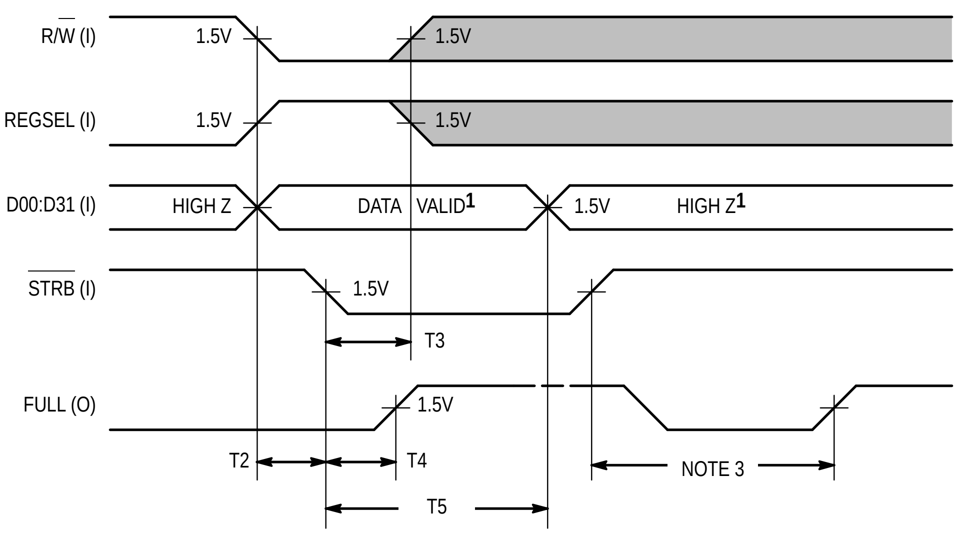
Figure 10. Definition of the Waveforms STRB → Data Valid

TIMING WAVEFORMS



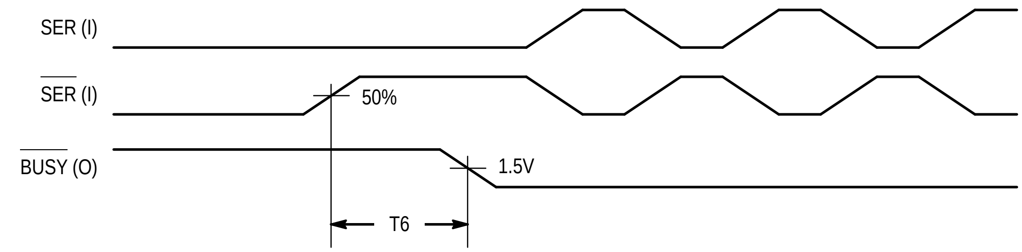
NOTE 2: T1 (STRB to SER differential) is indeterminate, varying from 3 to 9 bit clock cycles due to synchronization circuitry to avoid metastability.

Waveform 1. Start of Transmit Timing

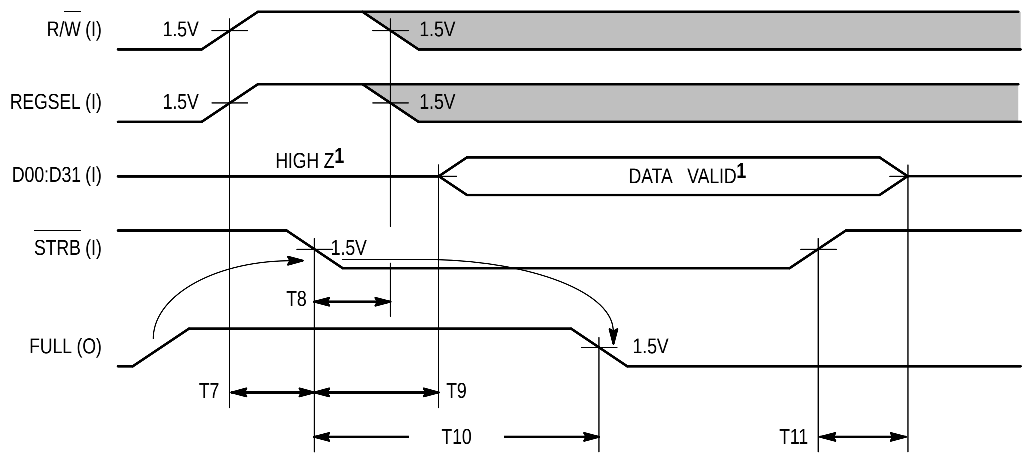


NOTE 3: STRB deassertion to next FULL a minimum of 18 nsec.

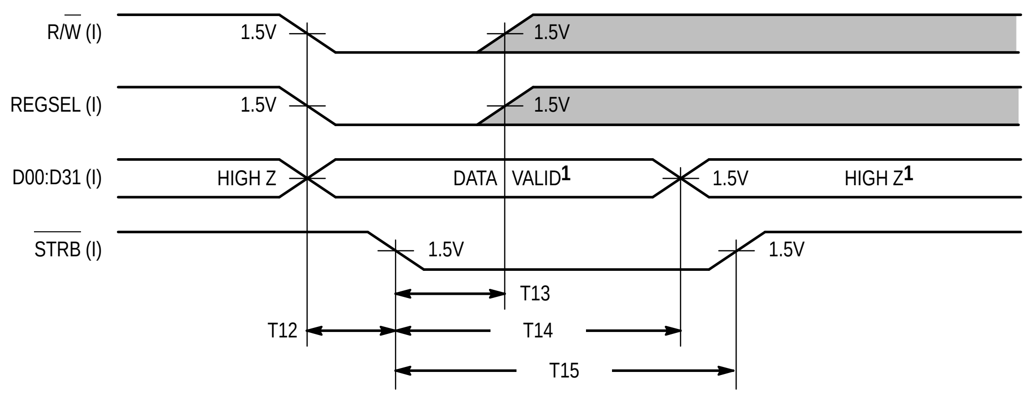
Waveform 2. Transmit Mode – Data Transfer Handshake



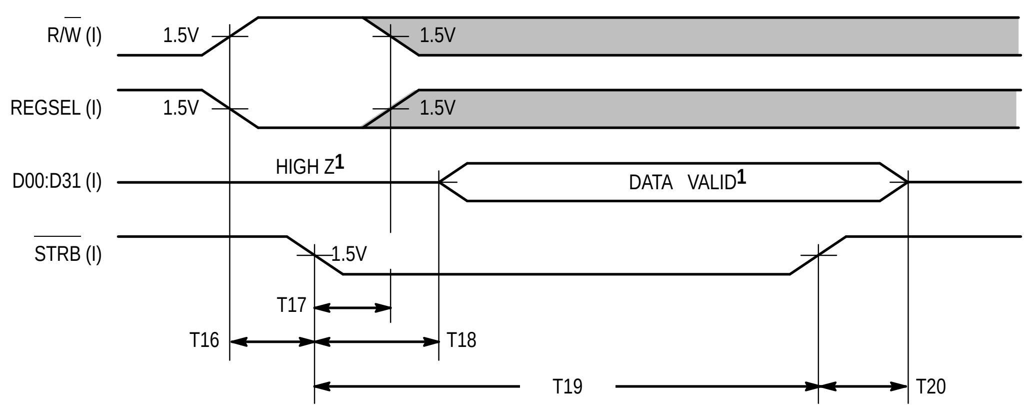
Waveform 3. Timing for Detection of a Steady–State Differential Condition on the Serial Bus



Waveform 4. Receive Mode – Data Transfer Handshake



Waveform 5. Write to Control Register



Waveform 6. Read from the Control and Error Registers

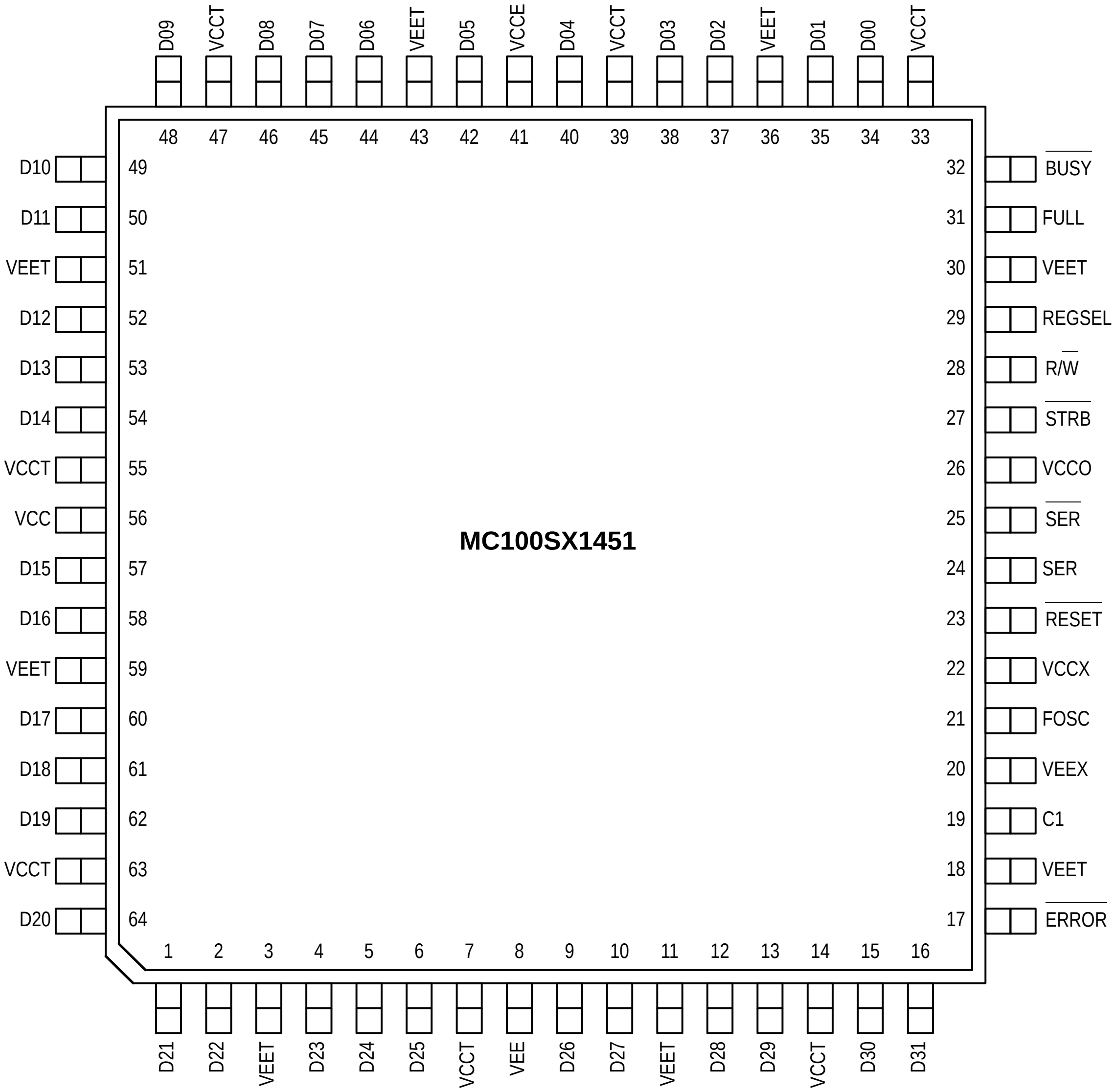
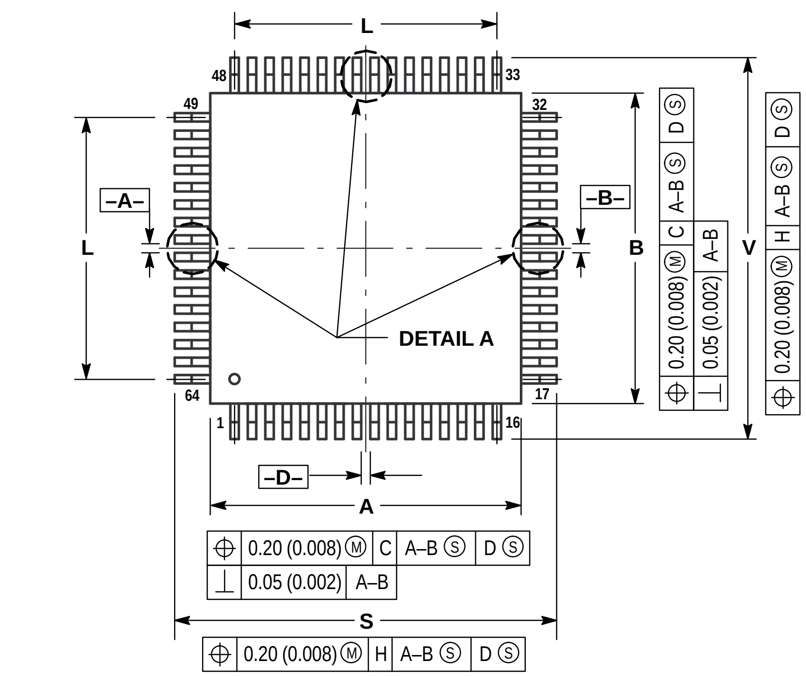
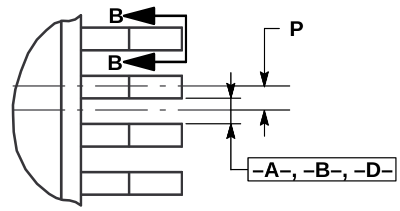


Figure 11. Pinout: 64–Lead CQFP (Top View)

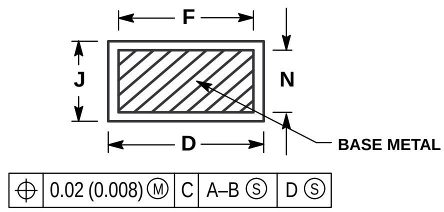
OUTLINE DIMENSIONS

FI SUFFIX
CERAMIC QFP PACKAGE
CASE 963–02
ISSUE A



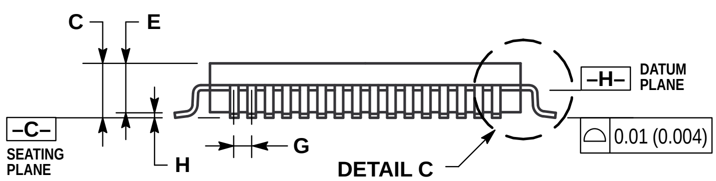


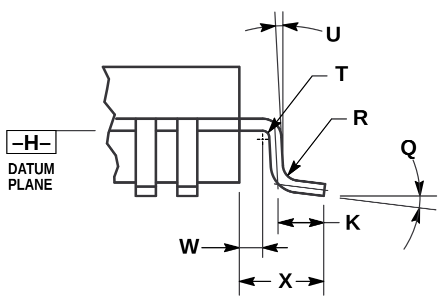
DETAIL A



VIEW ROTATED 90° CLOCKWISE

SECTION B–B





DETAIL C

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –H– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –A–, –B– AND –D– TO BE DETERMINED AT DATUM PLANE –H–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –C–.
6. DIMENSIONS A AND B DEFINE MAXIMUM CERAMIC BODY DIMENSION INCLUDING GLASS PROTRUSION AND MISMATCH BETWEEN CERAMIC BODY AND COVER.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	13.90	14.10	0.547	0.555
B	13.90	14.10	0.547	0.555
C	3.00	4.11	0.118	0.162
D	0.30	0.45	0.012	0.018
E	2.54	3.22	0.100	0.127
F	0.30	0.40	0.012	0.016
G	0.80 BSC		0.031 BSC	
H	0.45	0.89	0.018	0.035
J	0.13	0.23	0.005	0.009
K	0.65	0.95	0.026	0.037
L	12.00 REF		0.472 REF	
N	0.13	0.17	0.005	0.007
P	0.40 BSC		0.016 BSC	
Q	0°	7°	0°	7°
R	0.13	0.30	0.005	0.012
S	16.95	17.45	0.667	0.687
T	0.13	—	0.005	—
U	0°	—	0°	—
V	16.95	17.45	0.667	0.687
W	0.35	0.45	0.014	0.018
X	1.60 REF		0.063 REF	

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