CCD 134
1024-Element
Linear Image Sensor

FEATURES

- **1024 x 1 photosite array**
- **13 µm x 13 µm photosites on 13µm pitch**
- **Anti-blooming and integration control**
- **Enhanced spectral response (particularly in the blue region)**
- **Improved low-light performance over CCD133A**
- **Low dark signal**
- **High responsivity**
- **High-speed operation**
- **On-chip clock drivers**
- **Dynamic range typical: 7500:1**
- **Over 1V peak -to-peak outputs**
- **Dark and white references contained in sample- and -held outputs**
- **Special selections available —consult factory**

GENERAL DESCRIPTION

The CCD134 is a 1024-element line image sensor designed for industrial measurement, telecine, and document scanning applications which require high resolution, high sensitivity and high data rate. The incorporation of on-chip antiblooming and integration control allow the CCD134 to be extremely useful in an industrial measurement and control environment or environments where lighting conditions are difficult to control.

PIN NAME	DESCRIPTION
V_{OUT_A}	Output Amplifier A Source
ϕSH_{GA}	Sample and Hold Gate A
ϕSH_{CA}	Sample and Hold Clock A
V_{CD}	Clock Driver Drain
NC	No Connection (Do Not Ground)
V_{CG}	Clock Ground
V_{SINK}	Anti-blooming Sink
TP	Test Point
ϕIC	Integration Control Clock
V_T	Transport Register DC Electrode
V_{EI}	Electrical Input Bias
V_{SS}	Substrate Ground
V_{PG}	Photogate
ϕX	Transfer Clock
ϕT	Transport Clock
V_{BIAS}	Amplifier Bias
V_{SG}	Amplifier Signal Ground
ϕSH_{CB}	Sample and Hold Clock B
ϕSH_{GB}	Sample and Hold Gate B
V_{OUT_B}	Output Amplifier B Source
V_{DD}	Output Amplifier Drain

PIN CONNECTION DIAGRAM (TOP VIEW)

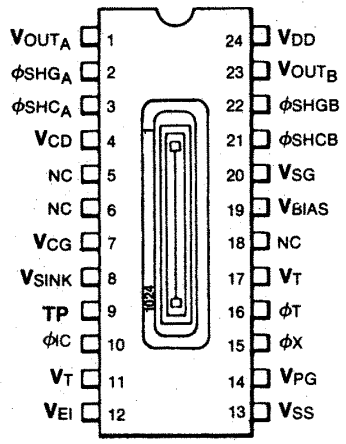

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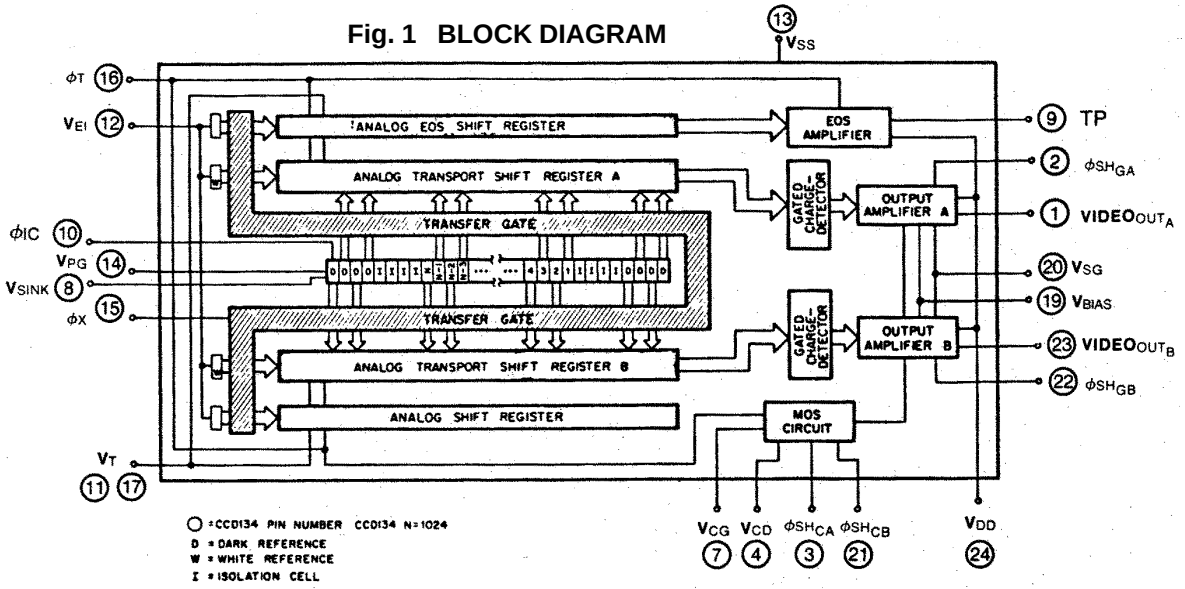
Fig. 1 BLOCK DIAGRAM



The CCD134 is similar to the CCD133A except for the additional features of anti-blooming and integration control. The CCD134 is a third generation device having an overall improved performance compared with first and second generation devices, including enhanced blue response and excellent low light level performance. The device incorporates on-chip clock driver circuitry and is capable of high-speed operation up to a 20MHz data rate. The photoelement size is 13µm (0.51 mils) x 13µm (0.51 mils) on 13µm (0.51 mils) centers. The device is manufactured using Fairchild Weston advanced charge-coupled device n-channel isoplanar buried-channel technology.

FUNCTIONAL DESCRIPTION

The CCD134 consists of the following functional elements illustrated in the Block Diagram and Circuit Diagram (Fig1.).

Photosites — A row of 1024 image sensor elements separated by a diffused channel stop and covered by a silicon dioxide surface passivation layer. Image photons pass through the transparent silicon creating hole-electron pairs. The photon generated electrons are accumulated in the photosites. The amount of charge accumulated in each photosite is a linear function of the incident illumination intensity and the integration period. The output signal will vary in an analog manner from a thermally generated background level at zero illumination to a maximum at saturation under bright illumination.

Transfer Gates — This gate is a structure adjacent to the row of image sensor elements. The charge packets accumulated in the photosites are transferred in parallel via the transfer gate to the transport shift registers whenever the transfer gate voltage goes high. Alternate charge packets are transferred to the A and B transport registers.

Four 529 Bit Analog Transport Shift Registers — Two registers are on each side of the line of image sensor elements and are separated from it by the transfer gate. The two inside registers, called the transport shift registers are used to move the light generated charge packets delivered by the transfer gates serially to the charge detector amplifier. The complementary phase relationship of the last elements of the two transport registers provides for alternate delivery of charge packets at the output amplifiers. The outer two registers serve to reduce peripheral electron noise in the inner shift registers.

Two Gated Charge Detector/Amplifiers — Charge packets are transported to a precharged capacitor whose potential changes linearly in response to the quantity of the signal charge delivered. This potential is applied to the input gate of the two-stage NMOS amplifiers producing a signal at the output "V_{out} pins. The sample-and-hold gate is a switching MOS transistor in the output amplifier that allows the output to be delivered as a sample-and held waveform. The diode is recharged internally before the arrival of each new signal charge-packet from the transport shift register.

Integration and Anti-Blooming Control — In many applications the dynamic range in parts of the image is larger than the dynamic range of the CCD, which may cause more electrons to be generated in the photosite area than can be stored in the CCD shift register. This is particularly common in industrial inspection and satellite applications. The excess electrons generated by bright illumination tend to "bloom" or "spill over" to neighboring pixels along the shift register, thus "smearing" the information. This smearing can be eliminated using two methods:

Anti-Blooming Operation:

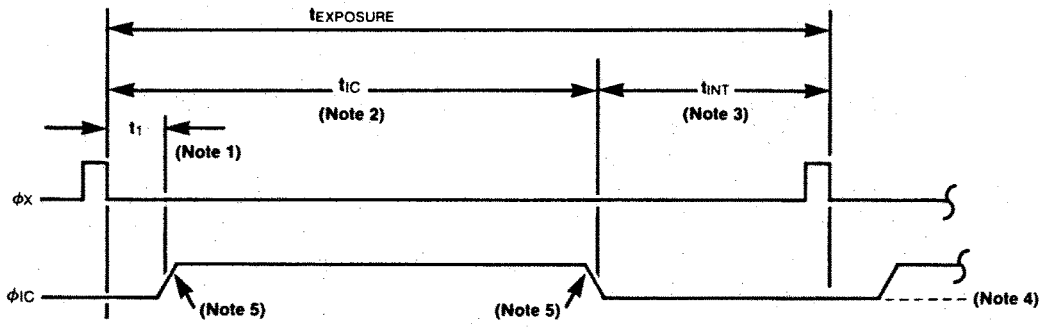
A DC voltage applied to the integration control gate (approximately 5 to 7 volts) will cause excess charge generated in the photosites to be diverted to the anti-blooming sink (V_{SINK}) instead of the shift registers. This acts as a "clipping circuit" for the CCD output (see Fig. 2)

Integration Control Operation:

Variable integration times which are less than the CCD exposure time may be attained by supplying a clock to the integration control gate. Clocking ϕ_{IC} reduces the photosite signal in all photosites by the ration $t_{EXPOSURE}/t_{INT}$. Greater than 10:1 reduction in the average photosite signal can be achieved with integration control.

The integration-control and anti-blooming features can be implemented simultaneously. This is done by setting the ϕ_{IC} clock-low level to approximately 5 to 7 volts.

Fig. 2 INTEGRATION-CONTROL TIMING DIAGRAM AND NOTES



NOTES:

1. $t_1 > (t_{fall}$ of $\phi X)$.
2. All charge generated in photosites during t_{IC} is dumped in V_{SINK}.
3. All charge generated in photosites < Q_{SAT} during t_{INT} is transferred into the shift registers during ϕx clock-high period. Photosite charge > Q_{SAT} (shift reg.) generated during t_{INT} goes into V_{SINK} if anti-blooming voltage is optimized.
4. ϕ_{IC} clock-low ≈ 5 to 7 volts will give best anti-blooming operation.
5. ϕ_{IC} t_{rise} & $t_{fall} > 4\mu s$ to minimize clock coupling of ϕ_{IC} into V_{OUT}.
6. To eliminate integration control, but retain anti-blooming $\phi_{IC} \approx +5$ VDC.
7. To eliminate both integration control and anti-blooming, ϕ_{IC} = 0VDC or $V_{SS}(-2V)$.
8. To use integration control without anti-blooming, use ϕ_{IC} clock-low = 0.0 to 0.7 volts and ϕ_{IC} clock-high = same range as ϕ_T clock-high voltage.

Fig. 3 TEST LOAD CONFIGURATION (INTERNAL SAMPLE-AND-HOLD ENABLED)

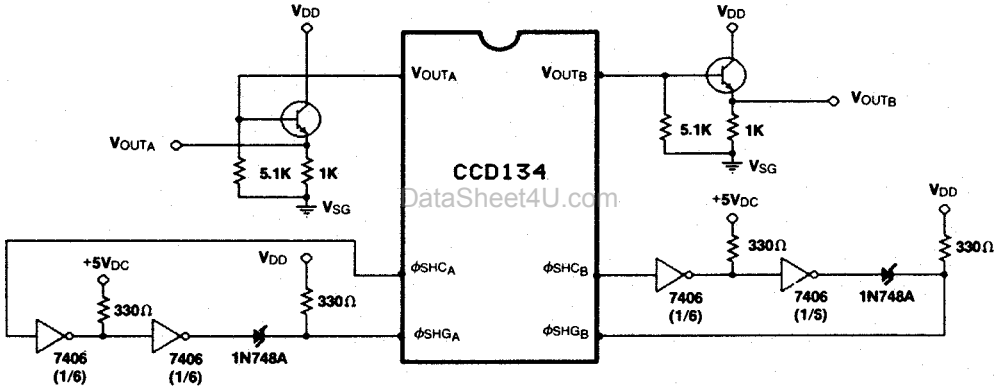


Fig. 4 TEST LOAD CONFIGURATION (INTERNAL SAMPLE-AND-HOLD DISABLED)

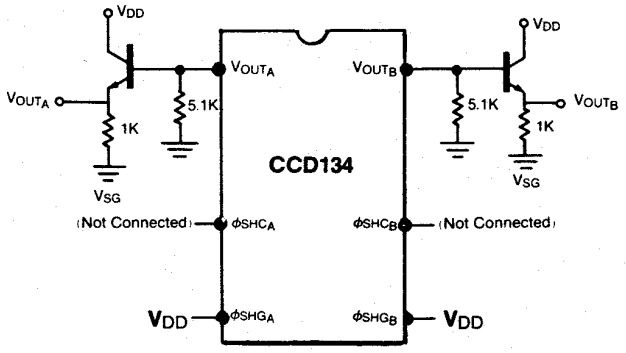
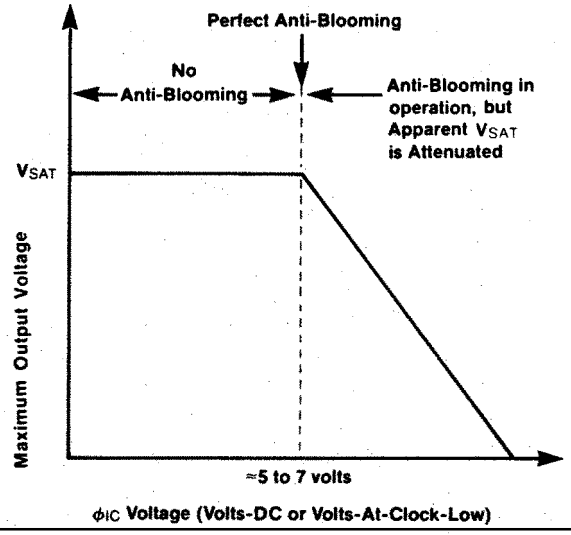


Fig. 5 MAXIMUM OUTPUT VOLTAGE vs. ϕ_{IC} VOLTAGE



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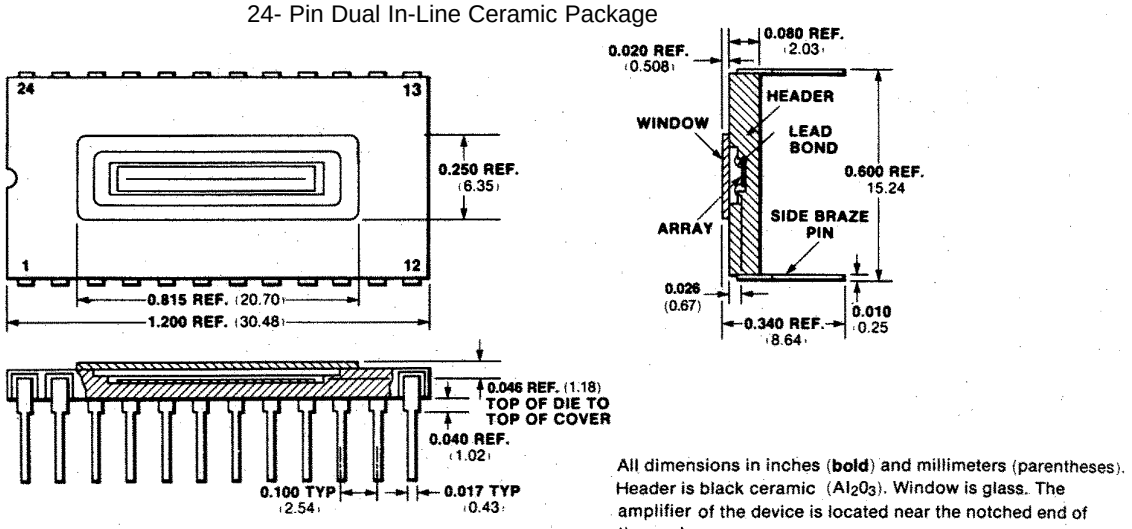
PACKAGE OUTLINE

24- Pin Dual In-Line Ceramic Package



All dimensions in inches (**bold**) and millimeters (parentheses). Header is black ceramic (Al_2O_3). Window is glass. The amplifier of the device is located near the notched end of the package.

DEFINITION OF TERM

Charge-Coupled Device — A Charge-coupled device is a semiconductor device in which finite isolated charge-packets are transported from one position in the semiconductor to an adjacent position by sequential clocking of an array of gates. The charge-packets are minority carriers with respect to the semiconductor substrate.

Sample-and Hold Clock (ϕSHCA, ϕSHCB) - The voltage wave form for triggering the sample-and-hold gates in the output amplifiers to create a continuous sampled video signal at the output. The sample-and-hold feature may be defeated by connecting ϕSHCA and ϕSHCB to V_{DD}. Use of the internal sample-and-hold capability is possible for data rates upt to 13MHz. For use above 13MHz consult factory.

Dark Reference — Video output level generated from sensing elements covered with opague metalization which provides a reference voltage equivalent to device operation in the dark. This permits use of external DC restoration circuitry.

Isolation Cell — This is a site on-chip producing an element in the video output that serves as a buffer between valid video data and dark reference signals. The output from an isolation cell contains no valid information and should be ignored.

Dynamic Range — The saturation exposure divided by the RMS temporal noise equivalent exposure., Dynamic range is sometimes defined in terms of peak-to-peak noise. To compare the two definitions a factor of four to six is generally appropriate in that peak-to-peak noise is approximately equal to four to six times RMS noise.

RMS Noise Equivalent Exposure — The exposure level that gives an output signal equal to the RMS noise level at the output in the dark.

Saturation Exposures — The minimum exposure level that will provide a saturation output signal. Exposure is equal to the light intensity times the photosite integration time.

Charge Transfer Efficiency — Percentage of valid charge information that is transferred between each successive stage of the transport registers.

Responsivity — The output signal voltage per unit exposure for a specified spectral type of radiation. Responsivity equals output voltage divided by exposure.

Total Photoresponse Non-Uniformity - The difference of the response levels of the most and the least sensitive element under uniform illumination. Measurement of PRNU excludes first and last elements.

Dark Signal - The output signal in the dark caused by thermally generated electrons that is a linear function of the integration time and is highly sensitive to temperature.

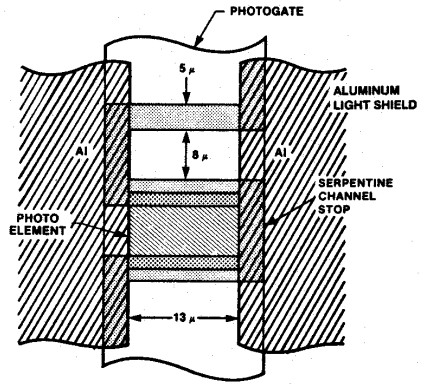
Saturation Output Voltage - The maximum usable signal output voltage. Charge transfer efficiency decreases sharply when the saturation output voltage is exceeded.

Integration Time - The time interval between the falling edge of the integration control clock and the falling edge of the transfer clock. The integration time is the time in which charge is accumulated in the photosites.

Exposure Time - The time interval between the falling edge of the two transfer pulses (ϕX) as shown in the timing diagram. The exposure time is the time between transfers of signal charge from the photosites into the transport registers.

Pixel - A picture element (photosite).

PHOTOELEMENT DIMENSIONS



All dimensions are typical values.

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ABSOLUTE MAXIMUM RATINGS (above which useful life may be impaired)

Storage Temperature	-25° C to +125° C
Operating Temperature	-25° C to +70° C
CCD 134: Pins 2, 3, 4, 7, 8, 9, 10, 11, 12, 14, 15, 16, 17, 19, 21, 22, 24	-0.3V to 18V
Pin 20	0.0V to +0.7V
Pin 13	-3.0V to 0V
Pins 5, 6, 18	NC
Pins 1, 23	SEE CAUTION NOTE

CAUTION NOTE:
These devices have limited built-in gate protection. It is recommended that static discharge be controlled and minimized. Care must be taken to avoid shorting pins $VIDEO_{OUT_{A+B}}$ to V_{SS}, V_{SG}, V_{CG} or V_{DD} during operation of the devices. Shorting these pins temporarily to V_{SS}, V_{SG}, V_{CG} or V_{DD} may destroy the output amplifiers.

DC CHARACTERISTICS: T_P = 25°C (Note 1, 2) Use typical values for optimum performance

SYMBOL	CHARACTERISTIC	RANGE			UNIT	CONDITION
		MIN	TYP	MAX		
V_{CD}	Clock Driver Drain Supply Voltages	13.5	14.0	14.5	V	
V_{DD}	Output Amplifier Drain Supply Voltage	13.5	14.0	14.5	V	
V_{SINK}	Anti-Blooming Sink Voltage	13.5	14.0	14.5	V	
V_{BIAS}	Amplifier Bias Voltage	3.0	3.5	4.0	V	
V_{PG}	Photogate Bias Voltage	5.5	6.0	6.5	V	
V_T	Shift Register DC Electrode Bias Voltages	5.5	6.0	6.5	V	Note 3
V_{EI}	Electrical Input Bias Voltage		10.5		V	Note 4
V_{CG}	Clock Ground	0.0	0.3	0.7	V	
V_{SG}	Amplifier Signal Ground	0.0	0.3	0.7	V	
V_{SS}	Substrate Ground	-3.0	-2.0	-1.0	V	Note 5
I_{CD}	Clock Driver Supply Current	0.0	7.0	15.0	mA	
I_{DD}	Output Amplifier Drain Supply Current		15.0	25.0	mA	

CLOCK CHARACTERISTICS: T_P = 25°C (Note 1) Use typical values for optimum performance

SYMBOL	CHARACTERISTIC	LIMITS			UNIT	CONDITION
		MIN	TYP	MAX		
$V_{\phi X\ HIGH}$	Transfer Clock HIGH	11.0	11.5	12.0	V	Note 6
$V_{\phi T\ HIGH}$	Transport Clock HIGH	11.0	11.5	12.0	V	Note 6
$V_{\phi IC\ HIGH}$	Integration Control Clock HIGH	11.0	11.5	12.0	V	Note 6
$V_{\phi X\ LOW}$	Transfer Clock LOW	0.0	0.3	0.7	V	Notes 5, 6
$V_{\phi T\ LOW}$	Transport Clock LOW	0.0	0.3	0.7	V	Notes 5, 6
$V_{\phi IC\ LOW}$	Integration Control Clock LOW		6.0		V	Note 15
f_{data} max	Maximum Output Data Rate	12.0	20.0		MHz	Notes 7, 8

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AC CHARACTERISTICS: T_P = 25°C, (Note 1), f_{data} = 5.0MHz, t_{int} = 1.0ms, Light Source = 2854°K + 2.0mm thick Schott BG-38 and OCLI WBHM Filters (Note 9), internal sample-and-hold enabled.

SYMBOL	CHARACTERISTIC	RANGE			UNIT	CONDITION
		MIN	TYP	MAX		
DR	Dynamic Range					
	(relative to peak-to-peak noise)		1500:1			
	(relative to rms noise)		7500:1			
NEE	RMS Noise					
	Equivalent Exposure		44×10^{-6}		$\mu J/cm^2$	
SE	Saturation Exposure		0.33		$\mu J/cm^2$	
CTE	Charge Transfer Efficiency	.99995	.99999			Note 10
V_O	Output DC Level		6.0			
Z	Output Impedance		0.75	3	K Ω	
P	On-Chip Power Dissipation:					
	Clock Drivers		100		mW	
	Amplifiers		200		mW	
N	Peak-to-Peak Temporal Noise		1		mV	

PERFORMANCE CHARACTERISTICS: T_P = 25°C, (Note 1), f_{data} = 5.0MHz, t_{int} = 1.0ms, Light Source = 2854°K + 2.0mm thick Schott BG-38 and OCLI WBHM Filters (Note 9), internal sample-and-hold enabled.

SYMBOL	CHARACTERISTIC	RANGE			UNIT	CONDITION
		MIN	TYP	MAX		
PRNU*	Photoresponse Non-uniformity					
	Peak-to-Peak		60	160	mV	
	Peak-to-Peak without single pixel and Positive and Negative Pulses		40		mV	
	Single-pixel Positive Pulses		10		mV	
	Single-pixel Negative Pulses		20		mV	
M Video	Video Mismatch		40	160	mV	Note 11
M DC	DC Mismatch		0.5	2.0	V	Note 12
DS	Dark Signal:					Notes 13, 14
	DC Component		1	2	mV	
	Low Frequency Component		1	2	mV	
SPDSNU	Single Pixel DS Non-Uniformity		1	2	mV	Note 14
R	Responsivity		4.5		$V/\mu J/cm^2$	
V_{SAT}	Saturation Output Voltage	1.0	1.5	3.0	V	

NOTES:

* All PRNU measurements taken at an 800 mvolt output level using an f/5.0 lens and exclude the outputs from the first and last elements of the array. The "f" number is defined as the distance from the lens to the array divided by the diameter of the lens aperture. As the "f" number increases, the resulting more highly collimated light causes the package window imperfections to dominate and increase PRNU. A lower "f" number results in less collimated light causing device photosite blemishes to dominate the PRNU.

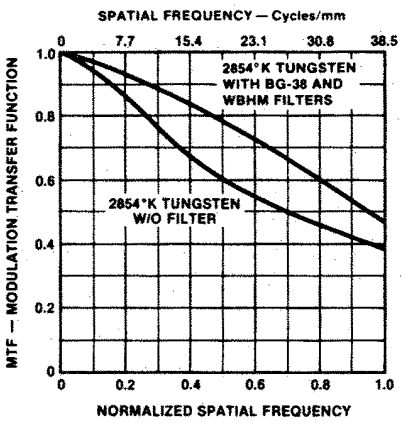
NOTES:

1. T_P is defined as the package temperature measured on a copper block in good thermal contact with the entire backside of the package.
2. NC pins must be left unconnected.
3. V_T = 0.55 ϕX_{HIGH} = 0.55 ϕT_{HIGH}
4. V_{EI} is used to generate the white reference outputs. These two signals can be reduced by connecting V_{EI} to V_{DD}.
5. Negative transients on any clock pin going below 0.0 volts may cause charge injection, which results in an increase in apparent DS. Adjusting V_{SS} to a more negative voltage than the clock low voltages will reduce charge injection, if present.
6. Pin Capacitances:
   C ϕT = 300 pF; C ϕX = 80 pF.
7. The minimum clock frequency is limited by increases in dark signal.
8. f_{data} = 2 (f ϕT)
9. OCLI WBHM = Optical Coating Laboratory, Inc. Wide Band Hot Mirror.
10. CTE is the measurement for a one-stage transfer.

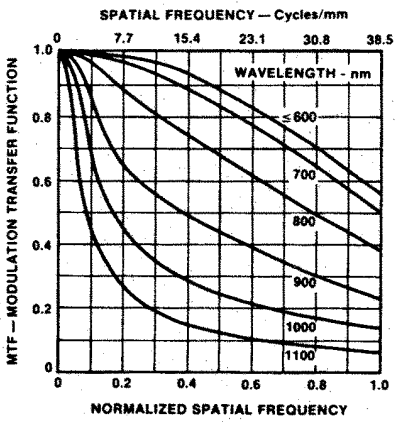
11. Video mismatch is the difference in AC amplitudes between V_{OUT_A} and V_{OUT_B} under uniform illumination. It can be eliminated by attenuation/amplification of one of the video outputs.
12. DC mismatch is the difference in DC output level V_O between V_{OUT_A} and V_{OUT_B}.
13. Dark signal component approximately doubles for every 5-10 °C in T_P.
14. Each SPDSNU is measured from the DS level adjacent to the base of the SPDSNU. The SPDSNU approximately doubles for every 5-15 °C increase in T_P.
15. See definitions of Anti-Blooming Control and Integration Control.

TYPICAL PERFORMANCE CURVES

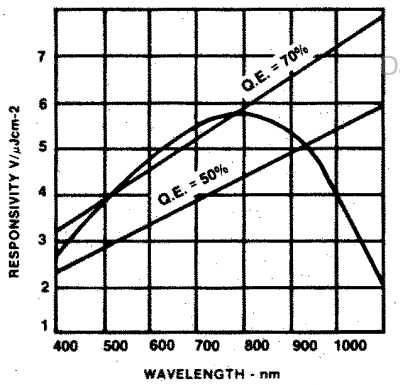
MODULATION TRANSFER FUNCTIONS FOR TWO BROADBAND ILLUMINATION SOURCES



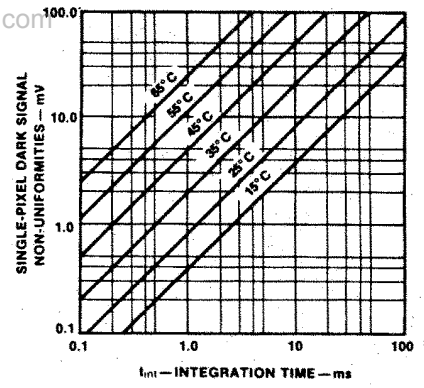
MODULATION TRANSFER FUNCTIONS FOR NARROW BAND ILLUMINATION SOURCES



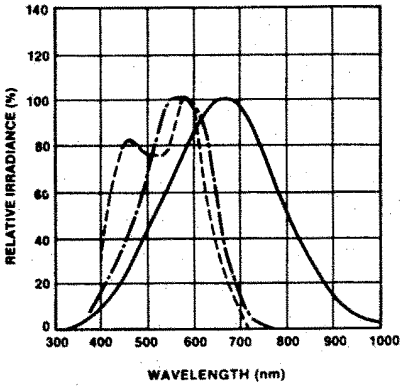
TYPICAL SPECTRAL RESPONSE



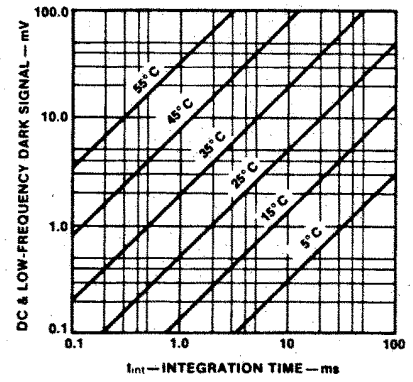
SINGLE-PIXEL DARK SIGNAL NON-UNIFORMITIES VERSUS INTEGRATION TIME



*RELATIVE RADIANT FLUX VS WAVELENGTH



DC AND LOW-FREQUENCY DARK SIGNAL VS INTEGRATION TIME



TYPICAL "DAYLIGHT FLUORESCENT" BULB
2854° K LIGHT SOURCE +WBHM + 2.0 mm THICK BG-38
2854° K LIGHT SOURCE + 3.0 mm THICK 1-75

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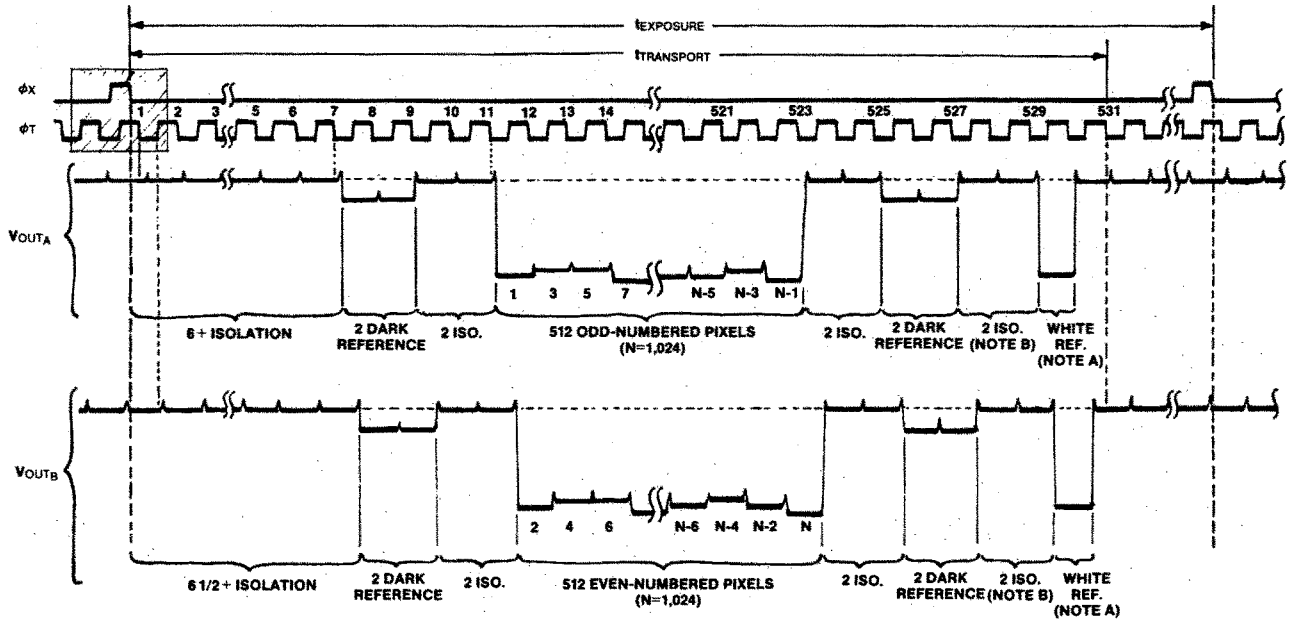
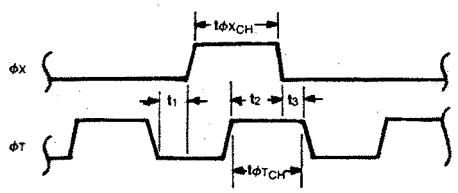
TIMING DIAGRAM (Internal Sample & Hold Enabled, See Fig. 5)



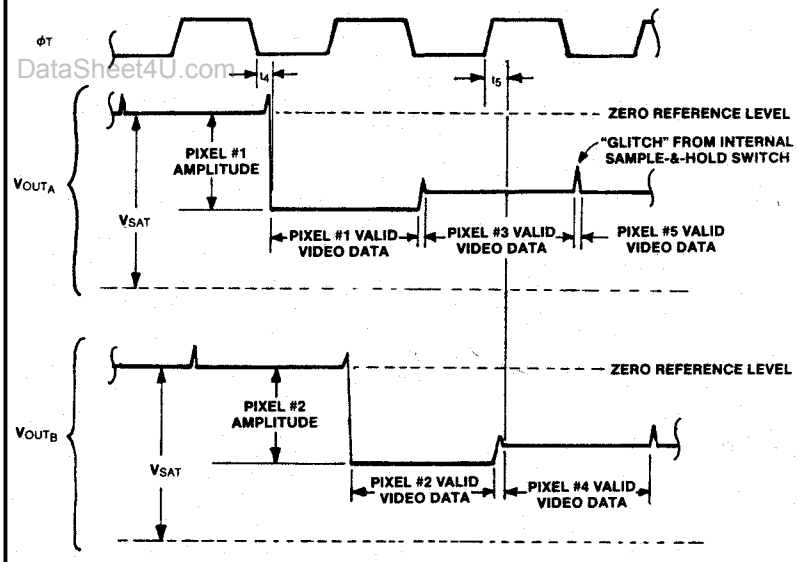
TIMING DETAILS BETWEEN φX AND φT:



TIMING REQUIREMENTS FOR φX AND φT:

$t_{\phi X_{CH}}$ > 60 ns MINIMUM; 500-1000 ns PREFERRED.
$t_{\phi T_{CH}}$ > 50 ns. 50% DUTY CYCLE PREFERRED.
t_1, t_3 > 10 ns
t_2 > 30 ns
t_{RISE}, t_{FALL} ≥ 10 ns MINIMUM. (> 20 ns PREFERRED) FOR BOTH φX AND φT.

TIMING DETAILS BETWEEN φT and VOUTA and VOUTB (NEAR PIXEL #1)



GENERAL NOTES:

1. White reference cell output signals will be approximately equal in height. This output can be reduced by connecting V_{EI} to V_{DD}.
2. The isolation cells may contain output signals as part of their buffer function. These signals should be disregarded.
3. Integration control clock (ϕ_{IC}) omitted for clarity. Refer to "Integration control clock timing diagram" (Figure 3) for details.

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