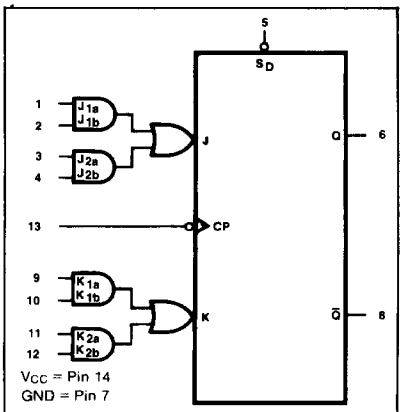
54H/74H71

DESCRIPTION

The "71" is a positive pulse triggered master slave flip-flop with AND-OR gated JK inputs and direct Set ($\overline{S}_D$) input. JK information is loaded into the master while the Clock is HIGH and transferred to the slave on the HIGH-to-LOW Clock transition. The J and K inputs should be stable while the Clock is HIGH for conventional operation. J or K input transitions from HIGH-to-LOW should be avoided while the Clock is HIGH due to "One's catching" feature of this flip-flop.

The Set ($\overline{S}_D$) is an asynchronous active LOW input. When LOW, the $\overline{S}_D$ overrides the Clock and data inputs forcing the Q output HIGH and the $\overline{Q}$ output LOW.

LOGIC SYMBOL



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	PIN CONF.	COMMERCIAL RANGES V_{CC} = 5V ± 5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ± 10%
Plastic DIP	Fig A	N74H71N	
Ceramic DIP	Fig A	N74H71F	S54H71F
Flatpak	Fig B		S54H71W

PIN CONFIGURATIONS

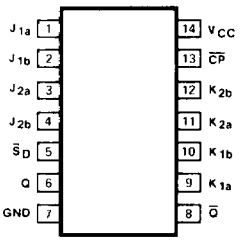


Figure A

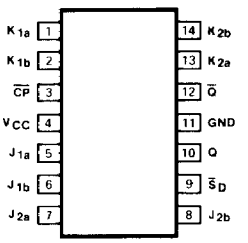


Figure B

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE [a]

PINS			54/74	54H/74H	54S/74S	54LS/74LS
$\overline{CP}$	Clock input	I_{IH} (μA) I_{IL} (mA)		100 -4.0		
$\overline{S}_D$	Set input	I_{IH} (μA) I_{IL} (mA)		150 -6.0		
JK	Data inputs	I_{IH} (μA) I_{IL} (mA)		50 -2.0		
Q & $\overline{Q}$ Outputs		I_{OH} (μA) I_{OL} (mA)		-500 20		

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE [b]

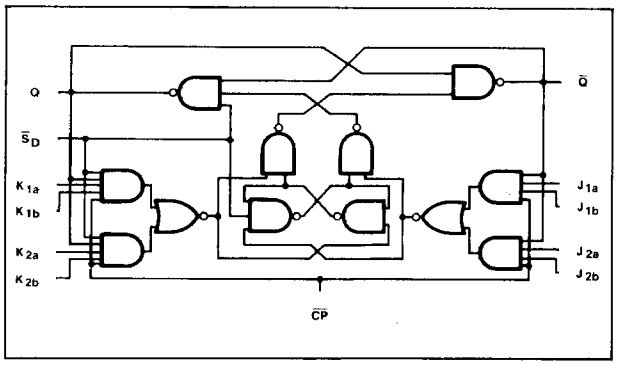
PARAMETER		TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
			Min	Max	Min	Max	Min	Max	Min	Max	
I_{CC}	Supply current	V_{CC} = Max, V_{CP} = 0V				30					mA

NOTES

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H and see inside back cover for 54S/74S and 54LS/74LS specification.

LOGIC DIAGRAM



MODE SELECT—TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	$\overline{S}_D$	$\overline{CP}$	J	K	Q	$\overline{Q}$
Asynchronous Set	L	X	X	X	H	L
Toggle	H	⎍	h	h	$\overline{q}$	q
Load "1" (Set)	H	⎍	h	l	H	L
Hold "no change"	H	⎍	l	l	q	$\overline{q}$

H = HIGH voltage level steady state.
L = LOW voltage level steady state.
h = HIGH voltage level prior to LOW-to-HIGH Clock transition. (c)
l = LOW voltage level prior to LOW-to-HIGH Clock transition. (c)
X = Don't care.
q = Lower case letters indicate the state of the referenced output prior to the HIGH to LOW Clock transition.
⎍ = Positive Clock pulse.

AC CHARACTERISTICS T_A = 25°C (See Section 4 for Waveforms and Conditions)

PARAMETER		TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
					C_L = 25pF, R_L = 280Ω						
			Min	Max	Min	Max	Min	Max	Min	Max	
f_{MAX}	Maximum Clock frequency	Waveform 4			25						MHz
t_{PLH} t_{PHL}	Propagation delay Clock to Output	Waveform 4				21 27					ns ns
t_{PLH} t_{PHL}	Propagation delay Set to Output	Waveform 5				13 24					ns ns

AC SETUP REQUIREMENTS T_A = 25°C (See Section 4 for Waveforms and Conditions)

PARAMETER		TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
			Min	Max	Min	Max	Min	Max	Min	Max	
$t_{W(H)}$	Clock pulse width (HIGH)	Waveform 4			12						ns
$t_{W(L)}$	Clock pulse width (LOW)	Waveform 4			28						ns
$t_{W(L)}$	Set pulse width (LOW)	Waveform 5			16						ns
t_s	Setup time J or K to Clock	Waveform 4			(c)						ns
t_h	Hold time J or K to Clock	Waveform 4			0						ns

NOTE

c. The J and K inputs must be stable while the Clock is HIGH for conventional operation.