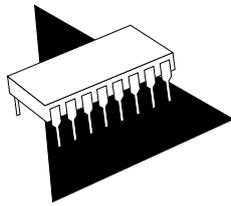


Revision History

- First Edition: March 1999

- Second Edition: February 2000

- Library name change STD111
- All characteristic values are updated with mass product line characteristics.
- Add high density compiled memories to second edition. (chapter 5)
- The name of previous compiled memories are changed for example: spsram into spsram_lp
- power equations are changed. (chapter 1)
- Updated PLL information
- Updated wire-load model



STD111

**0.25 μ m 2.5V CMOS Standard Cell Library
for Pure Logic Products**

STD111
0.25 μ m 2.5V CMOS Standard Cell Library
for Pure Logic Products
Data Book

© 1999-2000 Samsung Electronics Co., Ltd.

All rights reserved. No part of this document may be reproduced, in any form or by any means, without the prior written consent of the publisher. Samsung assumes no responsibility for any errors resulting from the use of the information contained herein, nor does it convey any license under the patent rights of Samsung or others. Samsung reserves the right to make changes in its products or product specification to improve function or design at any time, without notice.

SEC and STD111 are trademarks of Samsung Electronics Co., Ltd. Verilog is a registered trademark of Cadence Design Systems, Inc. Viewlogic is a registered trademark of Viewlogic Systems, Inc. Mentor is a registered trademark of Mentor Graphics Co. Synopsys is a registered trademark of Synopsys, Inc.

Head Office

Samsung Electronics Co., Ltd
System LSI Business,
ASIC Division, SOC Design Technology
San #24, Nongseo-Ri,
Kiheung-Eup, Yongin-City,
Kyunggi-Do, Korea

TEL 82-2-760-6500, 6501 (Hot Line)
FAX 82-331-209-4920
<http://www.intl.samsungsemi.com>

Marketing Team

Samsung Electronics Co., Ltd
System LSI Business,
ASIC Division,
ASIC Marketing Team
San #24, Nongseo-Ri,
Kiheung-Eup, Yongin-City,
Kyunggi-Do, Korea

TEL 82-2-331-209-1930
FAX 82-2-331-209-1919

Introduction

This databook contains information about STD111 0.25 μ m 2.5V standard cell library for pure Logic products developed by SEC (Samsung Electronics Corporation).

The “library” basically contains various kinds of internal and I/O cells and soft-macros which are used for developing ASIC (Application Specific Integrated Circuit). It also includes a design kit helping designers to work in a workstation platform, and all sorts of design environments needed for an automatic chip design.

There are seven chapters in this databook:

Chapter 1	Introduction
Chapter 2	Electrical Characteristics
Chapter 3	Internal Macrocells
Chapter 4	Input/Output Cells
Chapter 5	Compiled Macrocells
Chapter 6	PLL

In this databook each cell is followed by its AC electrical characteristics, and these characteristic values are almost equal when the corresponding cell is operated in a real chip.

The purpose of this databook is to prevent any misuse or misapplication of STD111 cell library by providing precise information about the cell list, electrical data, directions for use, and matters demanding special attention.

If you want to get more information about Digital cores and Analog cores that are not included in this databook, access the Samsung ASIC web site(<http://www.intl.samsungsemi.com>) or contact Head Office.

Contents

1 Introduction

1.1 Library Description	1-1
1.2 Features	1-2
1.3 EDA Support	1-4
1.4 Product Family	1-4
1.4.1 Analog Core Cell	1-4
1.4.2 Internal Macrocells	1-12
1.4.3 Compiled Macrocells	1-12
1.4.4 Input/Output Cells	1-14
1.5 Timings	1-16
1.6 Delay Model	1-22
1.7 Testability Design Methodology	1-24
1.8 Maximum Fanouts	1-27
1.9 Packages Capability by Lead Count	1-34
1.10 Power Dissipation	1-36
1.11 V_{DD}/V_{SS} Rules and Guidelines	1-39
1.12 Crystal Oscillator Considerations	1-45

2 Electrical Characteristics

DC Electrical Characteristics	2-1
-------------------------------------	-----

3 Internal Macrocells

Overview	3-1
Summary Tables	3-2
Logic Cells	
AD2DH/AD2/AD2D2/AD2D4	3-17
AD3DH/AD3/AD3D2/AD3D4	3-19
AD4DH/AD4/AD4D2/AD4D4	3-21
AD5/AD5D2/AD5D4	3-24
ND2DH/ND2/ND2D2/ND2D4	3-27
ND3DH/ND3/ND3D2/ND3D4	3-29
ND4DH/ND4/ND4D2/ND4D2B/ND4D4	3-32
ND5/ND5D2/ND5D4	3-35
ND6/ND6D2/ND6D4	3-38

Contents

ND8/ND8D2/ND8D4	3-42
NR2DH/NR2/NR2D2/NR2D2B/NR2D4/NR2A	3-46
NR3DH/NR3/NR3D2/NR3D2B/NR3D4/NR3A	3-49
NR4DH/NR4/NR4D2/NR4D2B/NR4D4	3-53
NR5/NR5D2/NR5D4	3-56
NR6/NR6D2/NR6D4	3-60
NR8/NR8D2/NR8D4	3-64
OR2DH/OR2/OR2D2/OR2D4	3-68
OR3DH/OR3/OR3D3/OR3D4	3-70
OR4DH/OR4/OR4D2/OR4D4	3-73
OR5/OR5D2/OR5D4	3-76
XN2/XN2D2/XN2D4	3-80
XN3/XN3D2/XN3D4	3-82
XO2/XO2D2/XO2D4	3-84
XO3/XO3D2/XO3D4	3-86
AO21DH/AO21/AO21D2/AO21D2B/AO21D4	3-88
AO211DH/AO211/AO211D2/AO211D2B/AO211D4	3-91
AO2111/AO2111D2	3-94
AO22DH/AO22/AO22D2/AO22D2B/AO22D4	3-97
AO22DHA/AO22A/AO22D2A/AO22D4A	3-100
AO221/AO221D2/AO221D4	3-103
AO222/AO222D2/AO222D2B/AO222D4	3-107
AO222A/AO222D2A/AO222D4A	3-112
AO2222/AO2222D2/AO2222D4	3-114
AO31DH/AO31/AO31D2/AO31D4	3-118
AO311/AO311D2/AO311D4	3-121
AO3111/AO3111D2	3-125
AO32/AO32D2/AO32D4	3-128
AO321/AO321D2/AO321D4	3-132
AO322/AO322D2/AO322D4	3-136
AO33/AO33D2/AO33D4	3-140
AO331/AO331D2/AO331D4	3-144
AO332/AO332D2/AO332D4	3-148
AO4111/AO4111D2	3-152
OA21DH/OA21/OA21D2/OA21D2B/OA21D4	3-155
OA211DH/OA211/OA211D2/OA211D2B/OA211D4	3-158
OA2111/OA2111D2	3-161
OA22DH/OA22/OA22D2/OA22D2B/OA22D4	3-164
OA22DHA/OA22A/OA22D2A/OA22D4A	3-167
OA221/OA221D2/OA221D4	3-170
OA222/OA222D2/OA222D2B/OA222D4	3-174
OA2222/OA2222D2/OA2222D4	3-179
OA31/OA31D2/OA31D4	3-183

OA311/OA311D2/OA311D4.....	3-186
OA3111/OA3111D2	3-190
OA32/OA32D2/OA32D4.....	3-193
OA321/OA321D2/OA321D.....	3-197
OA322/OA322D2/OA322D4.....	3-201
OA33/OA33D2/OA33D4.....	3-205
OA331/OA331D2/OA331D4.....	3-209
OA332/OA332D2/OA332D4.....	3-213
OA4111/OA4111D2	3-217
SCG1/SCG1D2	3-220
SCG2//SCG2D2	3-223
SCG3/SCG3D2	3-225
SCG4/SCG4D2	3-228
SCG5/SCG5D2	3-231
SCG6/SCG6D2	3-234
SCG7/SCG7D2	3-236
SCG8/SCG8D2	3-239
SCG9/SCG9D2	3-241
SCG10/SCG10D2	3-243
SCG11/SCG11D2	3-246
SCG12/SCG12D2	3-248
SCG13/SCG13D2	3-250
SCG14/SCG14D2	3-252
SCG15/SCG15D2	3-254
SCG16/SCG16D2	3-256
SCG17/SCG17D2	3-258
SCG18/SCG18D2	3-260
SCG19/SCG19D2	3-263
SCG20/SCG20D2	3-265
SCG21/SCG21D2	3-267
SCG22/SCG22D2	3-269
DL1D2/DL1D4	3-271
DL2D2/DL2D4	3-272
DL3D2/DL3D4	3-273
DL4D2/DL4D4	3-274
DL5D2/DL5D4	3-275
DL10D2/DL10D4	3-276
IVDH/IV/IVD2/IVD3/IVD4/IVD6/IVD8/IVD16	3-277
IVCD(11/13)/IVCD(22/26)/IVCD44.....	3-280
IVT/IVTD2/IVTD4/IVTD8/IVTD16	3-282
IVTN/IVTND2/IVTND4/IVTND8/IVTND16	3-284
NIDH/NID/NID2/NID3/NID4/NID6/NID8/NID16	3-286
OAK_NID10P/OAK_NID20P	3-289

Contents

NIT/NITD2/NITD4/NITD8/NITD16	3-290
NITN/NITND2/NITND4/NITND8/NITND16	3-293
OAK_DUCLK10/OAK_DUCLK16	3-296
CTSB/CTSBD2/CTSBD3/CTSBD4/CTSBD6/CTSBD8/CTSBD16.....	3-298
Flip-Flops	
FD1/FD1D2	3-303
FD1CS/FD1CSD2	3-305
FD1S/FD1SD2	3-307
FD1SQ/FD1SQD2.....	3-309
FD1Q/FD1QD2	3-311
FD2/FD2D2	3-313
FD2CS/FD2CSD2	3-315
FD2S/FD2SD2	3-319
FD2SQ/FD2SQD2.....	3-321
FD2Q/FD2QD2	3-323
FD3/FD3D2	3-325
FD3CS/FD3CSD2	3-327
FD3S/FD3SD2	3-331
FD3SQ/FD3SQD2.....	3-333
FD3Q/FD3QD2	3-335
FD4/FD4D2	3-337
FD4CS/FD4CSD2	3-340
FD4S/FD4SD2	3-344
FD4SQ/FD4SQD2.....	3-348
FD4Q/FD4QD2	3-351
FD5/FD5D2	3-353
FD5S/FD5SD2	3-355
FD6/FD6D2	3-357
FD6S/FD6SD2	3-359
FD7/FD7D2	3-361
FD7S/FD7SD2	3-363
FD8/FD8D2	3-365
FD8S/FD8SD2	3-368
FDS2/FDS2D2	3-372
FDS2CS/FDS2CSD2	3-374
FDS2S/FDS2SD2	3-376
FDS3/FDS3D2	3-378
FDS3CS/FDS3CSD2	3-380
FDS3S/FDS3SD2	3-382
FJ1/FJ1D2.....	3-384
FJ1S/FJ1SD2.....	3-386
FJ2/FJ2D2.....	3-388

FJ2S/FJ2SD2	3-390
FJ4/FJ4D2	3-392
FJ4S/FJ4SD2	3-395
FT2/FT2D2	3-398
Latches	
LD1/LD1D2	3-402
LD1A/LD1D2A	3-404
LD1Q/LD1QD2	3-406
LD2/LD2D2	3-408
LD2Q/LD2QD2	3-411
LD3/LD3D2	3-413
LD4/LD4D2	3-416
LD5/LD5D2	3-419
LD5Q/LD5QD2	3-421
LD6/LD6D2	3-423
LD6Q/LD6QD2	3-426
LD7/LD7D2	3-428
LD8/LD8D2	3-431
OAK_LDI2/OAK_LDI2D2	3-434
OAK_LDI3/OAK_LDI3D2	3-437
LS0/LS0D2	3-442
LS1/LS1D2	3-444
Bus Holder	
BUSHOLDER	3-448
Internal Clock Drivers	
CK(2/4/6/8)	3-449
Decoders	
DC4	3-452
DC4I	3-454
DC8I	3-456
Adders	
FADH/FA/FAD2	3-461
HADH/HA/HAD2	3-464
SCG23/SCG23D2	3-467
Multiplexers	
MX2DH/MX2/MX2D2/MX2D4	3-471
MX2X4	3-474
MX2IDH/MX2I/MX2ID2/MX2ID4	3-477
MX2IDHA/MX2IA/MX2ID2A/MX2ID4A	3-480

MX2IX4	3-483
MX3I/MX3ID2/MX3ID4	3-486
MX4/MX4D2/MX4D4	3-490
MX8/MX8D2/MX8D4	3-494

4 Input/Output Cells

Overview	4-1
Summary Tables	4-2

Input Buffers

PvIC/PvICD/PvICU	4-8
PvIS/PvISD/PvISU	4-12
PvIT/PvITD/PvITU	4-16

Output Buffers

PvOByz	4-20
PvODyz	4-29
PvOTyz	4-39

Bi-Directional Buffers

PvBaDyz/PvBaUDyz	4-59
PvBaTyz/PvBaDTyz/PvBaUTyz	4-59

Input Clock Drivers

PSCKDCaby	4-61
PSCKDSaby	4-65

Oscillators

PHSOSC(K1/K2/M1/M2/M3)	4-70
PHSOSC(K17/K27/M16/M26/M36)	4-76
PSOSC(K1/K2/M1/M2)	4-82

PCI Buffers

PTIPCI	4-89
PTOPCI	4-90
PTBPCI	4-91

USB I/O Buffers

PBUSB/PBUSB1/PBUSB_LS/PBUSB_FS	4-94
--------------------------------------	------

Power Pads

VDD2(I/P/O/IP/OP/T/R)/VDD3(P/O/OP)	4-103
VSS2(I/P/O/IP/OP/T/R)/VSS3(P/O/OP)	4-103

Analog Interface

PIC_ABB	4-105
PICC_ABB	4-105
PICEN_ABB	4-105
POT1/2/3/4_ABB	4-108

Voltage Detector

VDET01	4-111
--------------	-------

ESD Slot Cells

EV2I/EV2P/EV2O/EV2IP/EV2OP/EV2T/EV2P/EV2O/EV2OP	4-112
EV2I_ABB/EV2OP_ABB/EV2T_ABB	4-112

Common Slot Cells

EC0C0/EC0C0D/EC0CA0/EC0CA0D/EC0C0_BB/EC0C0D_BB/EC0C0_VBB/EC0C0D_VBB	4-113
--	-------

5 Compiled Macrocells

Overview to Compiled Memory	5-1
Compiled Memory Naming Convention	5-1
Characteristics for Timing and Power	5-2
Built-In Self Test for Compiled Memory	5-3
Selection Guide for Compiled Memory	5-4

High-Density Compiled Memory

SPSRAM_HD	5-7
SPSRAMBW_HD	5-17
DPSRAM_HD	5-27
SPARAM_HD	5-37
DROM_HD	5-48
MROM_HD	5-56
ARFRAM_HD	5-64
FIFO_HD	5-83

Low-Power Compiled Memory

SPSRAM_LP	5-95
DPSRAM_LP	5-105
SPARAM_LP	5-115
DROM_LP	5-125
MROM_LP	5-133

Overview to Compiled Datapath

Overview to Compiled Datapath	5-141
Compiled Macrocell Selection Guide	5-142

Contents

ADDER.....	5-143
BS	5-148
MPY	5-153

6 PLL

PLL2013X	6-1
----------------	-----

NOTE