

## MOS FIELD EFFECT TRANSISTOR 2SK3326

### SWITCHING N-CHANNEL POWER MOS FET INDUSTRIAL USE

### **DESCRIPTION**

The 2SK3326 is N-Channel DMOS FET device that features a low gate charge and excellent switching characteristics, and designed for high voltage applications such as switching power supply, AC adapter.

### ORDERING INFORMATION

PART NUMBER	PACKAGE
2SK3326	Isolated TO-220

### **FEATURES**

· Low gate charge :

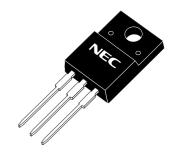
 $Q_G = 22 \text{ nC TYP}$ . ( $V_{DD} = 400 \text{ V}$ ,  $V_{GS} = 10 \text{ V}$ ,  $I_D = 10 \text{ A}$ )

- Gate voltage rating: ±30 V
- Low on-state resistance :

RDS(on) =  $0.85 \Omega$  MAX. (VGS = 10 V, ID = 5.0 A)

- · Avalanche capability ratings
- Isolated TO-220(MP-45F) package

(Isolated TO-220)



### ABSOLUTE MAXIMUM RATINGS (TA = 25°C)

Drain to Source Voltage (Vgs = 0 V)	VDSS	500	V
Gate to Source Voltage (Vps = 0 V)	VGSS(AC)	±30	V
Drain Current (DC)	ID(DC)	±10	Α
Drain Current (pulse) Note1	D(pulse)	±40	Α
Total Power Dissipation (Tc = 25°C)	P⊤	40	W
Total Power Dissipation (T <sub>A</sub> = 25°C)	PT	2.0	W
Channel Temperature	$T_ch$	150	°C
Storage Temperature	Tstg	-55 to +150	°C
Single Avalanche Current Note2	las	10	Α
Single Avalanche Energy Note2	Eas	10.7	mJ

**Notes 1.** PW  $\leq$  10  $\mu$ s, Duty Cycle  $\leq$  1 %

2. Starting T<sub>ch</sub> = 25 °C, V<sub>DD</sub> = 150 V, R<sub>G</sub> = 25  $\Omega$ , V<sub>GS</sub> = 20 V  $\rightarrow$  0 V

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Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

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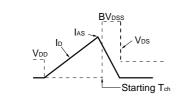


### **ELECTRICAL CHARACTERISTICS (TA = 25 °C)**

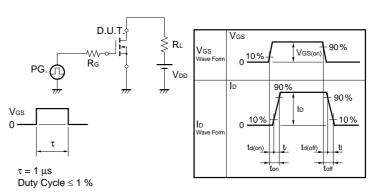
ww.DataShCHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain Leakage Current	IDSS	Vps = 500 V, Vgs = 0 V			100	μΑ
Gate to Source Leakage Current	Igss	V <sub>G</sub> S = ±30 V, V <sub>D</sub> S = 0 V			±100	nA
Gate to Source Cut-off Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA	2.5		3.5	V
Forward Transfer Admittance	yfs	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 5.0 A	2.0	4.0		S
Drain to Source On-state Resistance	RDS(on)	V <sub>G</sub> S = 10 V, I <sub>D</sub> = 5.0 A		0.68	0.85	Ω
Input Capacitance	Ciss	V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 0 V, f = 1 MHz		1200		pF
Output Capacitance	Coss			190		pF
Reverse Transfer Capacitance	Crss			10		pF
Turn-on Delay Time	td(on)	$V_{DD} = 150 \text{ V}, I_{D} = 5.0 \text{ A}, V_{GS(on)} = 10 \text{ V},$		21		ns
Rise Time	tr	$R_G = 10 \Omega$ , $R_L = 60 \Omega$		11		ns
Turn-off Delay Time	<b>t</b> d(off)			40		ns
Fall Time	tf			9.5		ns
Total Gate Charge	Q <sub>G</sub>	V <sub>DD</sub> = 400 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 10 A		22		nC
Gate to Source Charge	Qgs			6.5		nC
Gate to Drain Charge	Q <sub>GD</sub>			7.5		nC
Body Diode Forward Voltage	V <sub>F(S-D)</sub>	IF = 10 A, VGS = 0 V		1.0		V
Reverse Recovery Time	trr	$I_F = 10 \text{ A}, \text{ Vgs} = 0 \text{ V}, \text{ di/dt} = 50 \text{ A}/\mu\text{s}$		0.5		μs
Reverse Recovery Charge	Qrr			2.6		μC

### **TEST CIRCUIT 1 AVALANCHE CAPABILITY**

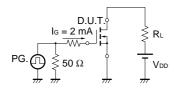
# $\begin{array}{c} \text{D.U.T.} \\ \text{Rg} = 25 \Omega \\ \text{VGS} = 20 \rightarrow 0 \text{V} \\ \end{array} \begin{array}{c} \text{PG.} \\ \text{W} \\ \text{W} \end{array} \begin{array}{c} \text{S} \\ \text{50 } \Omega \\ \text{W} \end{array}$



### **TEST CIRCUIT 2 SWITCHING TIME**

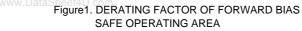


### **TEST CIRCUIT 3 GATE CHARGE**





### TYPICAL CHARACTERISTICS(TA = 25 °C)



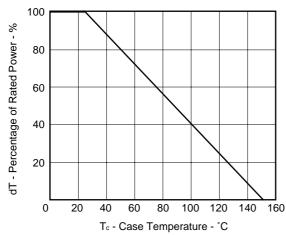


Figure3. FORWARD BIAS SAFE OPERATING AREA

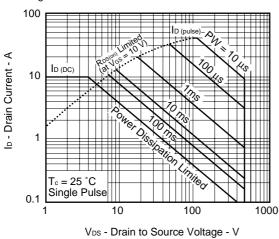


Figure 5. DRAIN CURRENT vs.

GATE TO SOURCE VOLTAGE

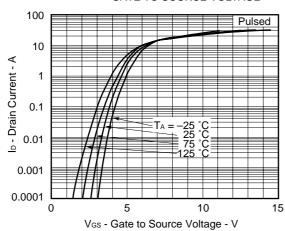


Figure 2. TOTAL POWER DISSIPATION vs. CASE TEMPERATURE

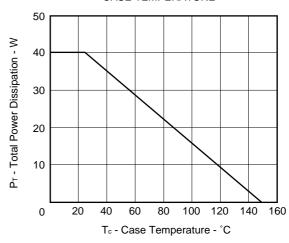
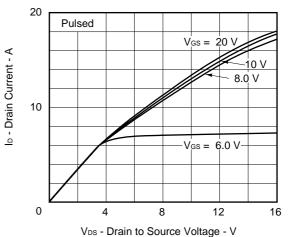


Figure4. DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



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### Figure 6. TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

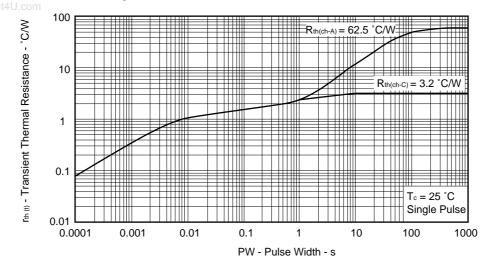


Figure7. FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT

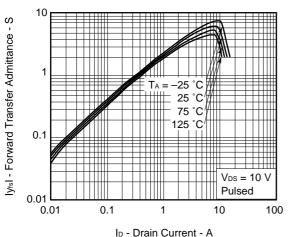


Figure9. DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

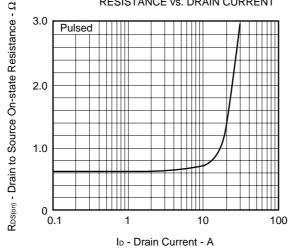


Figure8. DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

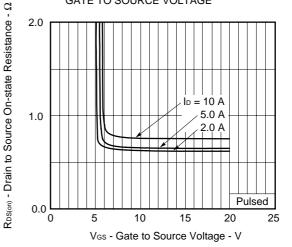


Figure 10. GATE TO SOURCE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE

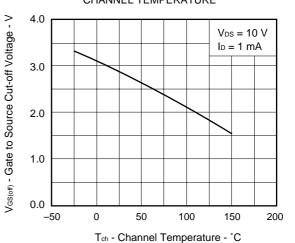




Figure 11. DRAIN TO SOURCE ON-STATE RESISTANCE vs. **CHANNEL TEMPERATURE** 

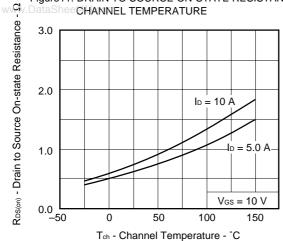


Figure 13. CAPACITANCE vs. DRAIN TO

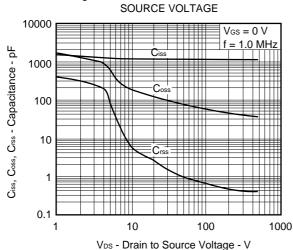


Figure 15. REVERSE RECOVERY TIME vs. **DRAIN CURRENT** 

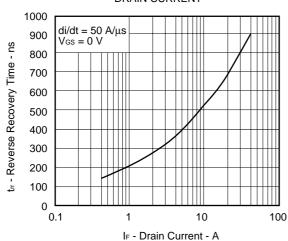


Figure 12. SOURCE TO DRAIN DIODE FORWARD VOLTAGE

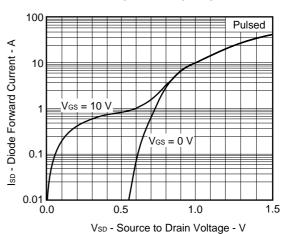


Figure 14. SWITCHING CHARACTERISTICS

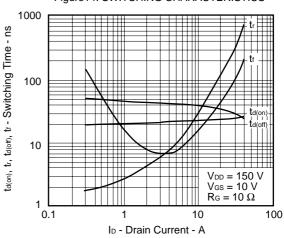


Figure 16. DYNAMIC INPUT/OUTPUT CHARACTERISTICS

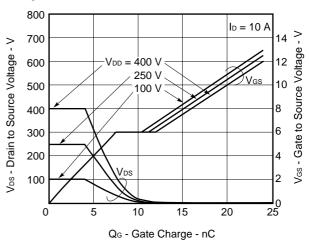


Figure 17. SINGLE AVALANCHE ENERGY vs www.DataSheet4U.coiSTARTING CHANNEL TEMPERATURE

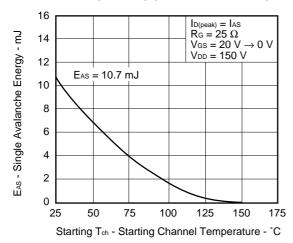
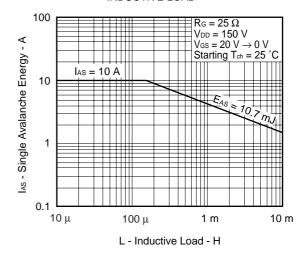


Figure 18. SINGLE AVALANCHE ENERGY vs INDUCTIVE LOAD

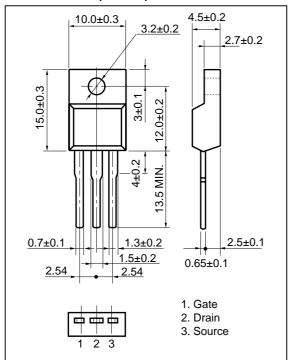




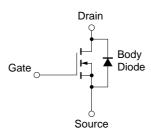
### PACKAGE DRAWING (Unit: mm)

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### Isolated TO-220(MP-45F)



### **EQUIVALENT CIRCUIT**



**Remark** Strong electric field, when exposed to this device, cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

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