SANYO

No.3924A

LC3564Q, QM, QS

CMOS LSI

64 Kbit (8192 × 8) CMOS Static RAM

OVERVIEW

LC3564Q series devices are silicon-gate, CMOS static RAMs configured as 8192 × 8 bits. They incorporate an output enable for high-speed memory access, two chip enables for easy memory expansion, and TTL-compatible, tristate outputs for direct interfacing with a bus.

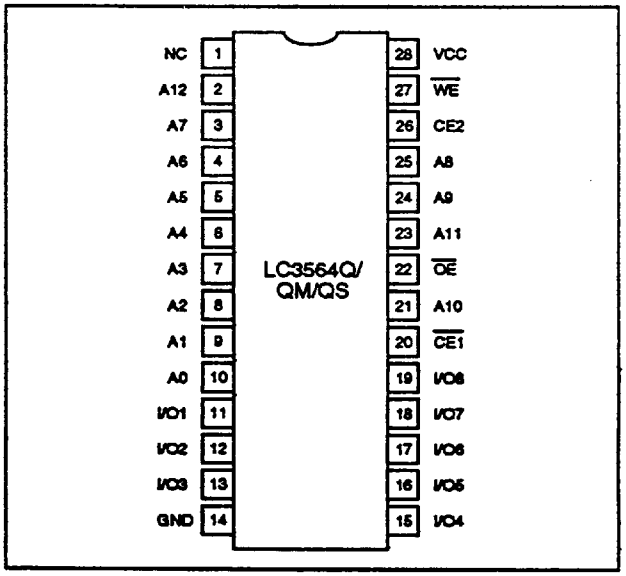
LC3564Q series ICs feature a data retention mode and a low standby current, making them ideal for low-power or battery-powered equipment.

LC3564Q series ICs operate from a 2.7 to 5.5 V supply and are available in 28-pin DIPs, 28-pin SOPs (450 mil) and 28-pin SDIPs.

FEATURES

- 8192 × 8 bits
- 70 ns (LC3564Q-70 series), 85 ns (LC3564Q-85 series) and 100 ns (LC3564Q-10 series) maximum address access times (5 V operation)
- 200 ns (LC3564Q-70 series), 250 ns (LC3564Q-85 series) and 500 ns (LC3564Q-10 series) maximum address access times (3 V operation)
- Asynchronous operation
- TTL-compatible input/outputs at V_{CC} = 5 V and V_{CC} − 0.2/0.2 V levels at V_{CC} = 3 V
- Output enable and two chip enables
- Common input/outputs and tristate outputs
- Silicon-gate CMOS
- Data retention for V_{CC} = 2.0 to 5.5 V
- 1 µA at V_{CC} = 5 V and $T_a \leq 70$ °C, 3 µA at V_{CC} = 5 V and $T_a \leq 85$ °C, and 0.8 µA at V_{CC} = 3 V and $T_a \leq 70$ °C maximum standby currents
- −40 to 85 °C operating temperature range at V_{CC} = 5 V, and 0 to 70 °C, at V_{CC} = 3 V
- 2.7 to 5.5 V supply
- 28-pin DIP, 28-pin SOP and 28-pin SDIP

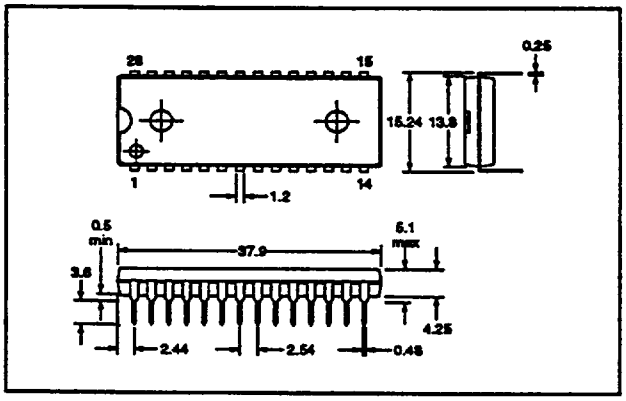
PINOUT



PACKAGE DIMENSIONS

Unit: mm

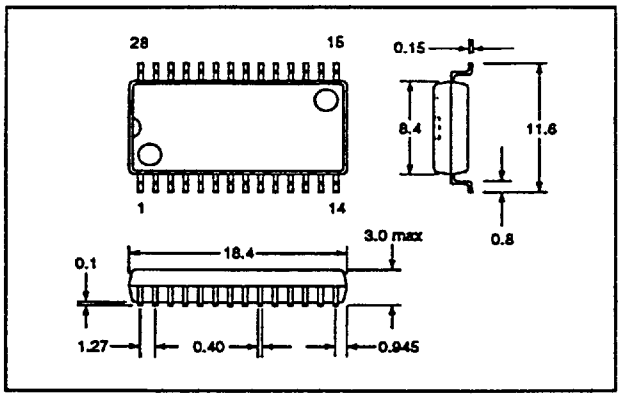
3081-DIP28NS (LC3564Q-70/85/10)



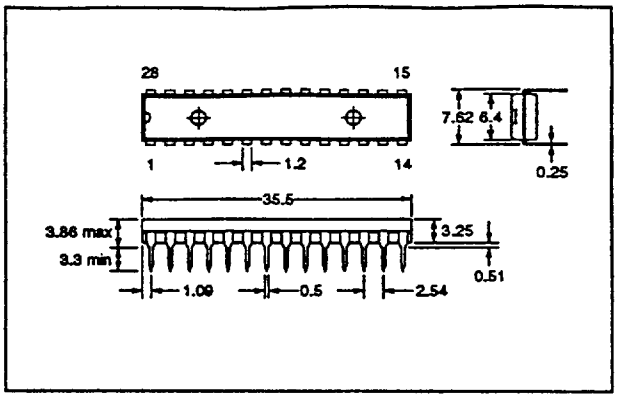
Specifications and information herein are subject to change without notice.

SANYO Electric Co.,Ltd. Semiconductor Division
Natsume Bldg., 18-6, 2-chome, Yushima, Bunkyo-ku, TOKYO 113 JAPAN

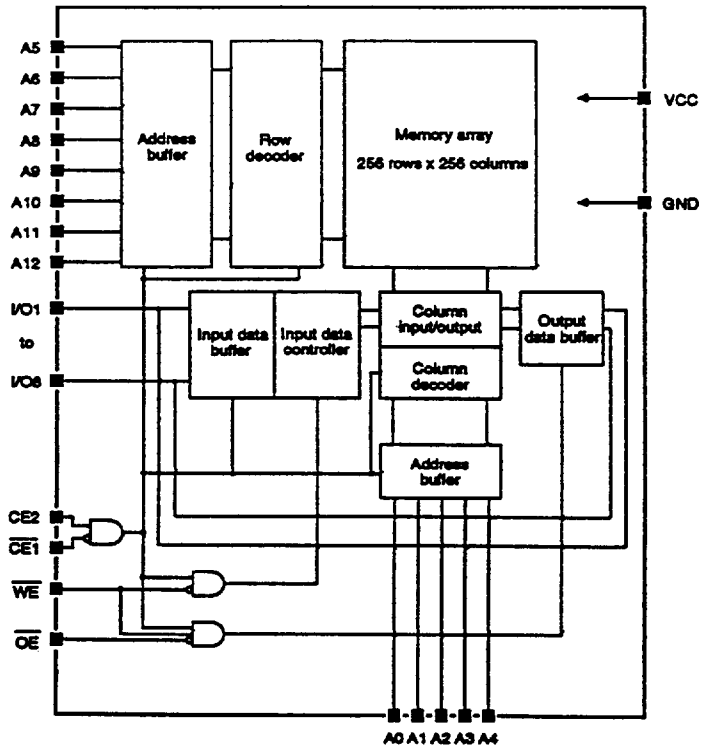
3158-SOP28 (LC3564QM-70/85/10)



3133-SDIP28 (LC3564QS-70/85/10)



BLOCK DIAGRAM



PIN DESCRIPTION

Number	Name	Description
1	NC	No connection
2 to 10, 21, 23 to 25	A0 to A12	Address inputs
11 to 13, 15 to 19	I/O1 to I/O8	Data inputs/outputs
14	GND	Ground
20, 26	$\overline{CE1}$, CE2	Chip enable inputs
22	$\overline{OE}$	Output enable input
27	$\overline{WE}$	Write enable input
28	VCC	Supply voltage

MODE SELECTION

Mode	$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	I/O1 to I/O8	Supply current
Read cycle	L	H	L	H	Data output	I_{CCA}
Write cycle	L	H	×	L	Data input	I_{CCA}
Output disable	L	H	H	H	High impedance	I_{CCA}
Standby	H	×	×	×	High impedance	I_{CCS}
	×	L	×	×	High impedance	I_{CCS}

Note
× = don't care

SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	V_{CC}	7	V
Input voltage range. See note.	V_I	−0.3 to V_{CC} + 0.3	V
Input/output voltage range	$V_{I/O}$	−0.3 to V_{CC} + 0.3	V
Power dissipation	P_D	1 (LC3564Q)	W
		1 (LC3564QS)	
		0.7 (LC3564QM)	
Operating temperature range	T_{opg}	0 to 70 (3 V operation)	°C
		−40 to 85 (5 V operation)	
Storage temperature range	T_{stg}	−55 to 125	°C

Notes

1. 3.0 V undershoot transient maximum rating for 30 ns/cycle
2. Stresses greater than those listed in the table above can cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods can affect reliability.

Capacitance

T_a = 25 °C, f = 1 MHz

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Input capacitance	C_I	V_I = 0 V	–	6	10	pF
Input/output capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V	–	6	10	pF

Note
Sampled values only

5 V Operation

Recommended Operating Conditions

T_a = 25 °C

Parameter	Symbol	Rating	Unit
Supply voltage	V_{CC}	5	V
Supply voltage range	V_{CC}	4.5 to 5.5	V

DC Electrical Characteristics

V_{CC} = 5 V ±10%, T_a = −40 to 85 °C unless otherwise noted

Parameter	Symbol	Condition		Rating min	Rating typ	Rating max	Unit
Operating supply current for V_{IL} = 0.2 V and V_{IH} = V_{CC} − 0.2 V input signal levels	I_{CCA1}	$V_{CE1} \le 0.2$ V, $V_{CE2} \ge V_{CC} - 0.2$ V, I_{VO} = 0 mA, $V_I \le 0.2$ V or $V_I \ge V_{CC} - 0.2$ V	$T_a \le 70$ °C	–	0.01	1.0	µA
			$T_a \le 85$ °C	–	–	3	
	I_{CCA4}	$V_{CE} \le 0.2$ V, $V_{CE2} \ge V_{CC} - 0.2$ V, I_{VO} = 0 mA	Minimum cycle time	–	–	35	mA
			1 µs cycle time	–	4	–	
Operating supply current for TTL-level input signals	I_{CCA2}	$V_{CE1} = V_I$, $V_{CE2} = V_{IH}$, I_{VO} = 0 mA, $V_I = V_{IH}$ or V_{IL}		–	–	7	mA
	I_{CCA3}	$V_{CE1} = V_{IL}$, $V_{CE2} = V_{IH}$, I_{VO} = 0 mA	Minimum cycle time	–	–	40	
			1 µs cycle time	–	7	–	
Standby supply current for V_{IL} = 0.2 V and V_{IH} = V_{CC} − 0.2 V input signal levels	I_{CCS1}	$V_{CE2} \le 0.2$ V or ($V_{CE1} \ge V_{CC} - 0.2$ V, $V_{CE2} \ge V_{CC} - 0.2$ V)	$T_a \le 70$ °C	–	0.01	1.0	µA
			$T_a \le 85$ °C	–	–	3	
Standby supply current for TTL-level input signals	I_{CCS2}	$V_{CE2} = V_{IL}$ or $V_{CE1} = V_{IH}$, V_I = 0 V to V_{CC}		–	–	2	mA
LOW-level input voltage	V_{IL}			−0.3	–	0.8	V
HIGH-level input voltage	V_{IH}			2.2	–	V_{CC} + 0.3	V
LOW-level output voltage	V_{OL}	I_{OL} = 2 mA		–	–	0.4	V
HIGH-level output voltage	V_{OH}	I_{OH} = −1 mA		2.4	–	–	V
Input leakage current	I_{LI}	V_I = 0 V to V_{CC}		−1	–	1	µA
Input/output leakage current	I_{LO}	$V_{CE1} = V_{IH}$ or $V_{CE2} = V_{IL}$ or $V_{OE} = V_{IH}$ or $V_{WE} = V_{IL}$, V_{VO} = 0 V to V_{CC}		−1	–	1	µA

Note

Typical values are measured at V_{CC} = 5 V and T_a = 25 °C.

AC Electrical Characteristics

Test conditions

- 0.6 V LOW-level input pulse
- 2.4 V HIGH-level input pulse
- 5 ns input rise and fall times
- 1.5 V input/output timing reference
- 1 TTL gate + 30 pF output load (including jig capacitance) (LC3564Q/QM/QS-70)
- 1 TTL gate + 100 pF output load (including jig capacitance) (LC3564Q/QM/QS-85/10)

Read cycle

V_{CC} = 5 V ±10%, T_a = –40 to 85 °C

Parameter	Symbol	LC3564Q/QM/QS-70		LC3564Q/QM/QS-85		LC3564Q/QM/QS-10		Unit
		min	max	min	max	min	max	
Read cycle time	t_{RC}	70	–	85	–	100	–	ns
Address access time	t_{AA}	–	70	–	85	–	100	ns
$\overline{CE1}$ access time	t_{CA1}	–	70	–	85	–	100	ns
CE2 access time	t_{CA2}	–	70	–	85	–	100	ns
$\overline{OE}$ access time	t_{OA}	–	35	–	45	–	50	ns
Output hold time	t_{OH}	10	–	10	–	10	–	ns
$\overline{CE1}$ to output enable time	t_{COE1}	10	–	10	–	10	–	ns
CE2 to output enable time	t_{COE2}	10	–	10	–	10	–	ns
$\overline{OE}$ to output enable time	t_{OOE}	5	–	5	–	5	–	ns
$\overline{CE1}$ to output disable time	t_{COD1}	–	30	–	35	–	35	ns
CE2 to output disable time	t_{COD2}	–	30	–	35	–	35	ns
$\overline{OE}$ to output disable time	t_{OOD}	–	25	–	25	–	25	ns

Write cycle

V_{CC} = 5 V ±10%, T_a = –40 to 85 °C

Parameter	Symbol	LC3564Q/QM/QS-70		LC3564Q/QM/QS-85		LC3564Q/QM/QS-10		Unit
		min	max	min	max	min	max	
Write cycle time	t_{WC}	70	–	85	–	100	–	ns
Address setup time	t_{AS}	0	–	0	–	0	–	ns
Write pulsewidth	t_{WP}	50	–	55	–	55	–	ns
$\overline{CE1}$ setup time	t_{CW1}	60	–	65	–	65	–	ns
CE2 setup time	t_{CW2}	60	–	65	–	65	–	ns
Write recovery time	t_{WR}	0	–	0	–	0	–	ns
$\overline{CE1}$ write recovery time	t_{WR1}	0	–	0	–	0	–	ns
CE2 write recovery time	t_{WR2}	0	–	0	–	0	–	ns
Data setup time	t_{DS}	40	–	50	–	50	–	ns
Data hold time	t_{DH}	0	–	0	–	0	–	ns
$\overline{CE1}$ data hold time	t_{DH1}	0	–	0	–	0	–	ns
CE2 data hold time	t_{DH2}	0	–	0	–	0	–	ns
$\overline{WE}$ to output enable time	t_{WOE}	5	–	5	–	5	–	ns
$\overline{WE}$ to output disable time	t_{WOD}	–	30	–	35	–	35	ns

3 V Operation

Recommended Operating Conditions

T_a = 25 °C

Parameter	Symbol	Rating	Unit
Supply voltage	V_{CC}	3	V
Supply voltage range	V_{CC}	2.7 to 3.3	V

DC Electrical Characteristics

V_{CC} = 3 V ±10%, T_a = 0 to 70 °C unless otherwise noted

Parameter	Symbol	Condition		Rating min	Rating typ	Rating max	Unit
Operating supply current for V_{IL} = 0.2 V and V_{IH} = V_{CC} − 0.2 V input level signals	I_{CCA1}	$V_{CE1} \leq V_{IL}$, $V_{CE2} \geq V_{IH}$, $I_{I/O}$ = 0 mA, $V_I \leq V_{IL}$, $V_I \geq V_{IH}$		–	0.01	0.8	µA
	I_{CCA4}	$V_{CE1} = V_{IL}$, $V_{CE2} = V_{IH}$, $I_{I/O}$ = 0 mA	Minimum cycle time	–	–	20	mA
			1 µs cycle time	–	3	–	
Standby supply current for V_{IL} = 0.2 V and V_{IH} = V_{CC} − 0.2 V input level signals	I_{CCS1}	$V_{CE2} \leq$ 0.2 V or {$V_{CE1} \geq V_{CC}$ − 0.2 V, $V_{CE2} \geq V_{CC}$ − 0.2 V}		–	0.01	0.8	µA
LOW-level input voltage	V_{IL}			0	–	0.2	V
HIGH-level input voltage	V_{IH}			V_{CC} − 0.2	–	V_{CC}	V
LOW-level output voltage	V_{OL}	I_{OL} = 1 mA		–	–	0.2	V
HIGH-level output voltage	V_{OH}	I_{OH} = −0.5 mA		V_{CC} − 0.2	–	–	V
Input leakage current	I_{LI}	V_I = 0 V to V_{CC}		−1	–	1	µA
Input/output leakage current	I_{LO}	$V_{CE1} = V_{IH}$ or $V_{CE2} = V_{IL}$ or $V_{OE} = V_{IH}$ or $V_{WE} = V_{IL}$, $V_{I/O}$ = 0 V to V_{CC}		−1	–	1	µA

Note

Typical values are measured at V_{CC} = 3 V and T_a = 25 °C.

AC Electrical Characteristics

Test conditions

- 0.2 V LOW-level input pulse
- V_{CC} – 0.2 V HIGH-level input pulse
- 10 ns input rise and fall times
- 1.5 V input/output timing reference
- 30 pF output load (including jig capacitance) (LC3564Q/QM/QS-70)
- 100 pF output load (including jig capacitance) (LC3564Q/QM/QS-85/10)

Read cycle

V_{CC} = 3 V ±10%, T_a = 0 to 70 °C

Parameter	Symbol	LC3564Q/QM/QS-70		LC3564Q/QM/QS-85		LC3564Q/QM/QS-10		Unit
		min	max	min	max	min	max	
Read cycle time	t_{RC}	200	–	250	–	500	–	ns
Address access time	t_{AA}	–	200	–	250	–	500	ns
$\overline{CE1}$ access time	t_{CA1}	–	200	–	250	–	500	ns
CE2 access time	t_{CA2}	–	200	–	250	–	500	ns
$\overline{OE}$ access time	t_{OA}	–	100	–	130	–	250	ns
Output hold time	t_{OH}	20	–	20	–	20	–	ns
$\overline{CE1}$ to output enable time	t_{COE1}	20	–	20	–	20	–	ns
CE2 to output enable time	t_{COE2}	20	–	20	–	20	–	ns
$\overline{OE}$ to output enable time	t_{OOE}	10	–	10	–	10	–	ns
$\overline{CE1}$ to output disable time	t_{COD1}	–	60	–	80	–	120	ns
CE2 to output disable time	t_{COD2}	–	60	–	80	–	120	ns
$\overline{OE}$ to output disable time	t_{OOD}	–	50	–	70	–	100	ns

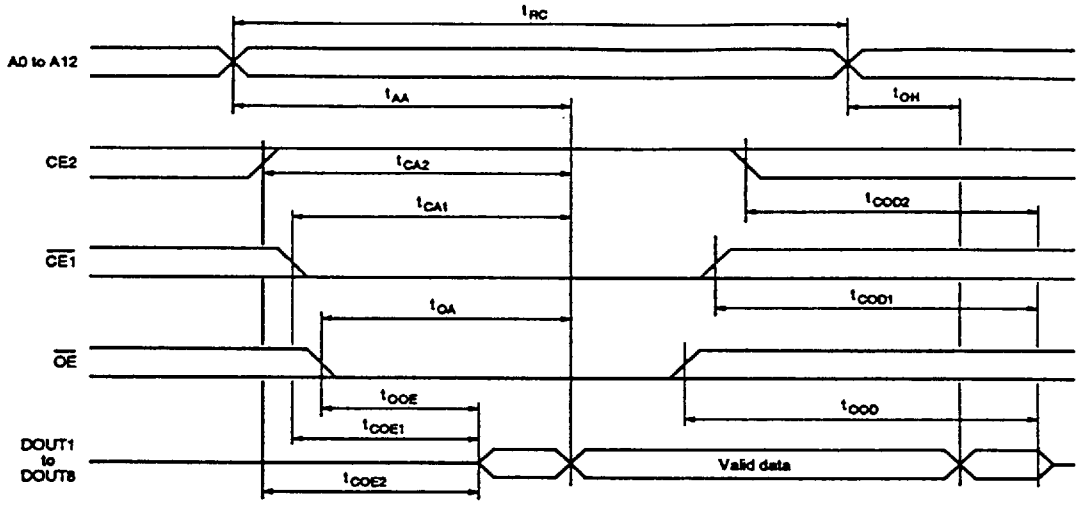
Write cycle

V_{CC} = 3 V ±10%, T_a = 0 to 70 °C

Parameter	Symbol	LC3564Q/QM/QS-70		LC3564Q/QM/QS-85		LC3564Q/QM/QS-10		Unit
		min	max	min	max	min	max	
Write cycle time	t_{WC}	200	–	250	–	500	–	ns
Address setup time	t_{AS}	0	–	0	–	0	–	ns
Write pulsewidth	t_{WP}	140	–	160	–	200	–	ns
$\overline{CE1}$ setup time	t_{CW1}	150	–	180	–	250	–	ns
CE2 setup time	t_{CW2}	150	–	180	–	250	–	ns
Write recovery time	t_{WR}	10	–	20	–	50	–	ns
$\overline{CE1}$ write recovery time	t_{WR1}	10	–	20	–	50	–	ns
CE2 write recovery time	t_{WR2}	10	–	20	–	50	–	ns
Data setup time	t_{DS}	130	–	150	–	180	–	ns
Data hold time	t_{DH}	0	–	0	–	0	–	ns
$\overline{CE1}$ data hold time	t_{DH1}	0	–	0	–	0	–	ns
CE2 data hold time	t_{DH2}	0	–	0	–	0	–	ns
$\overline{WE}$ to output enable time	t_{WOE}	10	–	10	–	10	–	ns
$\overline{WE}$ to output disable time	t_{WOD}	–	60	–	80	–	120	ns

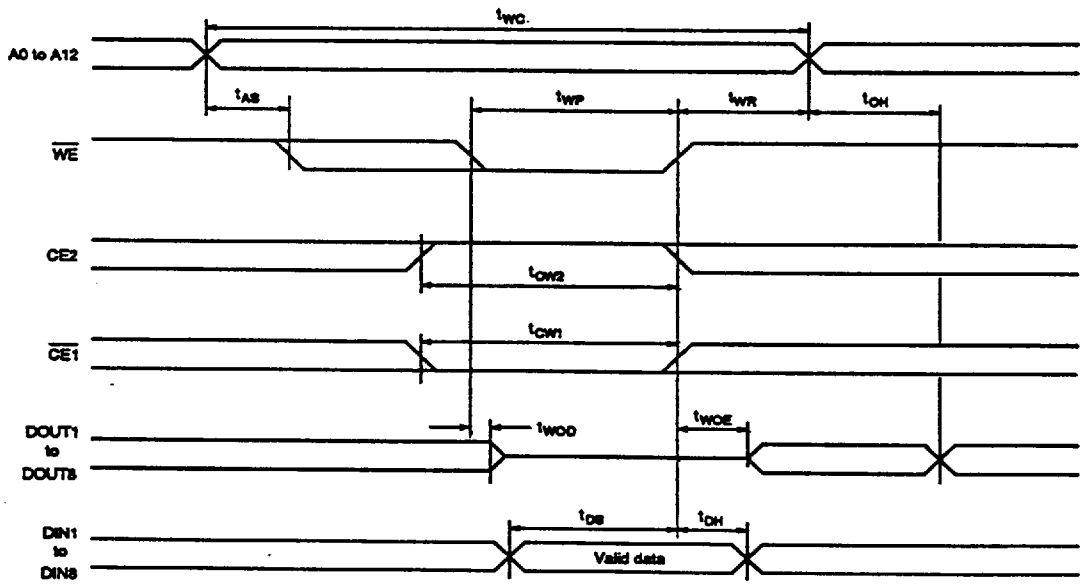
Timing Diagrams

Read cycle waveform

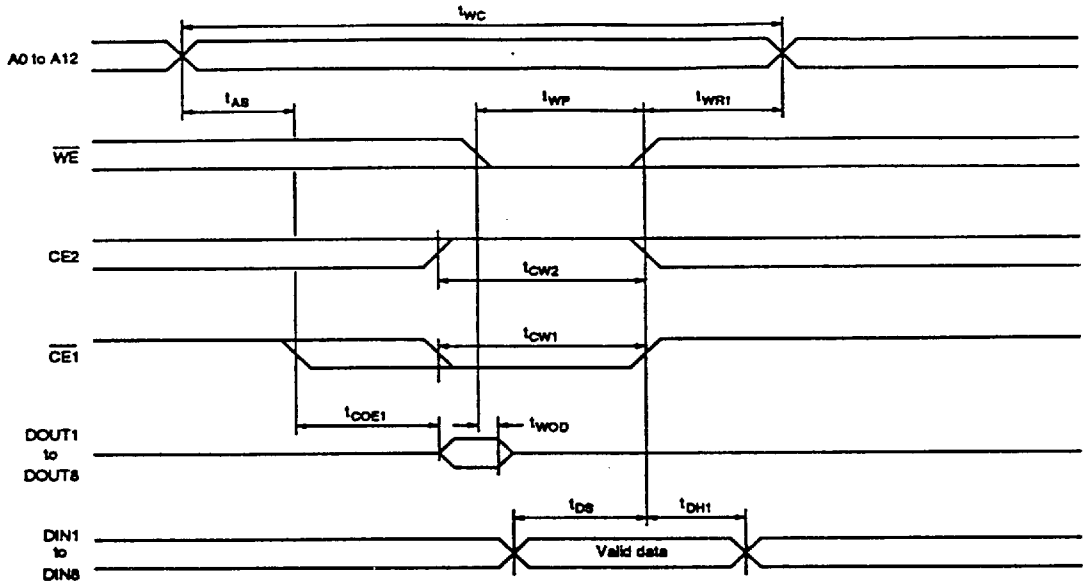


Write cycle waveforms

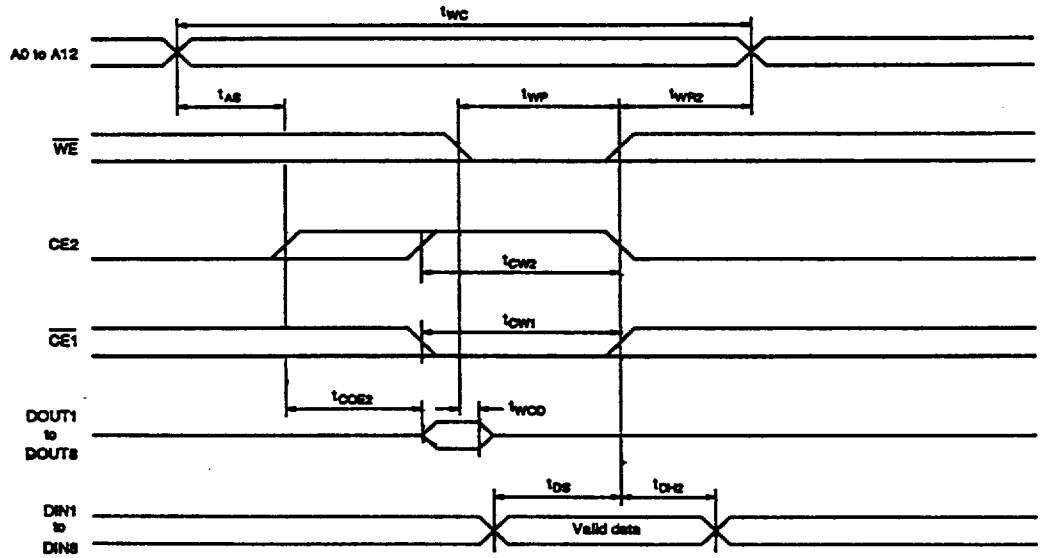
Write cycle 1 ($\overline{WE}$)



Write cycle 2 ($\overline{CE1}$)



Write cycle 3 (CE2)



Notes

1. Hold $\overline{WE}$ HIGH during the read cycle.
2. Do not apply signals to DOUT1 to DOUT8 of opposite phase to the internal lines during write cycle 1.
3. t_{WP} is measured from when $\overline{CE1}$ and $\overline{WE}$ go LOW and CE2 goes HIGH until one of these pins changes state.
4. t_{CW1} and t_{CW2} are measured from when both $\overline{CE1}$ and $\overline{WE}$ go LOW and CE2 goes HIGH until one of these pins changes state.
5. DOUT1 to DOUT8 are high impedance when either $\overline{CE1}$ or $\overline{OE}$ is HIGH, or CE2 or $\overline{WE}$ is LOW.
6. $\overline{OE}$ can be either V_{IH} or V_{IL} during the write cycles.
7. Data is output on DOUT1 to DOUT8 during write cycle 1.

Data Retention Characteristics

T_a = –40 to 85 °C

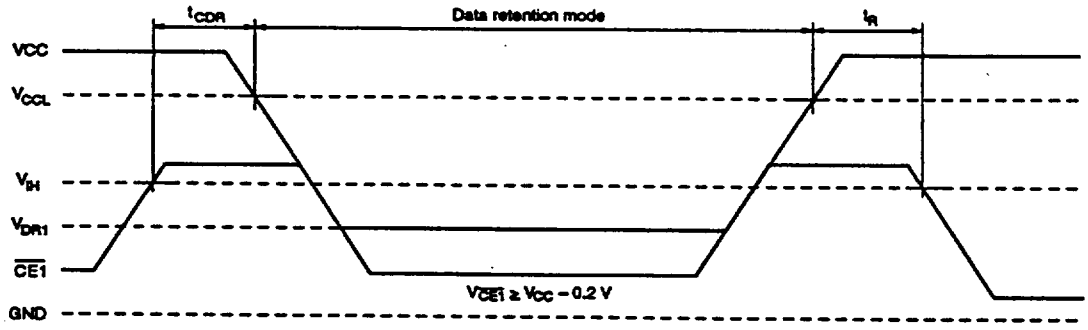
Parameter	Symbol	Condition		Rating min	Rating typ	Rating max	Unit
Data retention mode supply voltage	V_{DR1}	$V_{\overline{CE1}} \geq V_{CC} - 0.2$ V, $V_{CE2} \geq V_{CC} - 0.2$ V or $V_{CE2} \leq 0.2$ V		2.0	–	5.5	V
	V_{DR2}	$V_{CE2} \leq 0.2$ V		2.0	–	5.5	
Data retention mode supply current	I_{CCDR1}	V_{CC} = 3 V, $V_{\overline{CE1}} \geq V_{CC} - 0.2$ V, $V_{CE2} \geq V_{CC} - 0.2$ V or $V_{CE2} \leq 0.2$ V	$T_a \leq 70$ °C	–	–	0.8	µA
			$T_a \leq 85$ °C	–	–	2.5	
	I_{CCDR2}	V_{CC} = 3 V, $V_{CE2} \leq 0.2$ V	$T_a \leq 70$ °C	–	–	0.8	
			$T_a \leq 85$ °C	–	–	2.5	
$\overline{CE1}$ and CE2 setup time	t_{CDR}			0	–	–	ns
$\overline{CE1}$ and CE2 hold time	t_R			t_{RC}	–	–	ns

Notes

1. t_{RC} = read cycle time
2. Typical values are measured at T_a = 25 °C.

Data retention waveforms

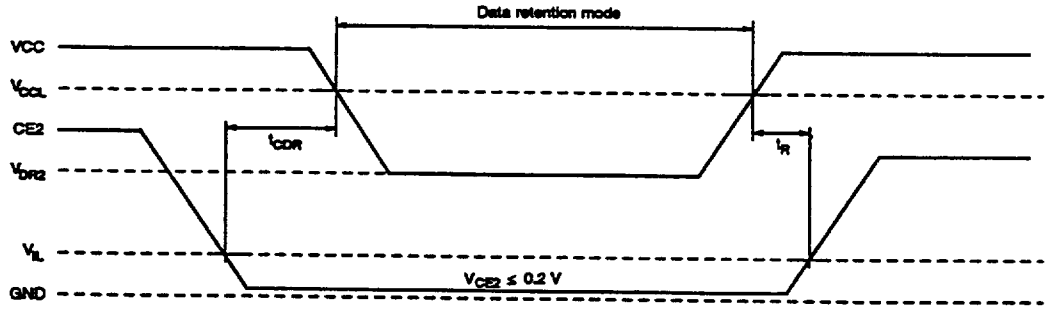
Chip enable 1 control



Note

When V_{CC} = 5 V, V_{CCL} = 4.5 V. When V_{CC} = 3 V, V_{CCL} = 2.7 V.

Chip enable 2 control



Note

When V_{CC} = 5 V, V_{CCL} = 4.5 V. When V_{CC} = 3 V, V_{CCL} = 2.7 V.