NEC

MOS INTEGRATED CIRCUIT

μPD784224, 784225, 784224Y, 784225Y

16/8-BIT SINGLE-CHIP MICROCONTROLLERS

The μPD784224 and 784225 are products of the μPD784225 Subseries in the 78K/IV Series. Besides a high-speed and high performance CPU, these controllers have ROM, RAM, I/O ports, 8-bit resolution A/D and D/A converters, timers, serial interfaces, a real-time output port, interrupt functions, and various other peripheral hardware.

The μPD784224Y and 784225Y are based on the μPD784225 Subseries with the addition of a multimaster-supporting I^2C bus interface.

Flash memory versions, the μPD78F4225 and 78F4225Y, which replace the internal ROM of the mask ROM version with flash memory, and various development tools are also available.

The functions are explained in detail in the following user's manuals. Be sure to read this manual when designing your system.

μPD784225, 784225Y Subseries User's Manual - Hardware : U12697E
78K/IV Series User's Manual - Instruction : U10905E

FEATURES

- I^2C bus
- ROM correction
- Inherits peripheral functions of μPD780058Y Subseries
- Minimum instruction execution time
  160 ns (main system clock f_{XX} = 12.5 MHz)
  61 μs (subsystem clock f_{XT} = 32.768 kHz)
- I/O port: 67 pins
- Timer/counter: 16-bit timer/counter × 1 unit
  8-bit timer/counter × 4 units
- Serial interface: 3 channels
  UART/IOE (3-wire serial I/O): 2 channels
  CSI (3-wire serial I/O, multi-master supporting I^2C bus[Note]): 1 channel
  Note μPD784225Y Subseries only
- Standby function
  HALT/STOP/IDLE mode
  In power-saving mode: HALT/IDLE mode (with subsystem clock)
- Clock division function
- Watch timer: 1 channel
- Watchdog timer: 1 channel
- Clock output function
  f_{XX}, $f_{XX}/2$, $f_{XX}/2^2$, $f_{XX}/2^3$, $f_{XX}/2^4$, $f_{XX}/2^5$, $f_{XX}/2^6$, $f_{XX}/2^7$, f_{XT} selectable
- Buzzer output function
  $f_{XX}/2^{10}$, $f_{XX}/2^{11}$, $f_{XX}/2^{12}$, $f_{XX}/2^{13}$ selectable
- A/D converter: 8-bit resolution × 8 channels
- D/A converter: 8-bit resolution × 2 channels
- Supply voltage: V_{DD} = 1.8 to 5.5 V

APPLICATION FIELD

Car audio, portable audio, telephones, etc.

Unless contextually excluded, references in this document to μPD784225 mean μPD784224, 784225, 784224Y, and 784225Y.

Document No. U12376EJ1V0DS00 (1st edition)
Date Published May 2000 J CP(K)
Printed in Japan

The mark ★ shows major revised points.

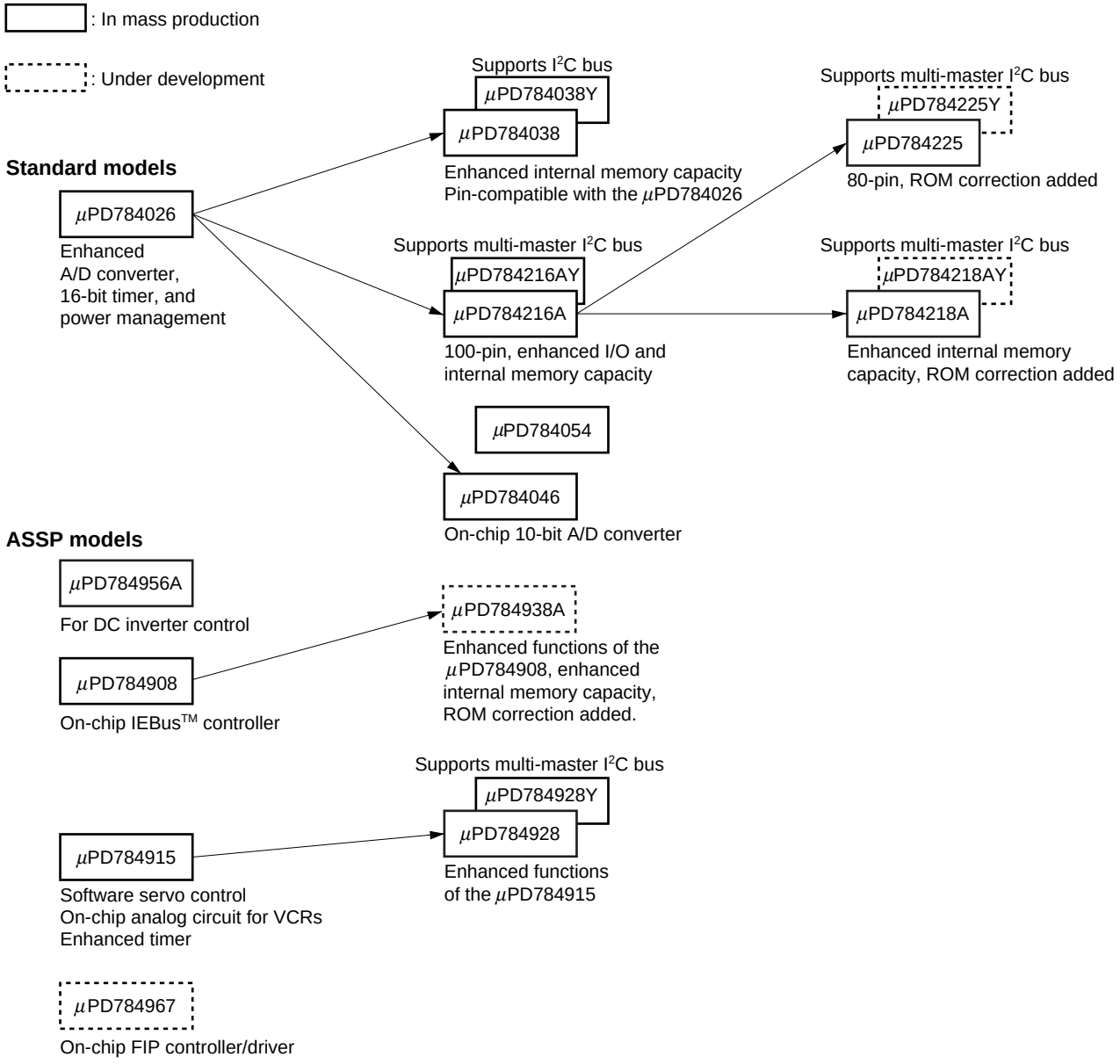
★ ORDERING INFORMATION

Part Number	Package	Internal ROM (Bytes)	Internal RAM (Bytes)
μPD784224GC-×××-8BT	80-pin plastic QFP (14 × 14 mm)	96 K	3,584
μPD784224GK-×××-9EU[Note]	80-pin plastic TQFP (fine pitch) (14 × 20 mm)	96 K	3,584
μPD784225GC-×××-8BT	80-pin plastic QFP (14 × 14 mm)	128 K	4,352
μPD784225GK-×××-9EU	80-pin plastic TQFP (fine pitch) (14 × 20 mm)	128 K	4,352
μPD784224YGC-×××-8BT	80-pin plastic QFP (14 × 14 mm)	96 K	3,584
μPD784224YGK-×××-9EU	80-pin plastic TQFP (fine pitch) (14 × 20 mm)	96 K	3,584
μPD784225YGC-×××-8BT[Note]	80-pin plastic QFP (14 × 14 mm)	128 K	4,352
μPD784225YGK-×××-9EU[Note]	80-pin plastic TQFP (fine pitch) (14 × 20 mm)	128 K	4,352

Note Under development

Remark ××× indicates a ROM code suffix.

★ 78K/IV SERIES LINEUP



FUNCTIONS

Item \ Part Number		μPD784224, μPD784224Y	μPD784225, μPD784225Y
Number of basic instructions (mnemonics)		113	
General-purpose register		8 bits × 16 registers × 8 banks, or 16 bits × 8 registers × 8 banks (memory mapping)	
Minimum instruction execution time		• 160 ns/320 ns/640 ns/1,280 ns/2,560 ns (main system clock: f_{XX} = 12.5 MHz) • 61 μs (subsystem clock: f_{XT} = 32.768 kHz)	
Internal memory	ROM	96 Kbytes	128 Kbytes
	RAM	3,584 bytes	4,352 bytes
Memory space		1 MB with program and data spaces combined	
I/O port	Total	67	
	CMOS Input	8	
	CMOS I/O	59	
Pins with ancillary functions[Note 1]	Pins with pull-up resistor	57	
	LEDs direct drive output	16	
Real-time output port		4 bits × 2, or 8 bits × 1	
Timer		Timer/event counter (16-bit) : Timer counter × 1, Capture/compare register × 2 — Pulse output: • PWM/PPG output • Square wave output • One-shot pulse output	
		Timer/event counter 1 (8-bit) : Timer counter × 1, Compare register × 1 — Pulse output: • PWM output • Square wave output	
		Timer/event counter 2 (8-bit) : Timer counter × 1, Compare register × 1 — Pulse output: • PWM output • Square wave output	
		Timer 5 (8-bit) : Timer counter × 1, Compare register × 1	
		Timer 6 (8-bit) : Timer counter × 1, Compare register × 1	
Serial interface		• UART/IOE (3-wire serial I/O): 2 channels (on-chip baud rate generator) • CSI (3-wire serial I/O, I^2C bus[Note 2] supporting multi master): 1 channel	
A/D converter		8-bit resolution × 8 channels	
D/A converter		8-bit resolution × 2 channels	
Clock output		Selectable from f_{XX}, $f_{XX}/2$, $f_{XX}/2^2$, $f_{XX}/2^3$, $f_{XX}/2^4$, $f_{XX}/2^5$, $f_{XX}/2^6$, $f_{XX}/2^7$, f_{XT}	
Buzzer output		Selectable from $f_{XX}/2^{10}$, $f_{XX}/2^{11}$, $f_{XX}/2^{12}$, $f_{XX}/2^{13}$	
Watch timer		1 channel	
Watchdog timer		1 channel	
Standby		• HALT/STOP/IDLE mode • In power-saving mode (with subsystem clock): HALT/IDLE mode	
Interrupt	Hardware	25 (internal: 18, external: 7)	
	Software	BRK instruction, BRKCS instruction, operand error	
	Non-maskable	Internal: 1, external: 1	
	Maskable	Internal: 17, external: 6	
		• 4 programmable priority levels • 3 service modes: vectored interrupt/macro service/context switching	
Supply voltage		V_{DD} = 1.8 to 5.5 V	
Package		• 80-pin plastic QFP(14 × 14 mm) • 80-pin plastic TQFP (fine pitch) (12 × 12 mm)	

Notes 1. The pins with ancillary functions are included in the I/O pins.

2. μPD784225Y Subseries only

CONTENTS

★ 1. DIFFERENCES AMONG MODELS IN μPD784225, 784225Y SUBSERIES

The only difference among the μPD784224 and 784225 lies in the internal memory capacity.

The μPD784224Y and 784225Y are based on the μPD784224 and 784225 respectively, with the addition of an I^2C bus control function.

The μPD78F4225 and 78F4225Y are provided with a 128-Kbyte flash memory instead of the mask ROM of the above models. These differences are summarized in Table 1-1.

Table 1-1. Differences among Models in μPD784225, 784225Y Subseries

Part Number / Item	μPD784224, μPD784224Y	μPD784225, μPD784225Y	μPD78F4225, μPD78F4225Y
Internal ROM	96 Kbytes (mask ROM)	128 Kbytes (mask ROM)	128 Kbytes (Flash memory)
Internal RAM	3,584 bytes	4,352 bytes	
Internal memory size switching register (IMS)Note	None		Provided
Supply voltage	V_{DD} = 1.8 to 5.5 V		V_{DD} = 1.9 to 5.5 V
Electrical specifications	Refer to the data sheet for each device.		
Recommended soldering conditions			
TEST pin	Provided		None
V_{PP} pin	None		Provided

Note The internal flash memory capacity and internal RAM capacity can be changed using the internal memory size switching register (IMS).

Caution There are differences in noise immunity and noise radiation between the flash memory and mask ROM versions. When pre-producing an application set with the flash memory version and then mass-producing it with the mask ROM version, be sure to conduct sufficient evaluations on the commercial samples (not engineering samples) of the mask ROM version.

2. MAJOR DIFFERENCES BETWEEN μPD784216Y SUBSERIES AND μPD780058Y SUBSERIES

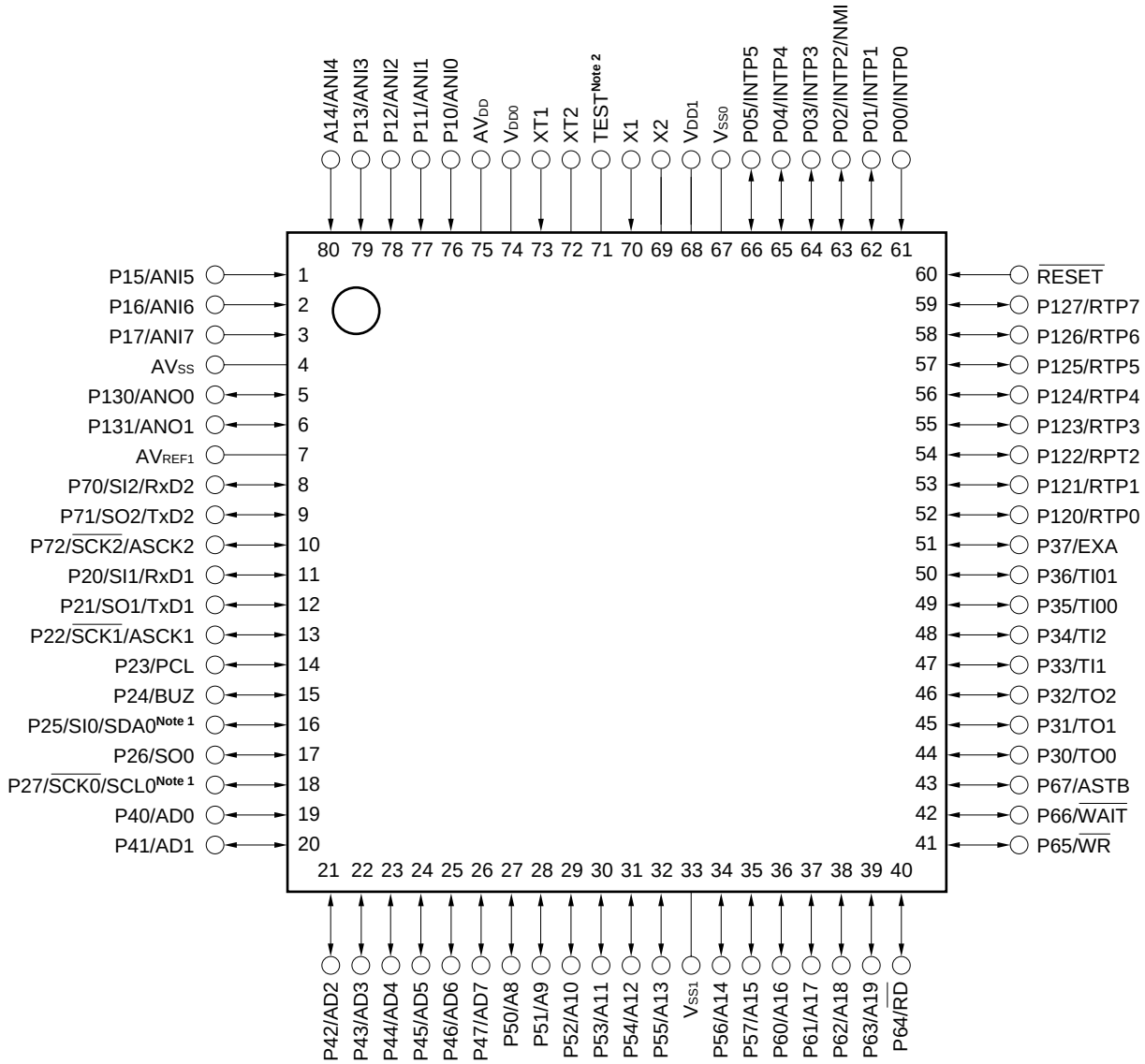
Item \ Series Name		μPD784225, 784225Y Subseries	μPD784216Y Subseries	μPD780058Y Subseries
CPU		16-bit CPU		8-bit CPU
Minimum instruction execution time	With main system clock selected	160 ns (at 12.5 MHz)		400 ns (at 5.0 MHz)
	With subsystem clock	61 μs (at 32.768 kHz)		122 μs (at 32.768 kHz)
Memory space		1 Mbytes		64 Kbytes
I/O port	Total	67 pins	86 pins	68 pins
	CMOS input	8 pins	8 pins	2 pins
	CMOS I/O	59 pins	72 pins	62 pins
	N-ch open-drain I/O	–	6 pins	4 pins
Pins with ancillary function[Note 1]	Pins with pull-up resistor	57 pins	70 pins	66 pins (flash memory model: 62 pins)
	LED direct drive output	16 pins	22 pins	12 pins
	Medium-voltage pin	–	6 pins	4 pins
Timer/counter		• 16-bit timer/event counter × 1 unit • 8-bit timer/event counter × 4 units	• 16-bit timer/event counter × 1 unit • 8-bit timer/event counter × 6 units	• 16-bit timer/event counter × 1 unit • 8-bit timer/event counter × 2 units
Serial interface		• UART/IOE (3-wire serial I/O) × 2 channels • CSI (3-wire serial I/O, multi-master supporting I^2C bus[Note 2]) × 1 channel		• UART (time-division transfer function)/IOE (3-wire serial I/O) × 2 channels • CSI (3-wire serial I/O, 2-wire serial I/O, I^2C bus) × 1 channel • CSI (3-wire serial I/O with automatic transmission/reception function) × 1 channel
Interrupt	NMI pin	Provided		None
	Macro service	Provided		None
	Context switching	Provided		None
	Programmable priority	4 levels		2 levels
Standby function		• HALT/STOP/IDLE mode • Power-saving mode: HALT/IDLE Mode		HALT/STOP mode
ROM correction		Provided	None	Provided
Package		• 80-pin plastic QFP (14 × 14 mm) • 80-pin plastic TQFP (fine pitch) (12 × 12 mm)	• 100-pin plastic QFP (fine pitch) (14 × 14 mm) • 100-pin plastic QFP (14 × 20 mm)	• 80-pin plastic QFP (14 × 14 mm) • 80-pin plastic TQFP (fine pitch) (12 × 12 mm)

Notes 1. Pins with ancillary function are included in the I/O pins.

2. μPD784225Y and 784216Y Subseries only

3. PIN CONFIGURATION (Top View)

- **80-pin plastic QFP (14 × 14 mm)**
  μPD784224GC-×××-8BT, μPD784224YGC-×××-8BT,
  μPD784225GC-×××-8BT, μPD784225YGC-×××-8BT
- **80-pin plastic TQFP (fine pitch) (12 × 12 mm)**
  μPD784224GK-×××-BE9, μPD784224YGK-×××-BE9,
  μPD784225GK-×××-BE9, μPD784225YGK-×××-BE9



Notes 1. The SCL0 and SDA0 pins are available in μPD784225Y Subseries only.

2. Connect the TEST pin to V_{SS0} directly or via a pull-down resistor. For the pull-down connection, use of a resistor with a resistance ranging from 470 Ω to 10 kΩ is recommended.

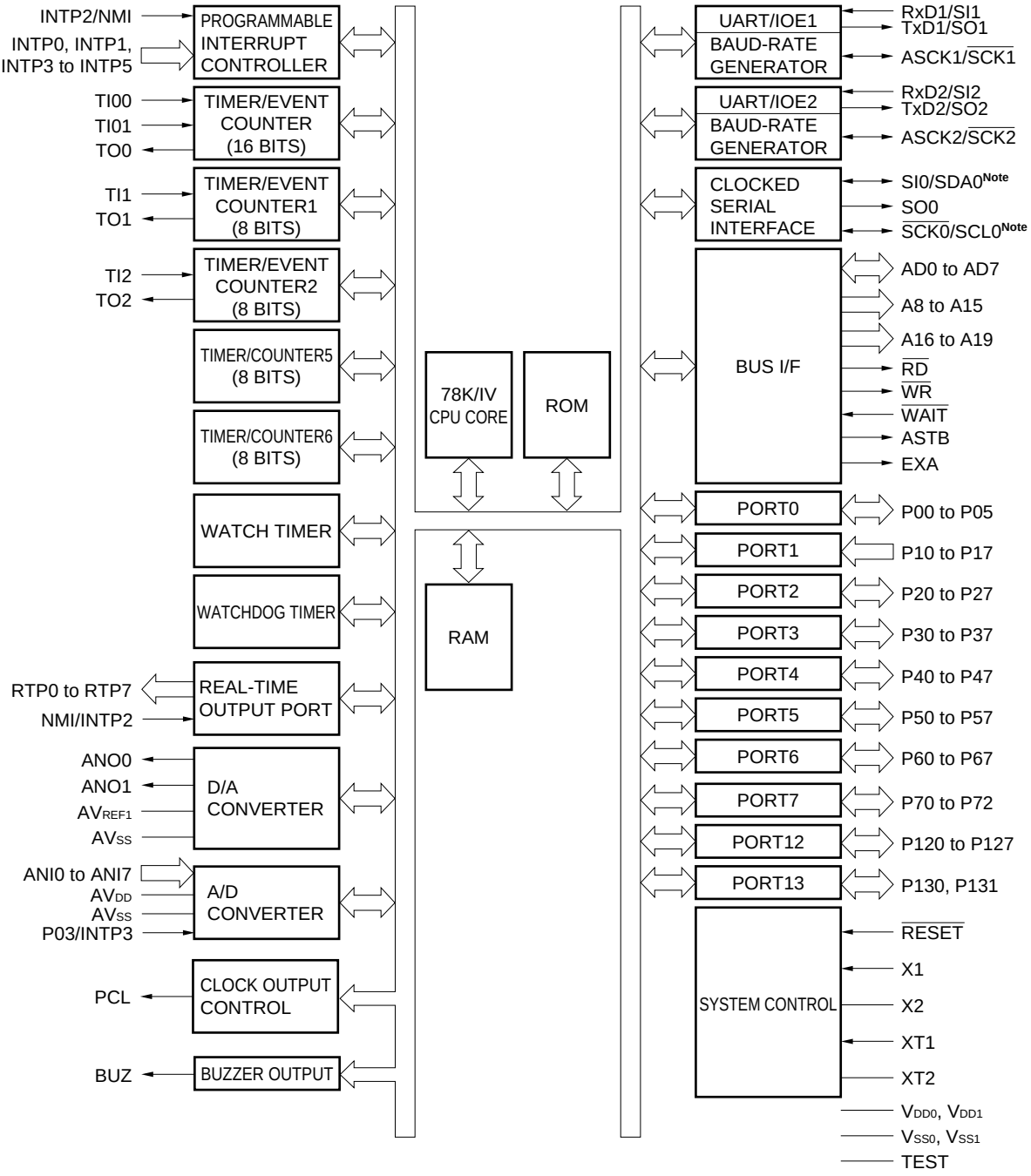
Caution Connect the AV_{SS} pin to V_{SS0}.

Remark When using in applications where noise from inside the microcomputer has to be reduced, it is recommended to take countermeasures against noise such as supplying power to V_{DD0} and V_{DD1} independently, and connecting V_{SS0} and V_{SS1} to different ground lines.

A8 to A19	: Address Bus	P130, P131	: Port13
AD0 to AD7	: Address/Data Bus	PCL	: Programmable Clock
ANI0 to ANI7	: Analog Input	$\overline{RD}$	: Read Strobe
ANO0, ANO1	: Analog Output	$\overline{RESET}$	: Reset
ASCK1, ASCK2	: Asynchronous Serial Clock	RTP0 to RTP7	: Real-time Output Port
ASTB	: Address Strobe	RxD1, RxD2	: Receive Data
AV_{DD}	: Analog Power Supply	$\overline{SCK0}$ to $\overline{SCK2}$	: Serial Clock
AV_{REF1}	: Analog Reference Voltage	SCL0**Note**	: Serial Clock
AV_{SS}	: Analog Ground	SDA0**Note**	: Serial Data
BUZ	: Buzzer Clock	SI0 to SI2	: Serial Input
EXA	: External Access Status Output	SO0 to SO2	: Serial Output
INTP0 to INTP5	: Interrupt from Peripherals	TEST	: Test
NMI	: Non-maskable Interrupt	TI00, TI01, TI1, TI2	: Timer Input
P00 to P05	: Port0	TO0 to TO2	: Timer Output
P10 to P17	: Port1	TxD1, TxD2	: Transmit Data
P20 to P27	: Port2	V_{DD0}, V_{DD1}	: Power Supply
P30 to P37	: Port3	V_{SS0}, V_{SS1}	: Ground
P40 to P47	: Port4	$\overline{WAIT}$	: Wait
P50 to P57	: Port5	$\overline{WR}$	: Write Strobe
P60 to P67	: Port6	X1, X2	: Crystal (Main System Clock)
P70 to P72	: Port7	XT1, XT2	: Crystal (Subsystem Clock)
P120 to P127	: Port12		

Note The SCL0 and SDA0 pins are available in μPD784225Y Subseries only.

4. BLOCK DIAGRAM



Note This function supports the I^2C bus interface and is available in μPD784225Y Subseries only.

Remark The internal ROM and RAM capacities differ depending on the model.

5. PIN FUNCTION

5.1 Port Pins (1/2)

Pin Name	I/O	Alternate Function	Function
P00	I/O	INTP0	Port 0 (P0): • 6-bit I/O port • Can be set in input or output mode bit-wise. • Pins set in input mode can be connected to internal pull-up resistors by software bit-wise.
P01		INTP1	
P02		INTP2/NM1	
P03		INTP3	
P04		INTP4	
P05		INTP5	
P10 to P17	Input	ANI0 to ANI7	Port 1 (P1): • 8-bit input port
P20	I/O	RxD1/SI1	Port 2 (P2): • 8-bit I/O port • Can be set in input or output mode bit-wise. • Pins set in input mode can be connected to internal pull-up resistors by software bit-wise.
P21		TxD1/SO1	
P22		ASCK1/$\overline{\text{SCK1}}$	
P23		PCL	
P24		BUZ	
P25		SI0/SDA0**Note**	
P26		SO0	
P27		$\overline{\text{SCK0}}$/SCL0**Note**	
P30	I/O	TO0	Port 3 (P3): • 8-bit I/O port • Can be set in input or output mode bit-wise. • Pins set in input mode can be connected to internal pull-up resistors by software bit-wise.
P31		TO1	
P32		TO2	
P33		TI1	
P34		TI2	
P35		TI00	
P36		TI01	
P37		EXA	
P40 to P47	I/O	AD0 to AD7	Port 4 (P4): • 8-bit I/O port • Can be set in input or output mode bit-wise. • All pins set in input mode can be connected to internal pull-up resistors by software. • Can drive LEDs.
P50 to P57	I/O	A8 to A15	Port 5 (P5): • 8-bit I/O port • Can be set in input or output mode bit-wise. • All pins set in input mode can be connected to internal pull-up resistors by software. • Can drive LEDs.

Note This function is available in μPD784255Y Subseries only.

5.1 Port Pins (2/2)

Pin Name	I/O	Alternate Function	Function
P60	I/O	A16	Port 6 (P6): • 8-bit I/O port • Can be set in input or output mode bit-wise. • All pins set in input mode can be connected to internal pull-up resistors by software.
P61		A17	
P62		A18	
P63		A19	
P64		$\overline{RD}$	
P65		$\overline{WR}$	
P66		$\overline{WAIT}$	
P67		ASTB	
P70	I/O	RxD2/SI2	Port 7 (P7): • 3-bit I/O port • Can be set in input or output mode bit-wise. • Pins set in input mode can be connected to internal pull-up resistor by software bit-wise.
P71		TxD2/SO2	
P72		ASCK2/$\overline{SCK2}$	
P120 to P127	I/O	RTP0 to RTP7	Port 12 (P12): • 8-bit I/O port • Can be set in input or output mode bit-wise. • Pins set in input mode can be connected to internal pull-up resistor by software bit-wise.
P130, P131	I/O	ANO0, ANO1	Port 13 (P13): • 2-bit I/O port • Can be set in input or output mode bit-wise.

5.2 Pins Other Than Port Pins (1/2)

Pin Name	I/O	Alternate Function	Function
TI00	Input	P35	External count clock input to 16-bit timer register
TI01		P36	Capture trigger signal input to capture/compare register 00
TI1		P33	External count clock input to 8-bit timer register 1
TI2		P34	External count clock input to 8-bit timer register 2
TO0	Output	P30	16-bit timer output (shared by 14-bit PWM output)
TO1		P31	8-bit timer output (shared by 8-bit PWM output)
TO2		P32	
RxD1	Input	P20/SI1	Serial data input (UART1)
RxD2		P70/SI2	Serial data input (UART2)
TxD1	Output	P21/SO1	Serial data output (UART1)
TxD2		P71/SO2	Serial data output (UART2)
ASCK1	Intput	P22/$\overline{\text{SCK1}}$	Baud rate clock input (UART1)
ASCK2		P72/$\overline{\text{SCK2}}$	Baud rate clock input (UART2)
SI0	Input	P25/SDA0**Note**	Serial data input (3-wire serial clock I/O0)
SI1		P20/RxD1	Serial data input (3-wire serial clock I/O1)
SI2		P70/RxD2	Serial data input (3-wire serial clock I/O2)
SO0	Output	P26	Serial data output (3-wire serial I/O0)
SO1		P21/TxD1	Serial data output (3-wire serial I/O1)
SO2		P71/TxD2	Serial data output (3-wire serial I/O2)
SDA0**Note**	I/O	P25/SI0	Serial data input/output (I^2C bus)
$\overline{\text{SCK0}}$	I/O	P27/SCL0**Note**	Serial clock input/output (3-wire serial I/O0)
$\overline{\text{SCK1}}$		P22/ASCK1	Serial clock input/output (3-wire serial I/O1)
$\overline{\text{SCK2}}$		P72/ASCK2	Serial clock input/output (3-wire serial I/O2)
SCL0**Note**		P27/$\overline{\text{SCK0}}$	Serial clock input/output (I^2C bus)
NMI	Input	P02/INTP2	Non-maskable interrupt request input
INTP0		P00	External interrupt request input
INTP1		P01	
INTP2		P02/NMI	
INTP3		P03	
INTP4		P04	
INTP5		P05	
PCL	Output	P23	Clock output (for trimming main system clock and subsystem clock)
BUZ	Output	P24	Buzzer output
RTP0 to RTP7	Output	P120 to P127	Real-time output port that outputs data in synchronization with trigger
AD0 to AD7	I/O	P40 to P47	Low-order address/data bus when external memory is connected
A8 to A15	Output	P50 to P57	Middle-order address bus when external memory is connected
A16 to A19		P60 to P63	High-order address bus when external memory is connected

Note This function is available in μPD784255Y Subseries only.

5.2 Pins Other Than Port Pins (2/2)

Pin Name	I/O	Alternate Function	Function
$\overline{RD}$	Output	P64	Strobe signal output for read operation of external memory
$\overline{WR}$		P65	Strobe signal output for write operation of external memory
$\overline{WAIT}$	Input	P66	To insert wait state(s) when external memory is accessed
ASTB	Output	P67	Strobe output to externally latch address information output to ports 4 to 6 to access external memory
EXA	Output	P37	External access status output
$\overline{RESET}$	Input	–	System reset input
X1	Input	–	To connect main system clock oscillation crystal
X2	–		
XT1	Input	–	To connect subsystem clock oscillation crystal
XT2	–		
ANI0 to ANI7	Input	P10 to P17	Analog voltage input for A/D converter
ANO0, ANO1	Output	P130, P131	Analog voltage output for D/A converter
AV_{REF1}	–	–	To apply reference voltage for D/A converter
AV_{DD}			Positive power supply for A/D converter. Connected to V_{DD0}.
AV_{SS}			GND for A/D converter and D/A converter. Connected to V_{SS0}.
V_{DD0}			Positive power supply for port block
V_{SS0}			GND potential for port block
V_{DD1}			Positive power supply (except port block)
V_{SS1}			GND potential (except port block)
★ TEST			Connect this pin to V_{SS0} directly or via pull-down resistor. For the pull-down connection, use of a resistor with a resistance ranging from 470 Ω to 10 kΩ is recommended.

5.3 I/O Circuit Type of Respective Pins and Recommended Connections of Unused Pins

Table 5-1 shows symbols indicating the I/O circuit types of the respective pins and the recommended connection of unused pins.

For the circuit diagram of each type of I/O circuit, refer to **Figure 5-1**.

★ **Table 5-1. I/O Circuit Type of Respective Pins and Recommended Connections of Unused Pins (1/2)**

Pin Name	I/O Circuit Type	I/O	Recommended Connections of Unused Pins
P00/INTP0	8-K	I/O	Input : Individually connected to V_{SS0} via resistor Output: Open
P01/INTP1			
P02/INTP2/NMI			
P03/INTP3 to P05/INTP5			
P10/ANI0 to P17/ANI7	9	Input	Connected to V_{SS0} or V_{DD0}
P20/RxD1/SI1	10-I	I/O	Input : Individually connected to V_{SS0} via resistor Output: Open
P21/TxD1/SO1	10-J		
P22/ASCK1/$\overline{SCK1}$	10-I		
P23/PCL	10-J		
P24/BUZ			
P25/SDA0[Note]/SI0	10-I		
P26/SO0	10-J		
P27/SCL0[Note]/$\overline{SCK0}$	10-I		
P30/TO0 to P32/TO2	8-M		
P33/TI1, P34/TI2	8-K		
P35/TI00, P36/TI01	8-L		
P37/EXA	8-M		
P40/AD0 to P47/AD7	5-H		
P50/A8 to P57/A15			
P60/A16 to P63/A19			
P64/$\overline{RD}$			
P65/$\overline{WR}$			
P66/$\overline{WAIT}$			
P67/ASTB			
P70/RxD2/SI2	8-K		
P71/TxD2/SO2	8-L		
P72/ASCK2/$\overline{SCK2}$	8-K		

Note This function is available in μPD784255Y Subseries only.

Remark Because the circuit type numbers are standardized among the 78K Series products, they are not sequential in some models (i.e., some circuits are not provided).

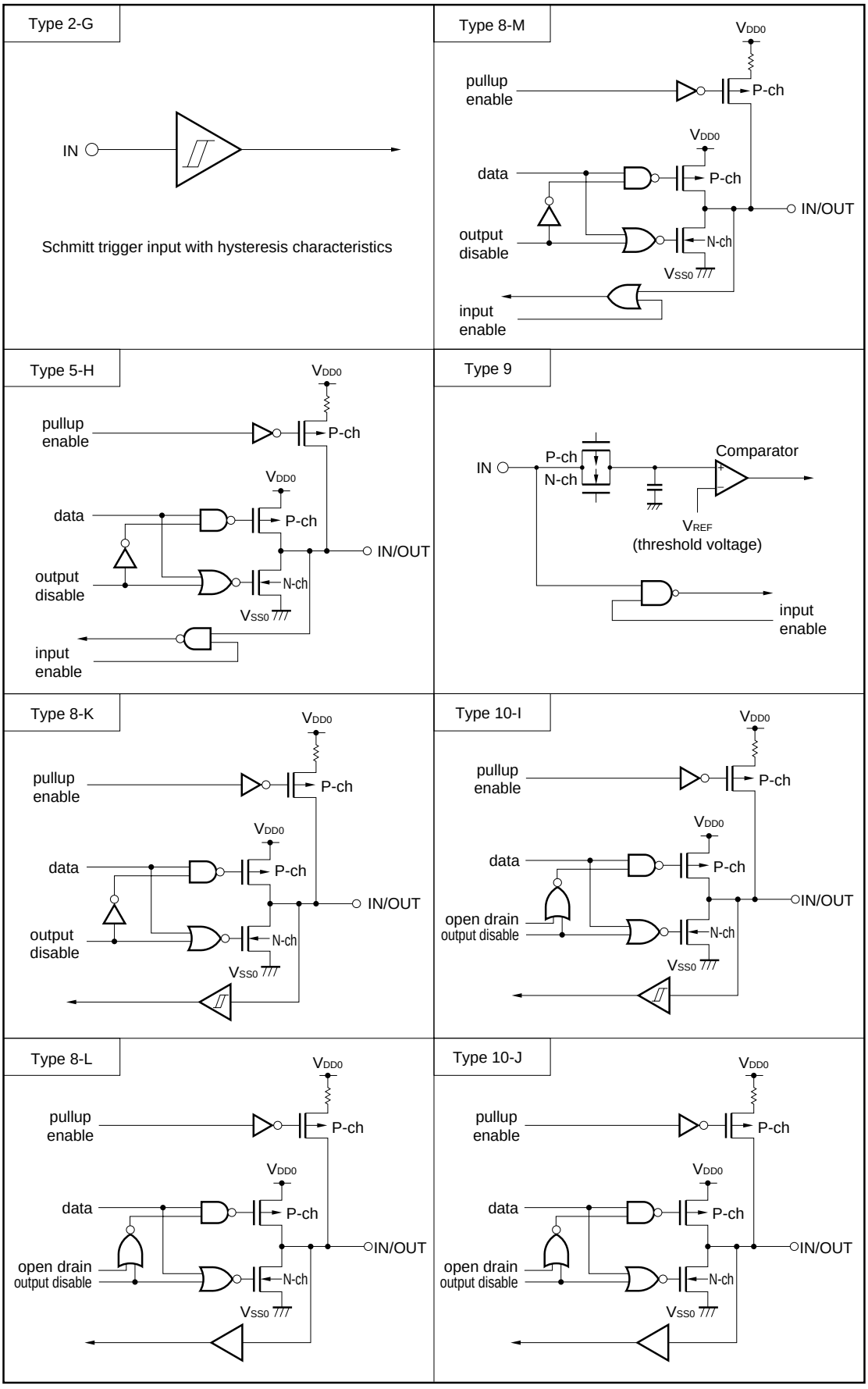
★ **Table 5-1. I/O Circuit Type of Respective Pins and Recommended Connections of Unused Pins (2/2)**

Pin Name	I/O Circuit Type	I/O	Recommended Connections of Unused Pins
P120/RTP0 to P127/RTP7	8-K	I/O	Input : Individually connected to V_{SS0} via resistor Output: Open
P130/ANO0, P131/ANO1	12-D		
$\overline{\text{RESET}}$	2-G	Input	–
XT1	16		Connected to V_{SS0}
XT2		–	Open
AV_{REF1}	–		Connected to V_{DD0}
AV_{DD}			
AV_{SS}			Connected to V_{SS0}
TEST/V_{PP}**Note**			Directly connected to V_{SS0}

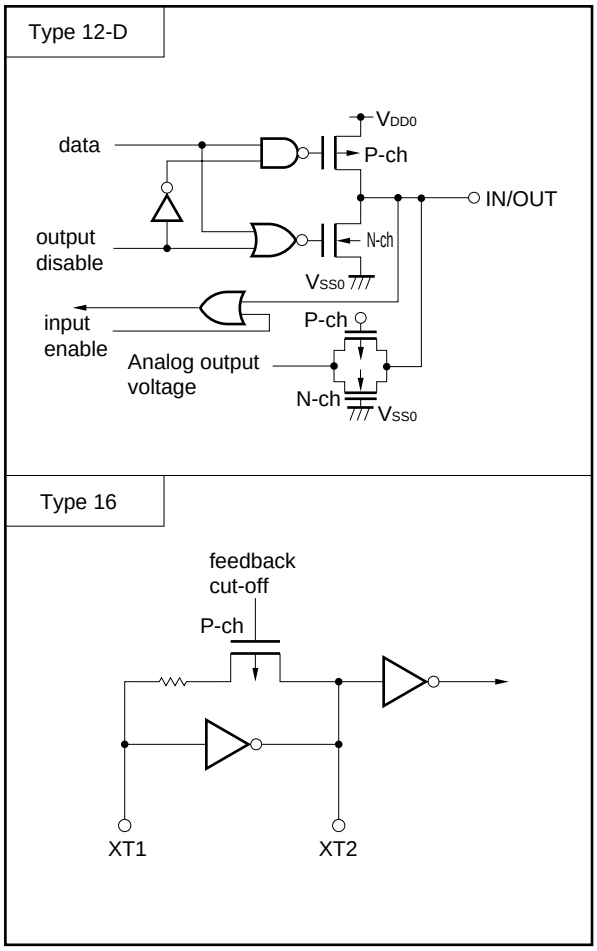
Note V_{PP} pin is available in μPD78F4225, 78F4255Y only.

Remark Because the circuit type numbers are standardized among the 78K Series products, they are not sequential in some models (i.e., some circuits are not provided).

★ **Figure 5-1. Types of Pin I/O Circuits (1/2)**



★ **Figure 5-1. Types of Pin I/O Circuits (2/2)**



6. CPU ARCHITECTURE

6.1 Memory Space

A memory space of 1 Mbyte can be accessed. Mapping of the internal data area (special function registers and internal RAM) can be specified the LOCATION instruction. The LOCATION instruction must be always executed after RESET cancellation, and must not be used more than once.

(1) When LOCATION 0H instruction is executed

• Internal memory

The internal data area and internal ROM area are mapped as follows:

Part Number	Internal Data Area	Internal ROM Area
μPD784224, μPD784224Y	0F100H to 0FFFFH	00000H to 0F0FFH 10000H to 17FFFH
μPD784225, μPD784225Y	0EE00H to 0FFFFH	00000H to 0EDFFH 10000H to 1FFFFH

Caution The following areas that overlap the internal data area of the internal ROM cannot be used when the LOCATION 0H instruction is executed.

Part Number	Unusable Area
μPD784224, μPD784224Y	0F100H to 0FFFFH (3,840 bytes)
μPD784225, μPD784225Y	0EE00H to 0FFFFH (4,608 bytes)

• External memory

The external memory is accessed in external memory expansion mode.

(2) When LOCATION 0FH instruction is executed

• Internal memory

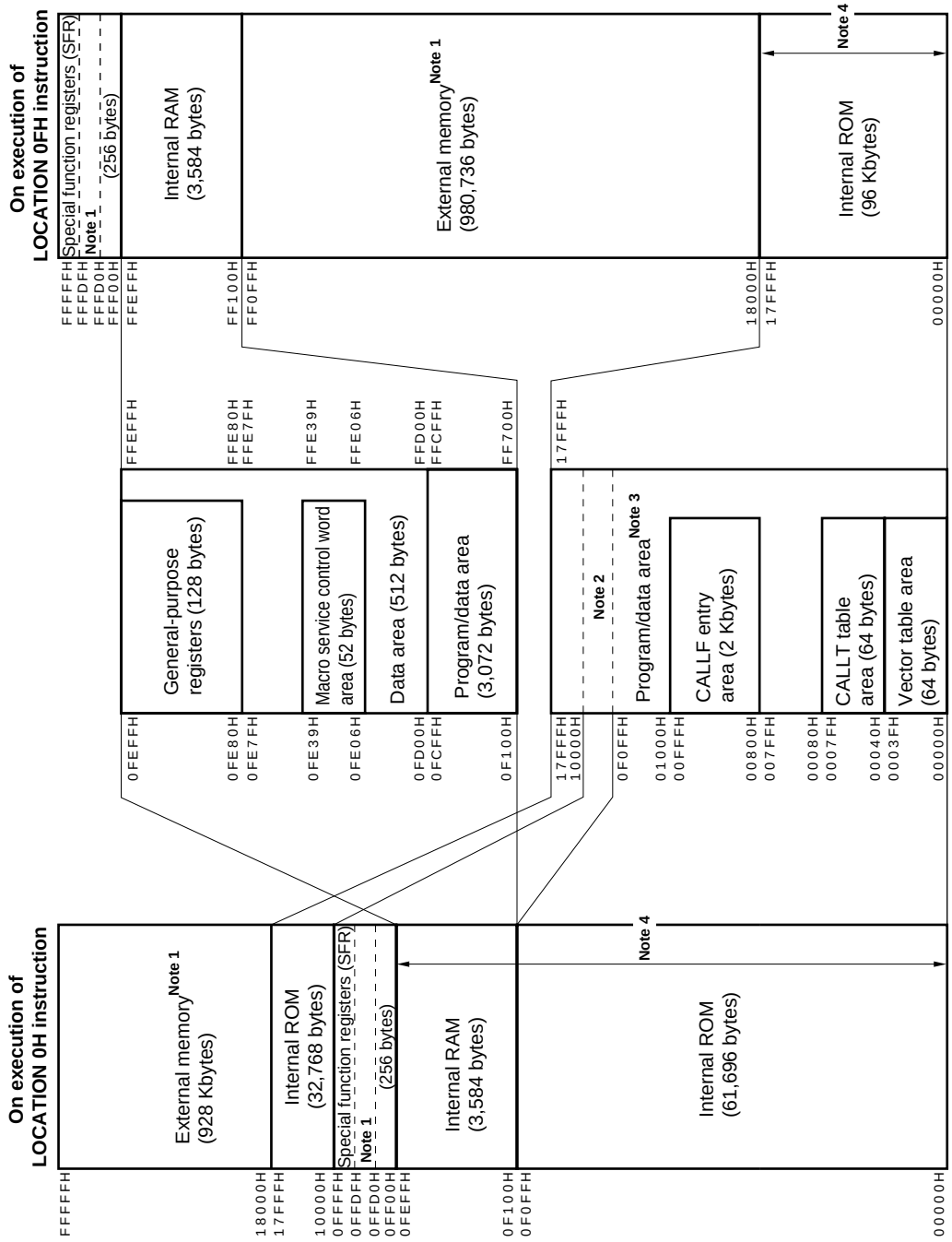
The internal data area and internal ROM area are mapped as follows:

Part Number	Internal Data Area	Internal ROM Area
μPD784224, μPD784224Y	FF100H to FFFFFH	00000H to 17FFFH
μPD784225, μPD784225Y	FEE00H to FFFFFH	00000H to 1FFFFH

• External memory

The external memory is accessed in external memory expansion mode.

Figure 6-1. Memory Map of μPD784224, 784224Y



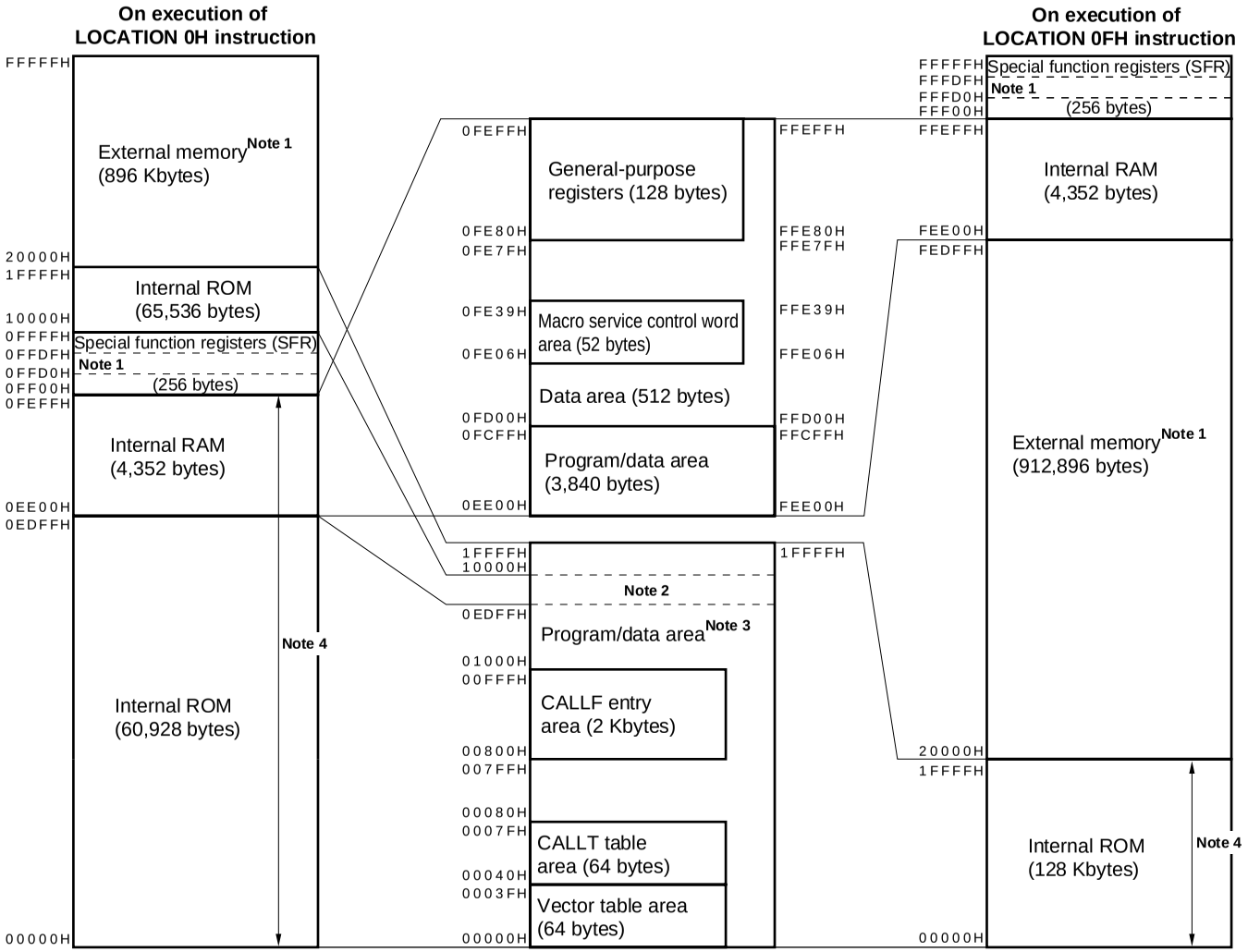
Notes 1. Accessed in external memory expansion mode.

2. This 3,840-byte area can be used as an internal ROM only when the LOCATION 0FH instruction is executed.

3. On execution of LOCATION 0H instruction: 94,464 bytes, on execution of LOCATION 0FH instruction: 98,304 bytes

4. Base area and entry area for reset or interrupt. However, the internal RAM area is not used as a reset entry area.

Figure 6-2. Memory Map of μPD784225, 784225Y



Notes 1. Accessed in external memory expansion mode.

2. This 4,608-byte area can be used as an internal ROM only when the LOCATION 0FH instruction is executed.

3. On execution of LOCATION 0H instruction: 126,464 bytes, on execution of LOCATION 0FH instruction: 131,072 bytes

4. Base area and entry area for reset or interrupt. However, the internal RAM area is not used as a reset entry area.

6.2 CPU Registers

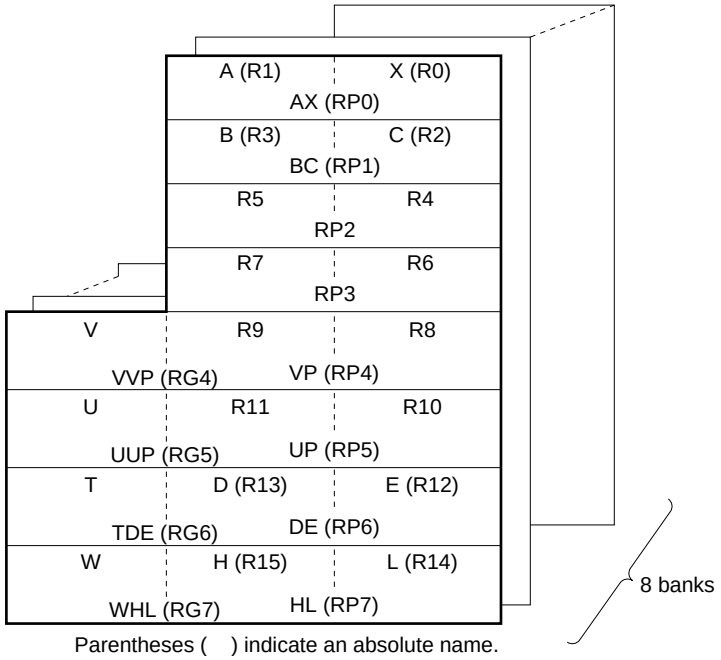
6.2.1 General-purpose registers

Sixteen 8-bit general-purpose registers are available. Two 8-bit registers can be also used in pairs as a 16-bit register. Of the 16-bit registers, four can be used in combination with an 8-bit register for address expansion as 24-bit address specification registers.

Eight banks of these registers are available which can be selected by using software or the context switching function.

The general-purpose registers except V, U, T, and W registers for address expansion are mapped to the internal RAM.

Figure 6-3. General-Purpose Register Format



Parentheses ( ) indicate an absolute name.

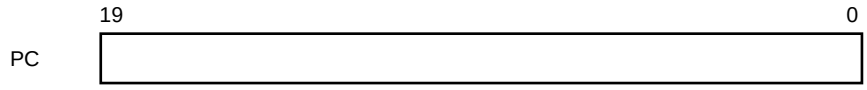
Caution Registers R4, R5, R6, R7, RP2, and RP3 can be used as X, A, C, B, AX, and BC registers, respectively, by setting the RSS bit of the PSW to 1. However, use this function only for recycling the program of the 78K/III Series.

6.2.2 Control registers

(1) Program counter (PC)

The program counter is a 20-bit register whose contents are automatically updated when the program is executed.

Figure 6-4. Program Counter (PC) Format



(2) Program status word (PSW)

This register holds the statuses of the CPU. Its contents are automatically updated when the program is executed.

Figure 6-5. Program Status Word (PSW) Format

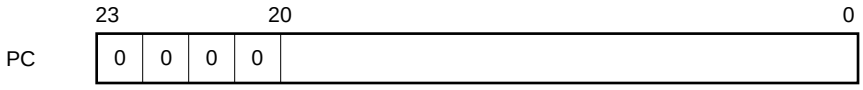
		15	14	13	12	11	10	9	8
PSW	PSWH	UF	RBS2	RBS1	RBS0	–	–	–	–
		7	6	5	4	3	2	1	0
	PSWL	S	Z	RSS[Note]	AC	IE	P/V	0	CY

Note This flag is provided to maintain compatibility with the 78K/III Series. Be sure to clear this flag to 0, except when the software for the 78K/III Series is used.

(3) Stack pointer (SP)

This is a 24-bit pointer that holds the first address of the stack. Be sure to write 0 to the higher 4 bits of this pointer.

Figure 6-6. Stack Pointer (SP) Format



6.2.3 Special function registers (SFRs)

The special function registers, such as the mode registers and control registers of the internal peripheral hardware, are registers to which special functions are allocated. These registers are mapped to a 256-byte space of addresses 0FF00H to 0FFFFH[Note].

Note On execution of the LOCATION 0H instruction. FFF00H to FFFFFH on execution of the LOCATION 0FH instruction.

Caution Do not access an address in this area to which no SFR is allocated. If such an address is accessed by mistake, the μPD784225 may be in the deadlock status. This deadlock status can be cleared only by inputting the $\overline{\text{RESET}}$ signal.

Table 6-1 lists the special function registers (SFRs). The meanings of the symbols in this table are as follows:

- Symbol ..... Symbol indicating an SFR. This symbol is reserved for NEC's assembler (RA78K4). It can be used an sfr variable by the #pragma sfr directive with the C compiler (CC78K4).

- R/W ..... Indicates whether the SFR is read-only, write-only, or read/write.
  R/W : Read/write
  R : Read-only
  W : Write-only

- Bit units for manipulation .. Bit units in which the value of the SFR can be manipulated.
  SFRs that can be manipulated in 16-bit units can be described as the operand sfrp of an instruction. To specify the address of this SFR, describe an even address.
  SFRs that can be manipulated in 1-bit units can be described as the operand of a bit manipulation instruction.

- At reset ..... Indicates the status of the register when the $\overline{\text{RESET}}$ signal has been input.

Table 6-1. Special Function Register (SFR) List (1/4)

Address[Note 1]	Special Function Register (SFR) Name	Symbol	R/W	Bit Units for Manipulation			At Reset
				1 Bit	8 Bits	16 Bits	
0FF00H	Port 0	P0	R/W	○	○	—	00H[Note 2]
0FF01H	Port 1	P1	R	○	○	—	
0FF02H	Port 2	P2	R/W	○	○	—	
0FF03H	Port 3	P3		○	○	—	
0FF04H	Port 4	P4		○	○	—	
0FF05H	Port 5	P5		○	○	—	
0FF06H	Port 6	P6		○	○	—	
0FF07H	Port 7	P7		○	○	—	
0FF0CH	Port 12	P12		○	○	—	
0FF0DH	Port 13	P13		○	○	—	
0FF10H	16-bit timer counter	TM0	R	—	—	○	0000H
0FF11H							
0FF12H	Capture/compare register 00 (16-bit timer/counter)	CR00	R/W	—	—	○	
0FF13H							
0FF14H	Capture/compare register 01 (16-bit timer/counter)	CR01		—	—	○	
0FF15H							
0FF16H	Capture/compare control register 0	CRC0		○	○	—	00H
0FF18H	16-bit timer mode control register	TMC0		○	○	—	
0FF1AH	16-bit timer output control register	TOC0		○	○	—	
0FF1CH	Prescaler mode register 0	PRM0		○	○	—	
0FF20H	Port 0 mode register	PM0		○	○	—	FFH
0FF22H	Port 2 mode register	PM2		○	○	—	
0FF23H	Port 3 mode register	PM3		○	○	—	
0FF24H	Port 4 mode register	PM4		○	○	—	
0FF25H	Port 5 mode register	PM5		○	○	—	
0FF26H	Port 6 mode register	PM6		○	○	—	
0FF27H	Port 7 mode register	PM7		○	○	—	
0FF2CH	Port 12 mode register	PM12		○	○	—	
0FF2DH	Port 13 mode register	PM13		○	○	—	
0FF30H	Pull-up resistor option register 0	PU0		○	○	—	00H
0FF32H	Pull-up resistor option register 2	PU2		○	○	—	
0FF33H	Pull-up resistor option register 3	PU3		○	○	—	
0FF37H	Pull-up resistor option register 7	PU7		○	○	—	
0FF3CH	Pull-up resistor option register 12	PU12		○	○	—	
0FF40H	Clock output control register	CKS		○	○	—	

Notes 1. When the LOCATION 0H instruction is executed. Add “F0000H” to this value when the LOCATION 0FH instruction is executed.

2. Because each port is initialized to input mode at reset, “00H” is not actually read. The output latch is initialized to “0”.

Table 6-1. Special Function Register (SFR) List (2/4)

Address[Note]	Special Function Register (SFR) Name	Symbol		R/W	Bit Units for Manipulation			At Reset
					1 Bit	8 Bits	16 Bits	
0FF42H	Port function control register	PF2		R/W	○	○	—	00H
0FF4EH	Pull-up resistor option register	PUO			○	○	—	
0FF50H	8-bit timer counter 1	TM1	TM1W	R	—	○	○	0000H
0FF51H	8-bit timer counter 2	TM2			—	○		
0FF52H	Compare register 10 (8-bit timer/counter 1)	CR10	CR1W	R/W	—	○	○	
0FF53H	Compare register 20 (8-bit timer/counter 2)	CR20			—	○		
0FF54H	8-bit timer mode control register 1	TMC1	TMC1W		○	○	○	
0FF55H	8-bit timer mode control register 2	TMC2			○	○		
0FF56H	Prescaler mode register 1	PRM1	PRM1W		○	○	○	
0FF57H	Prescaler mode register 2	PRM2			○	○		
0FF60H	8-bit timer counter 5	TM5	TM5W	R	—	○	○	
0FF61H	8-bit timer counter 6	TM6			—	○		
0FF64H	Compare register 50 (8-bit timer/counter 5)	CR50	CR5W	R/W	—	○	○	
0FF65H	Compare register 60 (8-bit timer/counter 6)	CR60			—	○		
0FF68H	8-bit timer mode control register 5	TMC5	TMC5W		○	○	○	
0FF69H	8-bit timer mode control register 6	TMC6			○	○		
0FF6CH	Prescaler mode register 5	PRM5	PRM5W		○	○	○	
0FF6DH	Prescaler mode register 6	PRM6			○	○		
0FF70H	Asynchronous serial interface mode register 1	ASIM1			○	○	—	00H
0FF71H	Asynchronous serial interface mode register 2	ASIM2			○	○	—	
0FF72H	Asynchronous serial interface status register 1	ASIS1		R	○	○	—	
0FF73H	Asynchronous serial interface status register 2	ASIS2			○	○	—	
0FF74H	Transmit shift register 1	TXS1		W	—	○	—	FFH
	Receive buffer register 1	RXB1		R	—	○	—	
0FF75H	Transmit shift register 2	TXS2		W	—	○	—	
	Receive buffer register 2	RXB2		R	—	○	—	
0FF76H	Baud rate generator control register 1	BRGC1		R/W	○	○	—	00H
0FF77H	Baud rate generator control register 2	BRGC2			○	○	—	
0FF7AH	Oscillation mode select register	CC			○	○	—	
0FF80H	A/D converter mode register	ADM			○	○	—	
0FF81H	A/D converter input select register	ADIS			○	○	—	
0FF83H	A/D conversion result register	ADCR		R	—	○	—	Undefined
0FF84H	D/A conversion value setting register 0	DACS0		R/W	○	○	—	00H
0FF85H	D/A conversion value setting register 1	DACS1			○	○	—	
0FF86H	D/A converter mode register 0	DAM0			○	○	—	
0FF87H	D/A converter mode register 1	DAM1			○	○	—	

Note When the LOCATION 0H instruction is executed. Add “F0000H” to this value when the LOCATION 0FH instruction is executed.

Table 6-1. Special Function Register (SFR) List (3/4)

Address[Note 1]	Special Function Register (SFR) Name	Symbol		R/W	Bit Units for Manipulation			At Reset
					1 Bit	8 Bits	16 Bits	
0FF88H	ROM correction control register	CORC		R/W	○	○	—	00H
0FF89H	ROM correction address pointer H	CORAH			—	○	—	
0FF8AH	ROM correction address pointer L	CORAL			—	—	○	0000H
0FF8BH								
0FF8DH	External access status enable register	EXAE			○	○	—	00H
0FF90H	Serial operation mode register 0	CSIM0			○	○	—	
0FF91H	Serial operation mode register 1	CSIM1			○	○	—	
0FF92H	Serial operation mode register 2	CSIM2			○	○	—	
0FF94H	Serial I/O shift register 0	SIO0			—	○	—	
0FF95H	Serial I/O shift register 1	SIO1			—	○	—	
0FF96H	Serial I/O shift register 2	SIO2			—	○	—	
0FF98H	Real-time output buffer register L	RTBL			—	○	—	
0FF99H	Real-time output buffer register H	RTBH			—	○	—	
0FF9AH	Real-time output port mode register	RTPM			○	○	—	
0FF9BH	Real-time output port control register	RTPC			○	○	—	
0FF9CH	Watch timer mode control register	WTM			○	○	—	
0FFA0H	External interrupt rising edge enable register	EGP0			○	○	—	
0FFA2H	External interrupt falling edge enable register	EGN0			○	○	—	
0FFA8H	In-service priority register	ISPR		R	○	○	—	
0FFA9H	Interrupt select control register	SNMI		R/W	○	○	—	
0FFAAH	Interrupt mode control register	IMC			○	○	—	80H
0FFACH	Interrupt mask flag register 0L	MK0L	MK0		○	○	○	FFFFH
0FFADH	Interrupt mask flag register 0H	MK0H			○	○		
0FFAEH	Interrupt mask flag register 1L	MK1L	MK1		○	○	○	
0FFAFH	Interrupt mask flag register 1H	MK1H			○	○		
0FFB0H	I^2C bus control register[Note 2]	IICCL0			○	○	—	00H
0FFB2H	Prescaler mode register for serial clock	SPRM0			○	○	—	
0FFB4H	Slave address register	SVA0			○	○	—	
0FFB6H	I^2C bus status register[Note 2]	IICS0		R	○	○	—	
0FFB8H	Serial shift register	IIC0		R/W	○	○	—	
0FFC0H	Standby control register	STBC			—	○	—	30H
0FFC2H	Watchdog timer mode register	WDM			—	○	—	00H
0FFC4H	Memory expansion mode register	MM			○	○	—	20H
0FFC7H	Programmable wait control register 1	PWC1			○	○	—	AAH
0FFC8H	Programmable wait control register 2	PWC2		W	—	—	○	AAAAH
00FFCEH	Clock status register	PCS		R	○	○	—	32H
0FFCFH	Oscillation stabilization time specification register	OSTS		R/W	○	○	—	00H
0FFD0H to 0FFDFH	External SFR area	—			○	○	—	—

Notes 1. When the LOCATION 0H instruction is executed. Add “F0000H” to this value when the LOCATION 0FH instruction is executed.

2. μPD784225Y Subseries only

Table 6-1. Special Function Register (SFR) List (4/4)

Address[Note]	Special Function Register (SFR) Name	Symbol	R/W	Bit Units for Manipulation			At Reset
				1 Bit	8 Bits	16 Bits	
0FFE0H	Interrupt control register (INTWDTM)	WDTIC	R/W	○	○	—	43H
0FFE1H	Interrupt control register (INTP0)	PIC0		○	○	—	
0FFE2H	Interrupt control register (INTP1)	PIC1		○	○	—	
0FFE3H	Interrupt control register (INTP2)	PIC2		○	○	—	
0FFE4H	Interrupt control register (INTP3)	PIC3		○	○	—	
0FFE5H	Interrupt control register (INTP4)	PIC4		○	○	—	
0FFE6H	Interrupt control register (INTP5)	PIC5		○	○	—	
0FFE8H	Interrupt control register (INTIIC0/INTCSI0)	CSIIC0		○	○	—	
0FFE9H	Interrupt control register (INTSER1)	SERIC1		○	○	—	
0FFEAH	Interrupt control register (INTSR1/INTCSI1)	SRIC1		○	○	—	
0FFEBH	Interrupt control register (INTST1)	STIC1		○	○	—	
0FFECH	Interrupt control register (INTSER2)	SERIC2		○	○	—	
0FFEDH	Interrupt control register (INTSR2/INTCSI2)	SRIC2		○	○	—	
0FFEEH	Interrupt control register (INTST2)	STIC2		○	○	—	
0FFEFH	Interrupt control register (INTTM3)	TMIC3		○	○	—	
0FFF0H	Interrupt control register (INTTM00)	TMIC00		○	○	—	
0FFF1H	Interrupt control register (INTTM01)	TMIC01		○	○	—	
0FFF2H	Interrupt control register (INTTM1)	TMIC1		○	○	—	
0FFF3H	Interrupt control register (INTTM2)	TMIC2		○	○	—	
0FFF4H	Interrupt control register (INTAD)	ADIC		○	○	—	
0FFF5H	Interrupt control register (INTTM5)	TMIC5		○	○	—	
0FFF6H	Interrupt control register (INTTM6)	TMIC6		○	○	—	
0FFF9H	Interrupt control register (INTWT)	WTIC		○	○	—	

Note When the LOCATION 0H instruction is executed. Add “F0000H” to this value when the LOCATION 0FH instruction is executed.

7. PERIPHERAL HARDWARE FUNCTIONS

7.1 Ports

The ports shown in Figure 7-1 are provided to make various control operations possible. Table 7-1 shows the function of each port. Ports 0, 2 to 7, and 12 can be connected to internal pull-up resistors by software when inputting.

Figure 7-1. Port Configuration

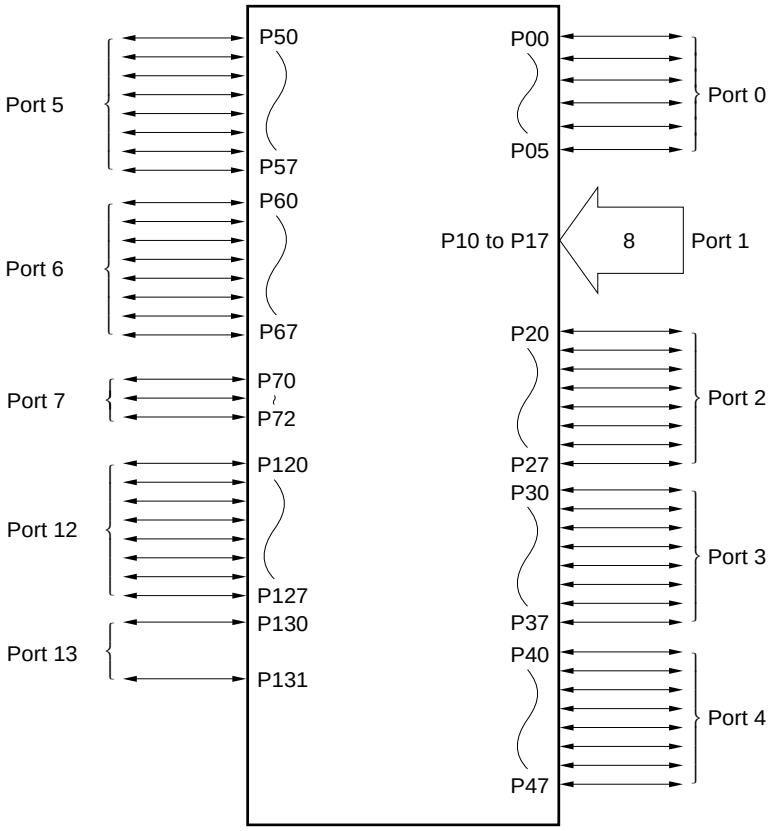


Table 7-1. Port Functions

Port Name	Pin Name	Function	Specification of Pull-up Resistor Connection by Software
Port 0	P00 to P05	• Can be set in input or output mode bit-wise	Can be specified bit-wise
Port 1	P10 to P17	• Input port	—
Port 2	P20 to P27	• Can be set in input or output mode bit-wise	Can be specified bit-wise
Port 3	P30 to P37	• Can be set in input or output mode bit-wise	Can be specified bit-wise
Port 4	P40 to P47	• Can be set in input or output mode bit-wise • Can directly drive LEDs	Can be specified in 1-port units
Port 5	P50 to P57	• Can be set in input or output mode bit-wise • Can directly drive LEDs	Can be specified in 1-port units
Port 6	P60 to P67	• Can be set in input or output mode bit-wise	Can be specified in 1-port units
Port 7	P70 to P72	• Can be set in input or output mode bit-wise	Can be specified bit-wise
Port 12	P120 to P127	• Can be set in input or output mode bit-wise	Can be specified bit-wise
Port 13	P130, P131	• Can be set in input or output mode bit-wise	—

7.2 Clock Generator

An on-chip clock generator necessary for operation is provided. This clock generator has a frequency divider. If high-speed operation is not necessary, the internal operating frequency can be lowered by the frequency divider to reduce the current consumption.

★ **Figure 7-2. Block Diagram of Clock Generator**

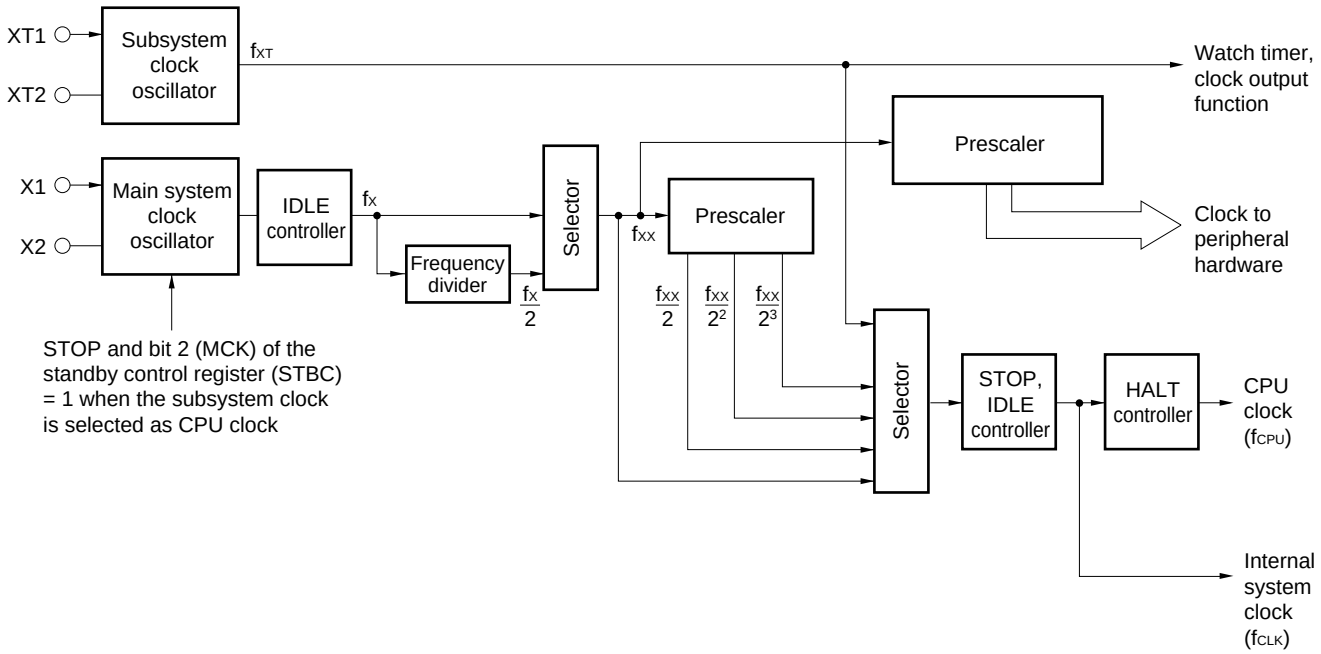
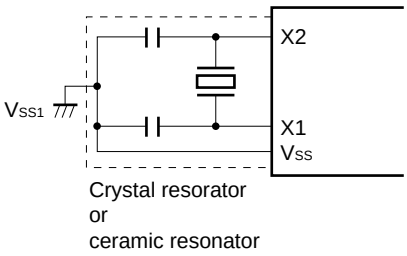


Figure 7-3. Example of Using Main System Clock Oscillator

(1) Crystal/ceramic oscillation



(2) External clock

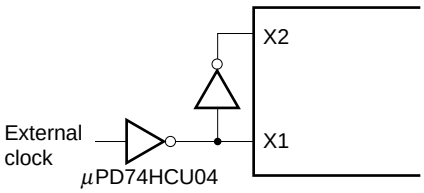
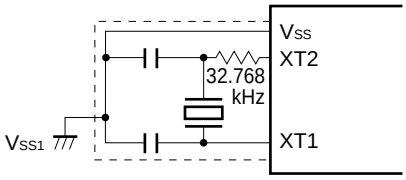
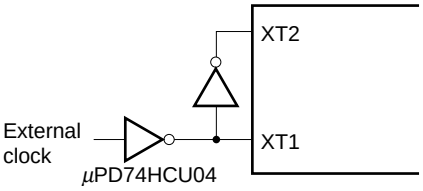


Figure 7-4. Example of Using Subsystem Clock Oscillator

(1) Crystal oscillation



(2) External clock



Caution When using the main system clock and subsystem clock oscillator, wire the dotted portions in Figures 7-3 and 7-4 as follows to avoid adverse influence from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with other signal lines.**
- **Do not route the wiring in the vicinity of lines through which a high alternating current flows.**
- **Always keep the potential at the ground point of the capacitor in the oscillator the same as V_{SS1}. Do not ground to a ground pattern through which a high current flows.**
- **Do not extract signals from the oscillator.**

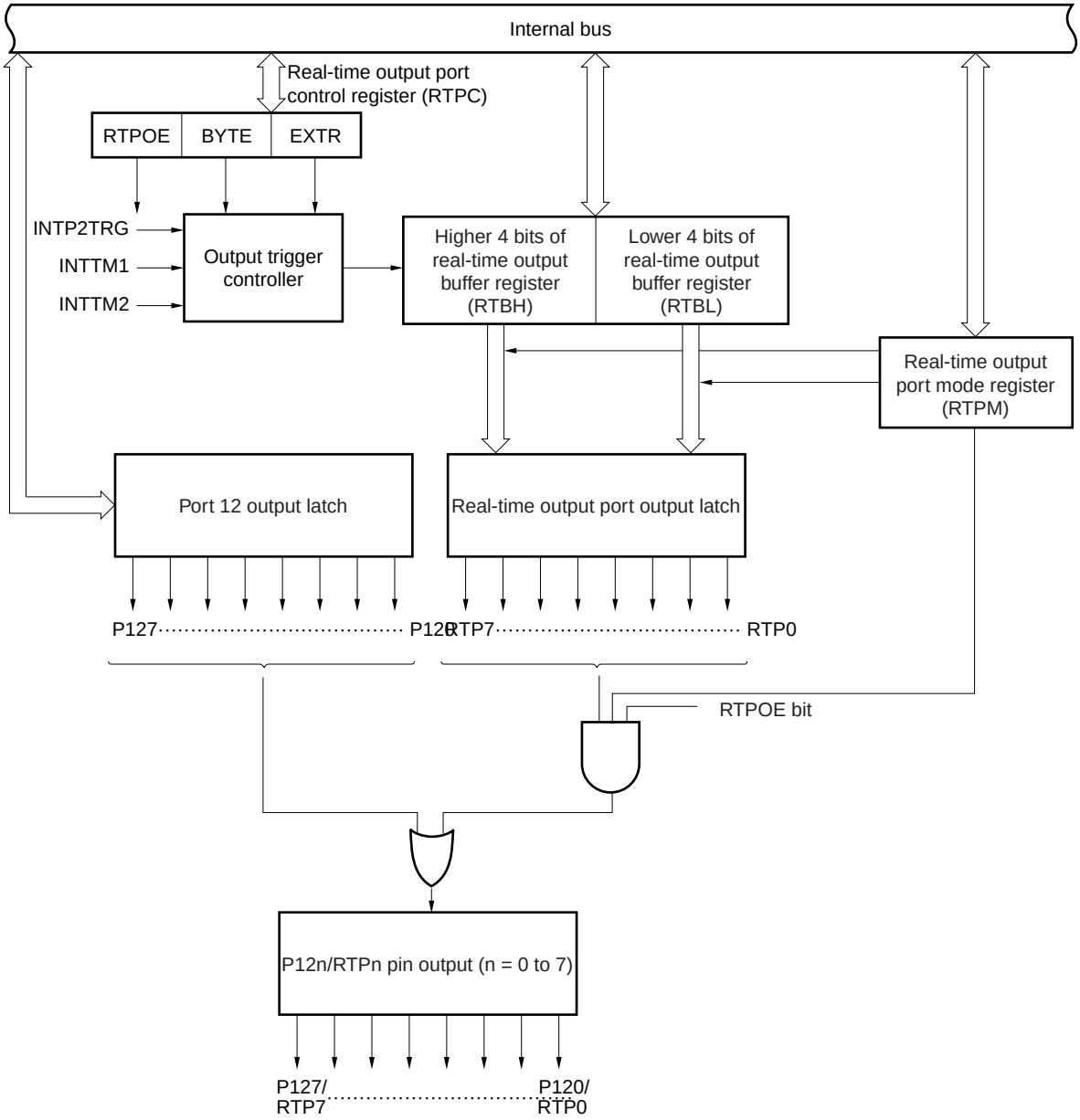
Note that the subsystem clock oscillator has a low amplification factor to reduce the current consumption.

7.3 Real-Time Output Port

The real-time output function is to transfer data set in advance to the real-time output buffer register to the output latch as soon as the timer interrupt or external interrupt has occurred in order to output the data to an external device. The pins that output the data to the external device constitute a port called a real-time output port.

Because the real-time output port can output signals without jitter, it is ideal for controlling a stepping motor.

Figure 7-5. Block Diagram of Real-Time Output Port



7.4 Timer

One unit of 16-bit timers/event counters, two units of timers/event counters, and two 8-bit timers are provided.

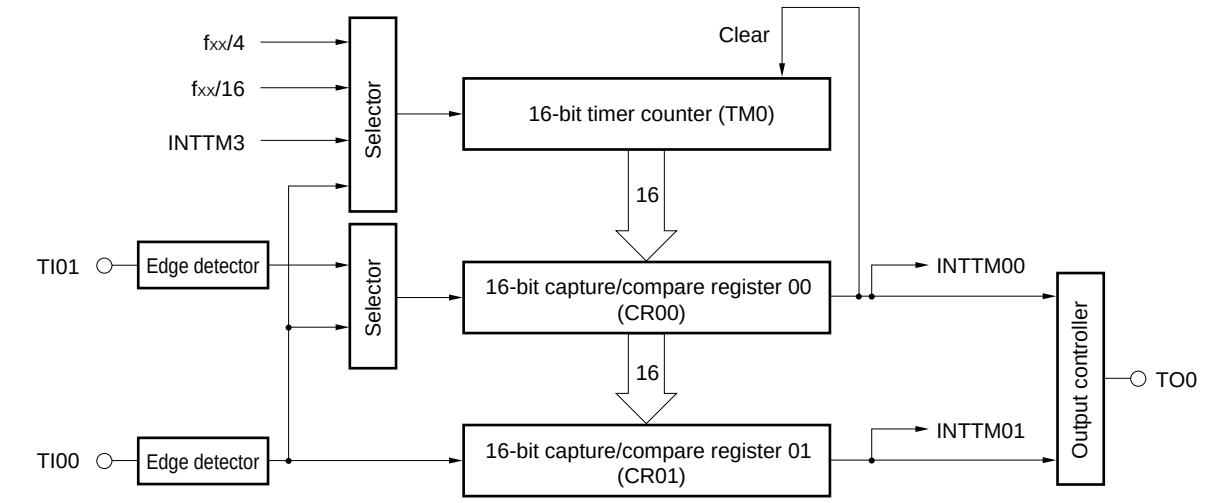
Because a total of six interrupt requests are supported, these timers/counters and timer can be used as six units of timers/counters.

Table 7-2. Operations of Timers

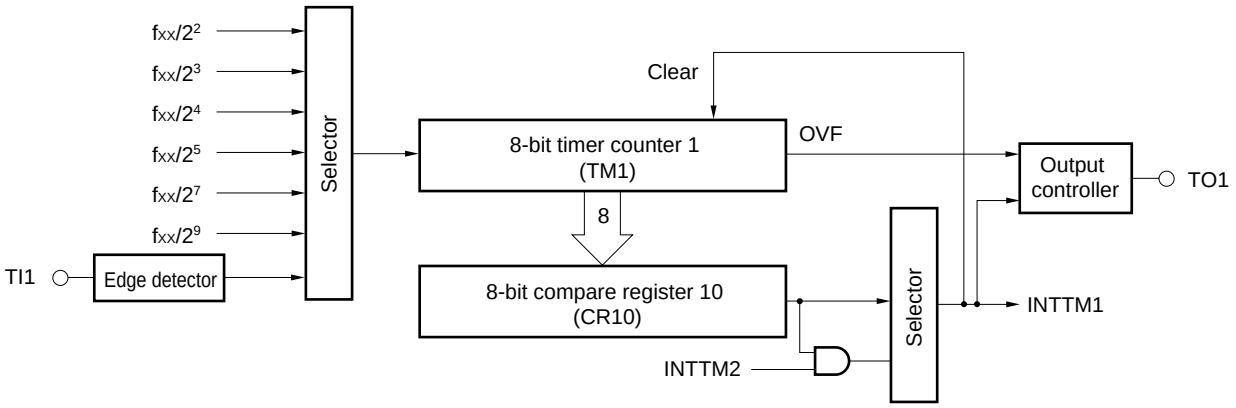
Item \ Name		16-Bit Timer/Event Counter	8-Bit Timer/Event Counter 1	8-Bit Timer/Event Counter 2	8-Bit Timer 5	8-Bit Timer 6
Count width	8 bits	—	○	○	○	○
	16 bits	○	○		○	
Operation mode	Interval timer	1ch	1ch	1ch	1ch	1ch
	External event counter	○	○	○	—	—
Function	Timer output	1ch	1ch	1ch	—	—
	PPG output	○	—	—	—	—
	PWM output	○	○	○	—	—
	Square wave output	○	○	○	—	—
	One-shot pulse output	○	—	—	—	—
	Pulse width measurement	2 inputs	—	—	—	—
	Number of interrupt requests	2	1	1	1	1

Figure 7-6. Block Diagram of Timers (1/2)

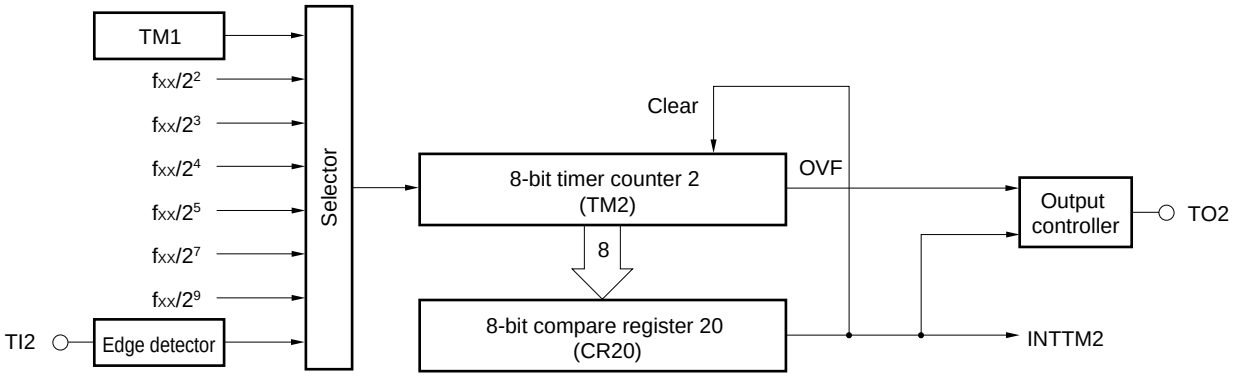
16-bit timer/event counter



8-bit timer/event counter 1



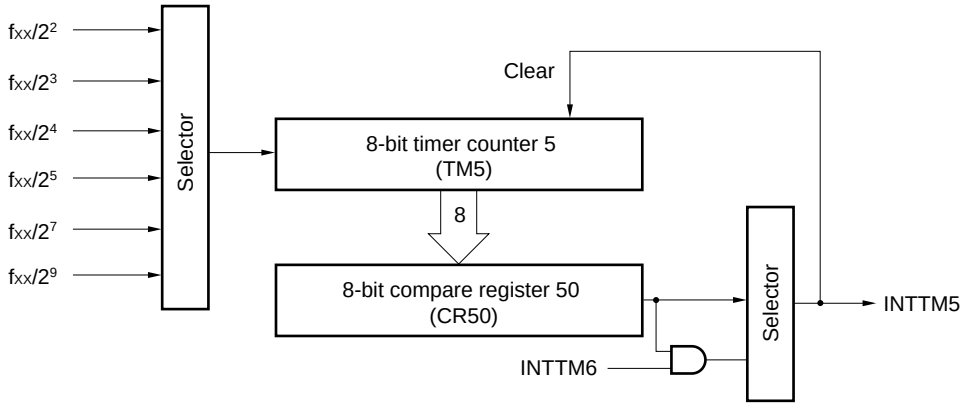
8-bit timer/event counter 2



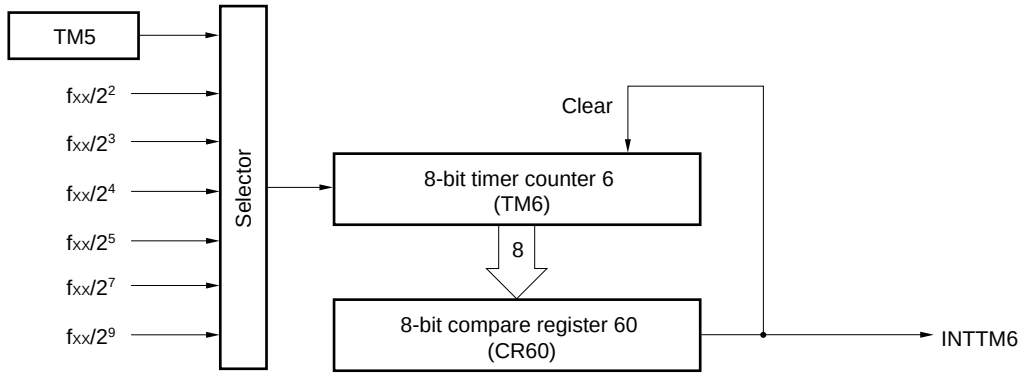
Remark OVF: Overflow flag

Figure 7-6. Block Diagram of Timers (2/2)

8-bit timer 5



8-bit timer 6



7.5 A/D Converter

An A/D converter converts an analog input variable into a digital signal. This microcontroller is provided with an A/D converter with a resolution of 8 bits and 8 channels (ANI0 to ANI7).

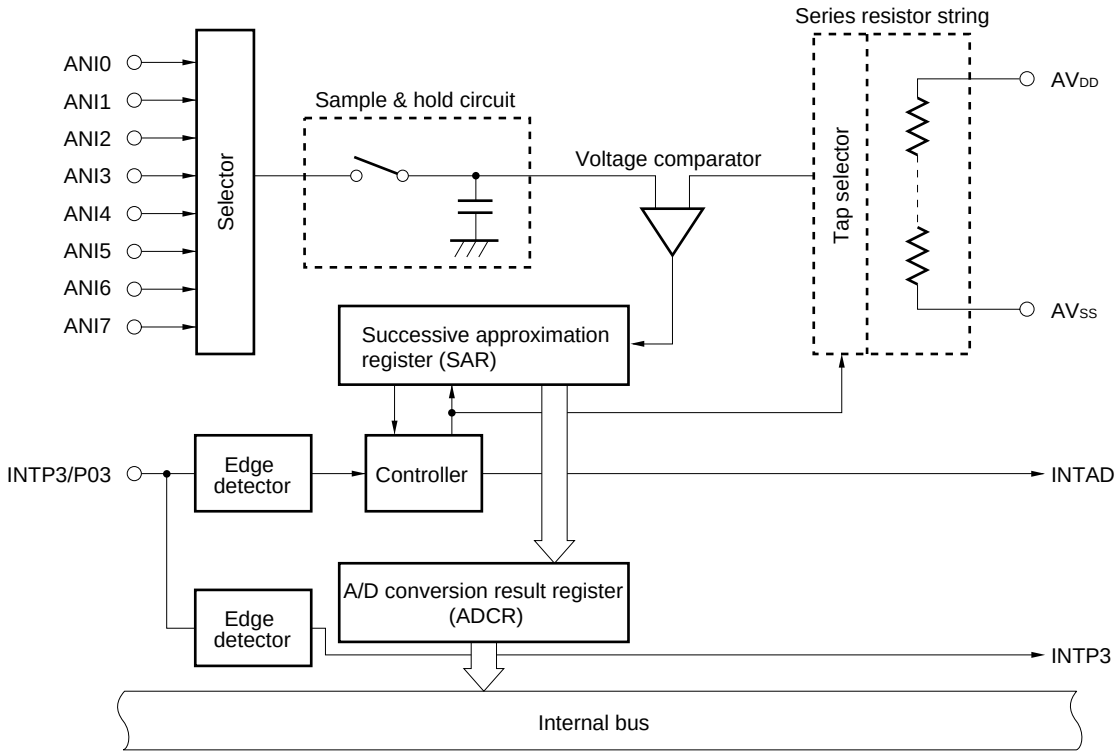
This A/D converter is of successive approximation type and the result of conversion is stored to an 8-bit A/D conversion result register (ADCR).

The A/D converter can be started in the following two ways:

- Hardware start
  Conversion is started by trigger input (P03).
- Software start
  Conversion is started by setting the A/D converter mode register.

One analog input channel is selected from ANI0 to ANI7 for A/D conversion. When A/D conversion is started by means of hardware start, conversion is stopped after it has been completed. When conversion is started by means of software start, A/D conversion is repeatedly executed, and each time conversion has been completed, an interrupt request (INTAD) is generated.

Figure 7-7. Block Diagram of A/D Converter



7.6 D/A Converter

A D/A converter converts an input digital signal into an analog voltage. This microcontroller is provided with a voltage output type D/A converter with a resolution of 8 bits and two channels.

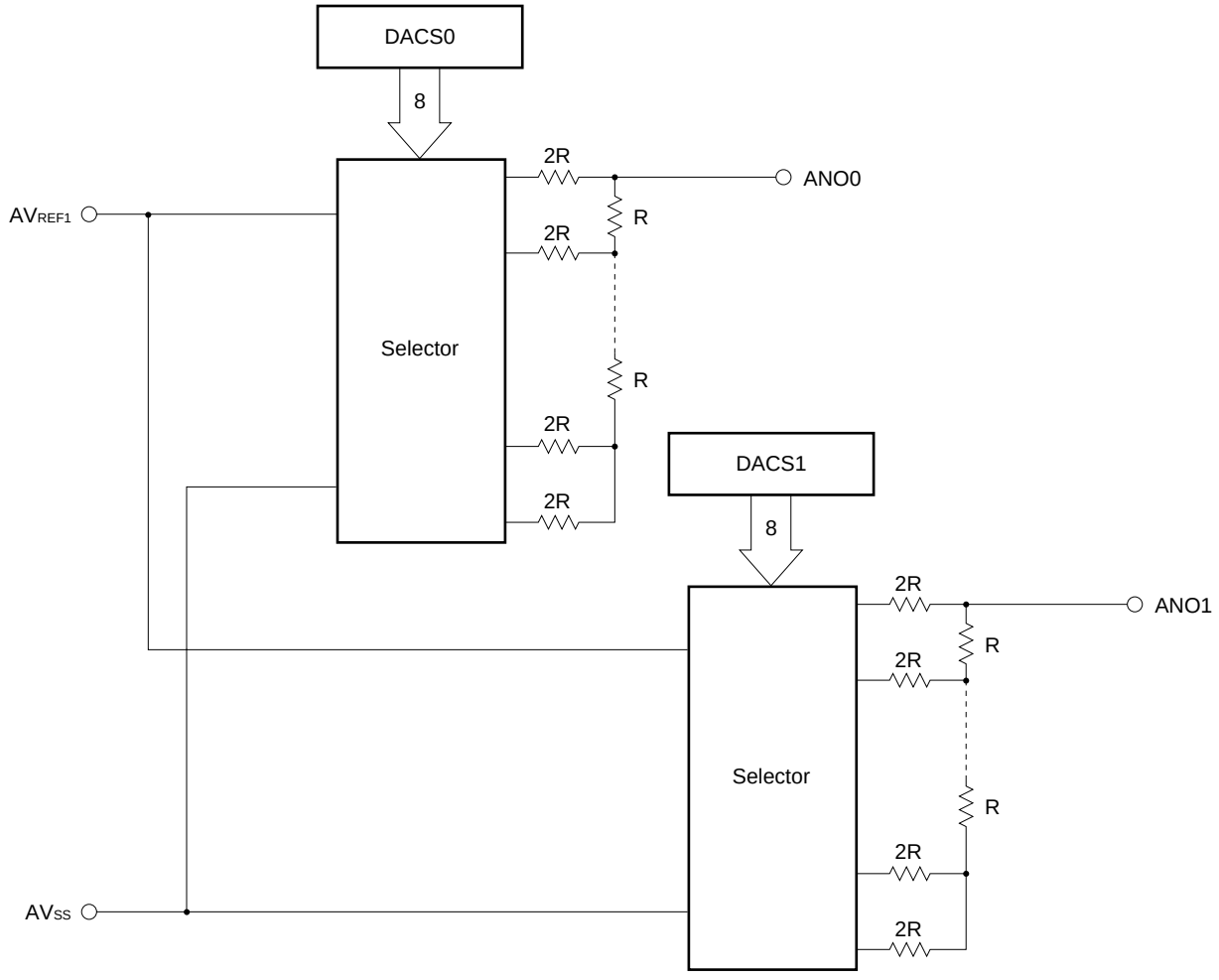
The conversion method is of R-2R resistor ladder type.

D/A conversion is started by setting DACE0 of the D/A converter mode register 0 (DAM0) and DACE1 of the D/A converter mode register 1 (DAM1).

The D/A converter operates in the following two modes:

- Normal mode
  The converter outputs an analog voltage immediately after it has completed D/A conversion.
- Real-time output mode
  The converter outputs an analog voltage in synchronization with an output trigger after it has completed D/A conversion.

Figure 7-8. Block Diagram of D/A Converter



7.7 Serial Interface

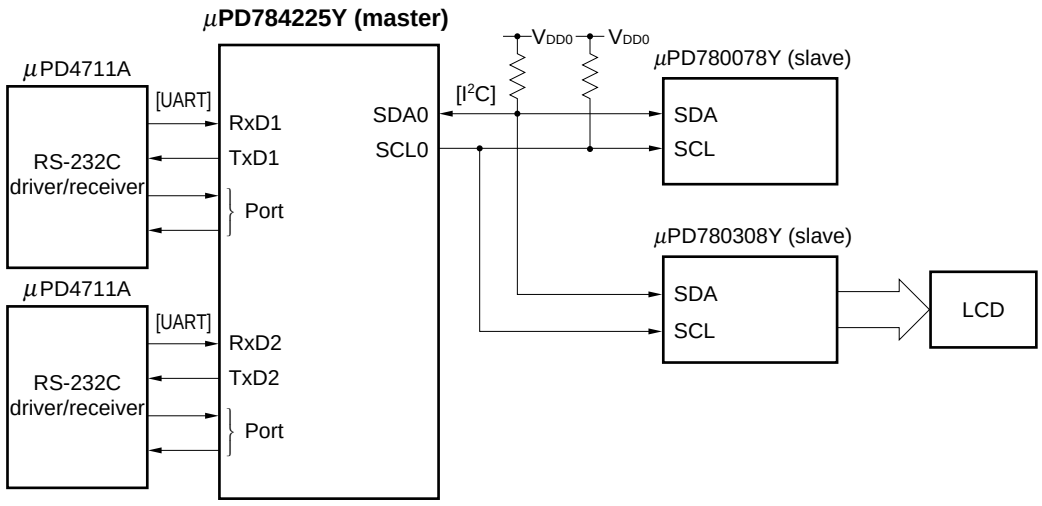
Three independent serial interface channels are provided.

- Asynchronous serial interface (UART)/3-wire serial I/O (IOE) × 2
- Clocked serial interface (CSI) × 1
  - 3-wire serial I/O (IOE)
  - I^2C bus interface (I^2C) (μPD784225Y Subseries only)

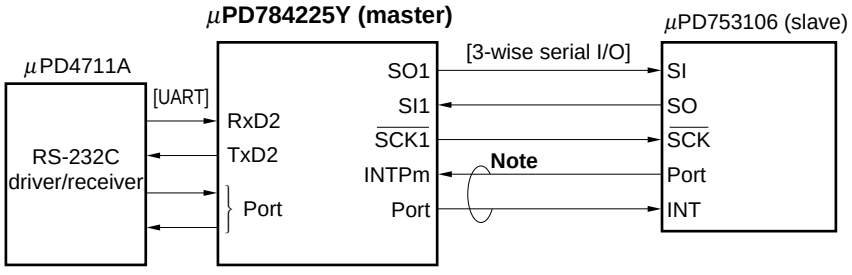
Therefore, communication with an external system and local communication within the system can be simultaneously executed (see **Figure 7-9**).

Figure 7-9. Example of Serial Interface

(a) UART + I^2C



(b) UART + 3-wire serial I/O



Note Handshake line

7.7.1 Asynchronous serial interface/3-wire serial I/O (UART/IOE)

Two channels of serial interfaces that can select an asynchronous serial interface mode and 3-wire serial I/O mode are provided.

(1) Asynchronous serial interface mode

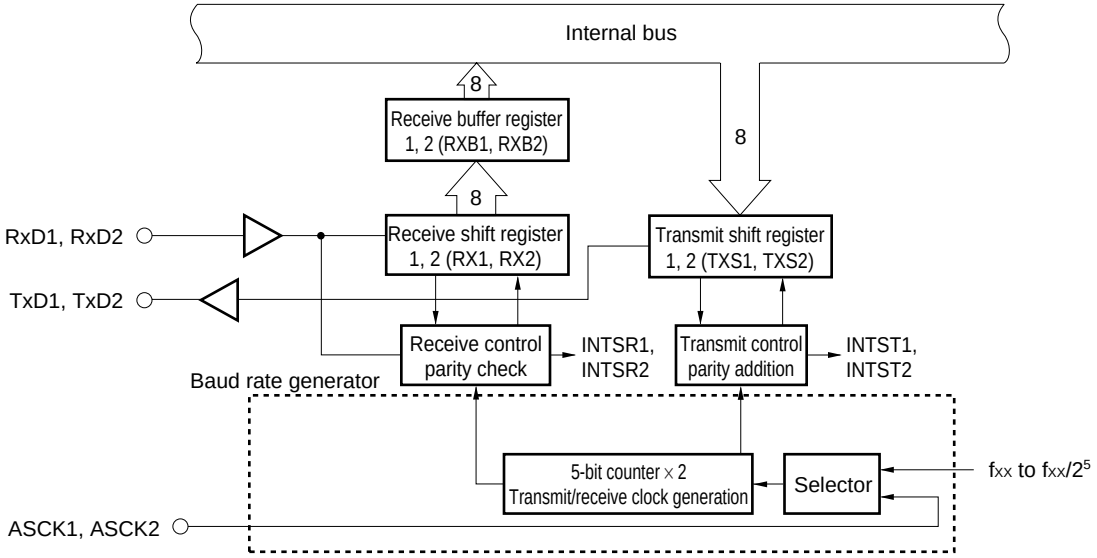
In this mode, data of 1 byte following the start bit is transferred or received.

Because an on-chip baud rate generator is provided, a wide range of baud rates can be set.

Moreover, the clock input to the ASCK pin can be divided to define a baud rate.

When the baud rate generator is used, a baud rate conforming to the MIDI standard (31.25 kbps) can be also obtained.

★ **Figure 7-10. Block Diagram in Asynchronous Serial Interface Mode**

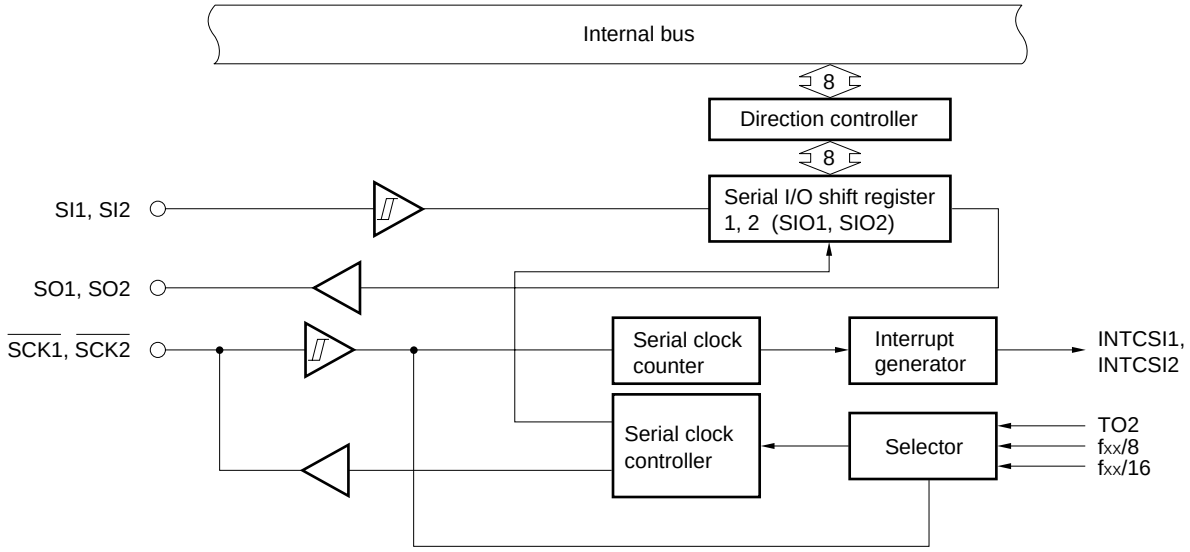


(2) 3-wire serial I/O mode

In this mode, the master device starts transfer by making the serial clock active and transfers 1-byte data in synchronization with this clock.

This mode is used to communicate with a device having the conventional clocked serial interface. Basically, communication is established by using three lines: serial clocks ($\overline{SCK1}$ and $\overline{SCK2}$), serial data inputs (SI1 and SI2), and serial data outputs (SO1 and SO2). To connect two or more devices, a handshake line is necessary.

★ **Figure 7-11. Block Diagram in 3-wire Serial I/O Mode**



7.7.2 Clocked serial interface (CSI)

In this mode, the master device starts transfer by making the serial clock active and communicates 1-byte data in synchronization with this clock.

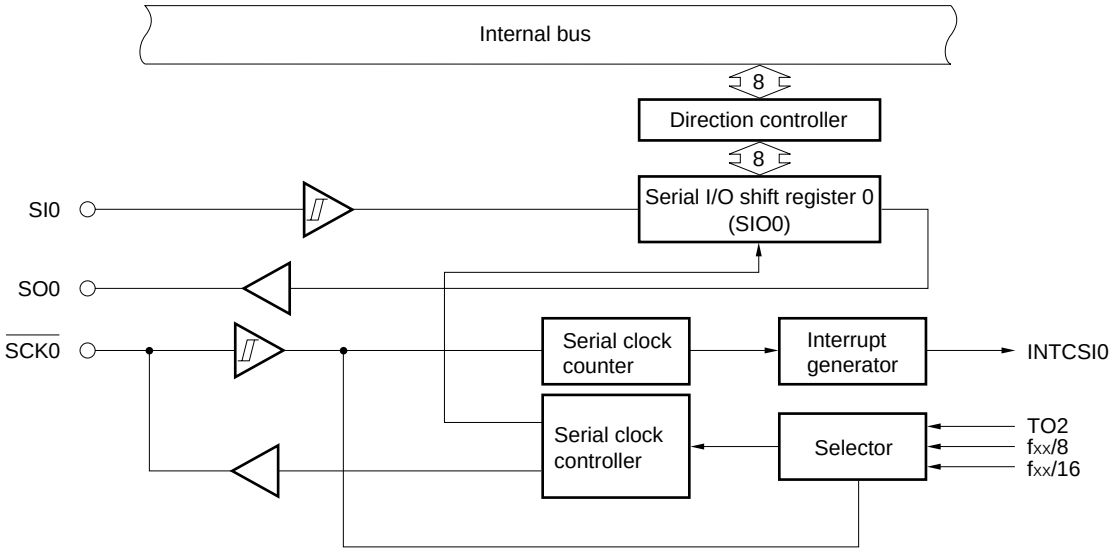
(1) 3-wire serial I/O mode

This mode is to communicate with devices having the conventional clocked serial interface.

Basically, communication is established in this mode with three lines: one serial clock ($\overline{SCK0}$) and two serial data (SI0 and SO0) lines.

Generally, a handshake line is necessary to check the reception status.

★ **Figure 7-12. Block Diagram in 3-Wise Serial I/O Mode**



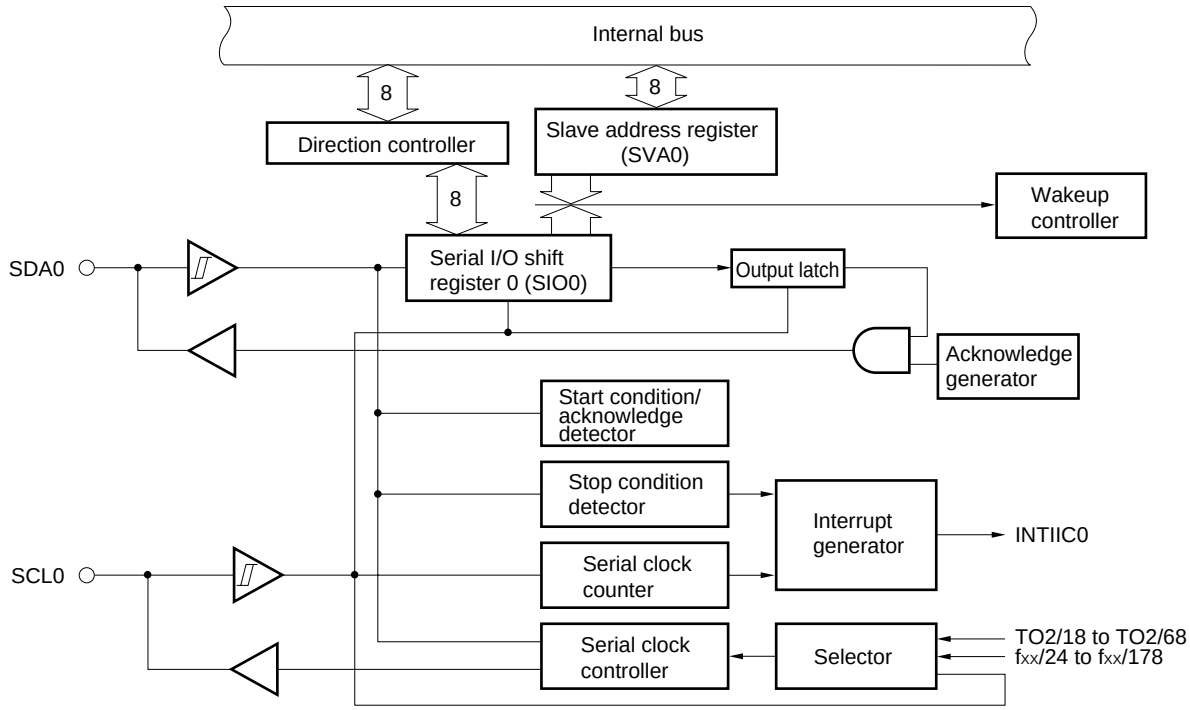
(2) I²C (Inter IC) bus mode (supporting multi-master) (μPD784225Y Subseries only)

This mode is to communicate with devices conforming to the I²C bus format.

This mode is to transfer 8-bit data with two or more devices by using two lines: serial clock (SCL0) and serial data bus (SDA0).

During transfer, a “start condition”, “data”, and “stop condition” can be output onto the serial data bus. During reception, these data can be automatically detected by hardware.

Figure 7-13. Block Diagram in I²C Bus Mode

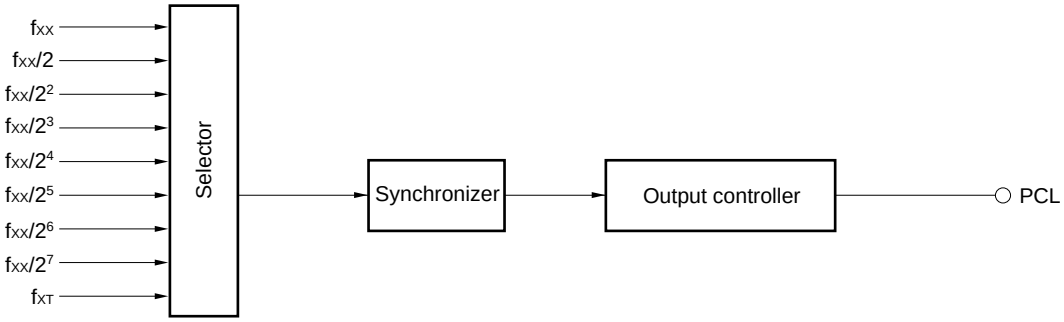


7.8 Clock Output Function

Clocks of the following frequencies can be output.

- 97.7 kHz/195 kHz/391 kHz/781 kHz/1.56 MHz/3.13 MHz/6.25 MHz/12.5 MHz (main system clock: 12.5 MHz)
- 32.768 kHz (subsystem clock: 32.768 kHz)

Figure 7-14. Block Diagram of Clock Output Function

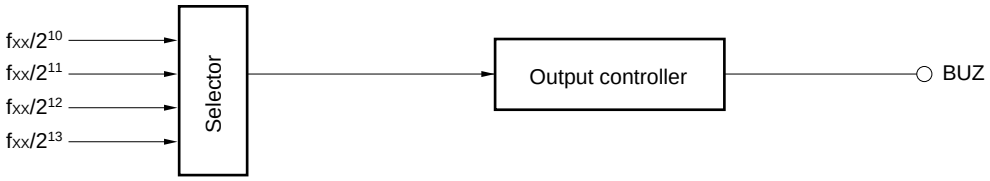


7.9 Buzzer Output Function

Clocks of the following frequencies can be output as buzzer output.

• 1.5 kHz/3.1 kHz/6.1 kHz/12.2 kHz (main system clock: 12.5 MHz)

Figure 7-15. Block Diagram of Buzzer Output Function



7.10 Edge Detection Function

The interrupt input pins (INTP0, INTP1, NMI/INTP2, INTP3 to INTP5) are used not only to input interrupt requests but also to input trigger signals to the internal hardware units. Because these pins operate at an edge of the input signal, they have a function to detect an edge. Moreover, a noise reduction circuit is also provided to prevent erroneous detection due to noise.

Pin Name	Detectable Edge	Noise Reduction
NMI	Either or both of rising and falling edges	By analog delay
INTP0 to INTP5		—

7.11 Watch Timer

The watch timer has the following functions:

• Watch timer
• Interval timer

The watch timer and interval timer functions can be used at the same time.

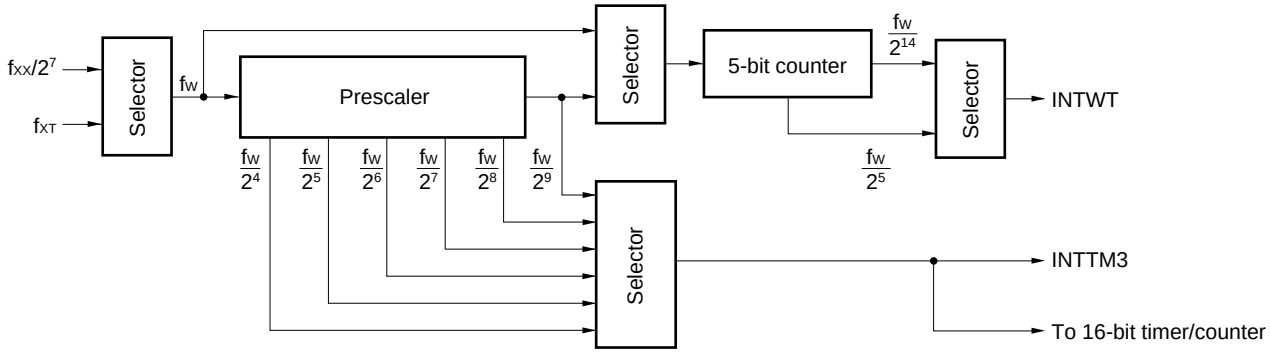
(1) Watch timer

The watch timer sets the WTIF flag of the interrupt control register (WTIC) at time intervals of 0.5 seconds by using the 32.768-kHz subsystem clock.

(2) Interval timer

The interval timer generates an interrupt request (INTTM3) at predetermined time intervals.

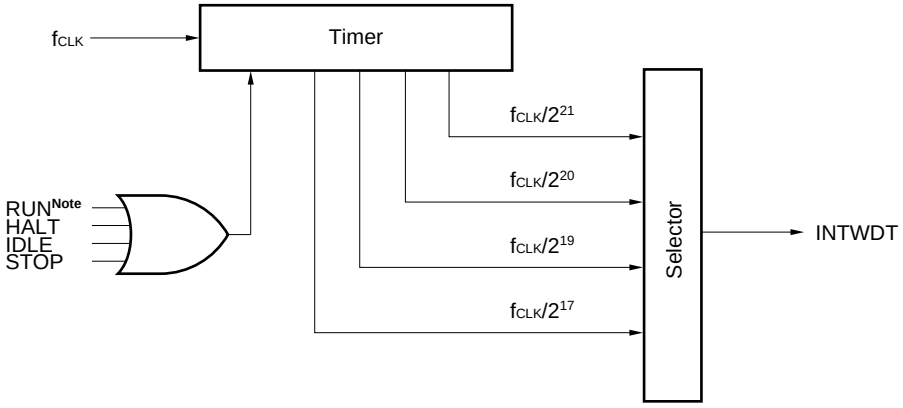
Figure 7-16. Block Diagram of Watch Timer



7.12 Watchdog Timer

A watchdog timer is provided to detect a hang up of the CPU. This watchdog timer generates a non-maskable or maskable interrupt unless it is cleared by software within a specified interval time. Once enabled to operate, the watchdog timer cannot be stopped by software. Whether the interrupt by the watchdog timer or the interrupt input from the NMI pin takes precedence can be specified.

★ **Figure 7-17. Block Diagram of Watchdog Timer**



Note Write 1 to bit 7 (RUN) of the watchdog timer (WDM).

Remark f_{CLK}: Internal system clock (f_{XX} to $f_{XX}/8$)

8. INTERRUPT FUNCTION

As the servicing in response to an interrupt request, the three types shown in Table 8-1 can be selected by program.

Table 8-1. Servicing of Interrupt Request

Servicing Mode	Entity of Servicing	Servicing	Contents of PC and PSW
Vectored interrupt	Software	Branches and executes servicing routine (servicing is arbitrary).	Saves to and restores from stack.
Context switching		Automatically switches register bank, branches and executes servicing routine (servicing is arbitrary).	Saves to or restores from fixed area in register bank
Macro service	Firmware	Executes data transfer between memory and I/O (servicing is fixed)	Retained

8.1 Interrupt Sources

Table 8-2 shows the interrupt sources available. As shown, interrupts are generated by 25 types of sources, execution of the BRK instruction, BRKCS instruction, or an operand error.

The priority of interrupt servicing can be set to four levels, so that nesting can be controlled during interrupt servicing and that which of the two or more interrupts that simultaneously occur should be serviced first. When the macro service function is used, however, nesting always proceeds.

The default priority is the priority (fixed) of the service that is performed if two or more interrupt requests, having the same request, simultaneously generate (see **Table 8-2**).

Table 8-2. Interrupt Sources

Type	Default Priority	Source		Internal/ External	Macro Service
		Name	Trigger		
Software	—	BRK instruction	Instruction execution	—	—
		BRKCS instruction	Instruction execution		
		Operand error	If result of exclusive OR between operands byte and $\overline{\text{byte}}$ is not FFH when MOV STBC, #byte instruction or MOV WDM, #byte instruction, LOCATION instruction is executed		
Non-maskable	—	NMI	Pin input edge detection	External	—
		INTWDT	Overflow of watchdog timer	Internal	
Maskable	0 (highest)	INTWDTM	Overflow of watchdog timer	Internal	○
	1	INTP0	Pin input edge detection	External	
	2	INTP1			
	3	INTP2			
	4	INTP3			
	5	INTP4			
	6	INTP5			
	7	INTIIC0**Note**	End of I^2C bus transfer by CSI0	Internal	
		INTCSI0	End of 3-wire transfer by CSI0		
	8	INTSER1	Occurrence of UART reception error in ASI1		
	9	INTSR1	End of UART reception by ASI1		
		INTCSI1	End of 3-wire transfer by CSI1		
	10	INTST1	End of UART transfer by ASI1		
	11	INTSER2	Occurrence of UART reception error in ASI2		
	12	INTSR2	End of UART reception by ASI2		
		INTCSI2	End of 3-wire transfer by CSI2		
	13	INTST2	End of UART transfer by ASI2		
	14	INTTM3	Reference time interval signal from watch timer		
	15	INTTM00	Signal indicating coincidence between 16-bit timer counter and capture/compare register (CR00)		
	16	INTTM01	Signal indicating coincidence between 16-bit timer counter and capture/compare register (CR01)		
	17	INTTM1	Occurrence of coincidence signal of 8-bit timer/counter 1		
	18	INTTM2	Occurrence of coincidence signal of 8-bit timer/counter 2		
	19	INTAD	End of conversion by A/D converter		
	20	INTTM5	Occurrence of coincidence signal of 8-bit timer/counter 5		
	21	INTTM6	Occurrence of coincidence signal of 8-bit timer/counter 6		
	22 (lowest)	INTWT	Overflow of watch timer		

Note μPD784255Y Subseries only

Remarks 1. ASI : Asynchronous Serial Interface
CSI : Clocked Serial Interface

★ **2.** There are two interrupt sources for the watchdog timer: non-maskable interrupts (INTWDT) and maskable interrupts (INTWDTM). Either one (but not both) should be selected for actual use.

8.2 Vectored Interrupt

Execution branches to a servicing routing by using the memory contents of a vector table address corresponding to the interrupt source as the address of the branch destination.

So that the CPU performs interrupt servicing, the following operations are performed:

- On branching: Saves the status of the CPU (contents of PC and PSW) to stack
- On returning : Restores the status of the CPU (contents of PC and PSW) from stack

To return to the main routine from an interrupt service routine, the RETI instruction is used.

The branch destination address is in a range of 0 to FFFFH.

Table 8-3. Vector Table Address

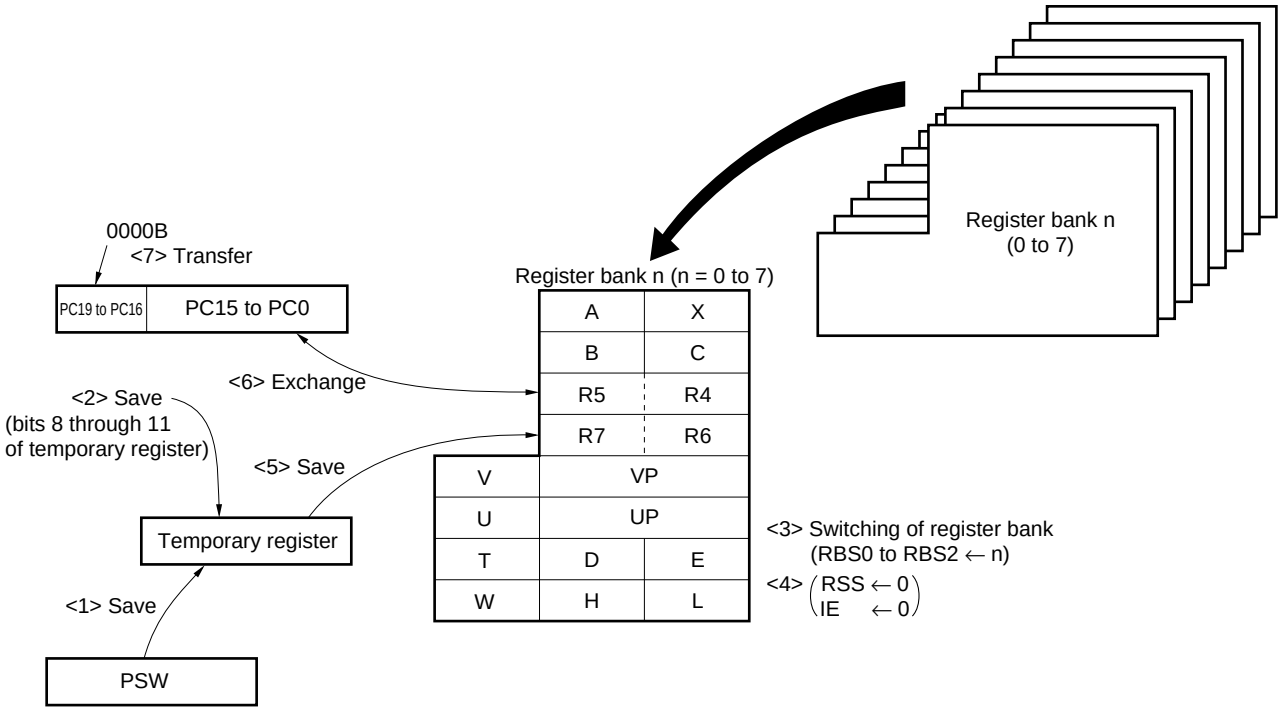
Interrupt Source	Vector Table Address	Interrupt Source	Vector Table Address
BRK instruction	003EH	INTST1	001CH
Operand error	003CH	INTSER2	001EH
NMI	0002H	INSR2	0020H
INTWDT (non-maskable)	0004H	INTCSI2	
INTWDTM (maskable)	0006H	INTST2	0022H
INTP0	0008H	INTTM3	0024H
INTP1	000AH	INTTM00	0026H
INTP2	000CH	INTTM01	0028H
INTP3	000EH	INTTM1	002AH
INTP4	0010H	INTTM2	002CH
INTP5	0012H	INTAD	002EH
INTIIC0	0016H	INTTM5	00030H
INTCSI0		INTTM6	0032H
INTSER1	0018H	INTWT	0038H
INTSR1	001AH		
INTCSI1			

8.3 Context Switching

When an interrupt request is generated or when the BRKCS instruction is executed, a predetermined register bank is selected by hardware. Context switching is a function that branches execution to a vector address stored in advance in the register bank, and to stack the current contents of the program counter (PC) and program status word (PSW) to the register bank.

The branch address is in a range of 0 to FFFFH.

Figure 8-1. Context Switching Operation When Interrupt Request Is Generated

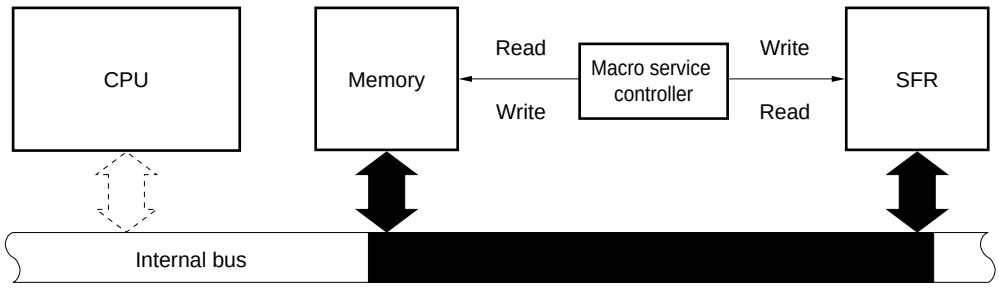


8.4 Macro Service

This function is to transfer data between memory and a special function register (SFR) without intervention by the CPU. A macro service controller accesses the memory and SFR in the same transfer cycle and directly transfers data without loading it.

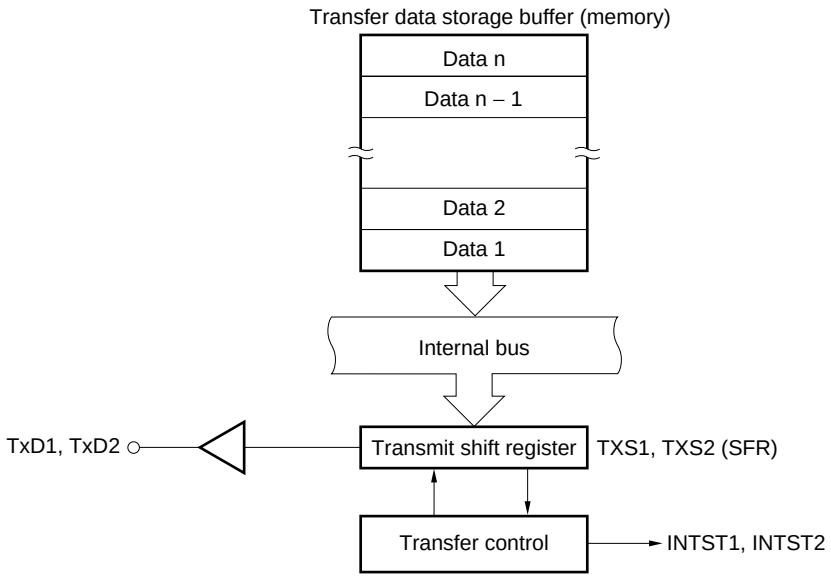
Because this function does not save or restore the status of the CPU, or load data, data can be transferred at high speeds.

Figure 8-2. Macro Service



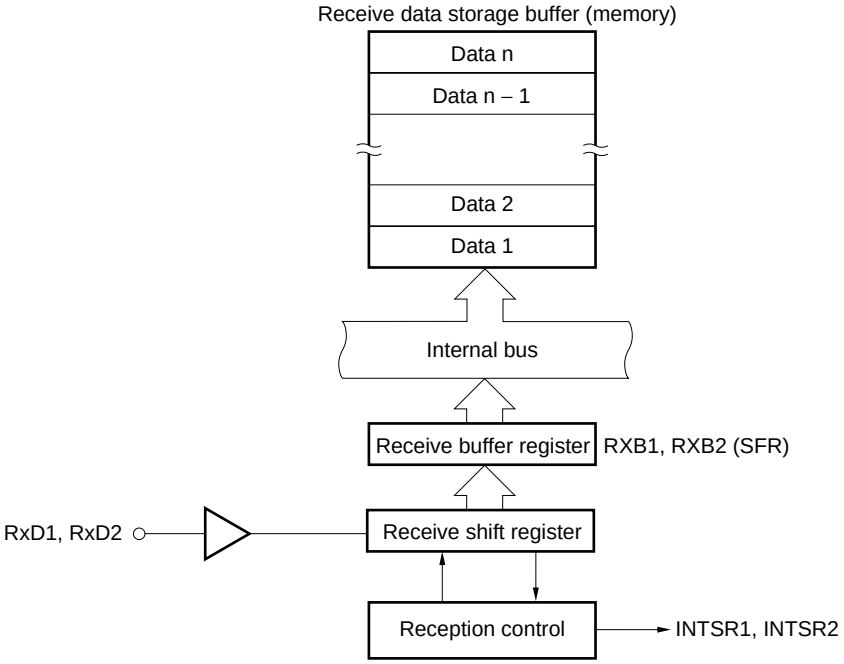
8.5 Application Example of Macro Service

(1) Transmission of serial interface



Each time macro service request INTST1 and INTST2 are generated, the next transmit data is transferred from memory to TXS1 and TXS2. When data n (last byte) has been transferred to TXS1 and TXS2 (when the transmit data storage buffer has become empty), vectored interrupt request INTST1 and INTST2 are generated.

(2) Reception of serial interface

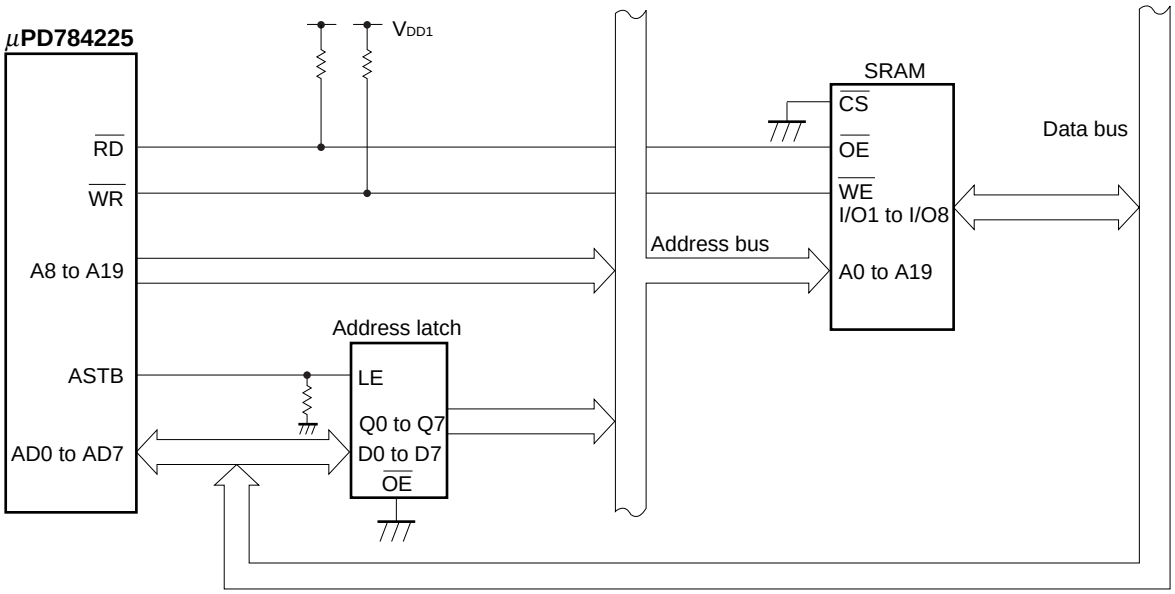


Each time macro service request INTSR1 and INTSR2 are generated, the receive data is transferred from RXB1 and RXB2 to memory. When data n (last byte) has been transferred to memory (when the receive data storage buffer has become full), vectored interrupt request INTSR1 and INTSR2 are generated.

9. LOCAL BUS INTERFACE

The local bus interface can connect an external memory or I/O (memory mapped I/O) and support a memory space of 1 Mbyte (refer to **Figure 9-1**).

Figure 9-1. Example of Local Bus Interface (Multiplexed bus)



9.1 Memory Expansion

External program and data memory can be connected in two stages: 256 Kbytes and 1 Mbytes.

To connect the external memory, ports 4 to 6 are used.

The external memory is connected by using a time-division address/data bus. The number of ports used when the external memory is connected can be reduced in this mode.

9.2 Programmable Wait

Wait state(s) can be inserted to the memory space (00000H to FFFFFH) while the $\overline{RD}$ and $\overline{WR}$ signals are active.

In addition, there is an address wait function that extends the active period of the ASTB signal to gain the address decode time.

9.3 External Access Status Function

An active low external access status signal is output from the P37/EXA pin. This signal notifies other devices connected to the external bus of the external access status, to disable data output to the external bus from other devices, or enables reception.

The external access status signal is output during external access.

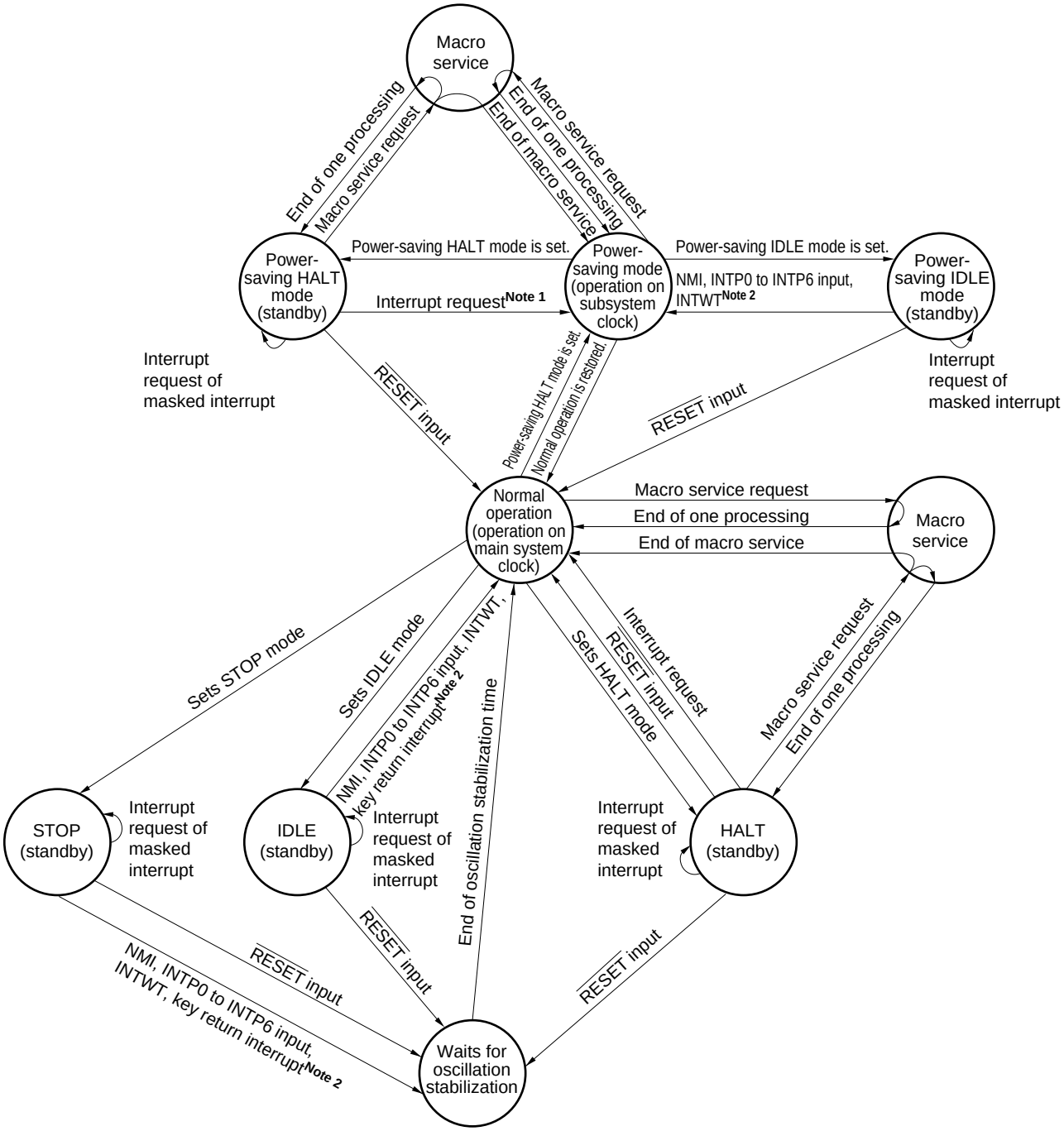
10. STANDBY FUNCTION

This function is to reduce the power consumption of the chip, and can be used in the following modes:

- HALT mode : Stops supply of the operating clock to the CPU. This mode is used in combination with the normal operation mode for intermittent operation to reduce the average power consumption.
- IDLE mode : Stops the entire system with the oscillator continuing operation. The power consumption in this mode is close to that in the STOP mode. However, the time required to restore the normal program operation from this mode is almost the same as that from the HALT mode.
- STOP mode : Stops the main system clock and thereby to stop all the internal operations of the chip. Consequently, the power consumption is minimized with only leakage current flowing.
- Power-saving mode : The main system clock is stopped with the subsystem clock used as the system clock. The CPU can operate on the subsystem clock to reduce the current consumption.
- Power-saving HALT mode : This is a standby function in the power-saving mode and stops the operation clock of the CPU, to reduce the power consumption of the entire system.
- Power-saving IDLE mode : This is a standby function in the power-saving mode and stops the entire system except the oscillator, to reduce the power consumption of the entire system.

These modes are programmable.
The macro service can be started from the HALT mode and power-saving HALT mode.
After executing macro service processing, it returns to the HALT mode.

★ **Figure 10-1. Transition of Standby Status**



Notes 1. Only unmasked interrupt requests

2. Only unmasked INTP0 to INTP6, INTWT, key return interrupt (P80 to P87)

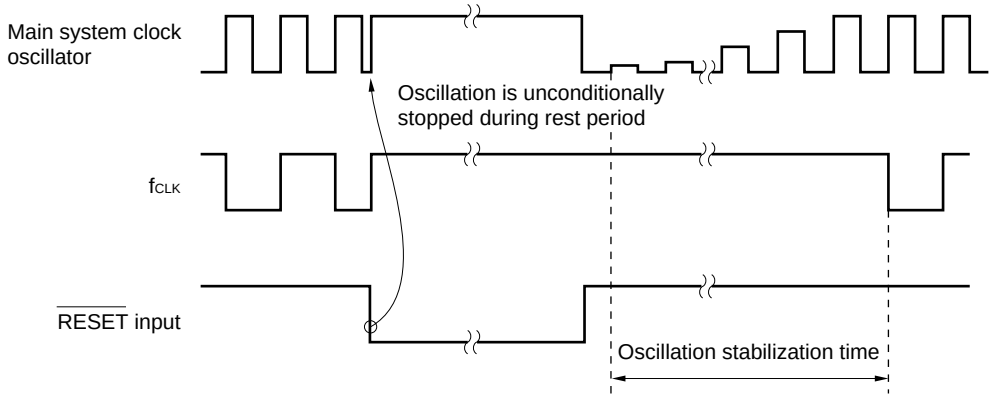
Remark NMI is valid only for an external input. The watchdog timer cannot be used for the release of standby (HALT mode/STOP mode/IDLE mode).

11. RESET FUNCTION

When a low-level signal is input to the $\overline{\text{RESET}}$ pin, the system is reset, and each hardware unit is initialized (reset). During the reset period, oscillation of the main system clock is unconditionally stopped. Consequently, the current consumption of the entire system can be reduced.

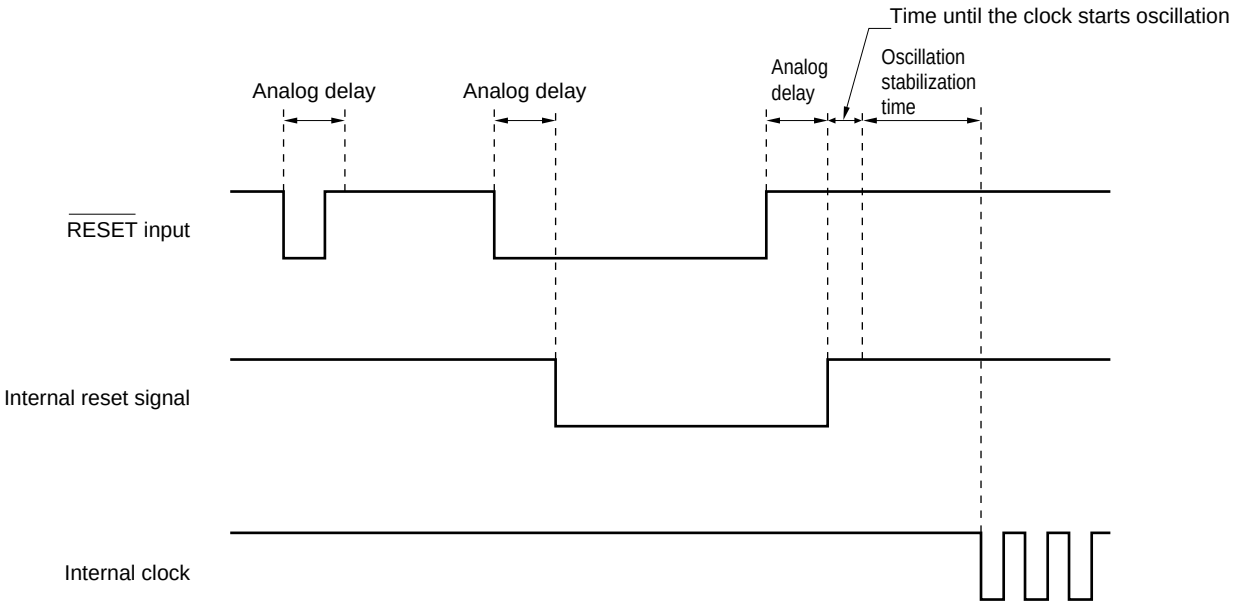
When the $\overline{\text{RESET}}$ signal goes high, the reset status is cleared, oscillation stabilization time (41.9 ms at 12.5 MHz) elapses, the contents of the reset vector table are set to the program counter (PC), execution branches to an address set to the PC, and program execution is started from that branch address. Therefore, the program can be reset and started from any address.

★ **Figure 11-1. Oscillation of Main System Clock during Reset Period**



The $\overline{\text{RESET}}$ input pin has an analog delay noise eliminator to prevent malfunctioning due to noise.

★ **Figure 11-2. Accepting Reset Signal**



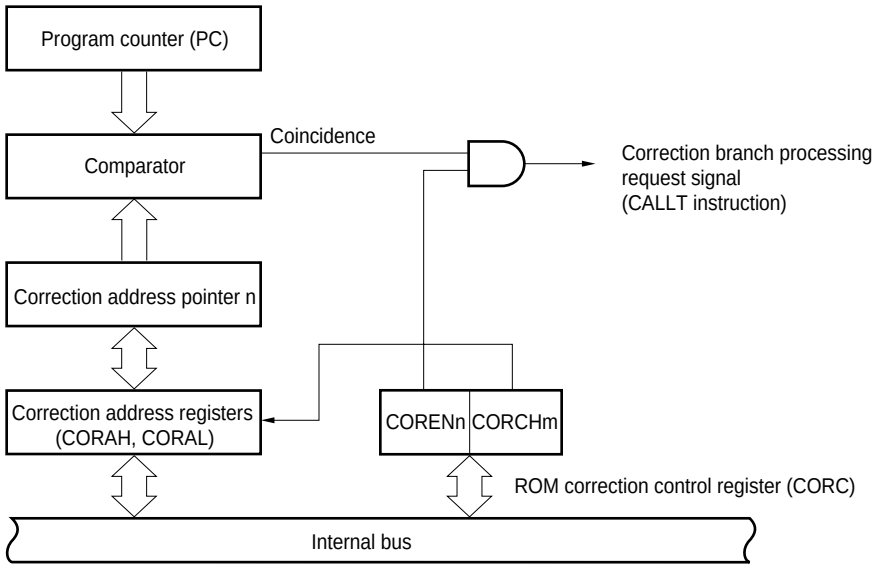
12. ROM CORRECTION

ROM correction is a function to replace part of the program in the internal ROM with a program in the internal RAM.

By using the ROM correction function, instruction bugs found in the internal ROM can be avoided or the flow of the program can be changed.

ROM correction can be used at up to four places in the internal ROM (program).

Figure 12-1. Block Diagram of ROM Correction



Remark n = 0 to 3, m = 0 or 1

13. INSTRUCTION SET

(1) 8-bit instructions (The instructions in parentheses are combinations realized by describing A as r)

MOV, XCH, ADD, ADDC, SUB, SUBC, AND, OR, XOR, CMP, MULU, DIVUW, INC, DEC, ROR, ROL, RORC, ROLC, SHR, SHL, ROR4, ROL4, DBNZ, PUSH, POP, MOVM, XCHM, CMPME, CMPMNE, CMPMNC, CMPMC, MOVBK, XCHBK, CMPBKE, CMPBKNE, CMPBKNC, CMPBKC, CHKL, CHKLA

Table 13-1. Instruction List by 8-Bit Addressing

Second Operand / First Operand	#byte	A	r r'	saddr saddr'	sfr	!addr16 !!addr24	mem [saddrp] [%saddrg]	r3 PSWL PSWH	[WHL+] [WHL–]	n	None[Note 2]
A	(MOV) ADD[Note 1]	(MOV) (XCH) (ADD)[Note 1]	MOV XCH (ADD)[Note 1]	(MOV)[Note 6] (XCH)[Note 6] (ADD)[Note 1,6]	MOV (XCH) (ADD)[Note 1]	(MOV) (XCH) ADD[Note 1]	MOV XCH ADD[Note 1]	MOV	(MOV) (XCH) (ADD)[Note 1]		
r	MOV ADD[Note 1]	(MOV) (XCH) (ADD)[Note 1]	MOV XCH ADD[Note 1]	MOV XCH ADD[Note 1]	MOV XCH ADD[Note 1]	MOV XCH				ROR[Note 3]	MULU DIVUW INC DEC
saddr	MOV ADD[Note 1]	(MOV)[Note 6] (ADD)[Note 1]	MOV ADD[Note 1]	MOV XCH ADD[Note 1]							INC DEC DBNZ
sfr	MOV ADD[Note 1]	MOV (ADD)[Note 1]	MOV ADD[Note 1]								PUSH POP CHKL CHKLA
!addr16 !!addr24	MOV	(MOV) ADD[Note 1]	MOV								
mem [saddrp] [%saddrg]		MOV ADD[Note 1]									
mem3											ROR4 ROL4
r3 PSWL PSWH	MOV	MOV									
B, C											DBNZ
STBC, WDM	MOV										
[TDE+] [TDE–]		(MOV) (ADD)[Note 1] MOVM[Note 4]							MOVBK[Note 5]		

Notes 1. The operands of ADDC, SUB, SUBC, AND, OR, XOR, and CMP are the same as that of ADD.

2. Either the second operand is not used, or the second operand is not an operand address.

3. The operands of ROL, RORC, ROLC, SHR, and SHL are the same as that of ROR.

4. The operands of XCHM, CMPME, CMPMNE, CMPMNC, and CMPMC are the same as that of MOVM.

5. The operands of XCHBK, CMPBKE, CMPBKNE, CMPBKNC, and CMPBKC are the same as that of MOVBK.

6. The code length of some instructions having saddr2 as saddr in this combination is short.

(2) 16-bit instructions (The instructions in parentheses are combinations realized by describing AX as rp)

MOVW, XCHW, ADDW, SUBW, CMPW, MULUW, MULW, DIVUX, INCW, DECW, SHRW, SHLW, PUSH, POP, ADDWG, SUBWG, PUSHU, POPU, MOVTBLW, MACW, MACSW, SACW

Table 13-2. Instruction List by 16-Bit Addressing

First Operand \ Second Operand	#word	AX	rp rp'	saddrp saddrp'	sfrp	!addr16 !!addr24	mem [saddrp] [%saddrg]	[WHL+]	byte	n	None[Note 2]
AX	(MOVW) ADDW[Note 1]	(MOVW) (XCHW) (ADD)[Note 1]	(MOVW) (XCHW) (ADDW)[Note 1]	(MOVW)[Note 3] (XCHW)[Note 3] (ADDW)[Note 1,3]	MOVW (XCHW) (ADDW)[Note 1]	(MOVW) XCHW	MOVW XCHW	(MOVW) (XCHW)			
rp	MOVW ADDW[Note 1]	(MOVW) (XCHW) (ADDW)[Note 1]	MOVW XCHW ADDW[Note 1]	MOVW XCHW ADDW[Note 1]	MOVW XCHW ADDW[Note 1]	MOVW				SHRW SHLW	MULW[Note 4] INCW DECW
saddrp	MOVW ADDW[Note 1]	(MOVW)[Note 3] (ADDW)[Note 1]	MOVW ADDW[Note 1]	MOVW XCHW ADDW[Note 1]							INCW DECW
sfrp	MOVW ADDW[Note 1]	MOVW (ADDW)[Note 1]	MOVW ADDW[Note 1]								PUSH POP
!addr16 !!addr24	MOVW	(MOVW)	MOVW						MOVTBLW		
mem [saddrp] [%saddrg]		MOVW									
PSW											PUSH POP
SP	ADDWG SUBWG										
post											PUSH POP PUSHU POPU
[TDE+]		(MOVW)						SACW			
byte											MACW MACSW

Notes 1. The operands of SUBW and CMPW are the same as that of ADDW.

2. Either the second operand is not used, or the second operand is not an operand address.

3. The code length of some instructions having saddrp2 as saddrp in this combination is short.

4. The operands of MULUW and DIVUX are the same as that of MULW.

(3) 24-bit instructions (The instructions in parentheses are combinations realized by describing WHL as rg)

MOVG, ADDG, SUBG, INCG, DECG, PUSH, POP

Table 13-3. Instruction List by 24-Bit Addressing

First Operand \ Second Operand	#imm24	WHL	rg rg'	saddrg	!!addr24	mem1	[%saddrg]	SP	None[Note]
WHL	(MOVG) (ADDG) (SUBG)	(MOVG) (ADDG) (SUBG)	(MOVG) (ADDG) (SUBG)	(MOVG) ADDG SUBG	(MOVG)	MOVG	MOVG	MOVG	
rg	MOVG ADDG SUBG	(MOVG) (ADDG) (SUBG)	MOVG ADDG SUBG	MOVG	MOVG				INCG DECG PUSH POP
saddrg		(MOVG)	MOVG						
!!addr24		(MOVG)	MOVG						
mem1		MOVG							
[%saddrg]		MOVG							
SP	MOVG	MOVG							INCG DECG

Note Either the second operand is not used, or the second operand is not an operand address.

(4) Bit manipulation instructions

MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BTCLR, BFSET

Table 13-4. Bit Manipulation Instructions

Second Operand / First Operand	CY	saddr.bit sfr.bit A.bit X.bit PSWL.bit PSWH.bit mem2.bit !addr16.bit !!addr24.bit	/saddr.bit /sfr. bit /A.bit /X.bit /PSWL.bit /PSWH.bit /mem2.bit /!addr16.bit /!!addr24.bit	None[Note]
CY		MOV1 AND1 OR1 XOR1	AND1 OR1	NOT1 SET1 CLR1
saddr.bit sfr.bit A.bit X.bit PSWL.bit PSWH.bit mem2.bit !addr16.bit !!addr24.bit	MOV1			NOT1 SET1 CLR1 BF BT BTCLR BFSET

Note Either the second operand is not used, or the second operand is not an operand address.

(5) Call and return/branch instructions

CALL, CALLF, CALLT, BRK, RET, RETI, RETB, RETCS, RETCSB, BRKCS, BR, BNZ, BNE, BZ, BE, BNC, BNL, BC, BL, BNV, BPO, BV, BPE, BP, BN, BLT, BGE, BLE, BGT, BNH, BH, BF, BT, BTCLR, BFSET, DBNZ

Table 13-5. Call and Return/Branch Instructions

Operand of Instruction Address	$addr20	$!addr20	!addr16	!!addr20	rp	rg	[rp]	[rg]	!addr11	[addr5]	RBn	None
Basic instruction	BC[Note] BR	CALL BR	CALL BR RETCS RETCSB	CALL BR	CALL BR	CALL BR	CALL BR	CALL BR	CALLF	CALLF	BRKCS	BRK RET RETI RETB
Compound instruction	BF BT BTCLR BFSET DBNZ											

Note The operands of BNZ, BNE, BZ, BE, BNC, BNL, BL, BNV, BPO, BV, BPE, BP, BN, BLT, BGE, BLE, BGT, BNH, and BH are the same as BC.

(6) Other instructions

ADJBA, ADJBS, CVTBW, LOCATION, SEL, NOT, EI, DI, SWRS

★ 14. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C)

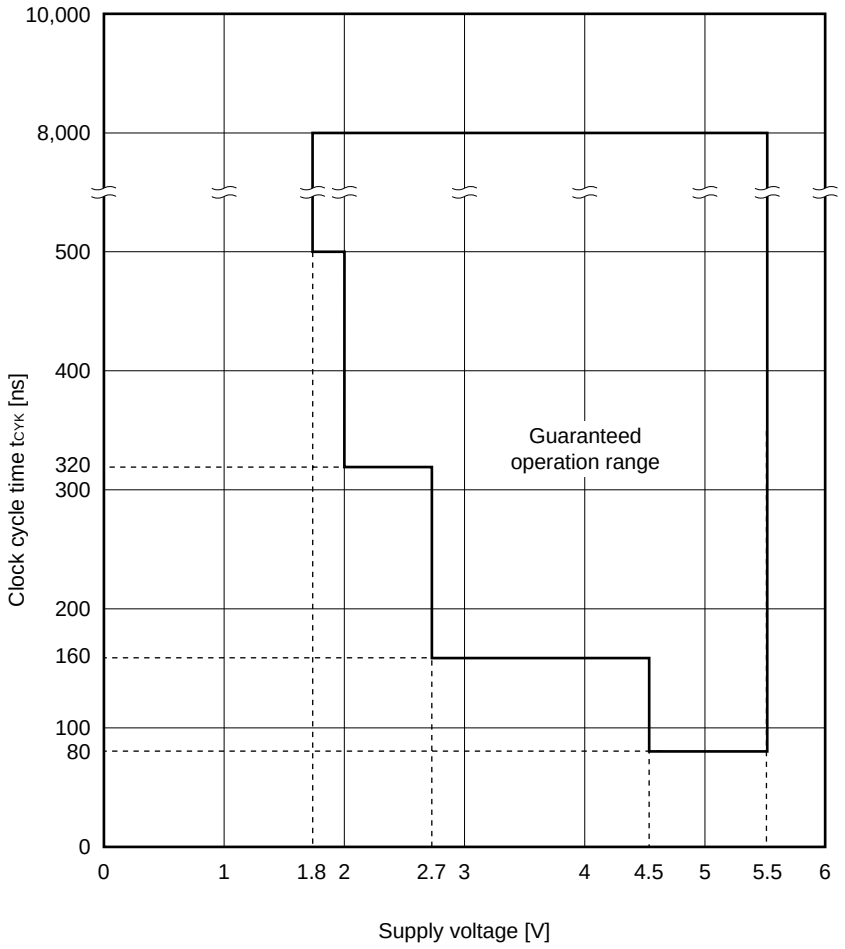
Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD0}		–0.3 to +6.5	V
	AV_{DD}		–0.3 to V_{DD0} + 0.3	V
	AV_{SS}		–0.3 to V_{SS0} + 0.3	V
	AV_{REF1}	D/A converter reference voltage input	–0.3 to V_{DD0} + 0.3	V
Input voltage	V_I		–0.3 to V_{DD0} + 0.3	V
Analog input voltage	V_{AN}	Analog input pin	AV_{SS} – 0.3 to AV_{REF1} + 0.3	V
Output voltage	V_O		–0.3 to V_{DD} + 0.3	V
Output current, low	I_{OL}	Per pin	15	mA
		Total of all pins	100	mA
Output current, high	I_{OH}	Per pin	–10	mA
		Total of all pins	–40	mA
Operating ambient temperature	T_A		–40 to +85	°C
Storage temperature	T_{stg}		–65 to +150	°C

Caution Absolute maximum ratings are rated values beyond which physical damage will be caused to the product; if the rated value of any of the parameters in the above table is exceeded, even momentarily, the quality of the product may deteriorate. Always use the product within its rated values.

Operating Conditions

- Operating ambient temperature (T_A): –40°C to +85°C
- Power supply voltage and clock cycle time: see **Figure 14-1**
- Operating voltage when the subsystem clock is operating: V_{DD} = 1.8 to 5.5 V

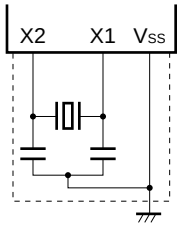
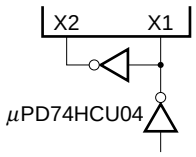
Figure 14-1. Power Supply Voltage and Clock Cycle Time (CPU Clock Frequency: f_{CPU})



Capacitance (T_A = 25°C, V_{DD} = V_{DD0} = V_{DD1} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f = 1 MHz			15	pF
Output capacitance	C_O	Unmeasured pins returned to 0 V.			15	pF
I/O capacitance	C_{IO}				15	pF

Main System Clock Oscillator Characteristics (T_A = −40°C to +85°C, V_{DD} = V_{DD0} = V_{DD1})

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator or crystal resonator		Oscillation frequency (f_X)	4.5 V ≤ V_{DD} ≤ 5.5 V	2		12.5	MHz
			2.7 V ≤ V_{DD} < 4.5 V	2		6.25	
			2.0 V ≤ V_{DD} < 2.7 V	2		3.125	
			1.8 V ≤ V_{DD} < 2.0 V	2		2	
External clock		X1 input frequency (f_X)	4.5 V ≤ V_{DD} ≤ 5.5 V	2		12.5	MHz
			2.7 V ≤ V_{DD} < 4.5 V	2		6.25	
			2.0 V ≤ V_{DD} < 2.7 V	2		3.125	
			1.8 V ≤ V_{DD} < 2.0 V	2		2	
		X1 input high-/low-level width (t_{WXH}, t_{WXL})		15		250	ns
		X1 input rising/falling time (t_{XR}, t_{XF})	4.5 V ≤ V_{DD} ≤ 5.5 V	0		5	ns
			2.7 V ≤ V_{DD} < 4.5 V	0		10	
			2.0 V ≤ V_{DD} < 2.7 V	0		20	
			1.8 V ≤ V_{DD} < 2.0 V	0		30	

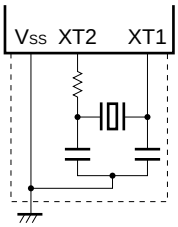
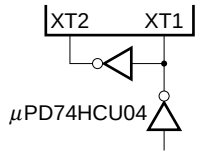
Cautions 1. When using the main system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. When the main system clock is stopped and the device is operating on the subsystem clock, wait until the oscillation stabilization time has been secured by the program before switching back to the main system clock.

Remark For the resonator selection and oscillator constant, customers are required to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

Subsystem Clock Oscillator Characteristics (T_A = −40°C to +85°C, V_{DD} = V_{DD0} = V_{DD1})

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillation frequency (f_{XT})		32	32.768	35	kHz
		Oscillation stabilization time[Note]	4.5 V ≤ V_{DD} ≤ 5.5 V		1.2	2	s
			1.8 V ≤ V_{DD} < 4.5 V			10	
External clock		XT1 input frequency (f_{XT})		32		35	kHz
		XT1 input high-/low-level width (t_{XTH}, t_{XTL})		14.3		15.6	μs

Note Time required to stabilize oscillation after applying supply voltage (V_{DD}).

Cautions 1. When using the subsystem clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. When the main system clock is stopped and the device is operating on the subsystem clock, wait until the oscillation stabilization time has been secured by the program before switching back to the main system clock.

Remark For the resonator selection and oscillator constant, customers are required to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

DC Characteristics

(T_A = –40°C to +85°C, V_{DD} = V_{DD0} = V_{DD1} = AV_{DD} = 1.8 to 5.5 V, V_{SS} = V_{SS0} = V_{SS1} = AV_{SS} = 0 V) (1/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, low	V_{IL1}	**Note 1**	2.2 V ≤ V_{DD} ≤ 5.5 V	0		0.3V_{DD}	V
			1.8 V ≤ V_{DD} < 2.2 V	0		0.2V_{DD}	
	V_{IL2}	P00 to P05, P20, P22, P33, P34, P70, P72, $\overline{\text{RESET}}$	2.2 V ≤ V_{DD} ≤ 5.5 V	0		0.2V_{DD}	V
			1.8 V ≤ V_{DD} < 2.2 V	0		0.15V_{DD}	
	V_{IL4}	P10 to P17, P130, P131	2.2 V ≤ V_{DD} ≤ 5.5 V	0		0.3V_{DD}	V
			1.8 V ≤ V_{DD} < 2.2 V	0		0.2V_{DD}	
	V_{IL5}	X1, X2, XT1, XT2	2.2 V ≤ V_{DD} ≤ 5.5 V	0		0.2V_{DD}	V
			1.8 V ≤ V_{DD} < 2.2 V	0		0.1V_{DD}	
	V_{IL6}	P25, P27	2.2 V ≤ V_{DD} ≤ 5.5 V	0		0.3V_{DD}	V
			1.8 V ≤ V_{DD} < 2.2 V	0		0.2V_{DD}	
Input voltage, high	V_{IH1}	**Note 1**	2.2 V ≤ V_{DD} ≤ 5.5 V	0.7V_{DD}		V_{DD}	V
			1.8 V ≤ V_{DD} < 2.2 V	0.8V_{DD}		V_{DD}	
	V_{IH2}	P00 to P05, P20, P22, P33, P34, P70, P72, $\overline{\text{RESET}}$	2.2 V ≤ V_{DD} ≤ 5.5 V	0.8V_{DD}		V_{DD}	V
			1.8 V ≤ V_{DD} < 2.2 V	0.85V_{DD}		V_{DD}	
	V_{IH4}	P10 to P17, P130, P131	2.2 V ≤ V_{DD} ≤ 5.5 V	0.7V_{DD}		V_{DD}	V
			1.8 V ≤ V_{DD} < 2.2 V	0.8V_{DD}		V_{DD}	
	V_{IH5}	X1, X2, XT1, XT2	2.2 V ≤ V_{DD} ≤ 5.5 V	0.8V_{DD}		V_{DD}	V
			1.8 V ≤ V_{DD} < 2.2 V	0.85V_{DD}		V_{DD}	
	V_{IH6}	P25, P27	2.2 V ≤ V_{DD} ≤ 5.5 V	0.7V_{DD}		V_{DD}	V
			1.8 V ≤ V_{DD} < 2.2 V	0.8V_{DD}		V_{DD}	
Output voltage, low	V_{OL1}	For pins other than P40 to P47, P50 to P57, I_{OL} = 1.6 mA**Note 2**	4.5 V ≤ V_{DD} ≤ 5.5 V			0.4	V
		P40 to P47, P50 to P57 I_{OL} = 8 mA**Note 2**	4.5 V ≤ V_{DD} ≤ 5.5 V			1.0	V
	V_{OL2}	I_{OL} = 400 μA**Note 2**				0.5	V
Output voltage, high	V_{OH1}	I_{OH} = –1 mA**Note 2**	4.5 V ≤ V_{DD} ≤ 5.5 V	V_{DD} – 1.0			V
		I_{OH} = –100 μA**Note 2**		V_{DD} – 0.5			V
Input leakage current, low	I_{LIL1}	V_{IN} = 0 V	Except X1, X2, XT1, XT2			–3	μA
	I_{LIL2}		X1, X2, XT1, XT2			–20	μA
Input leakage current, high	I_{LIH1}	V_{IN} = V_{DD0}	Except X1, X2, XT1, XT2			3	μA
	I_{LIH2}		X1, X2, XT1, XT2			20	μA
Output leakage current, low	I_{LOL1}	V_{OUT} = 0 V				–3	μA
Output leakage current, high	I_{LOH1}	V_{OUT} = V_{DD}				3	μA

Notes 1. P21, P23, P24, P26, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P60 to P67, P71, P80 to P87, P120 to P127

2. Per pin

DC Characteristics

(T_A = −40°C to +85°C, V_{DD} = V_{DD0} = V_{DD1} = AV_{DD} = 1.8 to 5.5 V, V_{SS} = V_{SS0} = V_{SS1} = AV_{SS} = 0 V) (2/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Supply voltage	I_{DD1}	Operation mode	f_{XX} = 12.5 MHz, V_{DD} = 5.0 V ±10%		17	40	mA
			f_{XX} = 6 MHz, V_{DD} = 3.0 V ±10%		5	17	mA
			f_{XX} = 2 MHz, V_{DD} = 2.0 V ±10%		2	8	mA
	I_{DD2}	HALT mode	f_{XX} = 12.5 MHz, V_{DD} = 5.0 V ±10%		7	20	mA
			f_{XX} = 6 MHz, V_{DD} = 3.0 V ±10%		2	8	mA
			f_{XX} = 2 MHz, V_{DD} = 2.0 V ±10%		0.5	3.5	mA
	I_{DD3}	IDLE mode	f_{XX} = 12.5 MHz, V_{DD} = 5.0 V ±10%		1	2.5	mA
			f_{XX} = 6 MHz, V_{DD} = 3.0 V ±10%		0.4	1.3	mA
			f_{XX} = 2 MHz, V_{DD} = 2.0 V ±10%		0.2	0.9	mA
	I_{DD4}	Operation mode**Note**	f_{XX} = 32 kHz, V_{DD} = 5.0 V ±10%		80	200	μA
			f_{XX} = 32 kHz, V_{DD} = 3.0 V ±10%		60	110	μA
			f_{XX} = 32 kHz, V_{DD} = 2.0 V ±10%		30	100	μA
	I_{DD5}	HALT mode**Note**	f_{XX} = 32 kHz, V_{DD} = 5.0 V ±10%		60	160	μA
			f_{XX} = 32 kHz, V_{DD} = 3.0 V ±10%		20	80	μA
			f_{XX} = 32 kHz, V_{DD} = 2.0 V ±10%		10	70	μA
	I_{DD6}	IDLE mode**Note**	f_{XX} = 32 kHz, V_{DD} = 5.0 V ±10%		50	150	μA
			f_{XX} = 32 kHz, V_{DD} = 3.0 V ±10%		15	70	μA
			f_{XX} = 32 kHz, V_{DD} = 2.0 V ±10%		5	60	μA
Data retention voltage	V_{DDDR}	HALT, IDLE modes		1.8		5.5	V
Data retention current	I_{DDDR}	STOP mode	V_{DD} = 2.0 V ±10%		2	10	μA
			V_{DD} = 5.0 V ±10%		10	50	μA
Pull-up resistor	R_L	V_{IN} = 0 V		10	30	100	kΩ

Note When main system clock is stopped.

Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.

AC Characteristics

(T_A = –40°C to +85°C, V_{DD} = V_{DD0} = V_{DD1} = AV_{DD} = 1.8 to 5.5 V, V_{SS} = V_{SS0} = V_{SS1} = AV_{SS} = 0 V)

(1) Read/write operation (1/3)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Cycle time	t_{CYK}	4.5 V ≤ V_{DD} ≤ 5.5 V	80			ns
		2.7 V ≤ V_{DD} < 4.5 V	160			ns
		2.0 V ≤ V_{DD} < 2.7 V	320			ns
		1.8 V ≤ V_{DD} < 2.0 V	500			ns
Address setup time (to ASTB↓)	t_{SAST}	V_{DD} = 5.0 V ±10%	(0.5 + a) T – 20			ns
		V_{DD} = 3.0 V ±10%	(0.5 + a) T – 40			ns
		V_{DD} = 2.0 V ±10%	(0.5 + a) T – 80			ns
Address hold time (from ASTB↓)	t_{HSTLA}	V_{DD} = 5.0 V ±10%	0.5T – 19			ns
		V_{DD} = 3.0 V ±10%	0.5T – 24			ns
		V_{DD} = 2.0 V ±10%	0.5T – 34			ns
ASTB high-level width	t_{WSTH}	V_{DD} = 5.0 V ±10%	(0.5 + a) T – 17			ns
		V_{DD} = 3.0 V ±10%	(0.5 + a) T – 40			ns
		V_{DD} = 2.0 V ±10%	(0.5 + a) T – 110			ns
Address hold time (from $\overline{RD}$↑)	t_{HRA}	V_{DD} = 5.0 V ±10%	0.5T – 14			ns
		V_{DD} = 3.0 V ±10%	0.5T – 14			ns
		V_{DD} = 2.0 V ±10%	0.5T – 14			ns
Delay time from address to $\overline{RD}$↓	t_{DAR}	V_{DD} = 5.0 V ±10%	(1 + a) T – 24			ns
		V_{DD} = 3.0 V ±10%	(1 + a) T – 35			ns
		V_{DD} = 2.0 V ±10%	(1 + a) T – 80			ns
Address float time (from $\overline{RD}$↓)	t_{FAR}	V_{DD} = 5.0 V ±10%			0	ns
		V_{DD} = 3.0 V ±10%			0	ns
		V_{DD} = 2.0 V ±10%			0	ns
Data input time from address	t_{DAID}	V_{DD} = 5.0 V ±10%			(2.5 + a + n) T – 37	ns
		V_{DD} = 3.0 V ±10%			(2.5 + a + n) T – 52	ns
		V_{DD} = 2.0 V ±10%			(2.5 + a + n) T – 120	ns
Data input time from ASTB↓	t_{DSTID}	V_{DD} = 5.0 V ±10%			(2 + n) T – 35	ns
		V_{DD} = 3.0 V ±10%			(2 + n) T – 50	ns
		V_{DD} = 2.0 V ±10%			(2 + n) T – 80	ns
Data input time from $\overline{RD}$↓	t_{DRID}	V_{DD} = 5.0 V ±10%			(1.5 + n) T – 40	ns
		V_{DD} = 3.0 V ±10%			(1.5 + n) T – 50	ns
		V_{DD} = 2.0 V ±10%			(1.5 + n) T – 90	ns

Remark T: t_{CYK} = 1/f_{XX} (f_{XX}: Main system clock frequency)
a: 1 (during address wait), otherwise, 0
n: Number of wait states (n ≥ 0)

AC Characteristics

(T_A = −40°C to +85°C, V_{DD} = V_{DD0} = V_{DD1} = AV_{DD} = 1.8 to 5.5 V, V_{SS} = V_{SS0} = V_{SS1} = AV_{SS} = 0 V)

(1) Read/write operation (2/3)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Delay time from ASTB↓ to $\overline{RD}$↓	t_{DSTR}	V_{DD} = 5.0 V ±10%	0.5T – 9			ns
		V_{DD} = 3.0 V ±10%	0.5T – 9			ns
		V_{DD} = 2.0 V ±10%	0.5T – 20			ns
Data hold time (from $\overline{RD}$↑)	t_{HRID}	V_{DD} = 5.0 V ±10%	0			ns
		V_{DD} = 3.0 V ±10%	0			ns
		V_{DD} = 2.0 V ±10%	0			ns
Address active time from $\overline{RD}$↑	t_{DRA}	V_{DD} = 5.0 V ±10%	0.5T – 2			ns
		V_{DD} = 3.0 V ±10%	0.5T – 12			ns
		V_{DD} = 2.0 V ±10%	0.5T – 35			ns
Delay time from $\overline{RD}$↑ to ASTB↑	t_{DRST}	V_{DD} = 5.0 V ±10%	0.5T – 9			ns
		V_{DD} = 3.0 V ±10%	0.5T – 9			ns
		V_{DD} = 2.0 V ±10%	0.5T – 40			ns
$\overline{RD}$ low-level width	t_{WRL}	V_{DD} = 5.0 V ±10%	(1.5 + n) T – 25			ns
		V_{DD} = 3.0 V ±10%	(1.5 + n) T – 30			ns
		V_{DD} = 2.0 V ±10%	(1.5 + n) T – 25			ns
Delay time from address to $\overline{WR}$↓	t_{DAW}	V_{DD} = 5.0 V ±10%	(1 + a) T – 24			ns
		V_{DD} = 3.0 V ±10%	(1 + a) T – 34			ns
		V_{DD} = 2.0 V ±10%	(1 + a) T – 70			ns
Address hold time (from $\overline{WR}$↑)	t_{HRD}	V_{DD} = 5.0 V ±10%	0.5T – 14			ns
		V_{DD} = 3.0 V ±10%	0.5T – 14			ns
		V_{DD} = 2.0 V ±10%	0.5T – 14			ns
Delay time from ASTB↓ to data output	t_{DSTOD}	V_{DD} = 5.0 V ±10%			0.5T + 15	ns
		V_{DD} = 3.0 V ±10%			0.5T + 30	ns
		V_{DD} = 2.0 V ±10%			0.5T + 240	ns
Delay time from $\overline{WR}$↓ to data output	t_{DWOD}	V_{DD} = 5.0 V ±10%			0.5T – 30	ns
		V_{DD} = 3.0 V ±10%			0.5T – 30	ns
		V_{DD} = 2.0 V ±10%			0.5T – 30	ns
Delay time from ASTB↓ to $\overline{WR}$↓	t_{DSTW}	V_{DD} = 5.0 V ±10%	0.5T – 9			ns
		V_{DD} = 3.0 V ±10%	0.5T – 9			ns
		V_{DD} = 2.0 V ±10%	0.5T – 20			ns
Data setup time (to $\overline{WR}$↑)	t_{SODWR}	V_{DD} = 5.0 V ±10%	(1.5 + n) T – 20			ns
		V_{DD} = 3.0 V ±10%	(1.5 + n) T – 25			ns
		V_{DD} = 2.0 V ±10%	(1.5 + n) T – 70			ns

Remark T: t_{CYK} = 1/f_{XX} (f_{XX}: Main system clock frequency)
a: 1 (during address wait), otherwise, 0
n: Number of wait states (n ≥ 0)

AC Characteristics

(T_A = –40°C to +85°C, V_{DD} = V_{DD0} = V_{DD1} = AV_{DD} = 1.8 to 5.5 V, V_{SS} = V_{SS0} = V_{SS1} = AV_{SS} = 0 V)

(1) Read/write operation (3/3)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data hold time (from $\overline{WR}$↑)	t_{HWOD}	V_{DD} = 5.0 V ±10%	0.5T – 14			ns
		V_{DD} = 3.0 V ±10%	0.5T – 14			ns
		V_{DD} = 2.0 V ±10%	0.5T – 50			ns
Delay time from $\overline{WR}$↑ to ASTB↑	t_{DWST}	V_{DD} = 5.0 V ±10%	0.5T – 9			ns
		V_{DD} = 3.0 V ±10%	0.5T – 9			ns
		V_{DD} = 2.0 V ±10%	0.5T – 30			ns
$\overline{WR}$ low-level width	t_{WWL}	V_{DD} = 5.0 V ±10%	(1.5 + n) T – 25			ns
		V_{DD} = 3.0 V ±10%	(1.5 + n) T – 30			ns
		V_{DD} = 2.0 V ±10%	(1.5 + n) T – 30			ns

Remark T: t_{CYK} = 1/f_{XX} (f_{XX}: Main system clock frequency)
a: 1 (during address wait), otherwise, 0
n: Number of wait states (n ≥ 0)

AC Characteristics (T_A = –40°C to +85°C, $V_{DD} = V_{DD0} = V_{DD1} = AV_{DD}$ = 1.8 to 5.5 V, $V_{SS} = V_{SS0} = V_{SS1} = AV_{SS}$ = 0 V)

(2) External wait timing (1/2)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input time from address to $\overline{WAIT}$↓	t_{DAWT}	V_{DD} = 5.0 V ±10%			(2 + a) T – 40	ns
		V_{DD} = 3.0 V ±10%			(2 + a) T – 60	ns
		V_{DD} = 2.0 V ±10%			(2 + a) T – 300	ns
Input time from ASTB↓ to $\overline{WAIT}$↓	t_{DSTWT}	V_{DD} = 5.0 V ±10%			1.5T – 40	ns
		V_{DD} = 3.0 V ±10%			1.5T – 60	ns
		V_{DD} = 2.0 V ±10%			1.5T – 260	ns
Hold time from ASTB↓ to $\overline{WAIT}$	t_{HSTWT}	V_{DD} = 5.0 V ±10%	(0.5 + n) T + 5			ns
		V_{DD} = 3.0 V ±10%	(0.5 + n) T + 10			ns
		V_{DD} = 2.0 V ±10%	(0.5 + n) T + 30			ns
Delay time from ASTB↓ to $\overline{WAIT}$↑	t_{DSTWTH}	V_{DD} = 5.0 V ±10%			(1.5 + n) T – 40	ns
		V_{DD} = 3.0 V ±10%			(1.5 + n) T – 60	ns
		V_{DD} = 2.0 V ±10%			(1.5 + n) T – 90	ns
Input time from $\overline{RD}$↓ to $\overline{WAIT}$↓	t_{DRWTL}	V_{DD} = 5.0 V ±10%			T – 40	ns
		V_{DD} = 3.0 V ±10%			T – 60	ns
		V_{DD} = 2.0 V ±10%			T – 70	ns
Hold time from $\overline{RD}$↓ to $\overline{WAIT}$↓	t_{HRWT}	V_{DD} = 5.0 V ±10%	nT + 5			ns
		V_{DD} = 3.0 V ±10%	nT + 10			ns
		V_{DD} = 2.0 V ±10%	nT + 30			ns
Delay time from $\overline{RD}$↓ to $\overline{WAIT}$↑	t_{DRWTH}	V_{DD} = 5.0 V ±10%			(1 + n) T – 40	ns
		V_{DD} = 3.0 V ±10%			(1 + n) T – 60	ns
		V_{DD} = 2.0 V ±10%			(1 + n) T – 90	ns
Input time from $\overline{WAIT}$↑ to data	t_{DWTID}	V_{DD} = 5.0 V ±10%			0.5T – 5	ns
		V_{DD} = 3.0 V ±10%			0.5T – 10	ns
		V_{DD} = 2.0 V ±10%			0.5T – 30	ns
Delay time from $\overline{WAIT}$↑ to $\overline{RD}$↑	t_{DWTR}	V_{DD} = 5.0 V ±10%	0.5T			ns
		V_{DD} = 3.0 V ±10%	0.5T			ns
		V_{DD} = 2.0 V ±10%	0.5T + 5			ns
Delay time from $\overline{WAIT}$↑ to $\overline{WR}$↑	t_{DWTW}	V_{DD} = 5.0 V ±10%	0.5T			ns
		V_{DD} = 3.0 V ±10%	0.5T			ns
		V_{DD} = 2.0 V ±10%	0.5T + 5			ns
Delay time from $\overline{WR}$↓ to $\overline{WAIT}$↓	t_{DWWTL}	V_{DD} = 5.0 V ±10%			T – 40	ns
		V_{DD} = 3.0 V ±10%			T – 60	ns
		V_{DD} = 2.0 V ±10%			T – 90	ns

Remark T: $t_{CYK} = 1/f_{XX}$ (f_{XX}: Main system clock frequency)
a: 1 (during address wait), otherwise, 0
n: Number of wait states ($n \geq 0$)

(2) External wait timing (2/2)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Hold time from $\overline{WR}\downarrow$ to $\overline{WAIT}$	t_{HWWT}	V_{DD} = 5.0 V ±10%	nT + 5			ns
		V_{DD} = 3.0 V ±10%	nT + 10			ns
		V_{DD} = 2.0 V ±10%	nT + 30			ns
Delay time from $\overline{WR}\downarrow$ to $\overline{WAIT}\uparrow$	t_{DWWTH}	V_{DD} = 5.0 V ±10%			(1 + n) T – 40	ns
		V_{DD} = 3.0 V ±10%			(1 + n) T – 60	ns
		V_{DD} = 2.0 V ±10%			(1 + n) T – 90	ns

Remark T: t_{CYK} = 1/f_{XX} (f_{XX}: Main system clock frequency)
a: 1 (during address wait), otherwise, 0
n: Number of wait states ($n \geq 0$)

Serial Operation (T_A = −40°C to +85°C, V_{DD} = V_{DD0} = V_{DD1} = AV_{DD} = 1.8 to 5.5 V, V_{SS} = V_{SS0} = V_{SS1} = AV_{SS} = 0 V)

(a) 3-wire serial I/O mode ($\overline{SCK}$: Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY1}	2.7 V ≤ V_{DD} ≤ 5.5 V	800			ns
			3,200			ns
$\overline{SCK}$ high-/low-level width	t_{KH1}, t_{KL1}	2.7 V ≤ V_{DD} ≤ 5.5 V	350			ns
			1,500			ns
SI setup time (to $\overline{SCK}$↑)	t_{SIK1}	2.7 V ≤ V_{DD} ≤ 5.5 V	10			ns
			30			ns
SI hold time (from $\overline{SCK}$↑)	t_{KSI1}		40			ns
SO output delay time (from $\overline{SCK}$↓)	t_{KSO1}				30	ns

(b) 3-wire serial I/O mode ($\overline{SCK}$: External clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY2}	2.7 V ≤ V_{DD} ≤ 5.5 V	800			ns
			3,200			ns
$\overline{SCK}$ high-/low-level width	t_{KH2}	2.7 V ≤ V_{DD} ≤ 5.5 V	400			ns
	t_{KL2}		1,600			ns
SI setup time (to $\overline{SCK}$↑)	t_{SIK2}	2.7 V ≤ V_{DD} ≤ 5.5 V	10			ns
			30			ns
SI hold time (from $\overline{SCK}$↑)	t_{KSI2}		40			ns
SO output delay time (from $\overline{SCK}$↓)	t_{KSO2}				30	ns

(c) UART mode

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
ASCK cycle time	t_{KCY3}	4.5 V ≤ V_{DD} ≤ 5.5 V	417			ns
		2.7 V ≤ V_{DD} < 4.5 V	833			ns
			1,667			ns
ASCK high-/low-level width	t_{KH3}	4.5 V ≤ V_{DD} ≤ 5.5 V	208			ns
	t_{KL3}	2.7 V ≤ V_{DD} < 4.5 V	416			ns
			833			ns

(d) I^2C bus mode (μPD784225Y only)

Parameter		Symbol	Standard Mode		High-Speed Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
SCL0 clock frequency		f_{CLK}	0	100	0	400	kHz
Bus free time (between stop and start conditions)		t_{BUF}	4.7	–	1.3	–	μs
Hold time**Note1**		$t_{HD:STA}$	4.0	–	0.6	–	μs
Low-level width of SCL0 clock		t_{LOW}	4.7	–	1.3	–	μs
High-level width of SCL0 clock		t_{HIGH}	4.0	–	0.6	–	μs
Setup time of start/restart conditions		$t_{SU:STA}$	4.7	–	0.6	–	μs
Data hold time	When using CBUS-compatible master	$t_{HD:DAT}$	5.0	–	–	–	μs
	When using I^2C bus		0**Note 2**	–	0**Note 2**	0.9**Note 3**	μs
Data setup time		$t_{SU:DAT}$	250	–	100**Note 4**	–	ns
Rising time of SDA0 and SCL0 signals		t_R	–	1,000	20 + 0.1Cb**Note 5**	300	ns
Falling time of SDA0 and SCL0 signals		t_F	–	300	20 + 0.1Cb**Note 5**	300	ns
Setup time of stop condition		$t_{SU:STO}$	4.0	–	0.6	–	μs
Pulse width of spike restricted by input filter		t_{SP}	–	–	0	50	ns
Load capacitance of each bus line		Cb	–	400	–	400	pF

Notes 1. For the start condition, the first clock pulse is generated after the hold time.

2. To fill the undefined area of the SCL0 falling edge, it is necessary for the device to provide an internal SDA0 signal (on $V_{IHmin.}$) with at least 300 ns of hold time.

3. If the device does not extend the SCL0 signal low-level hold time (t_{LOW}), only the maximum data hold time $t_{HD:DAT}$ needs to be satisfied.

4. The high-speed mode I^2C bus can be used in a standard mode I^2C bus system. In this case, the conditions described below must be satisfied.

- If the device does not extend the SCL0 signal low-level hold time
  $t_{SU:DAT} \geq 250$ ns
- If the device extends the SCL0 signal low-level hold time
  Be sure to transmit the data bit to the SDA0 line before the SCL0 line is released ($t_{Rmax.} + t_{SU:DAT}$ = 1,000 + 250 = 1,250 ns by standard mode I^2C bus specification)

5. Cb: Total capacitance per bus line (unit: pF)

Other Operations (T_A = –40°C to +85°C, $V_{DD} = V_{DD0} = V_{DD1} = AV_{DD}$ = 1.8 to 5.5 V, $V_{SS} = V_{SS0} = V_{SS1} = AV_{SS}$ = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
NMI high-/low-level width	t_{WNIL} t_{WNIH}		10			μs
INTP input high-/low-level width	t_{WITL} t_{WITH}	INTP0 to INTP6	100			ns
$\overline{\text{RESET}}$ high-/low-level width	t_{WRSL} t_{WRSH}		10			μs

Clock Output Operation

(T_A = –40°C to +85°C, $V_{DD} = V_{DD0} = V_{DD1} = AV_{DD}$ = 1.8 to 5.5 V, $V_{SS} = V_{SS0} = V_{SS1} = AV_{SS}$ = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
PCL cycle time	t_{CYCL}	4.5 V ≤ V_{DD} ≤ 5.5 V, nT	80		31,250	ns
PCL high-/low-level width	t_{CLL} t_{CLH}	4.5 V ≤ V_{DD} ≤ 5.5 V, 0.5T – 10	30		15,615	ns
PCL rising/falling time	t_{CLR} t_{CLF}	4.5 V ≤ V_{DD} ≤ 5.5 V			5	ns
		2.7 V ≤ V_{DD} < 4.5 V			10	ns
		1.8 V ≤ V_{DD} < 2.7 V			20	ns

Remark T: t_{CYK} = 1/f_{XX} (f_{XX}: Main system clock frequency)

n: Divided frequency ratio set by software in the CPU

- When using the main system clock: n = 1, 2, 4, 8, 16, 32, 64, 128
- When using the subsystem clock: n = 1

A/D Converter Characteristics

(T_A = –40°C to +85°C, V_{DD} = V_{DD0} = V_{DD1} = AV_{DD} = 1.8 to 5.5 V, V_{SS} = V_{SS0} = V_{SS1} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Overall error[Note]		6.25 MHz < f_{XX} ≤ 12.5 MHz, 4.5 V ≤ V_{DD} ≤ 5.5 V, AV_{DD} = V_{DD0}			±1.2	%FSR
		3.125 MHz < f_{XX} ≤ 6.25 MHz, 2.7 V ≤ V_{DD} ≤ 5.5 V, AV_{DD} = V_{DD0}			±1.2	%FSR
		2 MHz < f_{XX} ≤ 3.125 MHz, 2.0 V ≤ V_{DD} ≤ 5.5 V, AV_{DD} = V_{DD0}			±1.6	%FSR
		f_{XX} = 2 MHz, 1.8 V ≤ V_{DD} ≤ 5.5 V AV_{DD} = V_{DD0}			±1.6	%FSR
Conversion time	t_{CONV}		14		144	μs
Sampling time	t_{SAMP}		24/f_{XX}			μs
Analog input voltage	V_{IAN}		AV_{SS}		AV_{DD}	V
Reference voltage	AV_{DD}		V_{DD}	V_{DD}	V_{DD}	V
Resistance between AV_{DD} and AV_{SS}	R_{AVREF0}	A/D conversion is not performed		40		kΩ

Note Excludes quantization error (±0.2%FSR).

Remark FSR: Full-scale range

D/A Converter Characteristics

(T_A = –40°C to +85°C, V_{DD} = V_{DD0} = V_{DD1} = AV_{DD} = 1.8 to 5.5 V, V_{SS} = V_{SS0} = V_{SS1} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution				8	8	8	bit
Overall error[Note]		2.0 V ≤ V_{DD} ≤ 5.5 V R = 10 MΩ, 2.0 V ≤ AV_{REF1} ≤ 5.5 V				±0.6	%FSR
		1.8 V ≤ V_{DD} ≤ 2.0 V R = 10 MΩ, 1.8 V ≤ AV_{REF1} ≤ 5.5 V				±1.2	%FSR
Settling time		Load conditions: C = 30 pF	4.5 V ≤ AV_{REF1} ≤ 5.5 V			10	μs
			2.7 V ≤ AV_{REF1} < 4.5 V			15	μs
			1.8 V ≤ AV_{REF1} < 2.7 V			20	μs
Output resistance	R_O	DACS0, 1 = 55H			8		kΩ
Reference voltage	AV_{REF1}			1.8		V_{DD0}	V
AV_{REF1} current	AI_{REF1}	For only 1 channel				2.5	mA

Note Excludes quantization error (±0.2%FSR).

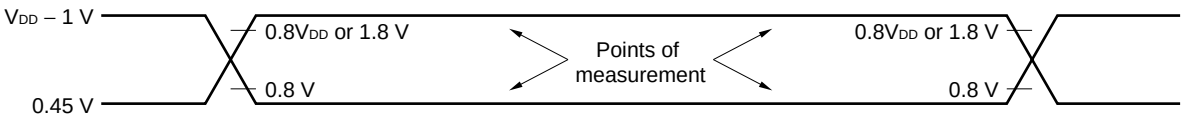
Remark FSR: Full-scale range

Data Retention Characteristics

(T_A = −40°C to +85°C, V_{DD} = V_{DD0} = V_{DD1} = AV_{DD} = 1.8 to 5.5 V, V_{SS} = V_{SS0} = V_{SS1} = AV_{SS} = 0 V)

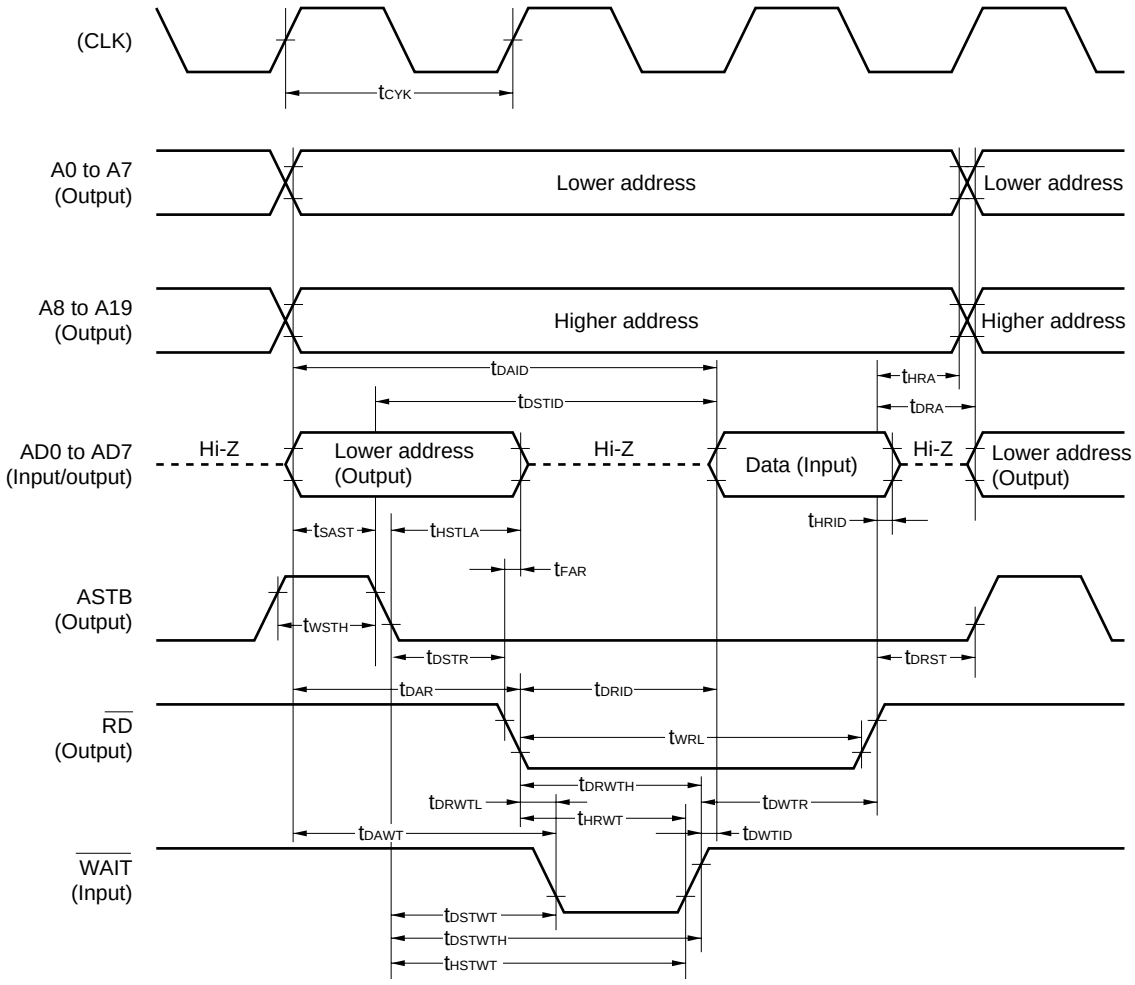
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention voltage	V_{DDDR}	STOP mode	1.8		5.5	V
Data retention current	I_{DDDR}	V_{DDDR} = 5.0 V ±10%		10	50	μA
		V_{DDDR} = 2.0 V ±10%		2	10	μA
V_{DD} rise time	t_{RVD}		200			μs
V_{DD} fall time	t_{FVD}		200			μs
V_{DD} hold time (from STOP mode setting)	t_{HVD}		0			ms
STOP release signal input time	t_{DREL}		0			ms
Oscillation stabilization wait time	t_{WAIT}	Crystal resonator	30			ms
		Ceramic resonator	5			ms
Low-level input voltage	V_{IL}	$\overline{\text{RESET}}$, P00/INTP0 to P06/INTP6	0		$0.1V_{DDDR}$	V
High-level input voltage	V_{IH}		$0.9V_{DDDR}$		V_{DDDR}	V

AC Timing Measurement Points

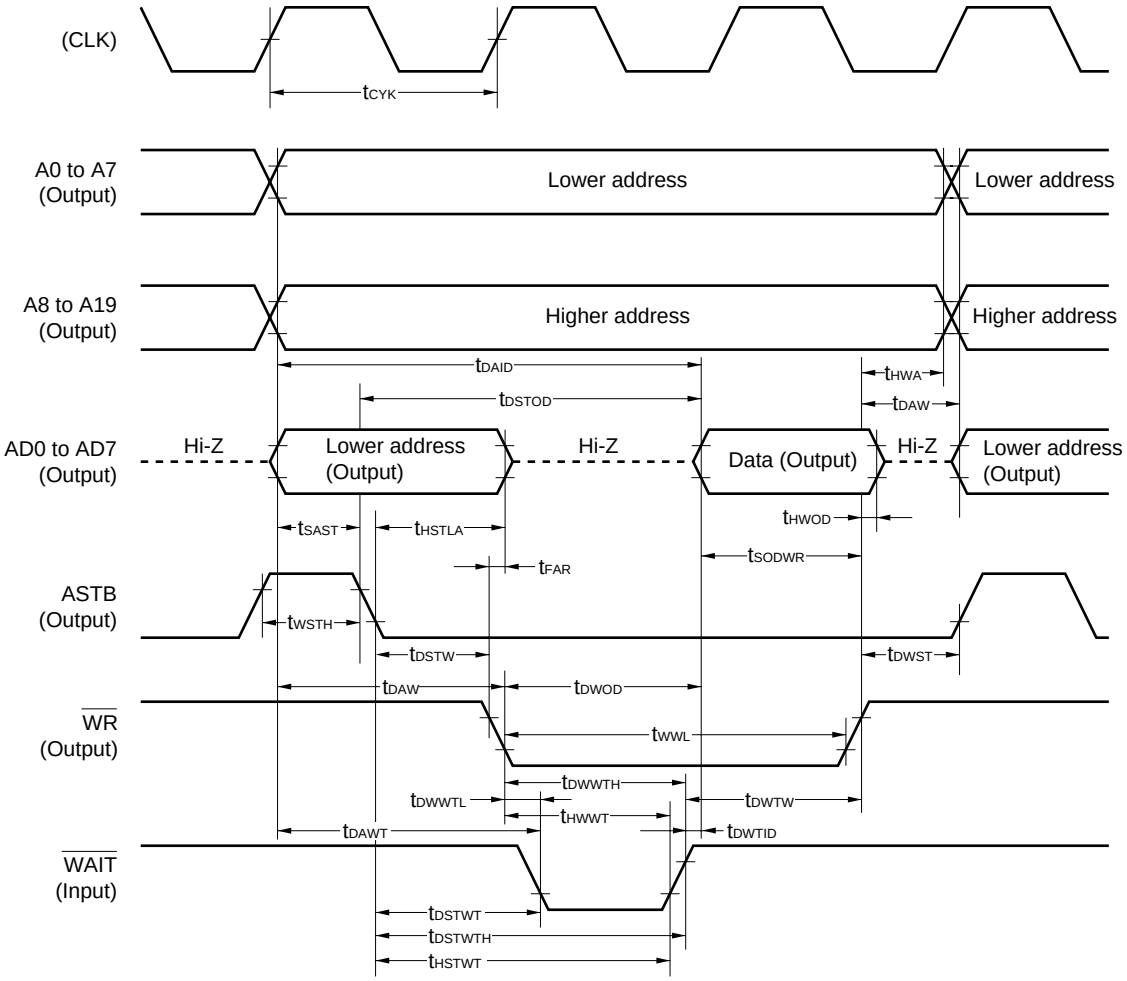


Timing Waveform

(1) Read operation

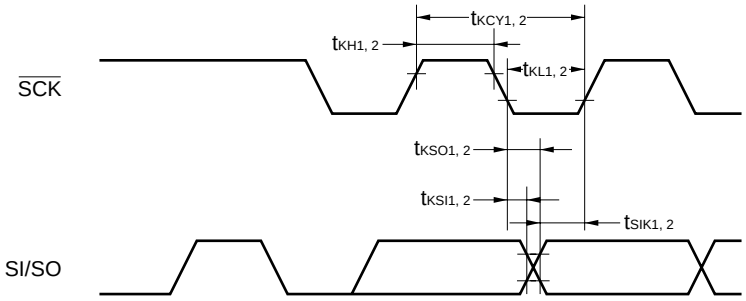


(2) Write operation

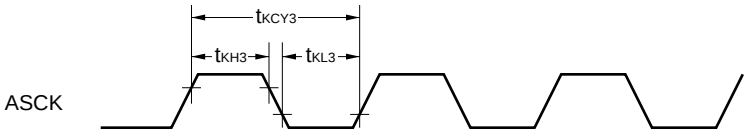


Serial Operation

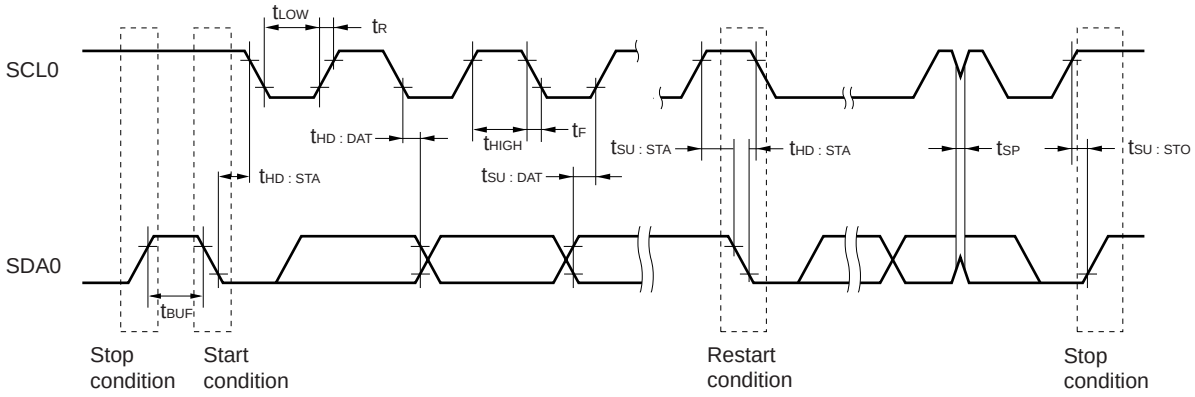
(1) 3-wire serial I/O mode



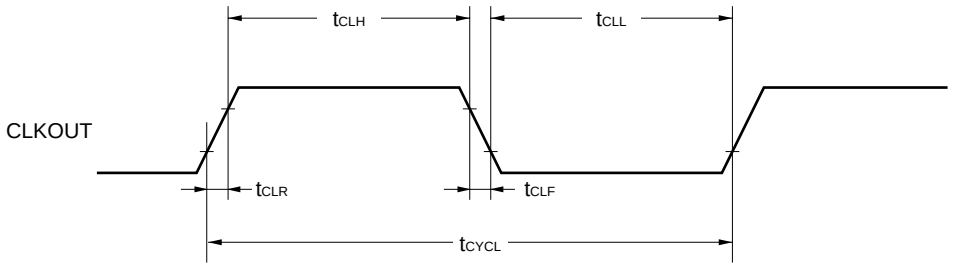
(2) UART mode



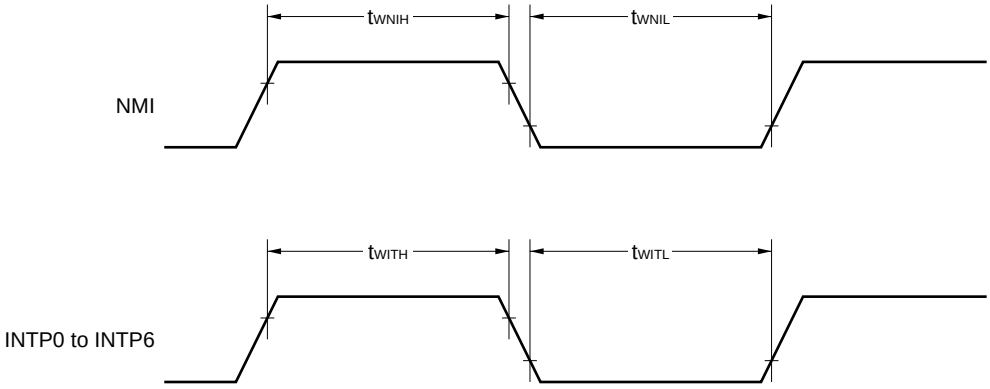
(3) I²C bus mode (μPD784255Y Subseries only)



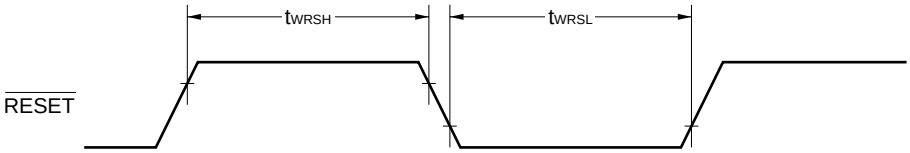
Clock Output Timing



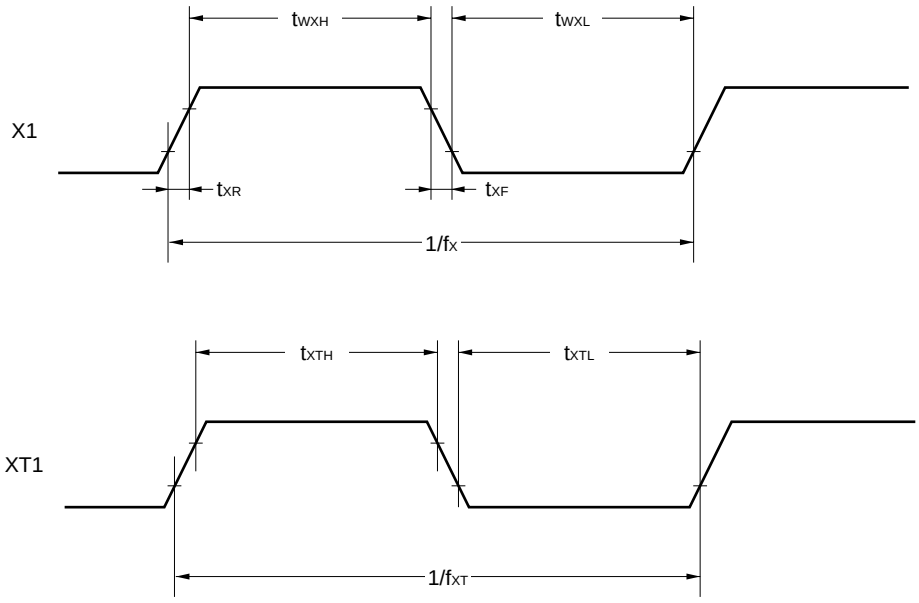
Interrupt Input Timing



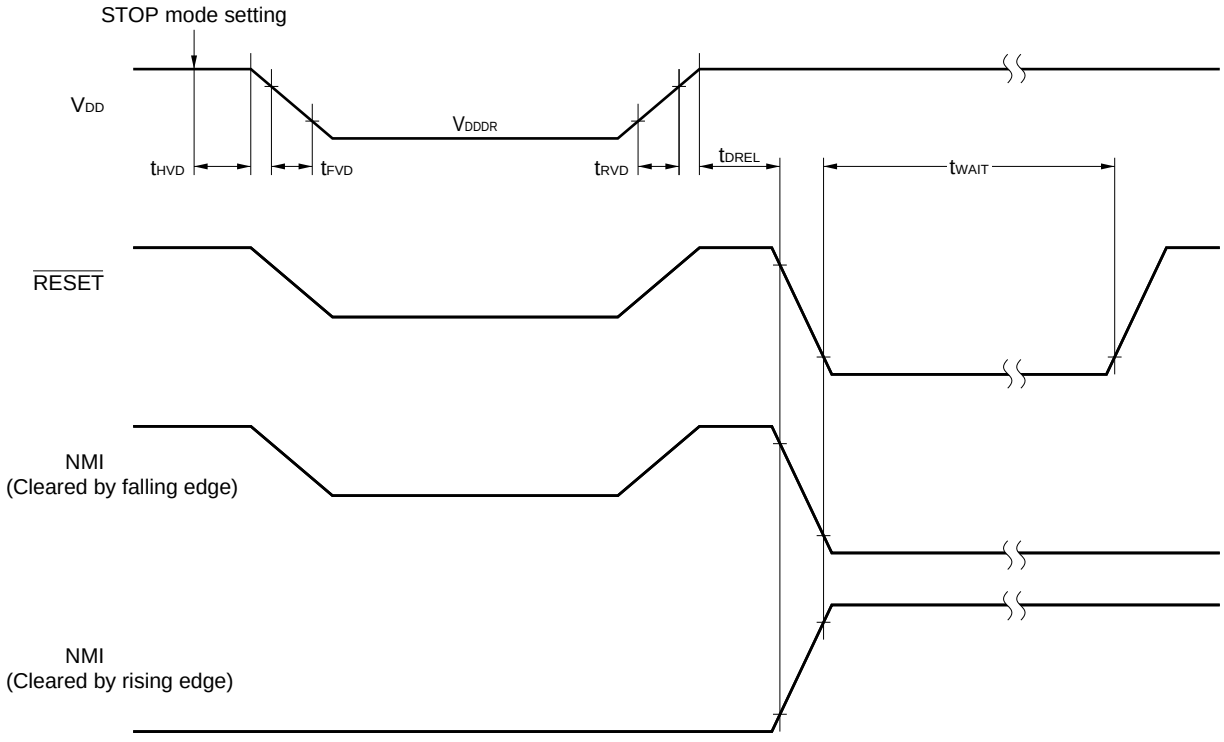
Reset Input Timing



Clock Timing

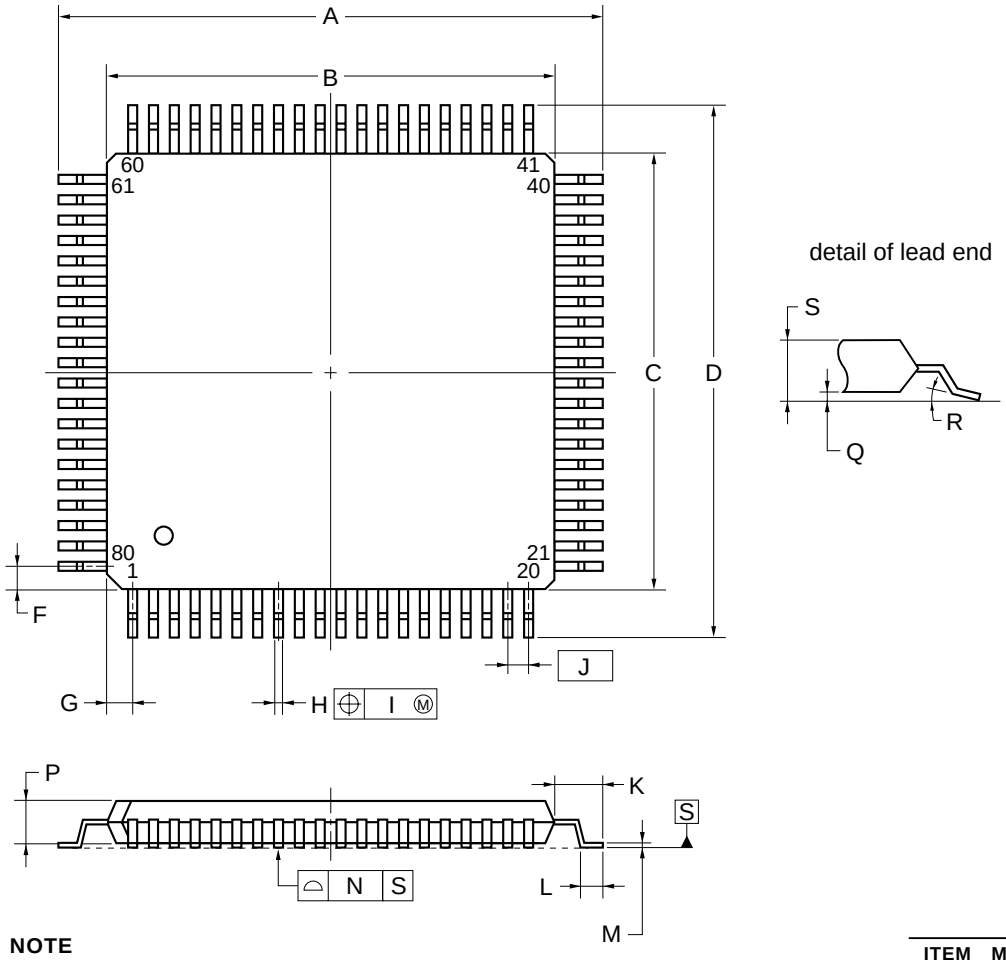


Data Retention Characteristics



★ 15. PACKAGE DRAWINGS

80-PIN PLASTIC QFP (14x14)



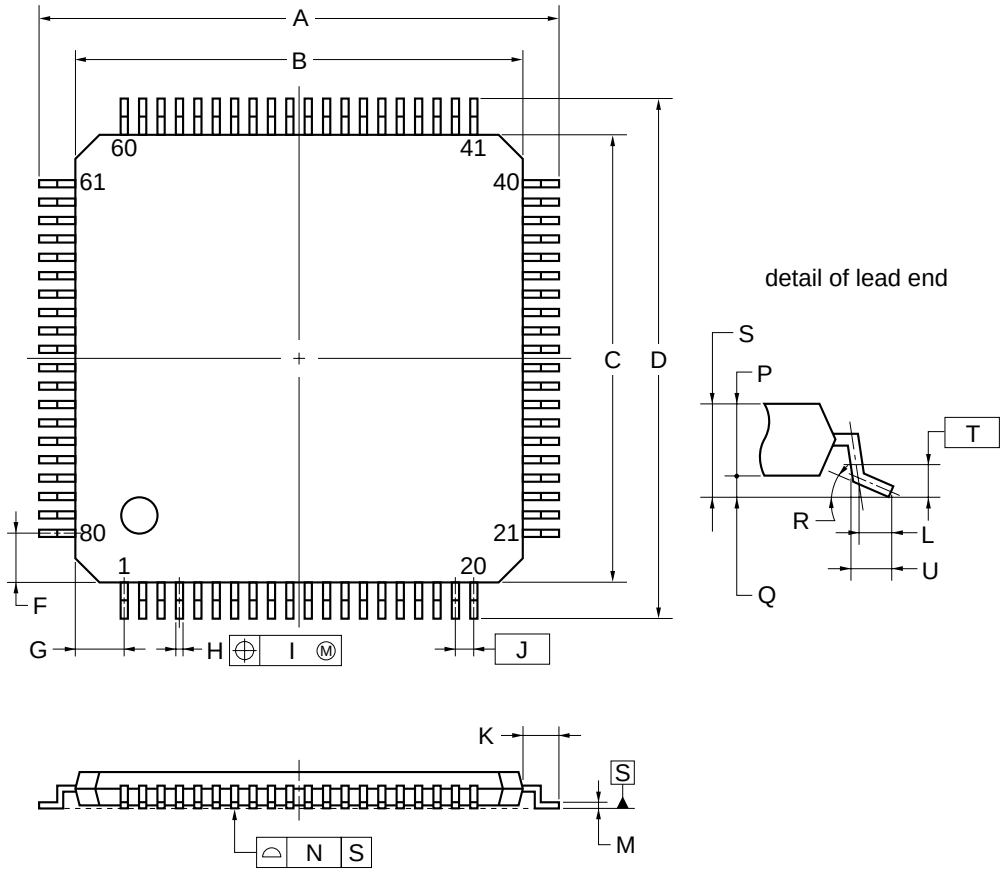
NOTE

Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	17.20±0.20
B	14.00±0.20
C	14.00±0.20
D	17.20±0.20
F	0.825
G	0.825
H	0.32±0.06
I	0.13
J	0.65 (T.P.)
K	1.60±0.20
L	0.80±0.20
M	$0.17^{+0.03}_{-0.07}$
N	0.10
P	1.40±0.10
Q	0.125±0.075
R	3^{+7}_{-3}
S	1.70 MAX.

P80GC-65-8BT-1

80-PIN PLASTIC TQFP (FINE PITCH) (12x12)



NOTE

Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	14.0±0.2
B	12.0±0.2
C	12.0±0.2
D	14.0±0.2
F	1.25
G	1.25
H	0.22±0.05
I	0.08
J	0.5 (T.P.)
K	1.0±0.2
L	0.5
M	0.145±0.05
N	0.08
P	1.0
Q	0.1±0.05
R	3^{+4}_{-3}
S	1.1±0.1
T	0.25
U	0.6±0.15

P80GK-50-9EU-1

★ 16. RECOMMENDED SOLDERING CONDITIONS

The μPD784225 should be soldered and mounted under the following recommended conditions.

For the details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

Caution Soldering conditions for the μPD784224GC-×××-8BT, μPD784225YGC-×××-8BT, and μPD784225YGK-×××-9EU are undetermined because these products are under development.

Table 16-1. Soldering Conditions for Surface Mount Type

(1) μPD784225GC-×××-8BT: 80-pin plastic QFP (14 × 14 mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Two times or less, Exposure limit: 7 days[Note] (after that, prebake at 125°C for 20 hours)	IR35-00-2
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: Two times or less, Exposure limit: 7 days[Note] (after that, prebake at 125°C for 20 hours)	VP15-00-2
Wave soldering	Solder bath temperature: 260°C max., Time: 10 seconds max., Count: Once, Preheating temperature: 120°C max. (package surface temperature) Exposure limit: 7 days[Note] (after that, prebake at 125°C for 20 hours)	—
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)	—

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

(2) μPD784224GK-×××-9EU: 80-pin plastic TQFP (fine pitch) (14 × 20 mm)
μPD784225GK-×××-9EU: 80-pin plastic TQFP (fine pitch) (14 × 20 mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Two times or less, Exposure limit: 7 days[Note] (after that, prebake at 125°C for 20 hours)	IR35-103-2
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: Two times or less, Exposure limit: 7 days[Note] (after that, prebake at 125°C for 20 hours)	VP15-103-2
Wave soldering	Solder bath temperature: 260°C max., Time: 10 seconds max., Count: Once, Preheating temperature: 120°C max. (package surface temperature)	—
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)	—

Caution Do not use different soldering methods together (except for partial heating).

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD784225. Also see **(5)**.

(1) Language Processing Software

RA78K4	Assembler package common to 78K/IV Series
CC78K4	C compiler package common to 78K/IV Series
DF784225	Device file common to μPD784225, 784225Y Subseries
CC78K4-L	C compiler library source file common to 78K/IV Series

(2) Flash Memory Writing Tools

Flashpro II (Part No.: FL-PR2), Flashpro III (Part No.: FL-PR3, PG-FP3)	Dedicated flash programmer for microcontroller incorporating flash memory
FA-80GC	Adapter for writing 80-pin plastic QFP (GC-8BT type) flash memory.
FA-80GK	Adapter for writing 80-pin plastic LQFP (GK-BE9 type) flash memory.

(3) Debugging Tools

- **When IE-78K4-NS in-circuit emulator is used**

IE-78K4-NS	In-circuit emulator common to 78K/IV Series
IE-70000-MC-PS-B	Power supply unit for IE-78K4-NS
IE-70000-98-IF-C	Interface adapter used when PC-9800 series PC (except notebook type) is used as host machine (C bus supported)
IE-70000-CD-IF-A	PC card and cable when notebook PC is used as host machine (PCMCIA socket supported)
IE-70000-PC-IF-C	Interface adapter when using IBM PC/AT™ or compatible as host machine (ISA bus supported)
IE-70000-PCI-IF	Interface adapter when using PC that incorporates PCI bus as host machine
IE-784225-NS-EM1	Emulation board to emulate μPD784225, 784225Y Subseries
NP-100GF	Emulation probe for 100-pin plastic QFP (GF-3BA type)
NP-100GC	Emulation probe for 100-pin plastic LQFP (GC-8EU type)
EV-9200GF-100	Socket to be mounted on a target system board made for 100-pin plastic QFP (GF-3BA type)
TGC-100SDW	Conversion adapter to connect the NP-100GC and a target system board on which a 100-pin plastic LQFP (GC-8EU type) can be mounted
ID78K4-NS	Integrated debugger for IE-78K4-NS
SM78K4	System simulator common to 78K/IV Series
DF784225	Device file common to μPD784225, 784225Y Subseries

- **When IE-784000-R in-circuit emulator is used**

IE-784000-R	In-circuit emulator common to 78K/IV Series
IE-70000-98-IF-C	Interface adapter used when PC-9800 series PC (except notebook type) is used as host machine (C bus supported)
IE-70000-PC-IF-C	Interface adapter when using IBM PC/AT or compatible as host machine (ISA bus supported)
IE-70000-PCI-IF	Interface adapter when using PC that incorporates PCI bus as host machine
IE-78000-R-SV3	Interface adapter and cable used when EWS is used as host machine
IE-784225-NS-EM1 IE-784218-R-EM1	Emulation board to emulate μPD784225, 784225Y Subseries
IE-784000-R-EM	Emulation board common to 78K/IV Series
IE-78K4-R-EX3	Emulation probe conversion board necessary when using IE-784225-NS-EM1 on IE-784000-R. Not necessary when IE-784216-R-EM1 is used.
EP-78064GF-R	Emulation probe for 100-pin plastic QFP (GF-3BA type)
EP-78064GC-R	Emulation probe for 100-pin plastic LQFP (GC-8EU type)
EV-9200GF-100	Socket to be mounted on a target system board made for 100-pin plastic QFP (GF-3BA type)
TGC-100SDW	Conversion adapter to connect the NP-100GC and a target system board on which a 100-pin plastic LQFP (GC-8EU type) can be mounted
ID78K4	Integrated debugger for IE-784000-R
SM78K4	System simulator common to 78K/IV Series
DF784225	Device file common to μPD784225, 784225Y Subseries

(4) Real-time OS

RX78K/IV	Real-time OS for 78K/IV Series
MX78K4	OS for 78K/IV Series

(5) Cautions on Using Development Tools

- The ID78K4-NS, ID78K4, and SM78K4 are used in combination with the DF784225.
- The CC78K4 and RX78K/IV are used in combination with the RA78K4 and DF784218.
- The FL-PR2, FL-PR3, FA-100GF, FA-100GC, NP-100GF, and NP-100GC are products made by Naito Densei Machida Mfg. Co., Ltd. (TEL: +81-44-822-3813).
- The TGC-100SDW is a product made by TOKYO ELETECH CORPORATION.
  For further information, contact Daimaru Kogyo, Ltd.
  Tokyo Electronic Division (TEL: +81-3-3820-7112)
  Osaka Electronic Division (TEL: +81-6-6244-6672)
- For third-party development tools, see the **78K/IV Series Selection Guide (U13355E)**.
- The host machine and OS suitable for each software are as follows:

Host Machine [OS] / Software	PC	EWS
	PC-9800 series [Windows] IBM PC/AT and compatibles [Japanese/English Windows]	HP9000 series 700™ [HP-UX™] SPARCstation™ [SunOS™, Solaris™] NEWS™ (RISC) [NEWS-OS™]
RA78K4	○Note	○
CC78K4	○Note	○
ID78K4-NS	○	–
ID78K4	○	○
SM78K4	○	–
RX78K/IV	○Note	○
MX78K4	○Note	○

Note DOS-based software

★ APPENDIX B. RELATED DOCUMENTS

Documents related to device

Document Name	Document No.	
	Japanese	English
μPD784224, 784225, 784224Y, 784225Y Data Sheet	U12376J	This document
μPD78F4225, 78F4225Y Data Sheet	U12377J	Planned
μPD784225, 784225Y Subseries User's Manual - Hardware	Planned	Planned
μPD784225Y Subseries Special Function Register Table	Planned	–
78K/IV Series User's Manual - Instruction	U10905J	U10905E
78K/IV Series Instruction Table	U10594J	–
78K/IV Series Instruction Set	U10595J	–
78K/IV Series Application Note - Software Basics	U10095J	U10095E

Documents related to development tools (User's Manuals)

Document Name		Document No.	
		Japanese	English
RA78K4 Assembler Package	Operation	U11334J	U11334E
	Language	U11162J	U11162E
RA78K Series Structured Assembler Preprocessor		U11743J	U11743E
CC78K4 C Compiler	Operation	U11572J	U11572E
	Language	U11571J	U11571E
IE-78K4-NS		U13356J	U13356E
IE-784000-R		U12903J	U12903E
IE-784218-R-EM1		U12155J	U12155E
IE-784225-NS-EM1		U13742J	U13742E
EP-78064		EEU-934	EEU-1469
SM78K4 System Simulator - Windows Base	Reference	U10093J	U10093E
SM78K Series System Simulator	External component user open interface specification	U10092J	U10092E
ID78K4-NS Integrated Debugger - PC Base	Reference	U12796J	U12796E
ID78K4 Integrated Debugger - Windows Base	Reference	U10440J	U10440E
ID78K4 Integrated Debugger - HP-UX, SunOS, NEWS-OS Base	Reference	U11960J	U11960E

Caution The contents of the above related documents are subject to change without notice. Be sure to use the latest edition of a document for designing.

Documents related to embedded software (User's Manual)

Document Name		Document No.	
		Japanese	English
78K/IV Series Real-Time OS	Basics	U10603J	U10603E
	Installation	U10604J	U10604E
	Debugger	U10364J	–
78K/IV Series OS MX78K4	Basics	U11779J	–

Other documents

Document Name	Document No.	
	Japanese	English
SEMICONDUCTOR SELECTION GUIDE Products & Packages (CD-ROM)	X13769X	
Semiconductor Device Mounting Technology Manual	C10535J	C10535E
Quality Grades on NEC Semiconductor Device	C11531J	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983J	C10983E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892J	C11892E
Semiconductor Device Quality Control/Reliability Handbook	C12769J	MEI-1202
Guide for Products Related to Micro-Computer: Other Companies	U11416J	–

Caution The contents of the above related documents are subject to change without notice. Be sure to use the latest edition of a document for designing.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Caution This product contains an I^2C bus interface circuit.
When using the I^2C bus interface, notify its use to NEC when ordering custom code. NEC can guarantee the following only when the customer informs NEC of the use of the interface:
Purchase of NEC I^2C components conveys a license under the Philips I^2C Patent Rights to use these components in an I^2C system, provided that the system conforms to the I^2C Standard Specification as defined by Philips.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, pIease contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

NEC Electronics Inc. (U.S.)
Santa Clara, California
Tel: 408-588-6000
800-366-9782
Fax: 408-588-6130
800-729-9288

NEC Electronics (Germany) GmbH
Duesseldorf, Germany
Tel: 0211-65 03 02
Fax: 0211-65 03 490

NEC Electronics (UK) Ltd.
Milton Keynes, UK
Tel: 01908-691-133
Fax: 01908-670-290

NEC Electronics Italiana s.r.l.
Milano, Italy
Tel: 02-66 75 41
Fax: 02-66 75 42 99

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Seoul Branch
Seoul, Korea
Tel: 02-528-0303
Fax: 02-528-4411

NEC Electronics Singapore Pte. Ltd.
United Square, Singapore 1130
Tel: 65-253-8311
Fax: 65-250-3583

NEC Electronics Taiwan Ltd.
Taipei, Taiwan
Tel: 02-2719-2377
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  - Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots
  - Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)
  - Specific: Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

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