KS0759

81 COM / 128 SEG DRIVER & CONTROLLER FOR STN LCD

August. 1999.

Ver. 0.2

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KS0759 Specification Revision History		
Version	**Content**	**Date**
0.0	Original	July.1999
0.1	Remove HPMB,CS2 Pin and Change Vol, Voh value	July.1999
0.2	Modify Pad Dimensions and Chip Configuration	Aug.1999

CONTENTS

INTRODUCTION

The KS0759 is a driver & controller LSI for graphic dot-matrix liquid crystal display systems. It contains 81 common and 128 segment driver circuits. This chip is connected directly to a microprocessor, accepts serial or 8-bit parallel display data and stores in an on-chip display data RAM of 81 x 128 bits. It provides a highly flexible display section due to 1-to-1 correspondence between on-chip display data RAM bits and LCD panel pixels. And it performs display data RAM read/write operation with no externally operating clock to minimize power consumption. In addition, because it contains power supply circuits necessary to drive liquid crystal, it is possible to make a display system with the fewest components.

FEATURES

Driver Output Circuits

– 81 common outputs / 128 segment outputs

Applicable Duty Ratios

Programmable duty ratio	Applicable LCD bias	Maximum display area
1/17 to 1/81	1/4 to 1/11	81 × 128

– Various partial display
– Partial window moving & data scrolling

On-chip Display Data RAM

– Capacity: 81 x 128 = 10,368 bits
– Bit data "1": a dot of display is illuminated.
– Bit data "0": a dot of display is not illuminated.

Microprocessor Interface

– 8-bit parallel bi-directional interface with 6800-series or 8080-series.
– SPI (Serial Peripheral Interface) available. (only write operation)

On-chip Low Power Analog Circuit

– On-chip oscillator circuit
– Voltage converter (x3, x4, x5 or x6)
– Voltage regulator (temperature coefficient: -0.05%/°C or external input)
– On-chip electronic contrast control function (64 steps)
– Voltage follower (LCD bias: 1/4 to 1/11)

Operating Voltage Range

– Supply voltage (V_{DD}): 1.8 to 3.3 V
– LCD driving voltage (V_{LCD} = V0 - V_{SS}): 4.0 to 15.0 V

Low power Consumption

– TBD μA Typ. (Internal power supply on and display OFF)

Package Type

– Gold bump chip or TCP

BLOCK DIAGRAM

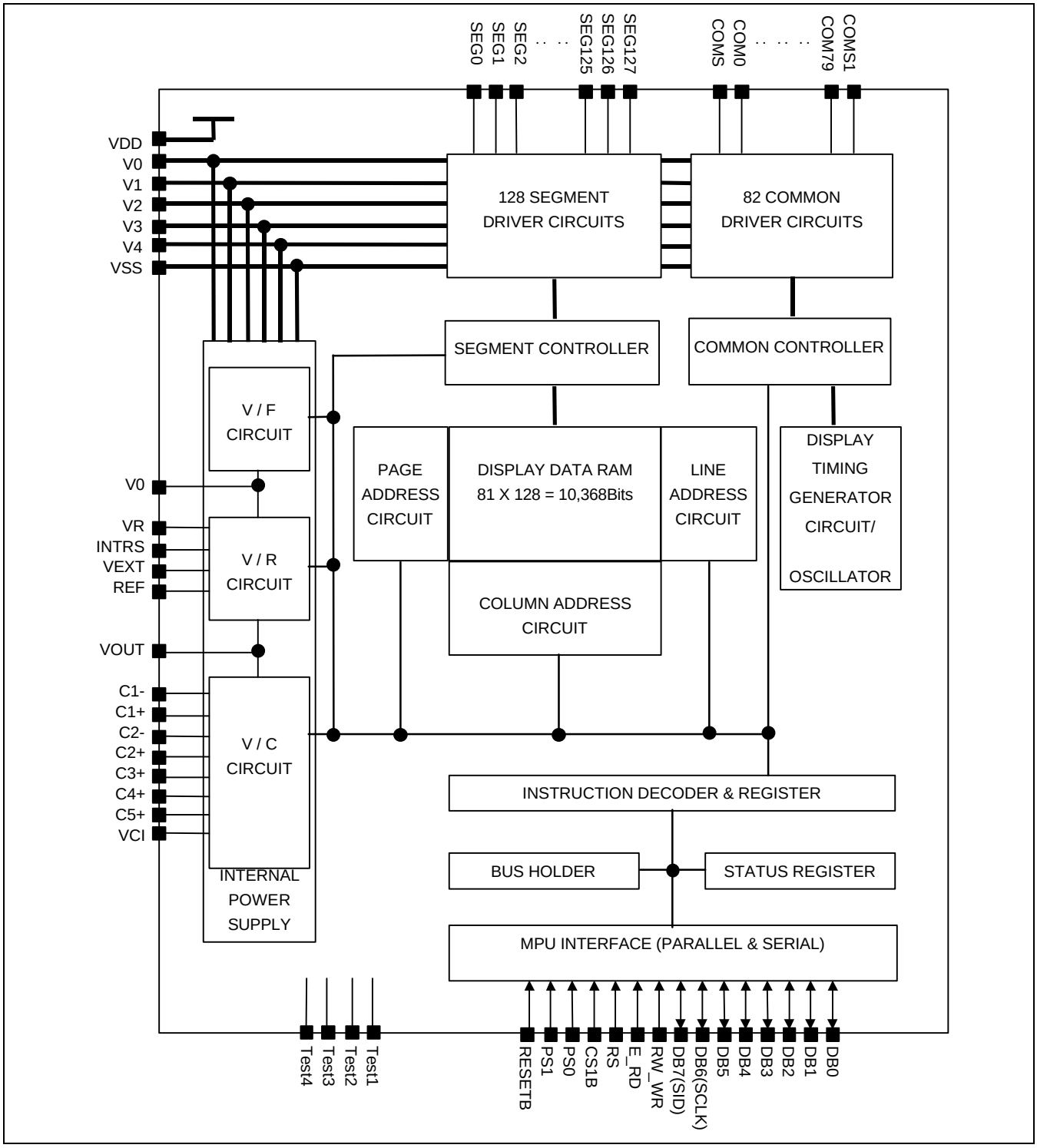


Figure 1. Block Diagram

PAD CONFIGURATION

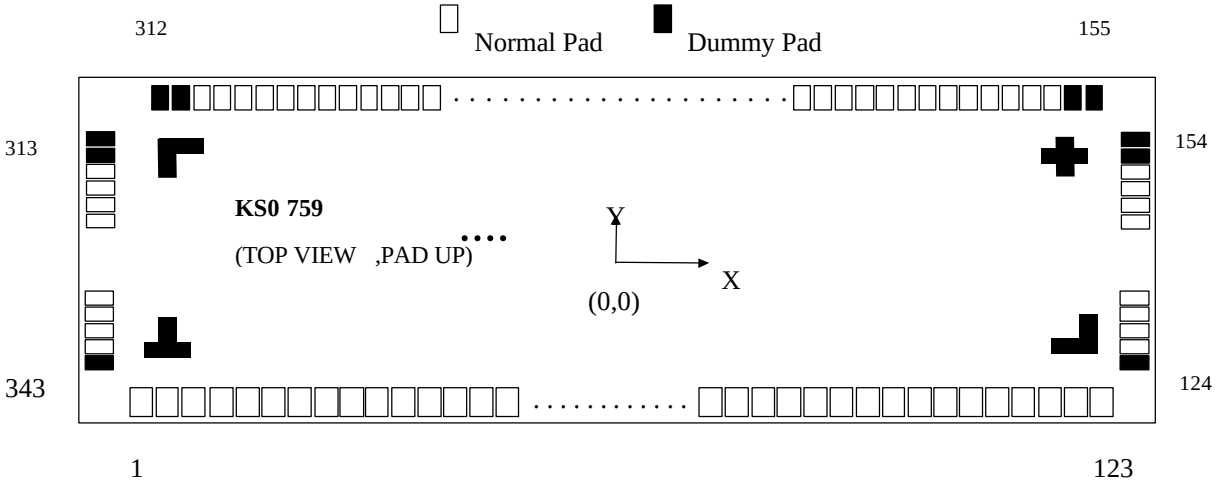


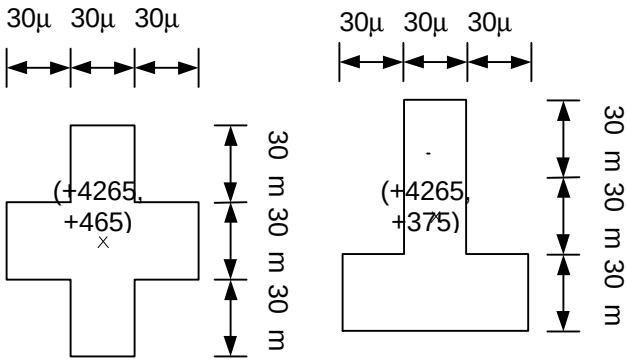
Figure 2. KS0759 Chip Configuration

Table 1. KS0759 Pad Dimension

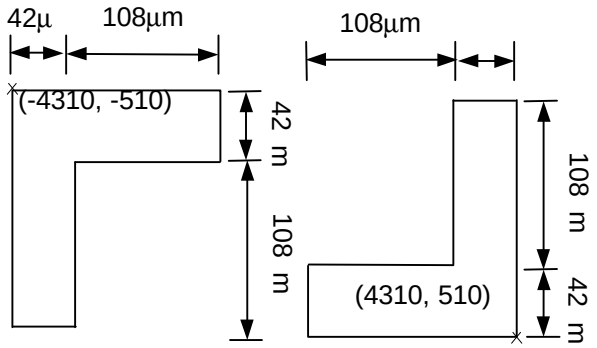
Item	Pad No.		Size X	Size Y	Unit
Chip size	-		9980	2380	um
Pad pitch	Input	1 to 123	70		
	Output	125 to 152	60		
		157 to 310			
		315 to 342			
	NC*	124,343	70		
		154,155,312,313	80		
		153,156,311,314	70 / 80		
Bumped pad size (Max.)	1 to 123		50	100	
	124		110	60	
	125 to 152		110	40	
	153 to 154		110	60	
	155 to 156		60	110	
	157 to 310		40	110	
	311 to 312		60	110	
	313 to 314		110	60	
	315 to 342		110	40	
	343		110	60	
Bumped pad height	All pad		14 (Typ.)		

[**Dummy to Dummy pad pitch is 80 um. Dummy to normal pad pitch is 70 um.**

COG Align Key Coordinate



ILB Align Key Coordinate



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PAD CENTER COORDINATES

Table 1. Pad Center Coordinates

[Unit: μm]

NO.	Name	X	Y	NO.	Name	X	Y	NO.	Name	X	Y	NO.	Name	X	Y
1	PAD_CK	-4270	-1075	51	VSS	-770	-1075	101	V4	2730	-1075	151	COM13	4843	650
2	TEST_CL	-4200	-1075	52	VSS	-700	-1075	102	V4	2800	-1075	152	COM12	4843	710
3	SCL	-4130	-1075	53	VSS	-630	-1075	103	V4	2870	-1075	153	DUMMY	4843	780
4	SDA	-4060	-1075	54	VOUT	-560	-1075	104	V3	2940	-1075	154	DUMMY	4843	860
5	VSS	-3990	-1075	55	VOUT	-490	-1075	105	V3	3010	-1075	155	DUMMY	4740	1043
6	VDD	-3920	-1075	56	VOUT	-420	-1075	106	V3	3080	-1075	156	DUMMY	4660	1043
7	VDD	-3850	-1075	57	VOUT	-350	-1075	107	V3	3150	-1075	157	COM11	4590	1043
8	PS0	-3780	-1075	58	VOUT	-280	-1075	108	V2	3220	-1075	158	COM10	4530	1043
9	VSS	-3710	-1075	59	VOUT	-210	-1075	109	V2	3290	-1075	159	COM9	4470	1043
10	VDD	-3640	-1075	60	VOUT	-140	-1075	110	V2	3360	-1075	160	COM8	4410	1043
11	PS1	-3570	-1075	61	VOUT	-70	-1075	111	V2	3430	-1075	161	COM7	4350	1043
12	VSS	-3500	-1075	62	C5+	0	-1075	112	V1	3500	-1075	162	COM6	4290	1043
13	CS1B	-3430	-1075	63	C5+	70	-1075	113	V1	3570	-1075	163	COM5	4230	1043
14	VDD	-3360	-1075	64	C5+	140	-1075	114	V1	3640	-1075	164	COM4	4170	1043
15	VDD	-3290	-1075	65	C5+	210	-1075	115	V1	3710	-1075	165	COM3	4110	1043
16	RESETB	-3220	-1075	66	C3+	280	-1075	116	V0	3780	-1075	166	COM2	4050	1043
17	RS	-3150	-1075	67	C3+	350	-1075	117	V0	3850	-1075	167	COM1	3990	1043
18	VSS	-3080	-1075	68	C3+	420	-1075	118	V0	3920	-1075	168	COM0	3930	1043
19	RW_WR	-3010	-1075	69	C3+	490	-1075	119	V0	3990	-1075	169	COMS	3870	1043
20	E_RD	-2940	-1075	70	C1-	560	-1075	120	VR	4060	-1075	170	SEG0	3810	1043
21	VDD	-2870	-1075	71	C1-	630	-1075	121	VR	4130	-1075	171	SEG1	3750	1043
22	DB0	-2800	-1075	72	C1-	700	-1075	122	VSS	4200	-1075	172	SEG2	3690	1043
23	DB1	-2730	-1075	73	C1-	770	-1075	123	VSS	4270	-1075	173	SEG3	3630	1043
24	DB2	-2660	-1075	74	C1-	840	-1075	124	DUMMY	4843	-980	174	SEG4	3570	1043
25	DB3	-2590	-1075	75	C1-	910	-1075	125	COM39	4843	-910	175	SEG5	3510	1043
26	DB4	-2520	-1075	76	C1+	980	-1075	126	COM38	4843	-850	176	SEG6	3450	1043
27	DB5	-2450	-1075	77	C1+	1050	-1075	127	COM37	4843	-790	177	SEG7	3390	1043
28	DB6	-2380	-1075	78	C1+	1120	-1075	128	COM36	4843	-730	178	SEG8	3330	1043
29	DB7	-2310	-1075	79	C1+	1190	-1075	129	COM35	4843	-670	179	SEG9	3270	1043
30	VDD	-2240	-1075	80	C2+	1260	-1075	130	COM34	4843	-610	180	SEG10	3210	1043
31	VDD	-2170	-1075	81	C2+	1330	-1075	131	COM33	4843	-550	181	SEG11	3150	1043
32	VDD	-2100	-1075	82	C2+	1400	-1075	132	COM32	4843	-490	182	SEG12	3090	1043
33	VDD	-2030	-1075	83	C2+	1470	-1075	133	COM31	4843	-430	183	SEG13	3030	1043
34	VDD	-1960	-1075	84	C2-	1540	-1075	134	COM30	4843	-370	184	SEG14	2970	1043
35	VDD	-1890	-1075	85	C2-	1610	-1075	135	COM29	4843	-310	185	SEG15	2910	1043
36	VCI	-1820	-1075	86	C2-	1680	-1075	136	COM28	4843	-250	186	SEG16	2850	1043
37	VCI	-1750	-1075	87	C2-	1750	-1075	137	COM27	4843	-190	187	SEG17	2790	1043
38	VCI	-1680	-1075	88	C2-	1820	-1075	138	COM26	4843	-130	188	SEG18	2730	1043
39	VCI	-1610	-1075	89	C2-	1890	-1075	139	COM25	4843	-70	189	SEG19	2670	1043
40	VCI	-1540	-1075	90	C4+	1960	-1075	140	COM24	4843	-10	190	SEG20	2610	1043
41	VCI	-1470	-1075	91	C4+	2030	-1075	141	COM23	4843	50	191	SEG21	2550	1043
42	VCI	-1400	-1075	92	C4+	2100	-1075	142	COM22	4843	110	192	SEG22	2490	1043
43	VCI	-1330	-1075	93	C4+	2170	-1075	143	COM21	4843	170	193	SEG23	2430	1043
44	VSS	-1260	-1075	94	VSS	2240	-1075	144	COM20	4843	230	194	SEG24	2370	1043
45	VSS	-1190	-1075	95	REF	2310	-1075	145	COM19	4843	290	195	SEG25	2310	1043
46	VSS	-1120	-1075	96	VEXT	2380	-1075	146	COM18	4843	350	196	SEG26	2250	1043
47	VSS	-1050	-1075	97	VDD	2450	-1075	147	COM17	4843	410	197	SEG27	2190	1043
48	VSS	-980	-1075	98	INTRS	2520	-1075	148	COM16	4843	470	198	SEG28	2130	1043
49	VSS	-910	-1075	99	VSS	2590	-1075	149	COM15	4843	530	199	SEG29	2070	1043
50	VSS	-840	-1075	100	V4	2660	-1075	150	COM14	4843	590	200	SEG30	2010	1043

Table 2. Pad Center Coordinates (Continued)

[Unit: μm]

NO.	Name	X	Y	NO.	Name	X	Y	NO.	Name	X	Y	NO.	Name	X	Y
201	SEG31	1950	1043	251	SEG81	-1050	1043	301	COM43	-4050	1043				
202	SEG32	1890	1043	252	SEG82	-1110	1043	302	COM44	-4110	1043				
203	SEG33	1830	1043	253	SEG83	-1170	1043	303	COM45	-4170	1043				
204	SEG34	1770	1043	254	SEG84	-1230	1043	304	COM46	-4230	1043				
205	SEG35	1710	1043	255	SEG85	-1290	1043	305	COM47	-4290	1043				
206	SEG36	1650	1043	256	SEG86	-1350	1043	306	COM48	-4350	1043				
207	SEG37	1590	1043	257	SEG87	-1410	1043	307	COM49	-4410	1043				
208	SEG38	1530	1043	258	SEG88	-1470	1043	308	COM50	-4470	1043				
209	SEG39	1470	1043	259	SEG89	-1530	1043	309	COM51	-4530	1043				
210	SEG40	1410	1043	260	SEG90	-1590	1043	310	COM52	-4590	1043				
211	SEG41	1350	1043	261	SEG91	-1650	1043	311	DUMMY	-4660	1043				
212	SEG42	1290	1043	262	SEG92	-1710	1043	312	DUMMY	-4740	1043				
213	SEG43	1230	1043	263	SEG93	-1770	1043	313	DUMMY	-4843	860				
214	SEG44	1170	1043	264	SEG94	-1830	1043	314	DUMMY	-4843	780				
215	SEG45	1110	1043	265	SEG95	-1890	1043	315	COM53	-4843	710				
216	SEG46	1050	1043	266	SEG96	-1950	1043	316	COM54	-4843	650				
217	SEG47	990	1043	267	SEG97	-2010	1043	317	COM55	-4843	590				
218	SEG48	930	1043	268	SEG98	-2070	1043	318	COM56	-4843	530				
219	SEG49	870	1043	269	SEG99	-2130	1043	319	COM57	-4843	470				
220	SEG50	810	1043	270	SEG100	-2190	1043	320	COM58	-4843	410				
221	SEG51	750	1043	271	SEG101	-2250	1043	321	COM59	-4843	350				
222	SEG52	690	1043	272	SEG102	-2310	1043	322	COM60	-4843	290				
223	SEG53	630	1043	273	SEG103	-2370	1043	323	COM61	-4843	230				
224	SEG54	570	1043	274	SEG104	-2430	1043	324	COM62	-4843	170				
225	SEG55	510	1043	275	SEG105	-2490	1043	325	COM63	-4843	110				
226	SEG56	450	1043	276	SEG106	-2550	1043	326	COM64	-4843	50				
227	SEG57	390	1043	277	SEG107	-2610	1043	327	COM65	-4843	-10				
228	SEG58	330	1043	278	SEG108	-2670	1043	328	COM66	-4843	-70				
229	SEG59	270	1043	279	SEG109	-2730	1043	329	COM67	-4843	-130				
230	SEG60	210	1043	280	SEG110	-2790	1043	330	COM68	-4843	-190				
231	SEG61	150	1043	281	SEG111	-2850	1043	331	COM69	-4843	-250				
232	SEG62	90	1043	282	SEG112	-2910	1043	332	COM70	-4843	-310				
233	SEG63	30	1043	283	SEG113	-2970	1043	333	COM71	-4843	-370				
234	SEG64	-30	1043	284	SEG114	-3030	1043	334	COM72	-4843	-430				
235	SEG65	-90	1043	285	SEG115	-3090	1043	335	COM73	-4843	-490				
236	SEG66	-150	1043	286	SEG116	-3150	1043	336	COM74	-4843	-550				
237	SEG67	-210	1043	287	SEG117	-3210	1043	337	COM75	-4843	-610				
238	SEG68	-270	1043	288	SEG118	-3270	1043	338	COM76	-4843	-670				
239	SEG69	-330	1043	289	SEG119	-3330	1043	339	COM77	-4843	-730				
240	SEG70	-390	1043	290	SEG120	-3390	1043	340	COM78	-4843	-790				
241	SEG71	-450	1043	291	SEG121	-3450	1043	341	COM79	-4843	-850				
242	SEG72	-510	1043	292	SEG122	-3510	1043	342	COMS1	-4843	-910				
243	SEG73	-570	1043	293	SEG123	-3570	1043	343	DUMMY	-4843	-980				
244	SEG74	-630	1043	294	SEG124	-3630	1043								
245	SEG75	-690	1043	295	SEG125	-3690	1043								
246	SEG76	-750	1043	296	SEG126	-3750	1043								
247	SEG77	-810	1043	297	SEG127	-3810	1043								
248	SEG78	-870	1043	298	COM40	-3870	1043								
249	SEG79	-930	1043	299	COM41	-3930	1043								
250	SEG80	-990	1043	300	COM42	-3990	1043								

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PIN DESCRIPTION

POWER SUPPLY

Table 2. Power Supply Pins

<table>
<tr><th>Name</th><th>I/O</th><th colspan="5">Description</th></tr>
<tr><td>VDD</td><td>Supply</td><td colspan="5">Power supply</td></tr>
<tr><td>VSS</td><td>Supply</td><td colspan="5">Ground</td></tr>
<tr><td rowspan="4">V0
V1
V2
V3
V4</td><td rowspan="4">I/O</td><td colspan="5">LCD driver supplies voltages
The voltage determined by LCD pixel is impedance converted by an operational amplifier for application.
Voltages should have the following relationship;
V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ Vss
When the internal power circuit is active, these voltages are generated as following table according to the state of LCD bias.</td></tr>
<tr><td>LCD bias</td><td>V1</td><td>V2</td><td>V3</td><td>V4</td></tr>
<tr><td>1/N bias</td><td>(N-1) / N x V0</td><td>(N-2) / N x V0</td><td>(2/N) x V0</td><td>(1/N) x V0</td></tr>
<tr><td colspan="5">NOTE: N = 4 to 11</td></tr>
</table>

LCD DRIVER SUPPLY

Table 3. LCD Driver Supply Pins

Name	I/O	Description
C1-	O	Capacitor 1 negative connection pin for voltage converter
C1+	O	Capacitor 1 positive connection pin for voltage converter
C2-	O	Capacitor 2 negative connection pin for voltage converter
C2+	O	Capacitor 2 positive connection pin for voltage converter
C3+	O	Capacitor 3 positive connection pin for voltage converter
C4+	O	Capacitor 4 positive connection pin for voltage converter
C5+	O	Capacitor 5 positive connection pin for voltage converter
VOUT	I/O	Voltage converter input / output pin
VCI	I	Voltage converter input voltage pin Voltages should have the following relationship: VDD ≤ VCI ≤ V0
VR	I	V0 voltage adjustment pin It is valid only when on-chip resistors are not used (INTRS = "L")
REF	I	Selects the external VREF voltage via VEXT pin – REF = "L": using the external VREF – REF = "H": using the internal VREF
VEXT	I	Externally input reference voltage (VREF) for the internal voltage regulator It is valid only when REF is "L".

SYSTEM CONTROL

Table 4. System Control Pins

Name	I/O	Description
INTRS	I	Internal resistors select pin This pin selects the resistors for adjusting V0 voltage level. – INTRS = "H": use the internal resistors – INTRS = "L": use the external resistors VR pin and external resistive divider control V0 voltage.
TEST1 to TEST4	I	Test pins Don't use these pins.

MICROPROCESSOR INTERFACE

Table 5. Microprocessor Interface Pins

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>RESETB</td><td>I</td><td>Reset the input pin
When RESETB is "L", initialization is executed.</td></tr>
<tr><td rowspan="5">PS0</td><td rowspan="5">I</td><td>Parallel/Serial data input select input
<table>
<tr><td>PS0</td><td>Interface Mode</td><td>Data/ Instruction</td><td>Data</td><td>Read / Write</td><td>Serial Clock</td></tr>
<tr><td>H</td><td>Parallel</td><td>RS</td><td>DB0 to DB7</td><td>E_RD
RW_WR</td><td>-</td></tr>
<tr><td>L</td><td>Serial</td><td>RS or None</td><td>SID(DB7)</td><td>Write only</td><td>SCLK(DB6)</td></tr>
</table></td></tr>
<tr><td>*NOTE: When PS is "L", DB0 to DB5 are high impedance and E_RD and RW_WR must be fixed to either "H" or "L".</td></tr>
<tr><td>PS1</td><td>I</td><td>Microprocessor interface select input pin
– PS0 = “H” , PS1 = "H": 6800-series parallel MPU interface
– PS0 = “H” , PS1 = "L": 8080-series parallel MPU interface
– PS0 = “L” , PS1 = "H": 4 Pin-SPI serial MPU interface
– PS0 = “L” , PS1 = "L": 3 Pin-SPI serial MPU interface</td></tr>
<tr><td>CS1B</td><td>I</td><td>Chip select input pins
Data/instruction I/O is enabled only when CS1B is "L" . When chip select is non-active, DB0 to DB7 may be high impedance.</td></tr>
<tr><td>RS</td><td>I</td><td>Register select input pin
– RS = "H": DB0 to DB7 are display data
– RS = "L": DB0 to DB7 are control data</td></tr>
<tr><td rowspan="3">RW_WR</td><td rowspan="3">I</td><td>Read / Write execution control pin
<table>
<tr><td>PS1</td><td>MPU Type</td><td>RW_WR</td><td>Description</td></tr>
<tr><td>H</td><td>6800-series</td><td>RW</td><td>Read/Write control input pin
– RW = "H": read
– RW = "L": write</td></tr>
<tr><td>L</td><td>8080-series</td><td>/WR</td><td>Write enable clock input pin
The data on DB0 to DB7 are latched at the rising edge of the /WR signal.</td></tr>
</table></td></tr>
<tr><td></td></tr>
</table>

Table 6 (Continued)

<table>
<tr><th>Name</th><th>I/O</th><th colspan="4">Description</th></tr>
<tr><td rowspan="5">E_RD</td><td rowspan="5">I</td><td colspan="4">Read / Write execution control pin</td></tr>
<tr><td>PS1</td><td>MPU Type</td><td>E_RD</td><td>Description</td></tr>
<tr><td>H</td><td>6800-series</td><td>E</td><td>Read/Write control input pin
– RW = "H": When E is "H", DB0 to DB7 are in an output status.
– RW = "L": The data on DB0 to DB7 are latched at the falling edge of the E signal.</td></tr>
<tr><td>L</td><td>8080-series</td><td>/RD</td><td>Read enable clock input pin
When /RD is "L", DB0 to DB7 are in an output status.</td></tr>
<tr><td colspan="4"></td></tr>
<tr><td>DB0
to
DB7</td><td>I/O</td><td colspan="4">8-bit bi-directional data bus that is connected to the standard 8-bit microprocessor data bus. When the serial interface selected (PS0 = "L");
– DB0 to DB5: high impedance
– DB6: serial input clock (SCLK)
– DB7: serial input data (SID)
When chip select is not active, DB0 to DB7 may be high impedance.</td></tr>
</table>

LCD DRIVER OUTPUTS

Table 6. LCD Driver Outputs Pins

<table>
<tr><th>Name</th><th>I/O</th><th colspan="4">Description</th></tr>
<tr><td rowspan="11">SEG0
to
SEG127</td><td rowspan="11">O</td><td colspan="4">LCD segment driver outputs
The display data and the M signal control the output voltage of segment driver.</td></tr>
<tr><td rowspan="2">Display data</td><td rowspan="2">M (Internal)</td><td colspan="2">Segment driver output voltage</td></tr>
<tr><td>Normal display</td><td>Reverse display</td></tr>
<tr><td>H</td><td>H</td><td>V0</td><td>V2</td></tr>
<tr><td>H</td><td>L</td><td>Vss</td><td>V3</td></tr>
<tr><td>L</td><td>H</td><td>V2</td><td>V0</td></tr>
<tr><td>L</td><td>L</td><td>V3</td><td>Vss</td></tr>
<tr><td colspan="2">Power save mode</td><td>Vss</td><td>Vss</td></tr>
<tr><td colspan="4"></td></tr>
<tr><td rowspan="8">COM0
to
COM79</td><td rowspan="8">O</td><td colspan="4">LCD common driver outputs
The internal scanning data and M signal control the output voltage of common driver.</td></tr>
<tr><td>Scan data</td><td>M (Internal)</td><td colspan="2">Common driver output voltage</td></tr>
<tr><td>H</td><td>H</td><td colspan="2">Vss</td></tr>
<tr><td>H</td><td>L</td><td colspan="2">V0</td></tr>
<tr><td>L</td><td>H</td><td colspan="2">V1</td></tr>
<tr><td>L</td><td>L</td><td colspan="2">V4</td></tr>
<tr><td colspan="2">Power save mode</td><td colspan="2">Vss</td></tr>
<tr><td colspan="4"></td></tr>
<tr><td>COMS
(COMS1)</td><td>O</td><td colspan="4">Common output for the icons
The output signals of two pins are same. When not used, these pins should be left open.</td></tr>
</table>

NOTE: **DUMMY – These pins should be opened (floated).**

FUNCTIONAL DESCRIPTION

MICROPROCESSOR INTERFACE

Chip Select Input

There are CS1B for chip selection. The KS0759 can interface with an MPU only when CS1B is "L" . When these pins are set to any other combination, RS, E_RD, and RW_WR inputs are disabled and DB0 to DB7 are to be high impedance. And, in case of serial interface, the internal shift register and the counter are reset.

Parallel / Serial Interface

KS0759 has four types of interface with an MPU, which are two serial and two parallel interface. This parallel or serial interface is determined by PS 0pin as shown in Table 7.

Table 7. Parallel / Serial Interface Mode

PS0	Type	CS1B	PS1	Interface mode
H	Parallel	CS1B	H	6800-series MPU mode
			L	8080-series MPU mode
L	Serial	CS1B	H	4 Pin-SPI MPU mode
			L	3 Pin-SPI MPU mode

Parallel Interface (PS0 = "H")

The 8-bit bi-directional data bus is used in parallel interface and the type of MPU is selected by PS1 as shown in Table 8. The type of data transfer is determined by signals at RS, E_RD and RW_WR as shown in Table 9.

Table 8. Microprocessor Selection for Parallel Interface

PS1	CS1B	RS	E_RD	RW_WR	DB0 to DB7	MPU bus
H	CS1B	RS	E	RW	DB0 to DB7	6800-series
L	CS1B	RS	/RD	/WR	DB0 to DB7	8080-series

Table 9. Parallel Data Transfer

Common	6800-series		8080-series		Description
RS	E_RD (E)	RW_WR (RW)	E_RD (/RD)	RW_WR (/WR)	
H	H	H	L	H	Display data read out
H	H	L	H	L	Display data write
L	H	H	L	H	Register status read
L	H	L	H	L	Writes to internal register (instruction)

Serial Interface (PS0 = "L")

When the KS0759 is active(CS1B=”L”), serial data (DB7) and serial clock (DB6) inputs are enabled. And not active, the internal 8-bit shift register and the 3-bit counter are reset. The display data/command indication may be controlled either via software or the Register Select(RS) Pin, based on the setting of PS1. When the RS pin is used (PS1 = “H”), data is display data when RS is high, and command data when RS is low. When RS is not used (PS1 = “L”), the LCD Driver will receive command from MPU by default. If messages on the data pin are data rather than command, MPU should send Data Direction command(11101000) to control the data direction and then one more command to define the number of data bytes will be write. After these two continuous commands are send, the following messages will be data rather than command. Serial data can be read on the rising edge of serial clock going into DB6 and processed as 8-bit parallel data on the eighth serial clock. And the DDRAM column address pointer will be increased by one automatically. The next bytes after the display data string is handled as command data.

Serial Mode	PS0	PS1	CS1B	RS
Serial-mode with RS pin	L	H	CS1B	Used
Serial-mode with software command	L	L	CS1B	Not used

4 Pin-SPI Interface (PS0 = "L" , PS1 = "H")

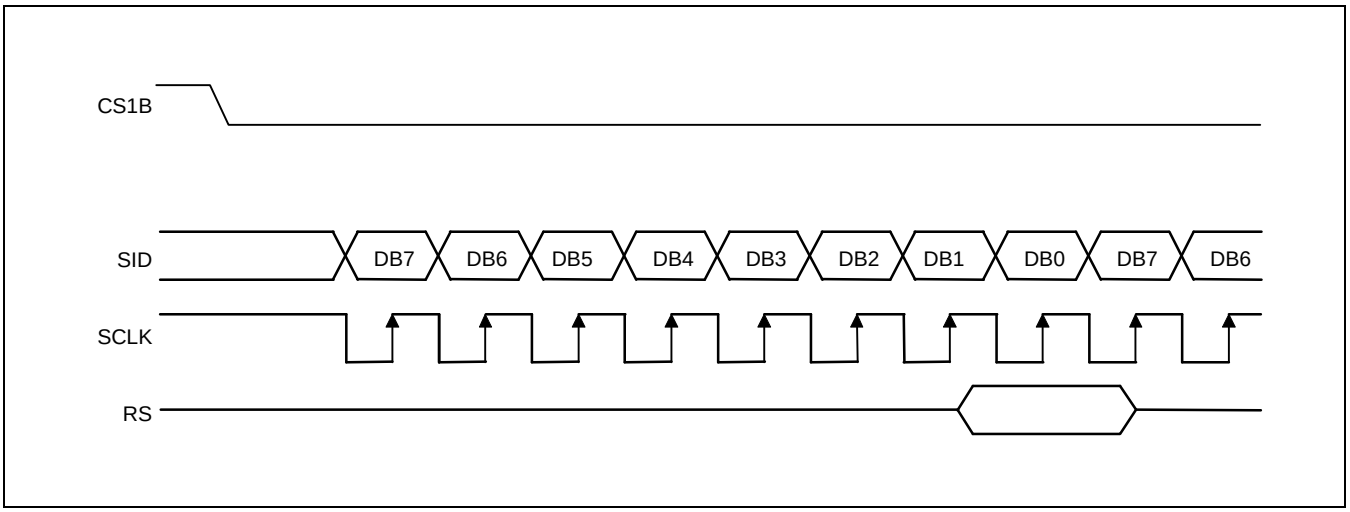

Figure 3. 4 Pin SPI Timing (RS is used)

3 Pin-SPI Interface (PS0 = "L" , PS1 = "L")

To write data to the DDRAM, send Data Direction Command in 3-Pin SPI mode. Data is latched at the rising edge of SCLK. And the DDRAM column address pointer will be increased by one automatically.

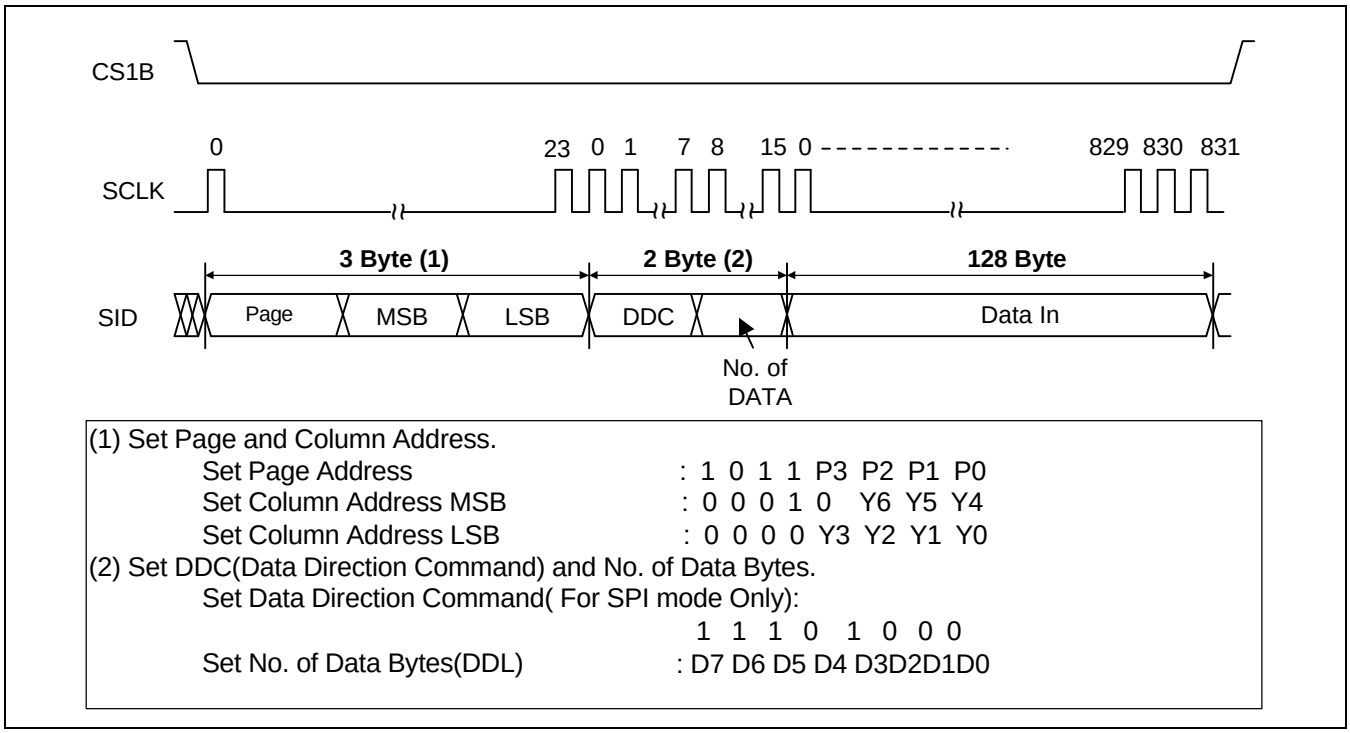

Figure 4. 3 Pin SPI Timing (RS is not used)

This command is used in 3-Pin SPI mode only. It will be two continuous commands, the first byte controls the data direction and informs the LCD driver the second byte will be number of data bytes will be write. After these two commands sending out, the following messages will be data. If data is stopped in transmitting, it is not valid data. New data will be transferred serially with most significant bit first.

Notes:

- In spite of transmission of data, if CS1B will be disable, state terminates abnormally. Next state is initialized.
- DDL Register value “0” → “1” , “127” → “128”. (decimal value)

Busy Flag

The Busy Flag indicates whether the KS0759 is operating or not. When DB7 is "H" in read status operation, this device is in busy status and will accept only read status instruction. If the cycle time is correct, the microprocessor needs not to check this flag before each instruction, which improves the MPU performance.

Data Transfer

The KS0759 uses bus holder and internal data bus for Data Transfer with the MPU. When writing data from the MPU to on-chip RAM, data is automatically transferred from the bus holder to the RAM as shown in Figure 5. And when reading data from on-chip RAM to the MPU, the data for the initial read cycle is stored in the bus holder (dummy read) and the MPU reads this stored data from bus holder for the next data read cycle as shown in Figure 6. This means that a dummy read cycle must be inserted between each pair of address sets when a sequence of address sets is executed. Therefore, the data of the specified address cannot be output with the read display data instruction right after the address sets, but can be output at the second read of data.

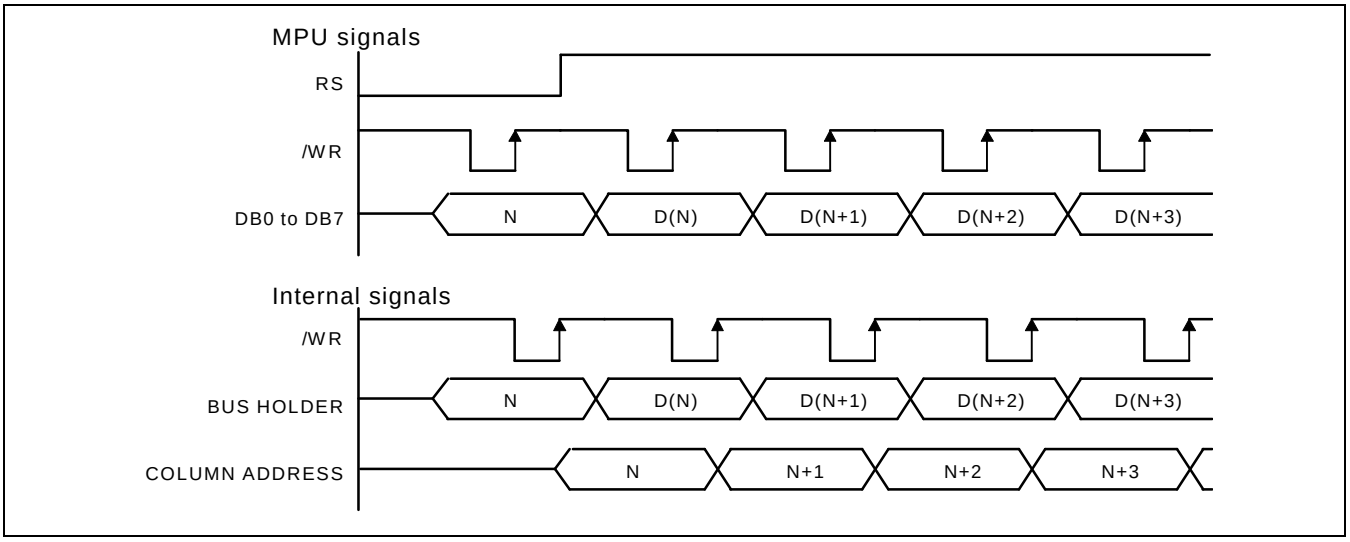

Figure 5. Write Timing

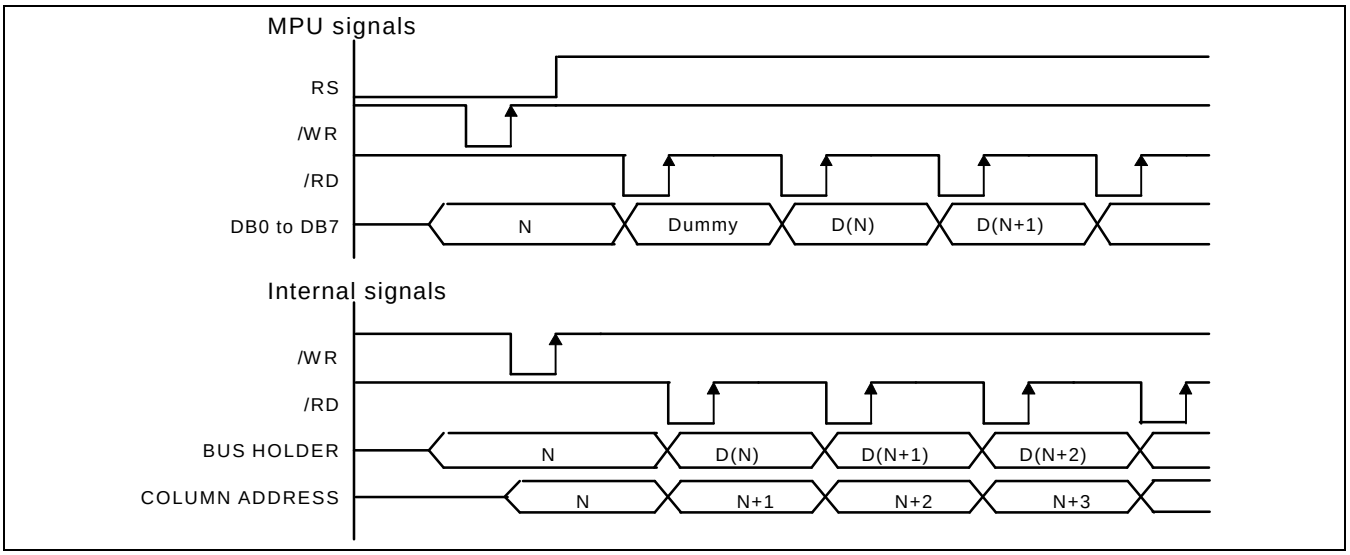

Figure 6. Read Timing

DISPLAY DATA RAM (DDRAM)

The Display Data RAM stores pixel data for the LCD. It is 81-row by 128-column addressable array. Each pixel can be selected when the page and column addresses are specified. The 81 rows are divided into 10 pages of 8 lines and the 11th page with a single line (DB0 only). Data is read from or written to the 8 lines of each page directly through DB0 to DB7. The display data of DB0 to DB7 from the microprocessor correspond to the LCD common lines as shown in Figure 7. The microprocessor can read from and write to RAM through the I/O buffer. Since the LCD controller operates independently, data can be written into RAM at the same time as data is being displayed without causing the LCD flicker.

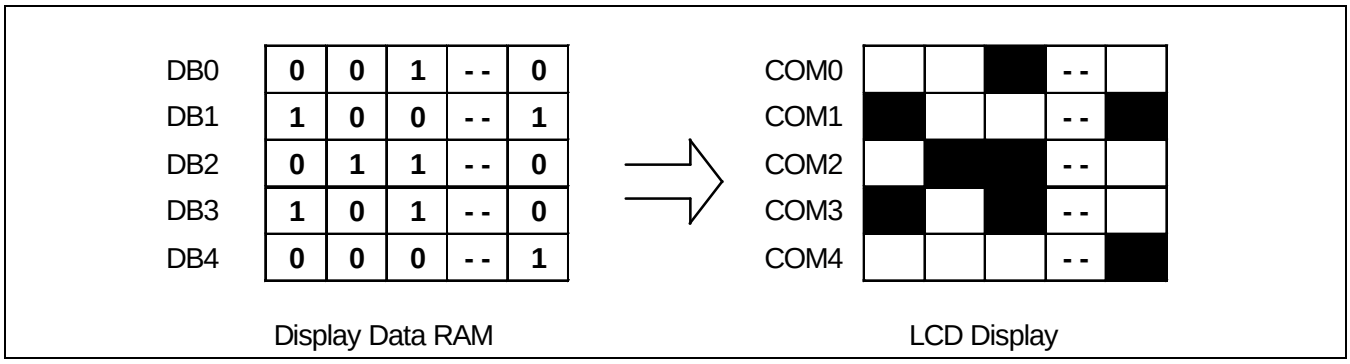

Figure 7. RAM-to-LCD Data Transfer

Page Address Circuit

This circuit is for providing a Page Address to Display Data RAM shown in Figure 9. It incorporates 4-bit Page Address register changed by only the "Set Page" instruction. Page Address 10 (DB3 and DB1 are "H", DB2 and DB0 is "L") is a special RAM area for the icons and display data DB0 is only valid.

Line Address Circuit

This circuit assigns DDRAM a Line Address corresponding to the first line (COM0) of the display. Therefore, by setting line address repeatedly, it is possible to realize the screen scrolling and page switching without changing the contents of on-chip RAM as shown in Figure 9 & Figure 10. It incorporates 7-bit Line Address register changed by only the initial display line instruction and 7-bit counter circuit. At the beginning of each LCD frame, the contents of register are copied to the line counter which is increased by CL signal and generates the Line Address for transferring the 128-bit RAM data to the display data latch circuit. However, display data of icons are not scrolled because the MPU can not access Line Address of icons.

Column Address Circuit

Column address circuit has a 7-bit preset counter that provides column address to the Display Data RAM as shown in Figure 9. When set Column Address MSB / LSB instruction is issued, 7-bit [Y6:Y0] is updated. And, since this address is increased by 1 each a read or write data instruction, microprocessor can access the display data continuously. And the Column Address counter is independent of page address register.

ADC Select instruction makes it possible to invert the relationship between the column address and the segment outputs. It is necessary to rewrite the display data on built-in RAM after issuing ADC Select instruction. Refer to the following Figure 8.

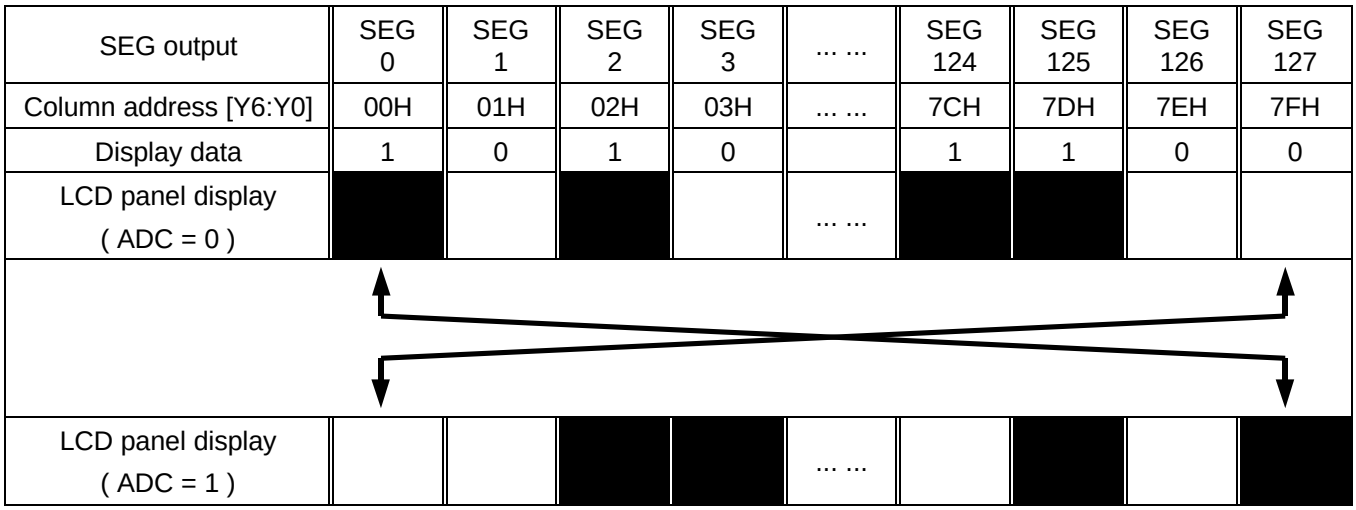

Figure 8. The Relationship between the Column Address and the Segment Outputs

Segment Control Circuit

This circuit controls the display data by the Display ON / OFF, reverse display ON / OFF and entire display ON / OFF instructions without changing the data in the display data RAM.

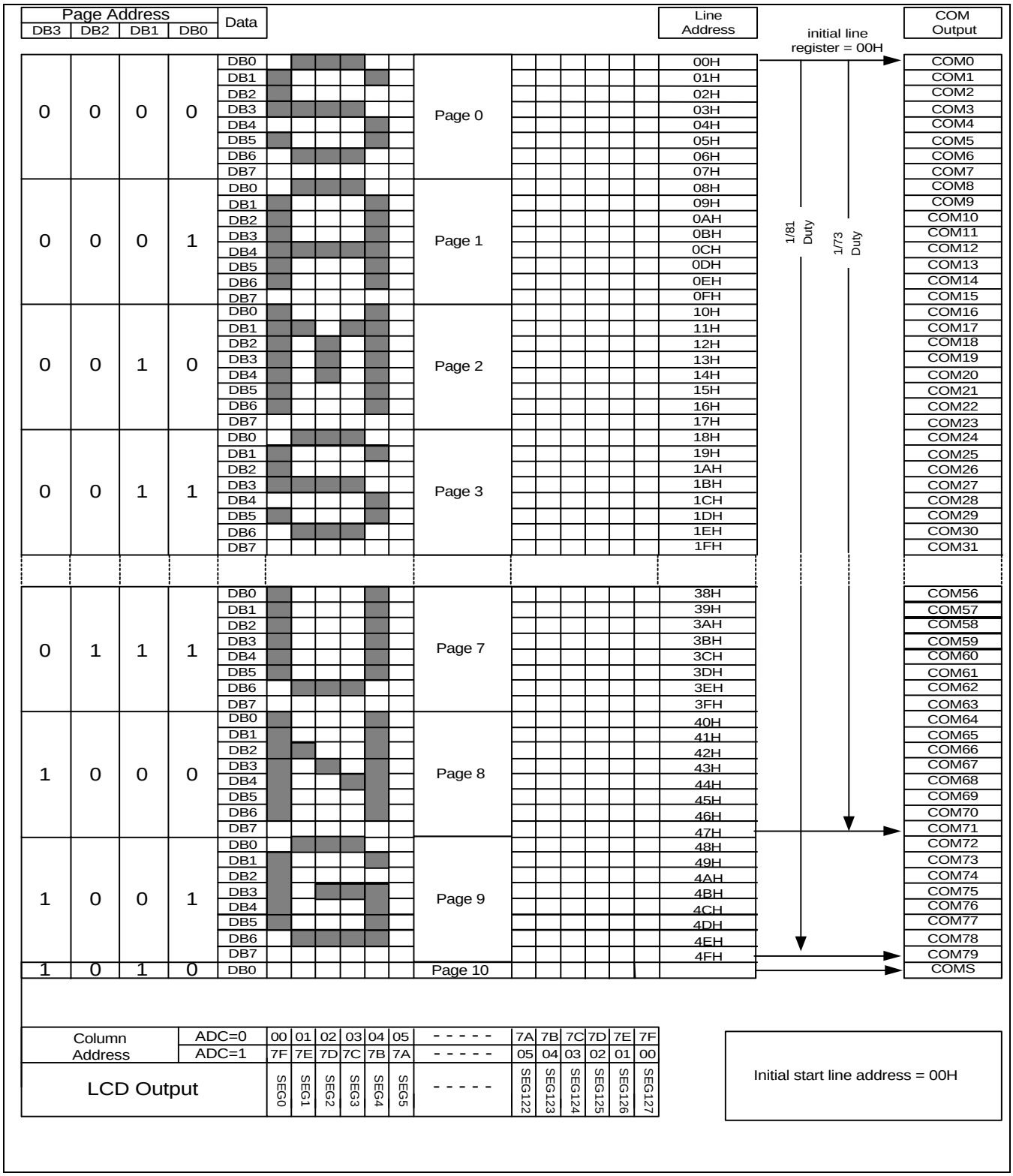

Figure 9. Display Data RAM Map (Initial Line Address = 00H)

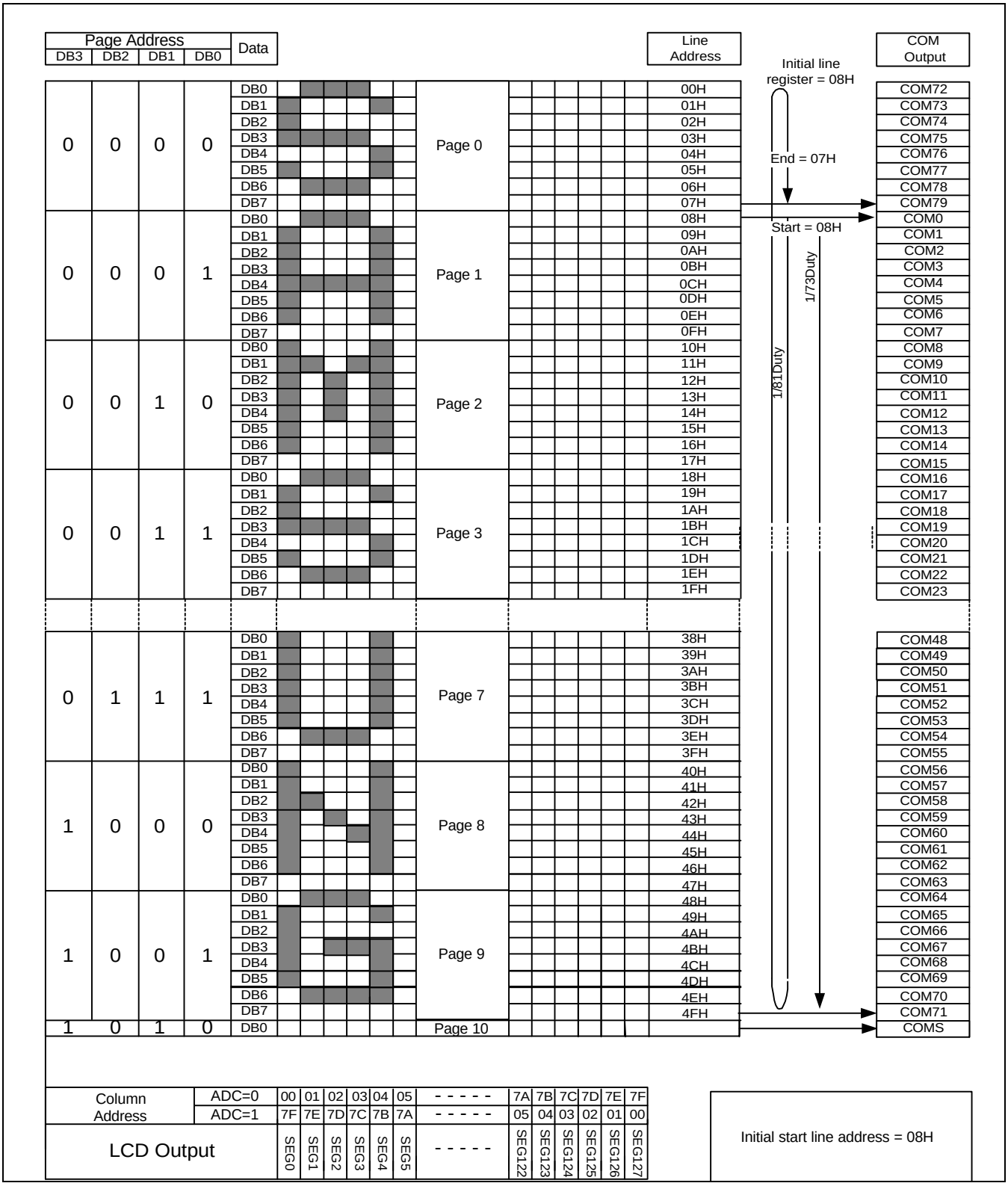

Figure 10. Display Data RAM Map (Initial Line Address = 08H)

LCD DISPLAY CIRCUITS

Oscillator

This is completely on-chip Oscillator and its frequency is nearly independent of V_{DD}. This Oscillator signal is used in the voltage converter and display timing generation circuit.

Display Timing Generator Circuit

This circuit generates some signals to be used for displaying LCD. The display clock, CL(internal), generated by oscillation clock, generates the clock for the line counter and the signal for the display data latch. The line address of on-chip RAM is generated in synchronization with the display clock and the display data latch circuit latches the 128-bit display data in synchronization with the display clock. The display data, which is read to the LCD driver, is completely independent of the access to the display data RAM from the microprocessor. The display clock generates an LCD AC signal (M) which enables the LCD driver to make a AC drive waveform, and also generates an internal common timing signal and start signal to the common driver. The frame signal or the line signal changes the M by setting internal instruction. Driving waveform and internal timing signal are shown in Figure 11.

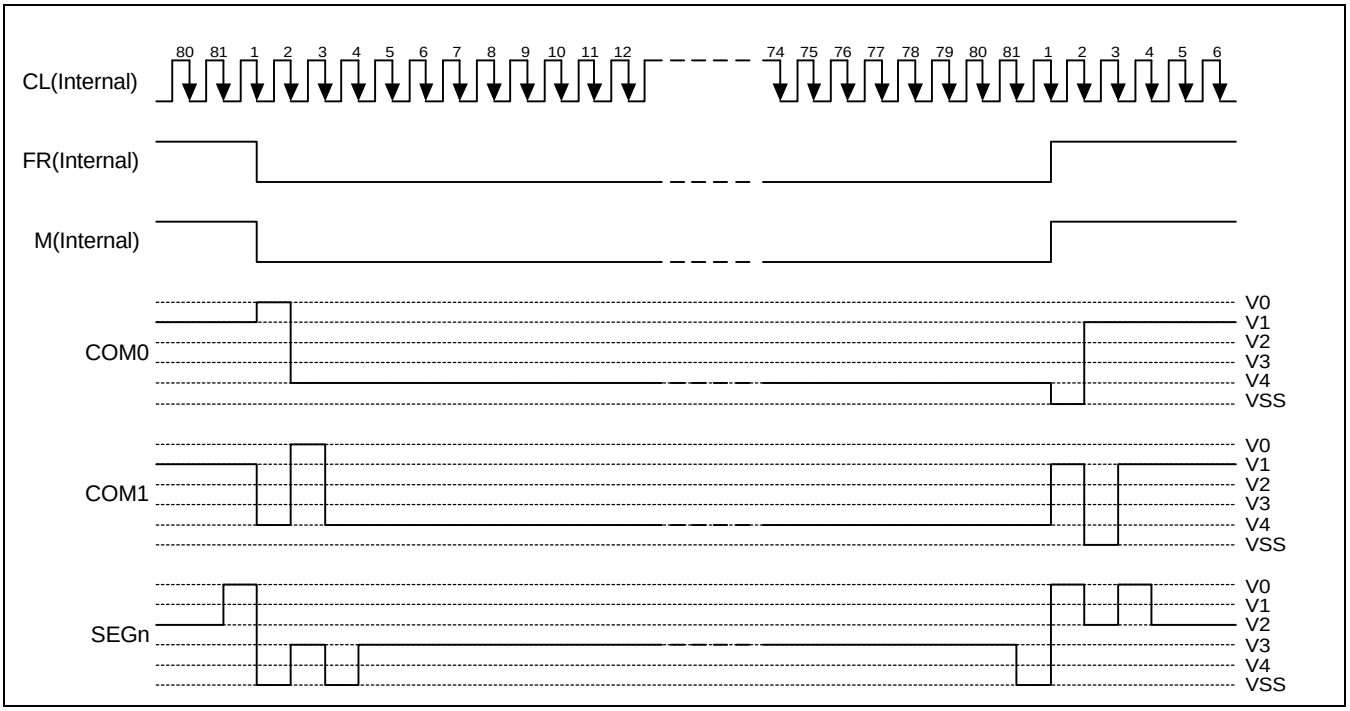

Figure 11. 2-frame AC Driving Waveform (Duty Ratio = 1/81)

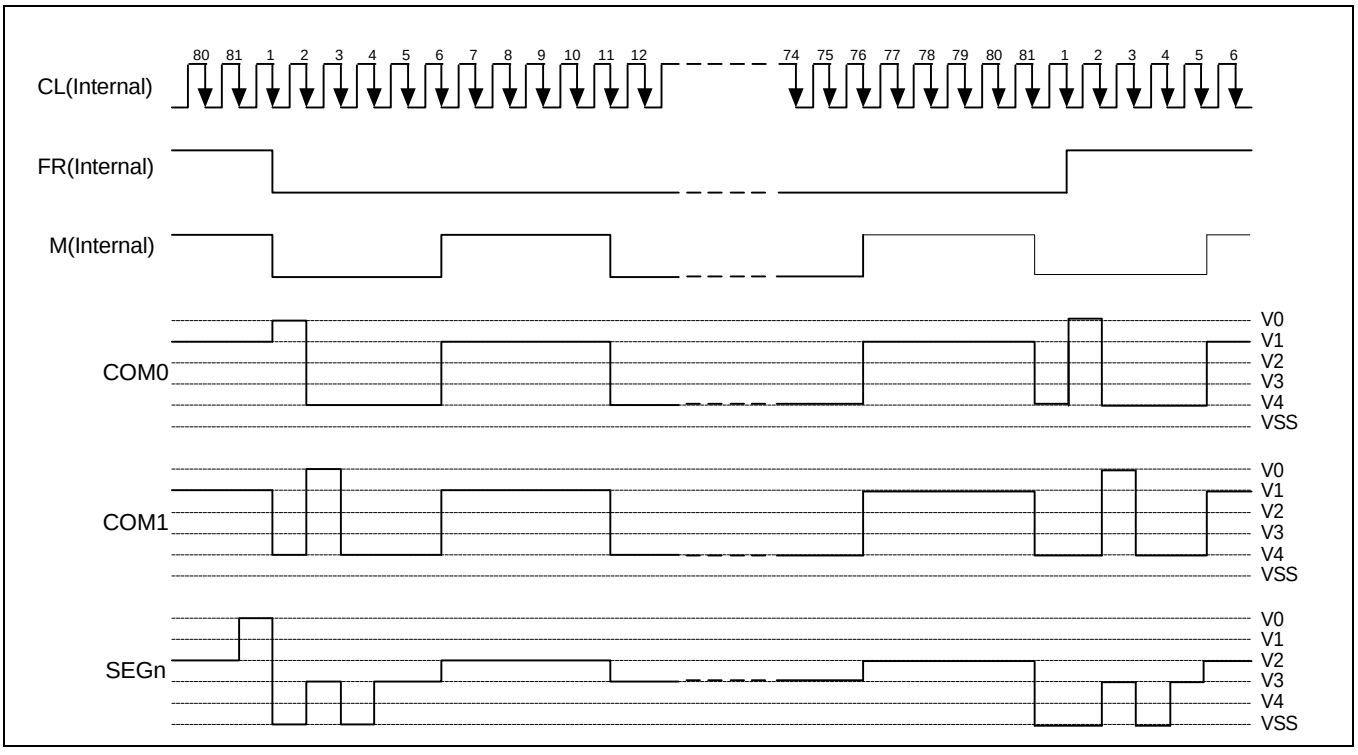

Figure 12. N-line Inversion Driving Waveform (N = 5 , Duty Ratio = 1/81)

LCD DRIVER CIRCUIT

81-channel common driver and 128-channel segment driver configure this driver circuit. This LCD panel driver voltage depends on the combination of display data and M signal.

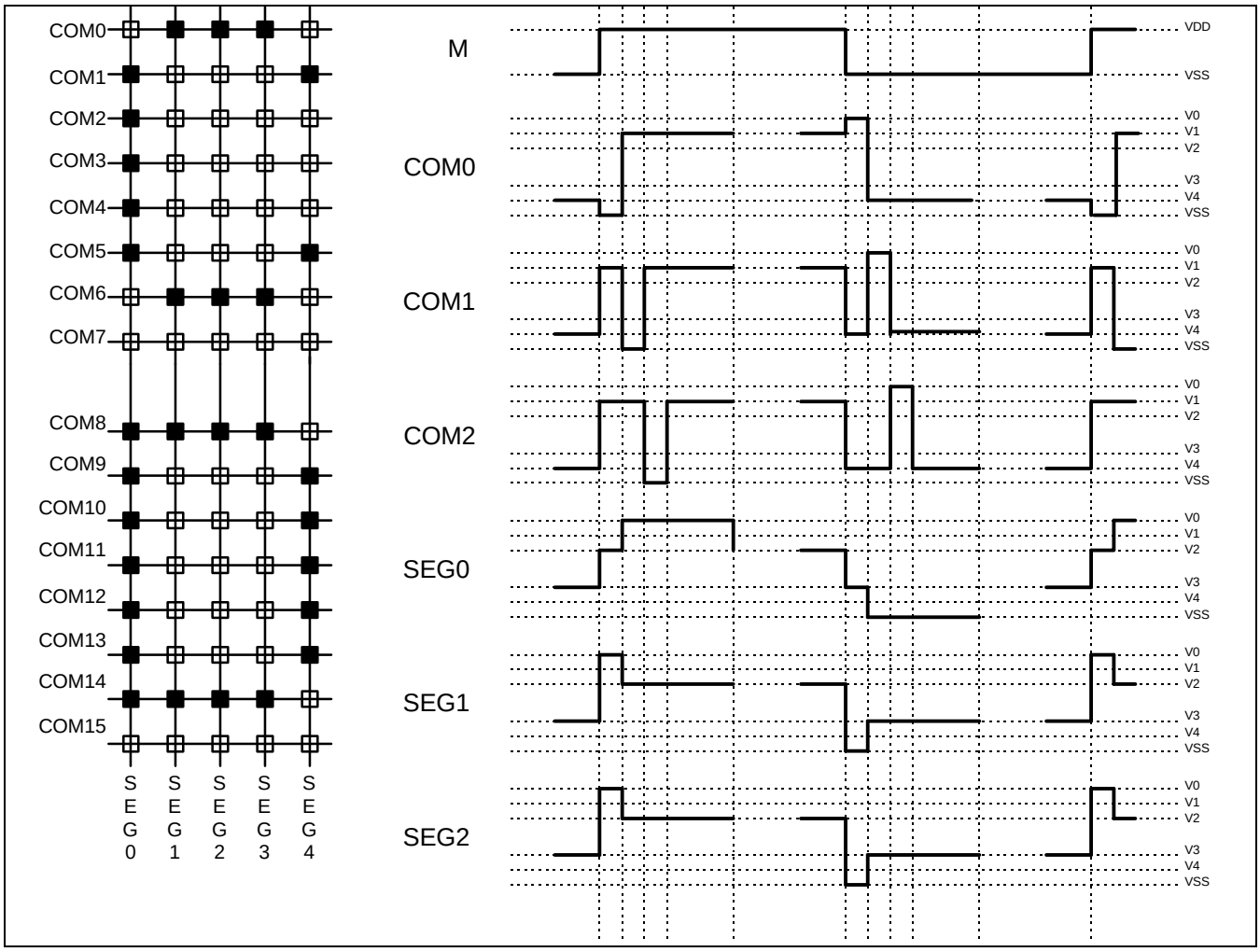

Figure 13. Segment and Common Timing

Partial Display on LCD

The KS0759 realizes the Partial Display function on LCD with low-duty driving for saving power consumption and showing the various display duty. To show the various display duty on LCD, LCD driving duty and bias are programmable via the instruction. And, built-in power supply circuits are controlled by the instruction for adjusting the LCD driving voltages

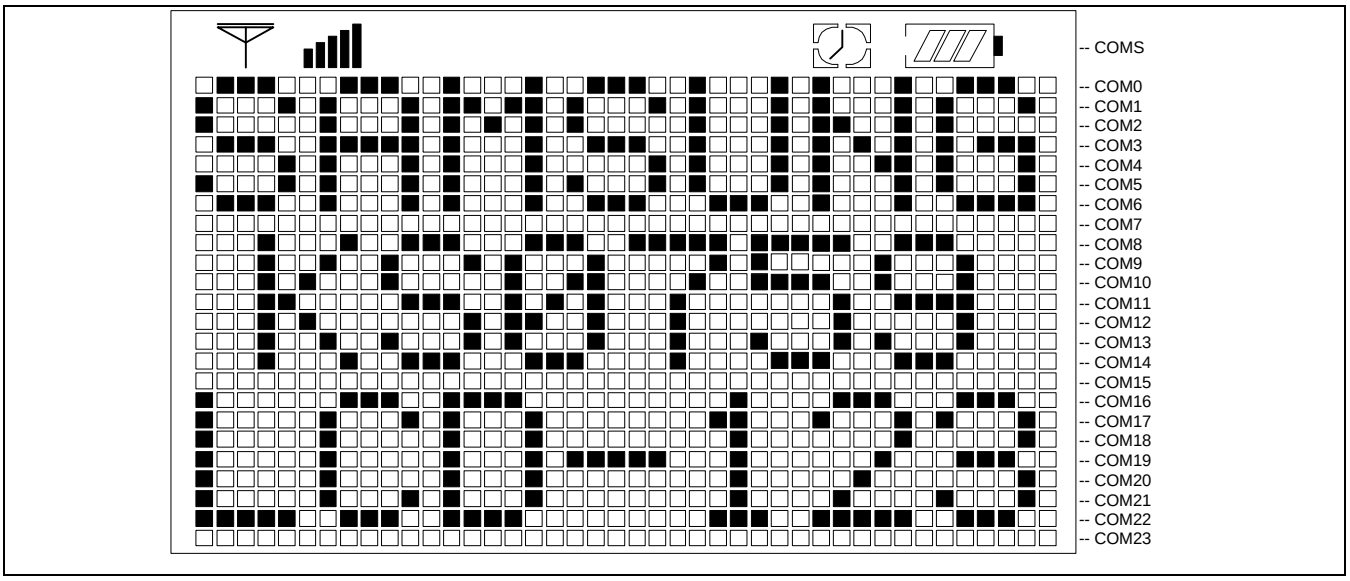

Figure 14. Reference Example for Partial Display (Display Duty = 25)

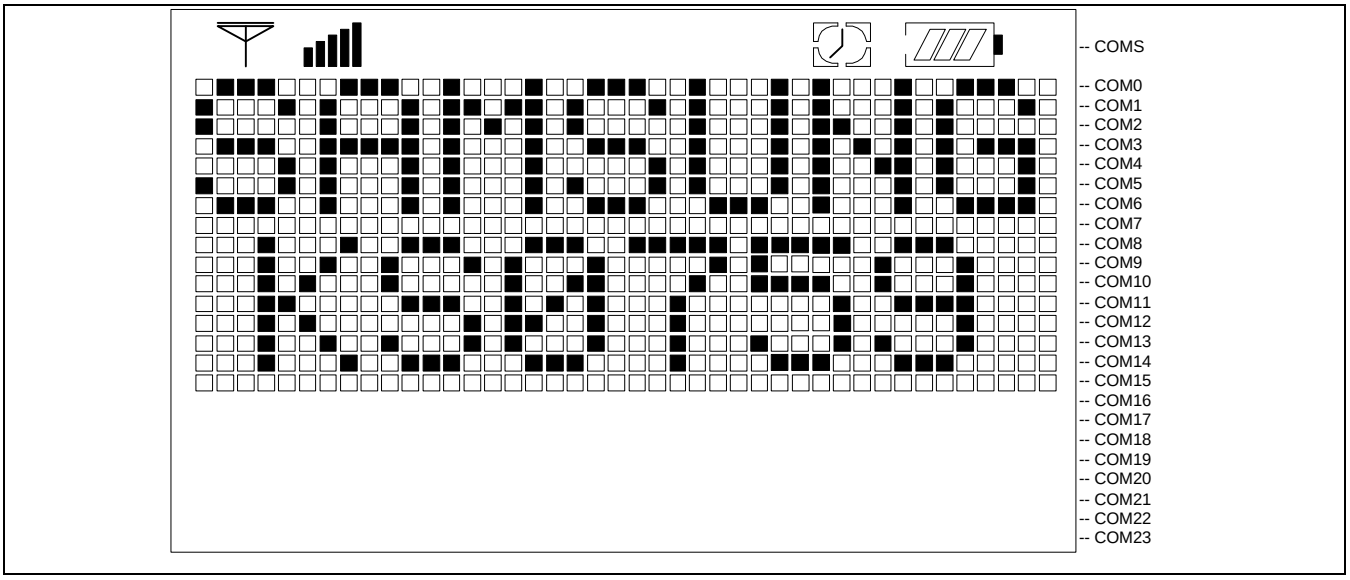

Figure 15. Partial Display (Partial Display Duty = 17, Initial COM0 = 0)

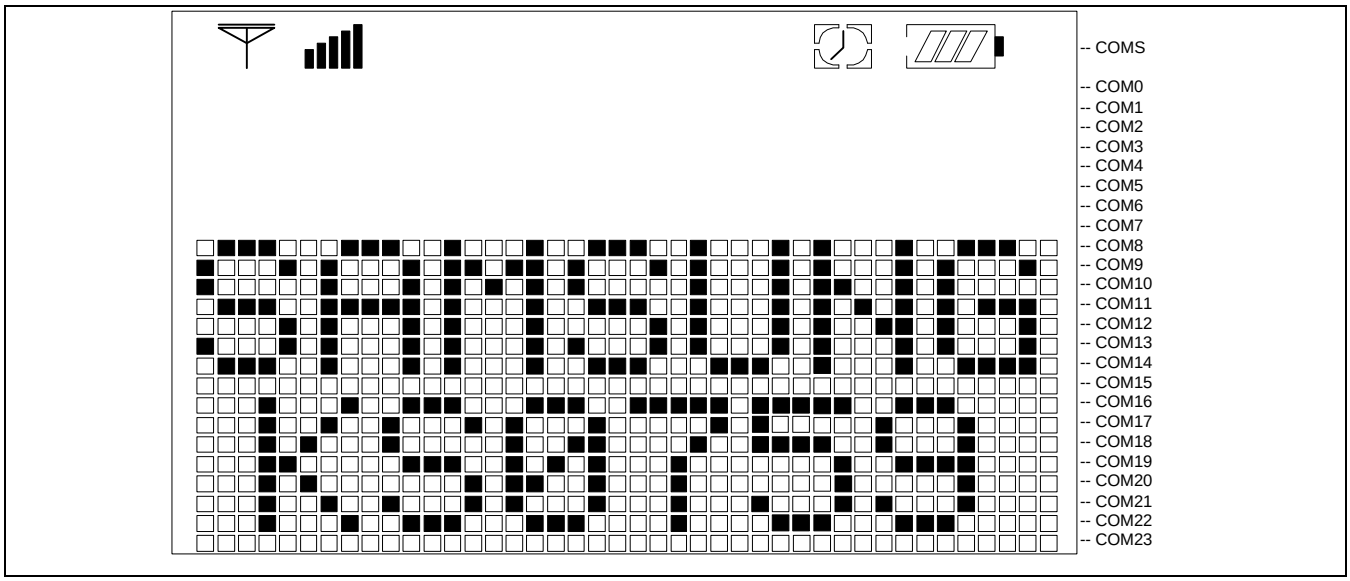

Figure 16. Moving Display (Partial Display Duty = 17, Initial COM0 = 8)

POWER SUPPLY CIRCUITS

The Power Supply circuits generate the voltage levels necessary to drive liquid crystal driver circuits with low-power consumption and the fewest components. There are voltage converter circuits, voltage regulator circuits, and voltage follower circuits. They are valid only in master operation and controlled by power control instruction. For details, refers to "Instruction Description". Table 10 shows the referenced combinations in using Power Supply circuits.

Table 10. Recommended Power Supply Combinations

User setup	Power control (VC VR VF)	V/C circuits	V/R circuits	V/F circuits	VOUT	V0	V1 to V4
Only the internal power supply circuits are used	1 1 1	ON	ON	ON	Open	Open	Open
Only the voltage regulator circuits and voltage follower circuits are used	0 1 1	OFF	ON	ON	External input	Open	Open
Only the voltage follower circuits are used	0 0 1	OFF	OFF	ON	External input	Open	Open
Only the external power supply circuits are used	0 0 0	OFF	OFF	OFF	Open	External input	External input

Voltage Converter Circuits

These circuits boost up the electric potential between VCI and Vss to 3, 4, 5 or 6 times toward positive side and boosted voltage is outputted from VOUT pin. It is possible to select the lower boosting level in any boosting circuit by “Set DC-DC Step-up” instruction. When the higher level is selected by instruction, VOUT voltage is not valid.

[C1 = 1.0 to 4.7 *m*F]

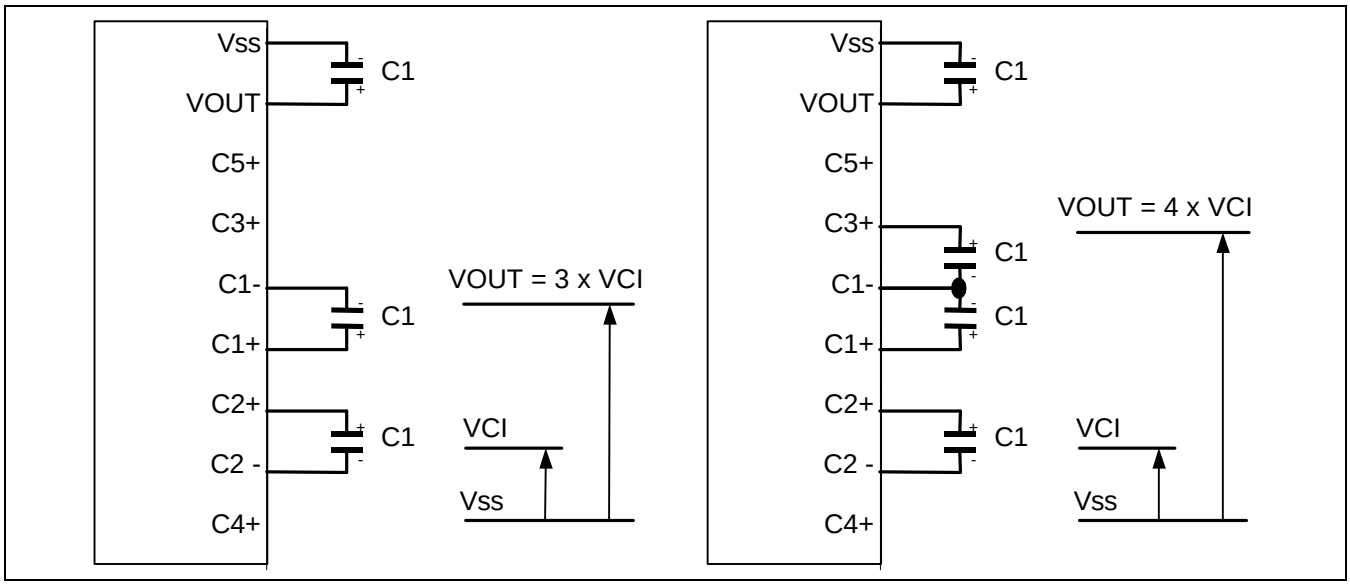

Figure 17. Three Times Boosting Circuit

Figure 18. Four Times Boosting Circuit

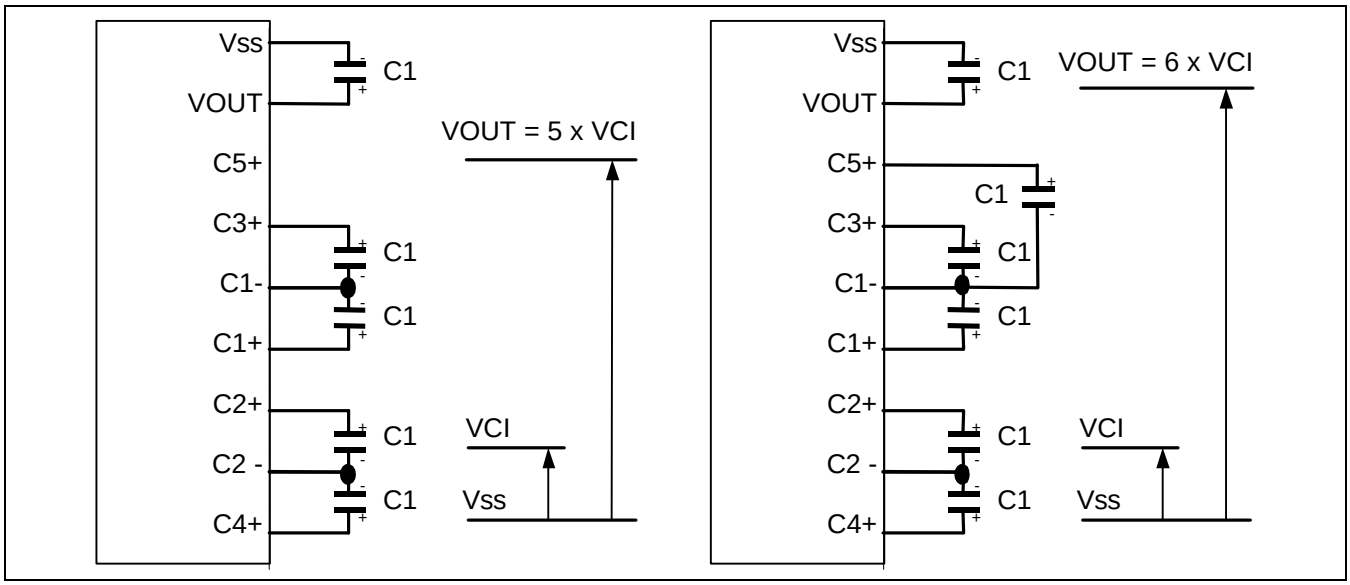

Figure 19. Five Times Boosting Circuit

Figure 20. Six Times Boosting Circuit

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Voltage Regulator Circuits

The function of the internal Voltage Regulator circuits is to determine liquid crystal operating voltage, V0, by adjusting resistors, Ra and Rb, within the range of |V0| < |VOUT|. Because VOUT is the operating voltage of operational-amplifier circuits shown in Figure 21, it is necessary to be applied internally or externally.

For the Eq. 1, we determine V0 by Ra, Rb and V_{EV}. The Ra and Rb are connected internally or externally by INTRS pin. And V_{EV} called the voltage of electronic volume is determined by Eq. 2, where the parameter α is the value selected by instruction, "Set Reference Voltage Register", within the range 0 to 63. V_{REF} voltage at Ta= 25°C is shown in Table 11.

$$V0 = \left(1 + \frac{Rb}{Ra}\right) \times V_{EV} \quad [V] \text{ ------ (Eq. 1)}$$

$$V_{EV} = \left(1 - \frac{(63 - \alpha)}{210}\right) \times V_{REF} \quad [V] \text{ ------ (Eq. 2)}$$

Table 11. . V_{REF} Voltage at Ta = 25°C

REF	Temp. coefficient	V_{REF} [V]
1	-0.05% / °C	2.1
0	External input	VEXT

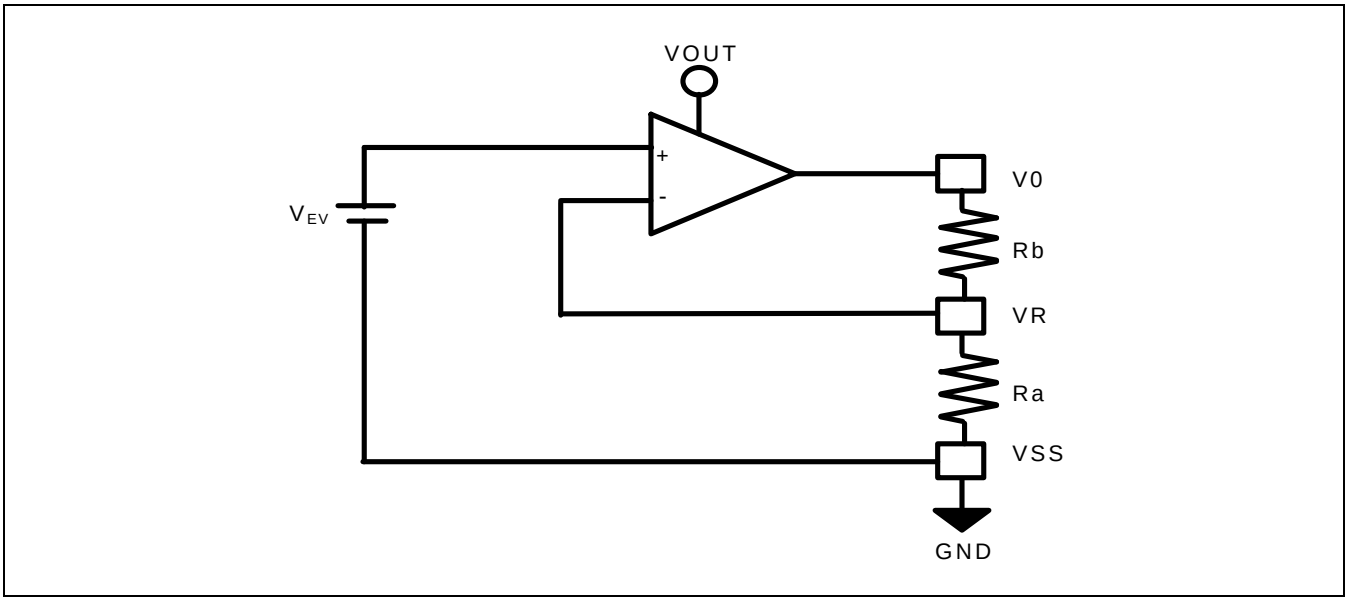

Figure 21. Internal Voltage Regulator Circuit

In Case of Using Internal Resistors, Ra and Rb (INTRS = "H")

When INTRS pin is **"H"**, resistor Ra is connected internally between VR pin and Vss, and Rb is connected between V0 and VR. We determine V0 by two instructions, "Regulator Resistor Select" and "Set Reference Voltage".

Table 12. Internal Rb / Ra Ratio depending on 3-bit Data (R2 R1 R0)

	3-bit data settings (R2 R1 R0)							
	0 0 0	**0 0 1**	**0 1 0**	**0 1 1**	**1 0 0**	**1 0 1**	**1 1 0**	**1 1 1**
1 + (Rb / Ra)	2.3	3.0	3.7	4.4	5.1	5.8	6.5	7.2

Figure 22 Shows V0 voltage measured by adjusting internal regulator register ratio (Rb / Ra) and 6-bit electronic volume registers for each temperature coefficient at Ta = 25 °C.

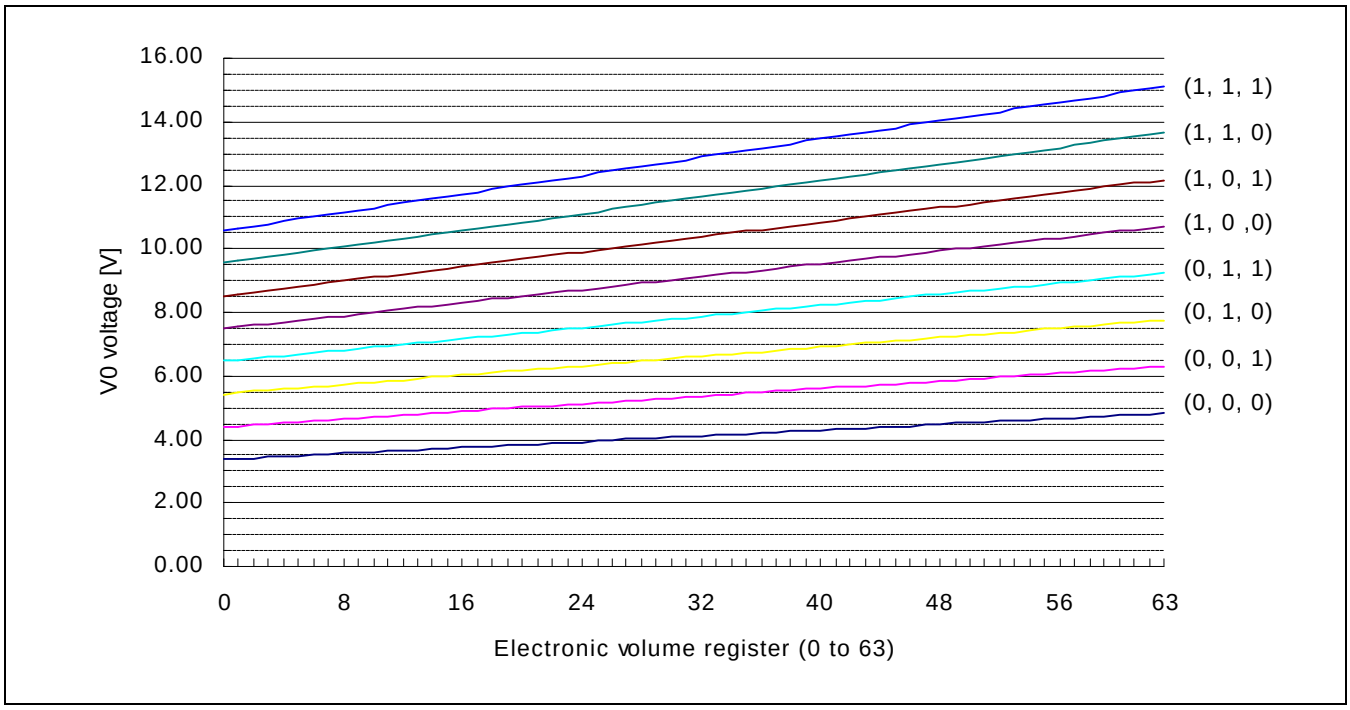

Figure 22. Electronic Volume Level (Temp. Coefficient = -0.05% / °C)

In Case of Using External Resistors, Ra and Rb (INTRS = "L")

When INTRS pin is **"L"**, it is necessary to connect external regulator resistor Ra between VR and VSS, and Rb between V0 and VR.

Example: For the following requirements

1. LCD driver voltage, V0 = 10V
2. 6-bit reference voltage register = (1, 0, 0, 0, 0, 0)
3. Maximum current flowing Ra, Rb = 1 uA

From Eq. 1

$$10 = \left(1 + \frac{Rb}{Ra}\right) \times V_{EV} \quad [V] \text{ ------ (Eq. 3)}$$

From Eq. 2

$$V_{EV} = \left(1 - \frac{(63 - 32)}{210}\right) \times 2.1 = 1.79 \quad [V] \text{ ------ (Eq. 4)}$$

From requirement 3.

$$\frac{10}{Ra + Rb} = 1 \text{ [uA]} \quad \text{------ (Eq. 5)}$$

From equations Eq. 3, 4 and 5

Ra = 1.79 [MΩ]

Rb = 8.21 [MΩ]

Table 13 Shows the Range of V0 depending on the above Requirements.

Table 13. The Range of V0

	Electronic volume level				
	0	**.....**	**32**	**.....**	**63**
V0	8.21	.....	10.00	.....	11.73

Voltage Follower Circuits

VLCD voltage (V0) is resistively divided into four voltage levels (V1, V2, V3 and V4), and those output impedance are converted by the Voltage Follower for increasing drive capability. Table 14 shows the relationship between V1 to V4 level and each duty ratio.

Table 14

LCD bias	V1	V2	V3	V4	Remarks
1/N	(N-1)/N x V0	(N-1)/N x V0	2/N x V0	1/N x V0	N = 4 to 11

REFERECE CIRCUIT EXAMPLES

[C1 = 1.0 to 4.7 [µF], C2 = 0.1 to 0.47 [µF]]

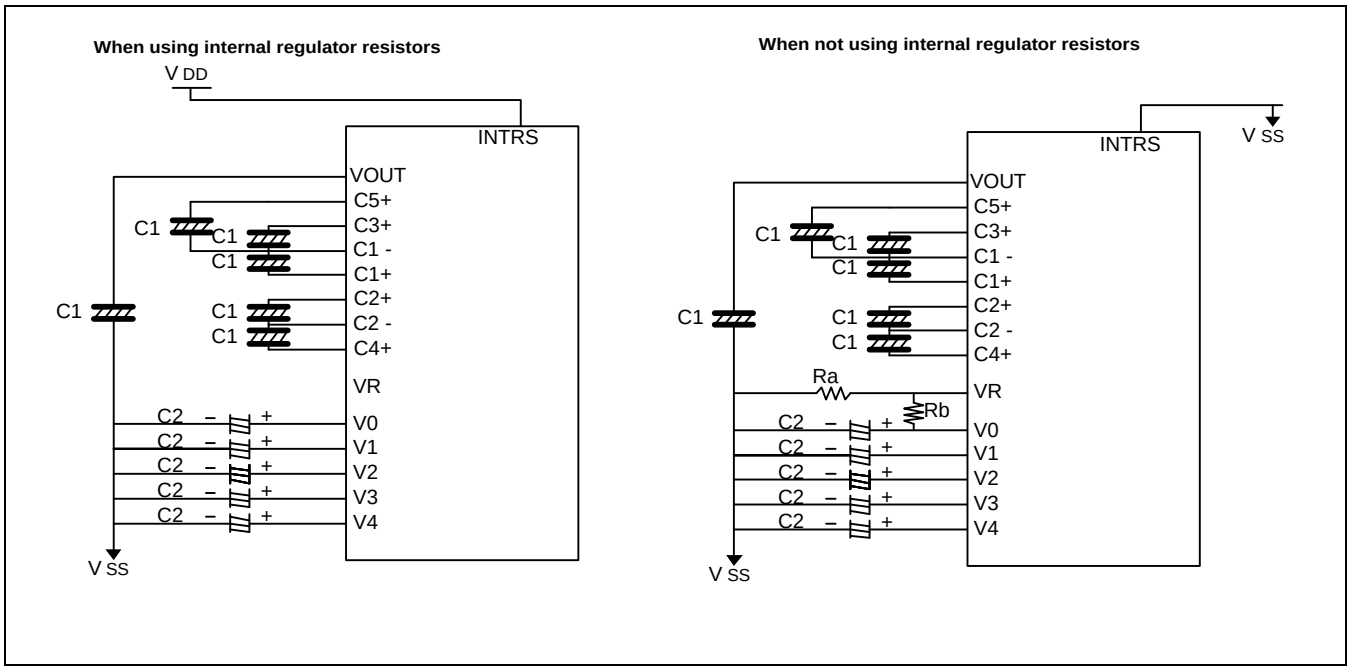

Figure 23. When Using all LCD Power Circuits (6-Time V/C: ON, V/R: ON, V/F: ON)

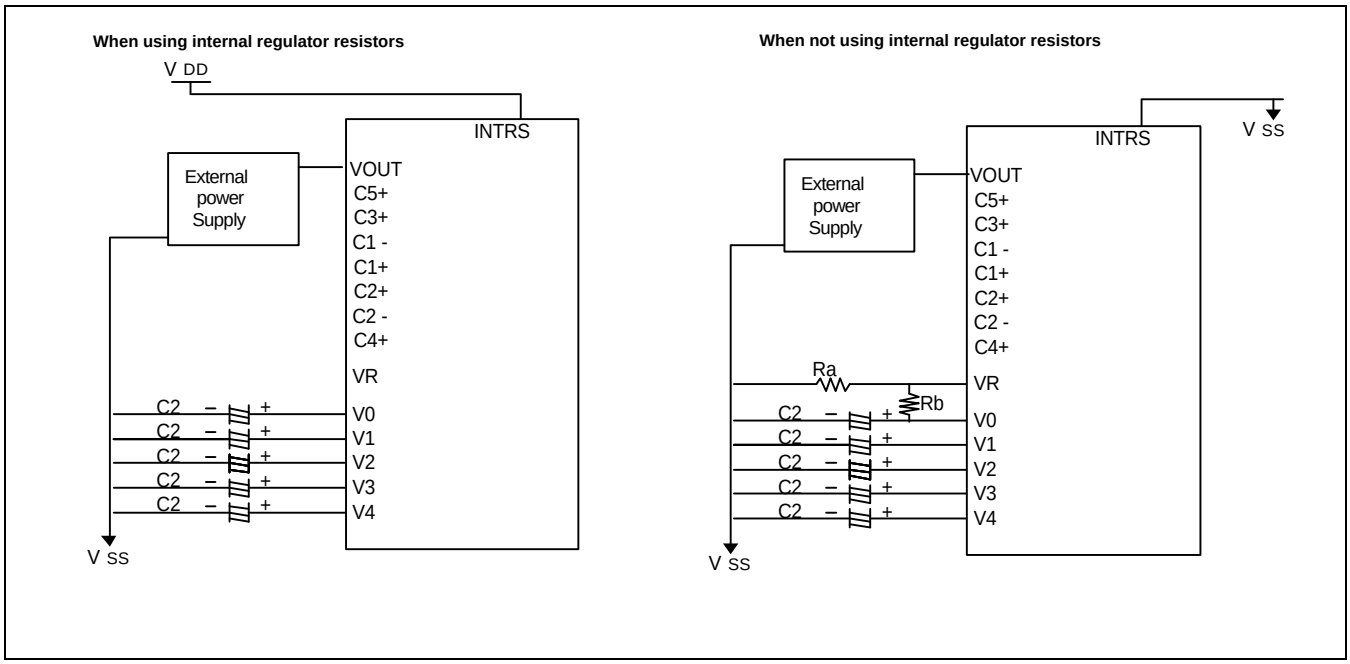

Figure 24. When Using some LCD Power Circuits (V/C: OFF, V/R: ON, V/F: ON)

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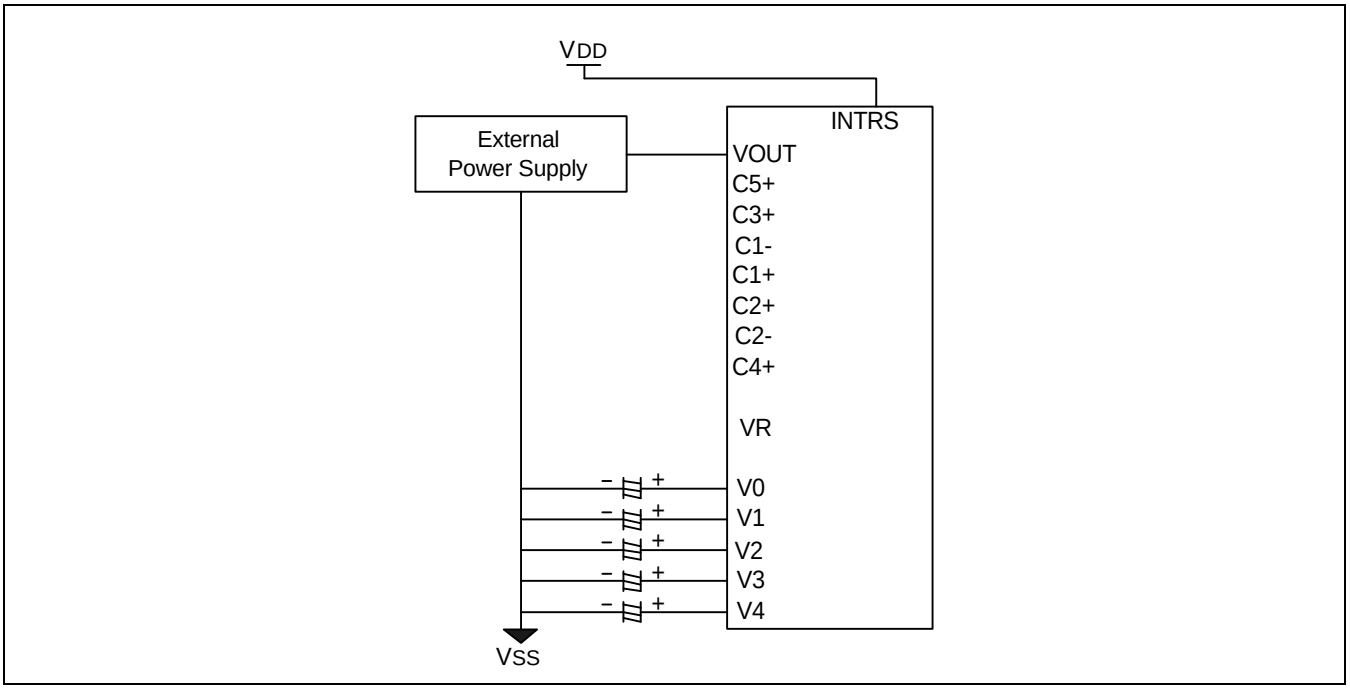

Figure 25. When Using only Voltage Follower Circuit (V/C: OFF, V/R: OFF, V/F: ON)

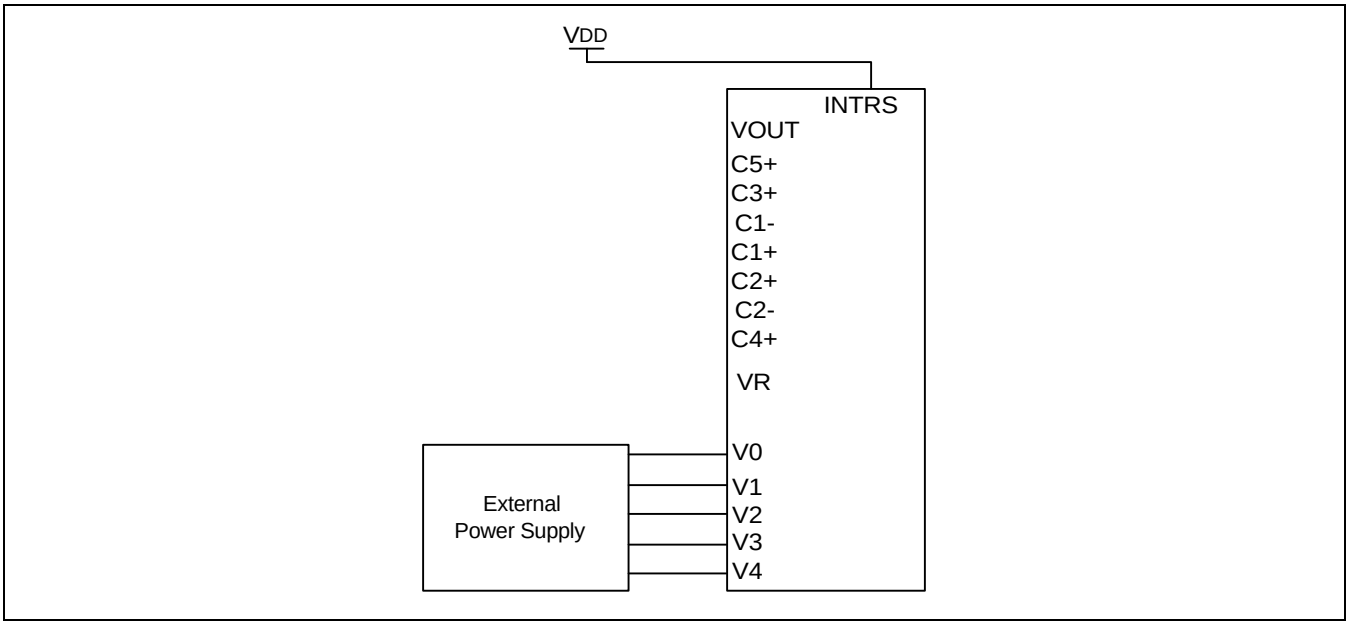

Figure 26. When Not Using all LCD Power Circuits (V/C: OFF, V/R: OFF, V/F: OFF)

RESET CIRCUIT

Setting RESETB to "L" or Reset instruction can initialize internal function.
When RESETB becomes "L", following procedure is occurred.

Page address: 0
Column address: 0
Modify-read: OFF
Display ON / OFF: OFF
Initial display line: 0 (first)
Initial COM0 register: 0 (COM0)
Partial display duty ratio: 1/81
Reverse display ON / OFF: OFF (normal)
n-line inversion register: 0 (disable)
Entire display ON / OFF: OFF (normal)
Power control register (VC, VR, VF) = (0, 0, 0)
DC-DC step up: 3 times converter circuit = (0, 0)
Regulator resistor select register: (R2, R1, R0) = (0, 0, 0)
Reference voltage control register: (EV5, EV4, EV3, EV2, EV1, EV0) = (1, 0, 0, 0, 0, 0)
LCD bias ratio: 1/10
SHL select: OFF (normal)
ADC select: OFF (normal)
Oscillator status: OFF
Power save mode: release

When RESET instruction is issued, following procedure is occurred.

Page address: 0
Column address: 0
Modify-read: OFF
Initial display line: 0 (First)
Regulator resistor select register: (R2, R1, R0) = (0, 0, 0)
Reference voltage control register (EV5, EV4, EV3, EV2, EV1, EV0) = (1, 0, 0, 0, 0, 0)
Other instruction registers : Not Chaned

While RESETB is "L" or reset instruction is executed, no instruction except read status can be accepted. Reset status appears at DB4. After DB4 becomes "L", any instruction can be accepted. RESETB must be connected to the reset pin of the MPU, and initialize the MPU and this LSI at the same time. The initialization by RESETB is essential before used.

INSTRUCTION DESCRIPTION

Table 15. Instruction Table

×: Don't care

Instruction	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
Read display data	1	1	Read data								Read data from DDRAM
Write display data	1	0	Write data								Write data into DDRAM
Read status	0	1	BUSY	ADC	ON	RES	0	0	0	0	Read the internal status
Set page address	0	0	1	0	1	1	P3	P2	P1	P0	Set page address
Set column address MSB	0	0	0	0	0	1	0	Y6	Y5	Y4	Set column address MSB
Set column address LSB	0	0	0	0	0	0	Y3	Y2	Y1	Y0	Set column address LSB
Set modify-read	0	0	1	1	1	0	0	0	0	0	Set modify-read mode
Reset modify-read	0	0	1	1	1	0	1	1	1	0	Release modify-read mode
Display ON / OFF	0	0	1	0	1	0	1	1	1	D	D = 0: display OFF D = 1: display ON
Set initial display line register	0	0	0	1	0	0	0	0	×	×	2-byte instruction to specify the initial display line to realize vertical scrolling
	0	0	×	S6	S5	S4	S3	S2	S1	S0	
Set initial COM0 register	0	0	0	1	0	0	0	1	×	×	2-byte instruction to specify the initial COM0 to realize window scrolling
	0	0	×	C6	C5	C4	C3	C2	C1	C0	
Set partial display duty ratio	0	0	0	1	0	0	1	0	×	×	2-byte instruction to set partial display duty ratio
	0	0	×	D6	D5	D4	D3	D2	D1	D0	
Set n-line inversion	0	0	0	1	0	0	1	1	×	×	2-byte instruction to set n-line inversion register
	0	0	×	×	×	N4	N3	N2	N 1	N0	
Release n-line inversion	0	0	1	1	1	0	0	1	0	0	Release n-line inversion mode
Reverse display ON / OFF	0	0	1	0	1	0	0	1	1	REV	REV = 0: normal display REV = 1: reverse display
Entire display ON / OFF	0	0	1	0	1	0	0	1	0	EON	EON = 0: normal display EON = 1: entire display ON

Table 16. Instruction Table (Continued)

Instruction	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
Power control	0	0	0	0	1	0	1	VC	VR	VF	Control power circuit operation
Select DC-DC step-up	0	0	0	1	1	0	0	1	DC1	DC0	Select the step-up of the internal voltage converter
Select regulator resistor	0	0	0	0	1	0	0	R2	R1	R0	Select internal resistance ratio of the regulator resistor
Set electronic volume register	0	0	1	0	0	0	0	0	0	1	2-byte instruction to specify the electronic volume register
	0	0	×	×	EV5	EV4	EV3	EV2	EV1	EV0	
Select LCD bias	0	0	0	1	0	1	0	B2	B1	B0	Select LCD bias
SHL select	0	0	1	1	0	0	SHL	×	×	×	COM bi-directional selection SHL = 0: normal direction SHL = 1: reverse direction
ADC select	0	0	1	0	1	0	0	0	0	ADC	SEG bi-directional selection ADC = 0: normal direction ADC = 1: reverse direction
Set Data Direction & Display Data Length(DDL)	×	×	1	1	1	0	1	0	0	0	2-byte Instruction to specify the number of data bytes(SPI Mode).
	×	×	D7	D6	D5	D4	D3	D2	D1	D0	
Oscillator ON start	0	0	1	0	1	0	1	0	1	1	Start the built-in oscillator
Set power save mode	0	0	1	0	1	0	1	0	0	P	P = 0: standby mode P = 1: sleep mode
Release power save mode	0	0	1	1	1	0	0	0	0	1	Release power save mode
Reset	0	0	1	1	1	0	0	0	1	0	Initialize the internal functions
NOP	0	0	1	1	1	0	0	0	1	1	***No operation***
Test instruction	0	0	1	1	1	1	×	×	×	×	***Don't use this instruction.***

Read Display Data

8-bit data from Display Data RAM specified by the column address and page address can be read by this instruction. As the column address is incremented by 1 automatically after each this instruction, the microprocessor can continuously read data from the addressed page. A dummy read is required after loading an address into the column address register. Display Data cannot be read through the serial interface.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	Read data							

Write Display Data

8-bit data of display data from the microprocessor can be written to the RAM location specified by the column address and page address. The column address is incremented by 1 automatically so that the microprocessor can continuously write data to the addressed page.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	Write data							

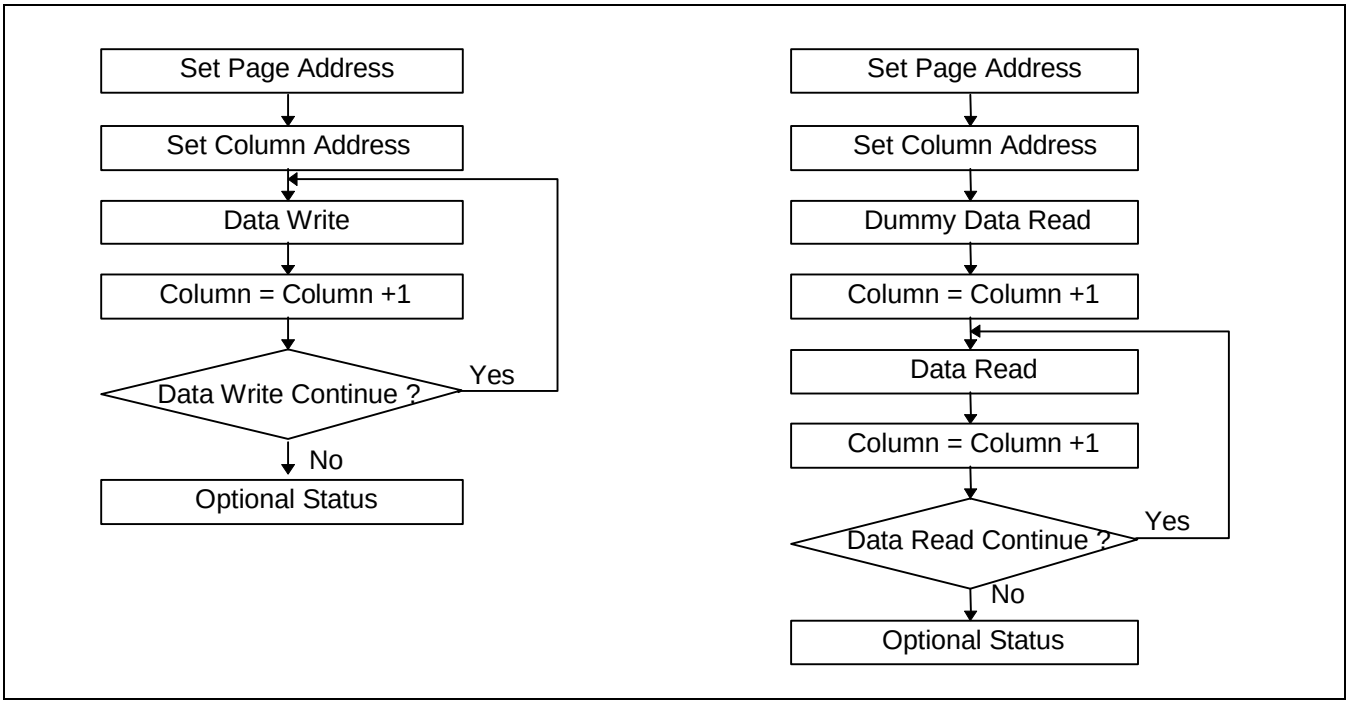

Figure 27. Sequence for Writing Display Data **Figure 28. Sequence for Reading Display Data**

Read Status

Indicates the internal status of the KS0759

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BUSY	ADC	ON	RES	0	0	0	0

Flag	Description
BUSY	The device is busy when internal operation or reset. Any instruction is rejected until BUSY goes Low. 0: chip is active, 1: chip is being busy.
ADC	Indicates the relationship between RAM column address and segment driver. 0: reverse direction (SEG127 → SEG0), 1: normal direction (SEG0 → SEG127)
ON	Indicates display ON / OFF status. 0: display ON, 1: display OFF
RES	Indicates the initialization is in progress by RESETB signal. 0: chip is active, 1: chip is being reset.

Set Page Address

Sets the Page Address of display data RAM from the microprocessor into the Page Address register. Any RAM data bit can be accessed when its Page Address and column address are specified. Along with the column address, the Page Address defines the address of the display RAM to write or read display data. Changing the Page Address doesn't effect to the display status.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	1	P3	P2	P1	P0

P3	P2	P1	P0	Selected page	Description
0	0	0	0	0	Accessible pages for displaying dot-matrix display data
0	0	0	1	1	
0	0	1	0	2	
:	:	:	:	:	
1	0	0	1	9	
1	0	1	0	10	Accessible page for displaying icons
1	0	1	1	11	Not accessible page. Do not use these pages.
1	1	0	0	12	
1	1	0	1	13	
1	1	1	0	14	
1	1	1	1	15	

Set Column Address

Sets the Column Address of display RAM from the microprocessor into the column address register. Along with the Column Address, the column address defines the address of the display RAM to write or read display data. When the microprocessor reads or writes display data to or from display RAM, Column Addresses are automatically incremented.

Set Column Address MSB

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	0	Y6	Y5	Y4

Set Column Address LSB

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	Y3	Y2	Y1	Y0

Y6	Y5	Y4	Y3	Y2	Y1	Y0	Selected column address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
0	0	0	0	0	1	0	2
:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:
1	1	1	1	1	0	1	125
1	1	1	1	1	1	0	126
1	1	1	1	1	1	1	127

Set Modify-Read

This instruction stops the automatic increment of the column address by the read display data instruction, but the column address is still increased by the Write display data instruction. And it reduces the load of microprocessor when the data of a specific area is repeatedly changed during cursor blinking or others. This mode is canceled by the reset Modify-read instruction.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	0	0

Reset Modify-Read

This instruction cancels the Modify-read mode, and makes the column address return to its initial value just before the set Modify-read instruction is started.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	1	1	1	0

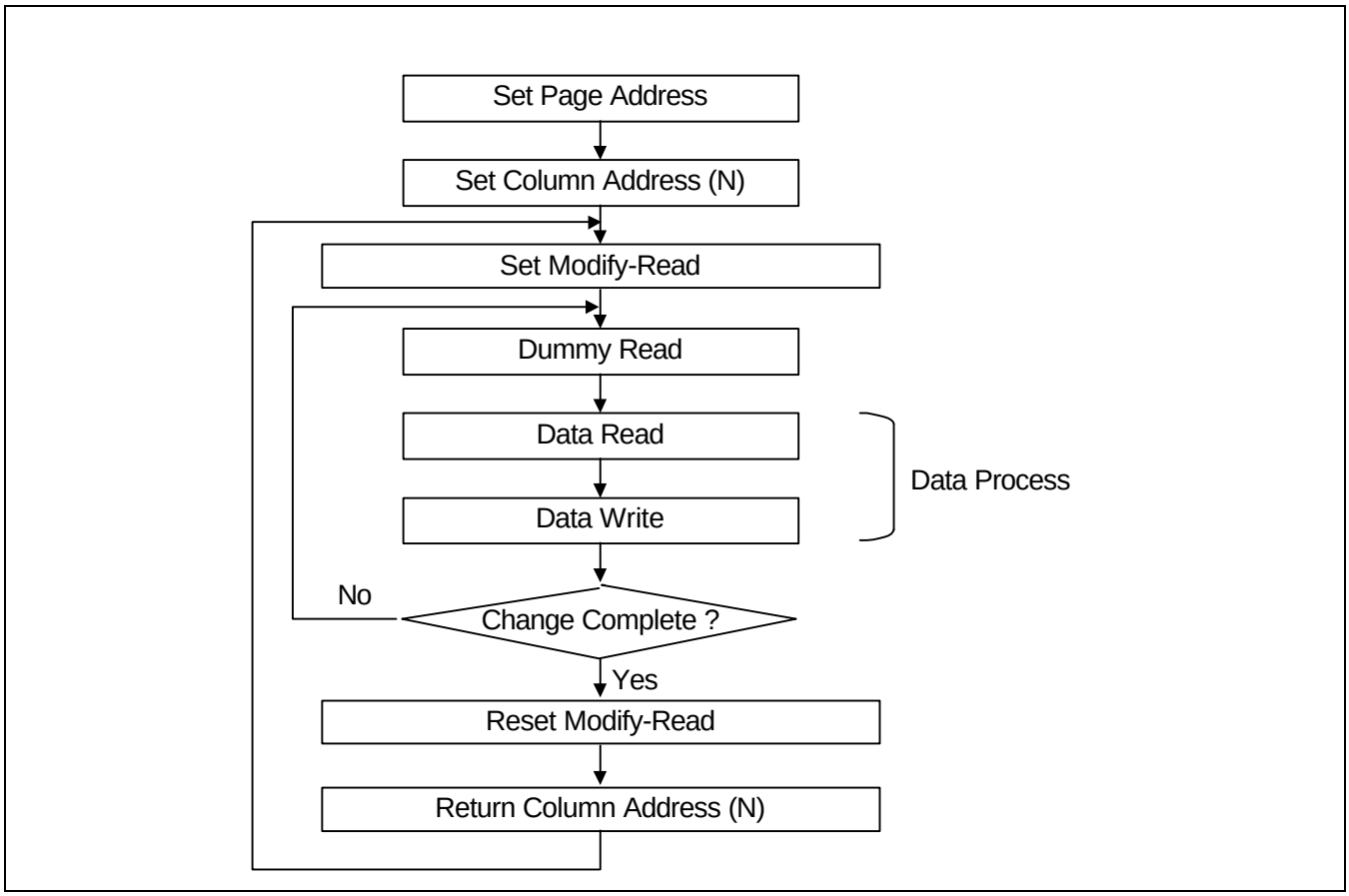

Figure 29. Sequence for Cursor Display

Display ON / OFF

Turns the display ON or OFF

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	1	1	D

D = 1: display ON
D = 0: display OFF

Set Initial Display Line Register

Sets the line address of display RAM to determine the initial display line using 2-byte instruction. The RAM display data is displayed at the top row (COM0) of LCD panel.

The 1st Instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	0	0	×	×

The 2nd Instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	×	S6	S5	S4	S3	S2	S1	S0

S6	S5	S4	S3	S2	S1	S0	Selected line address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
:	:	:	:	:	:	:	:
1	0	1	0	0	0	0	80
1	0	1	0	0	0	1	81
1	0	1	0	0	1	0	No operation
:	:	:	:	:	:	:	
1	1	1	1	1	1	1	

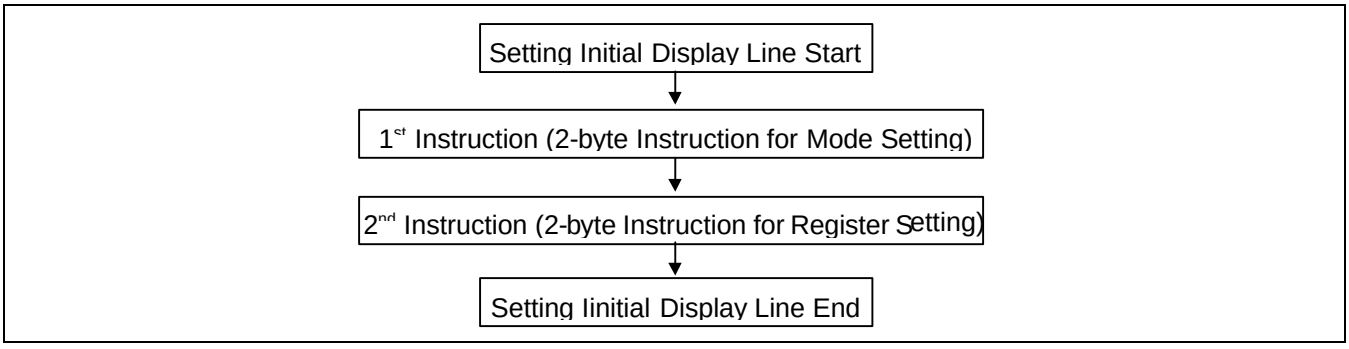

Figure 30. The Sequence for Setting the Initial Display Line

Set Initial COM0 Register

Sets the initial row (COM0) of the LCD panel using the 2-byte instruction. By using this instruction, it is possible to realize the window moving without the change of display data.

The 1st Instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	0	1	×	×

The 2nd Instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	×	C6	C5	C4	C3	C2	C1	C0

C6	C5	C4	C3	C2	C1	C0	Initial COM0
0	0	0	0	0	0	0	COM0
0	0	0	0	0	0	1	COM1
0	0	0	0	0	1	0	COM2
0	0	0	0	0	1	1	COM3
:	:	:	:	:	:	:	:
1	0	0	1	1	0	0	COM76
1	0	0	1	1	0	1	COM77
1	0	0	1	1	1	0	COM78
1	0	0	1	1	1	1	COM79
1	0	1	0	0	0	0	No operation
:	:	:	:	:	:	:	
1	1	1	1	1	1	1	

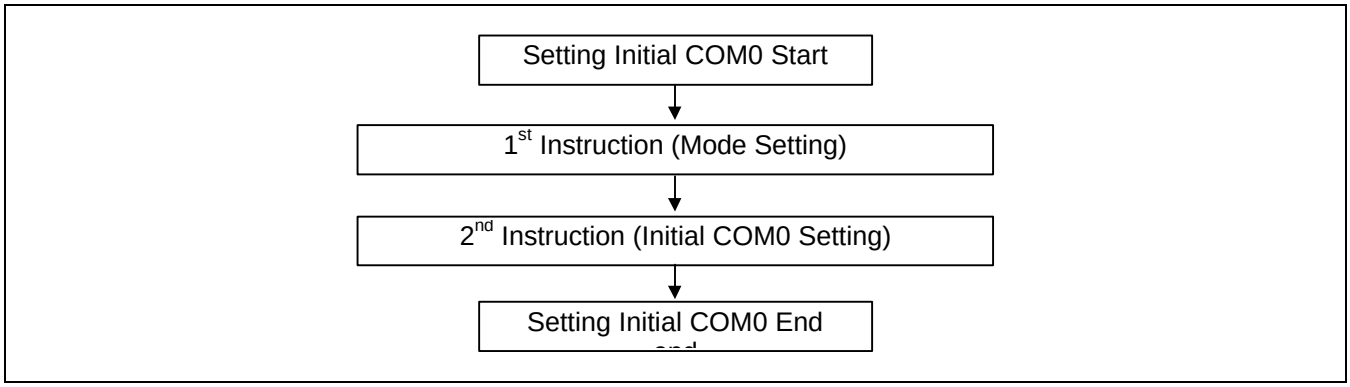

Figure 31. Sequence for Setting the Initial COM0

Set Partial Display Duty Ratio

Sets the duty ratio within range of 17 to 81 to realize partial display by using the 2-byte instruction.

The 1st Instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	1	0	×	×

The 2nd Instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	×	D6	D5	D4	D3	D2	D1	D0

D6	D5	D4	D3	D2	D1	D0	Selected partial duty ratio
0	0	0	0	0	0	0	No operation
:	:	:	:	:	:	:	
0	0	1	0	0	0	0	
0	0	1	0	0	0	1	1/17
0	0	1	0	0	1	0	1/18
0	0	1	0	0	1	1	1/19
0	0	1	0	1	0	0	1/20
:	:	:	:	:	:	:	:
1	0	0	1	1	1	0	1/78
1	0	0	1	1	1	1	1/79
1	0	1	0	0	0	0	1/80
1	0	1	0	0	0	1	1/81
1	0	1	0	0	1	0	No operation
:	:	:	:	:	:	:	
1	1	1	1	1	1	1	

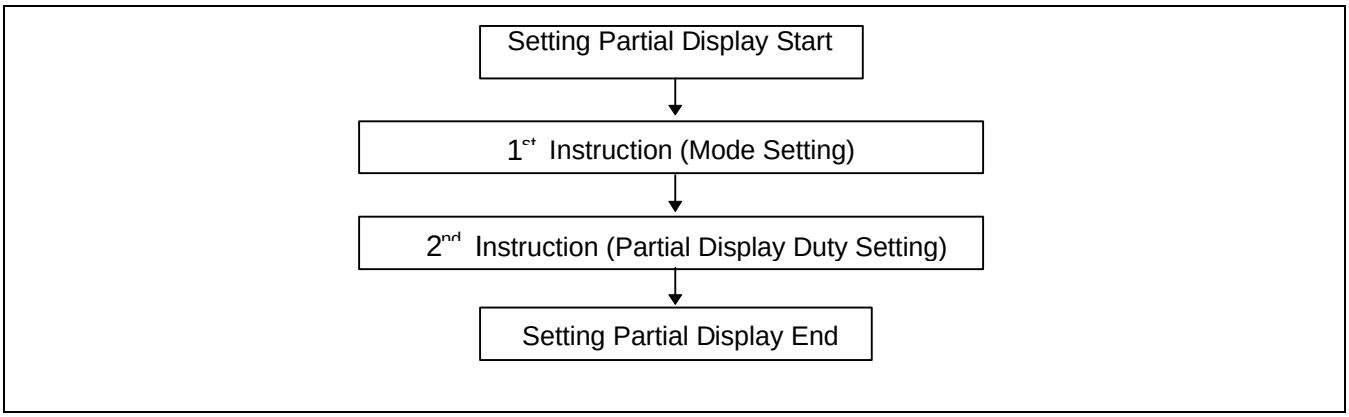

Figure 32. Sequence for Setting Partial Display

Set N-line Inversion Register

Sets the inverted line number within range of 3 to 33 to improve the display quality by controlling the phase of the internal LCD AC signal (Internal M) by using the 2-byte instruction.

The 1st Instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	1	1	×	×

The 2nd Instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	×	×	×	N4	N3	N2	N1	N0

N4	N3	N2	N1	N0	Selected n-line inversion
0	0	0	0	0	0-line inversion (frame inversion)
0	0	0	0	1	3-line inversion
0	0	0	1	0	4-line inversion
:	:	:	:	:	:
1	1	1	0	1	31-line inversion
1	1	1	1	0	32-line inversion
1	1	1	1	1	33-line inversion

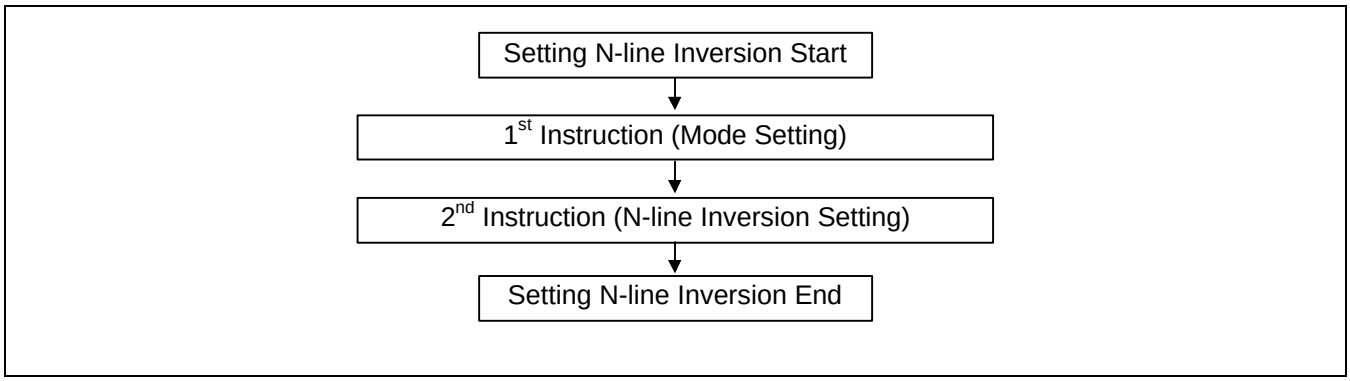

Figure 33. Sequence for Setting Partial Display

Release N-line Inversion

Returns to the frame inversion condition from the n-line inversion condition.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	1	0	0

Reverse Display ON / OFF

Reverses the display status on LCD panel without rewriting the contents of the display data RAM.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	1	1	REV

REV	RAM bit data = “1”	RAM bit data = “0”
0 (normal)	LCD pixel is illuminated	LCD pixel is not illuminated
1 (reverse)	LCD pixel is not illuminated	LCD pixel is illuminated

Entire Display ON / OFF

Forces the whole LCD points to be turned on regardless of the contents of the display data RAM. At this time, the contents of the display data RAM are held. This instruction has priority over the reverse display ON / OFF instruction.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	1	0	EON

EON	RAM bit data = “1”	RAM bit data = “0”
0 (normal)	LCD pixel is illuminated	LCD pixel is not illuminated
1 (entire)	LCD pixel is illuminated	LCD pixel is illuminated

Power Control

Selects one of eight power circuit functions by using 3-bit register. An external power supply and part of internal power supply functions can be used simultaneously.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	1	VC	VR	VF

VC	VR	VF	Status of internal power supply circuits
0 1			Internal voltage converter circuit is OFF Internal voltage converter circuit is ON
	0 1		Internal voltage regulator circuit is OFF Internal voltage regulator circuit is ON
		0 1	Internal voltage follower circuit is OFF Internal voltage follower circuit is ON

Select DC-DC Step-up

Selects one of 4 DC-DC step-up to reduce the power consumption by this instruction. It is very useful to realize the partial display function.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	1	0	0	1	DC1	DC0

DC1	DC0	Selected DC-DC converter circuit
0	0	3 times boosting circuit
0	1	4 times boosting circuit
1	0	5 times boosting circuit
1	1	6 times boosting circuit

Regulator Resistor Select

Selects resistance ratio of the internal resistor used in the internal voltage regulator. See voltage regulator section in power supply circuit. Refer to Table 13.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	0	R2	R1	R0

R2	R1	R0	[Rb / Ra] ratio
0	0	0	Small
0	0	1	:
:	:	:	:
1	1	0	:
1	1	1	Large

Set Electronic Volume Register

Consists of 2-byte instruction
The 1st instruction sets electronic volume mode, the 2nd one updates the contents of electronic volume register. After second instruction, electronic volume mode is released.

The 1st Instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	0	0	0	0	1

The 2nd Instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	×	×	EV5	EV4	EV3	EV2	EV1	EV0

EV5	EV4	EV3	EV2	EV1	EV0	Reference voltage (α)
0	0	0	0	0	0	0
0	0	0	0	0	1	1
:	:	:	:	:	:	:
:	:	:	:	:	:	:
1	1	1	1	1	0	62
1	1	1	1	1	1	63

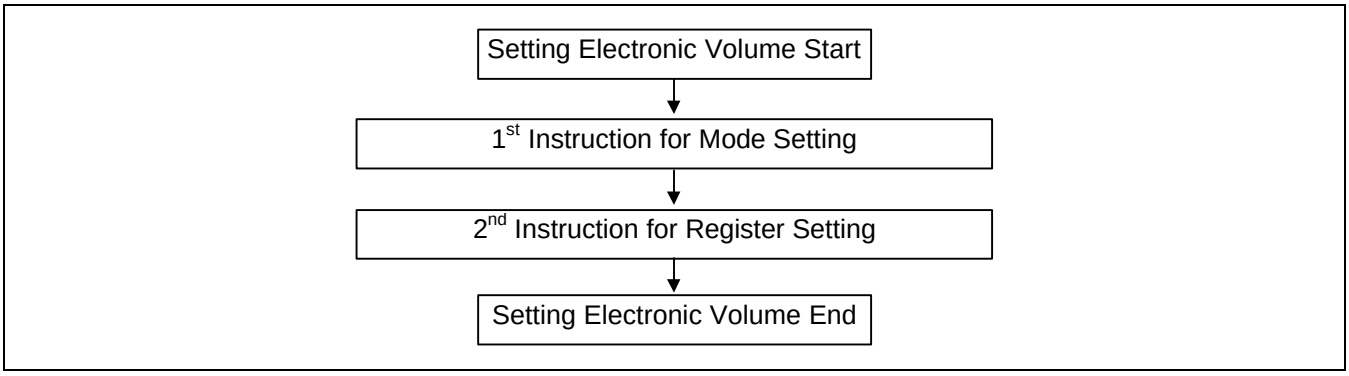

Figure 34. Sequence for Setting the Electronic Volume

Select LCD Bias

Selects LCD Bias ratio of the voltage required for driving the LCD.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	1	0	B2	B1	B0

B2	B1	B0	Selected LCD bias
0	0	0	1/4
0	0	1	1/5
0	1	0	1/6
0	1	1	1/7
1	0	0	1/8
1	0	1	1/9
1	1	0	1/10
1	1	1	1/11

SHL Select

COM output scanning direction is selected by this instruction which determines the LCD driver output status.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	0	0	SHL	×	×	×

SHL = 0: normal direction (COM0 → COM79)
SHL = 1: reverse direction (COM79 → COM0)

ADC Select

Changes the relationship between RAM column address and segment driver. The direction of segment driver output pins could be reversed by software. This makes IC layout flexible in LCD module assembly.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	0	ADC

ADC = 0: normal direction (SEG0 → SEG127)
ADC = 1: reverse direction (SEG127 → SEG0)

Set Data Direction & Display Data Length (3-Pin SPI Mode)

Consists of two bytes instruction.
This command is used in 3-Pin SPI mode only(PS0 = "L" and PS1 = "L"). It will be two continuous commands, the first byte control the data direction(write mode only) and inform the LCD driver the second byte will be number of data bytes will be write. When RS is not used, the Display Data Length instruction is used to indicate that a specified number of display data bytes are to be transmitted. The next byte after the display data string is handled as command data.

The 1st Instruction: Set Data Direction (Only Write Mode)

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
x	x	1	1	1	0	1	0	0	0

The 2nd Instruction: Set Display Data Length (DDL) Register

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
x	x	D7	D6	D5	D4	D3	D2	D1	D0

D7	D6	D5	D4	D3	D2	D1	D0	Display Data Length
0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	1	2
0	0	0	0	0	0	1	0	3
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	0	1	254
1	1	1	1	1	1	1	0	255
1	1	1	1	1	1	1	1	256

Oscillator ON Start

This instruction enables the built-in oscillator circuit.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	1	1

Reset

This instruction resets initial display line, column address, page address, and common output status select to their initial status, but dose not affect the contents of display data RAM. This instruction cannot initialize the LCD power supply, which is initialized by the RESETB pin.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	1	0

Power Save

The KS0759 enters the Power Save status to reduce the power consumption to the static power consumption value and returns to the normal operation status by the following instructions.

Set Power Save Mode

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	0	P

P = 0: standby mode
P = 1: sleep mode

Release Power Save Mode

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	0	1

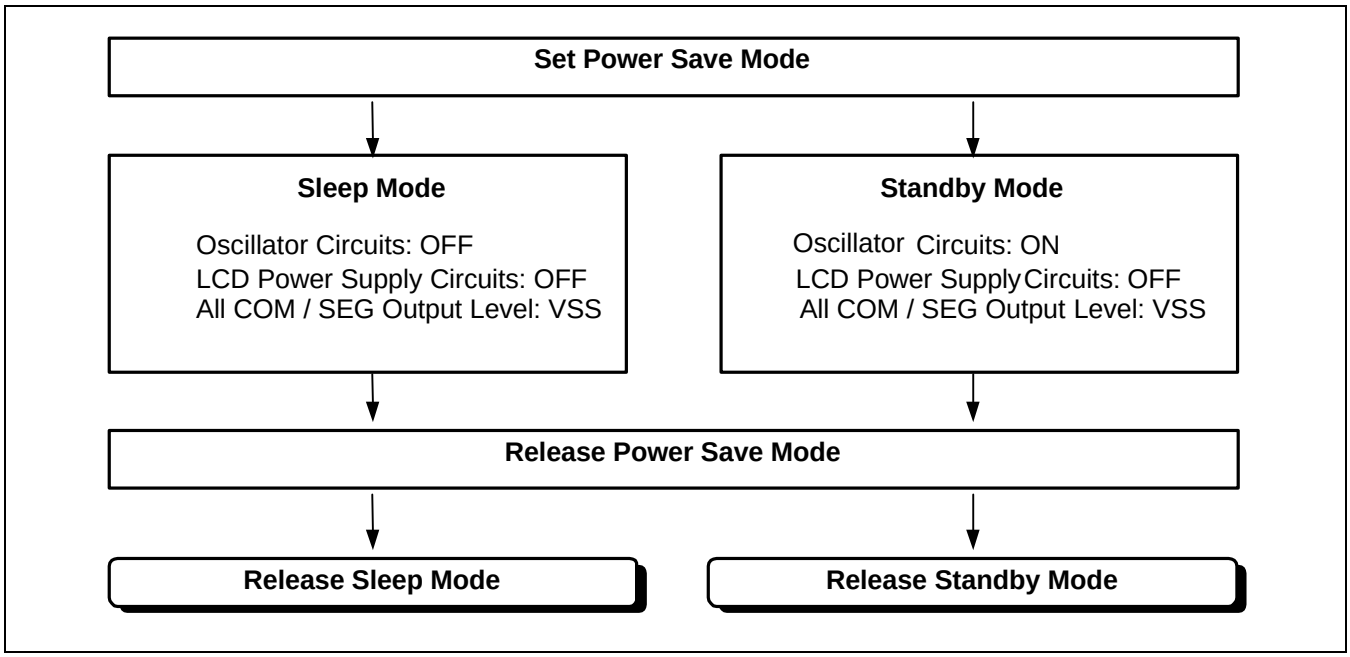

Figure 35. Power Save Routine

NOP

Non Operation Instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	1	1

Test Instruction

This instruction is for testing IC. Please do not use it.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	1	×	×	×	×

Referential Instruction Setup Flow: Initializing with the Built-in Power Supply Circuits

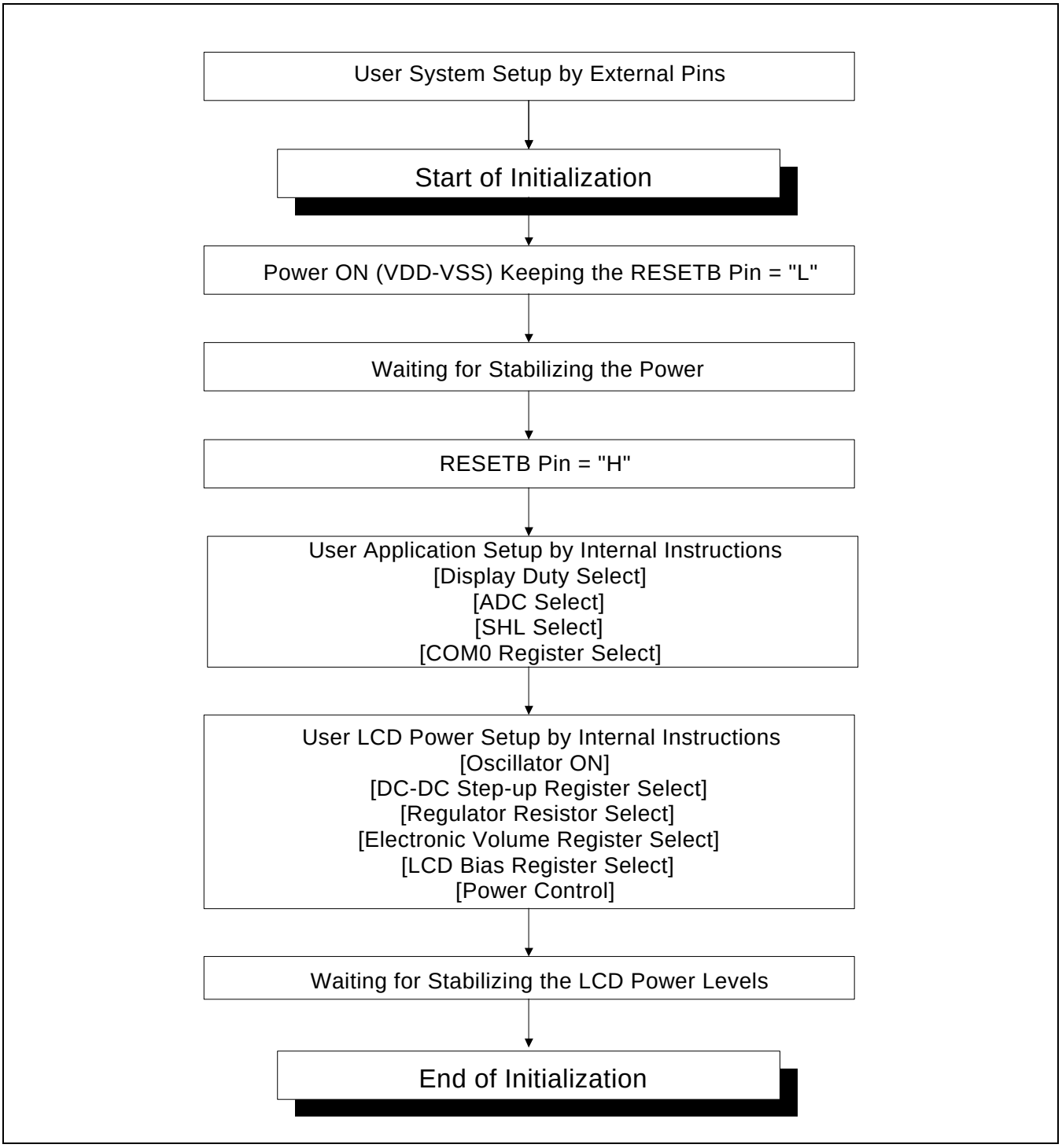

Figure 36. Initializing with the Built-in Power Supply Circuits

Referential Instruction Setup Flow: Initializing without the Built-in Power Supply Circuits

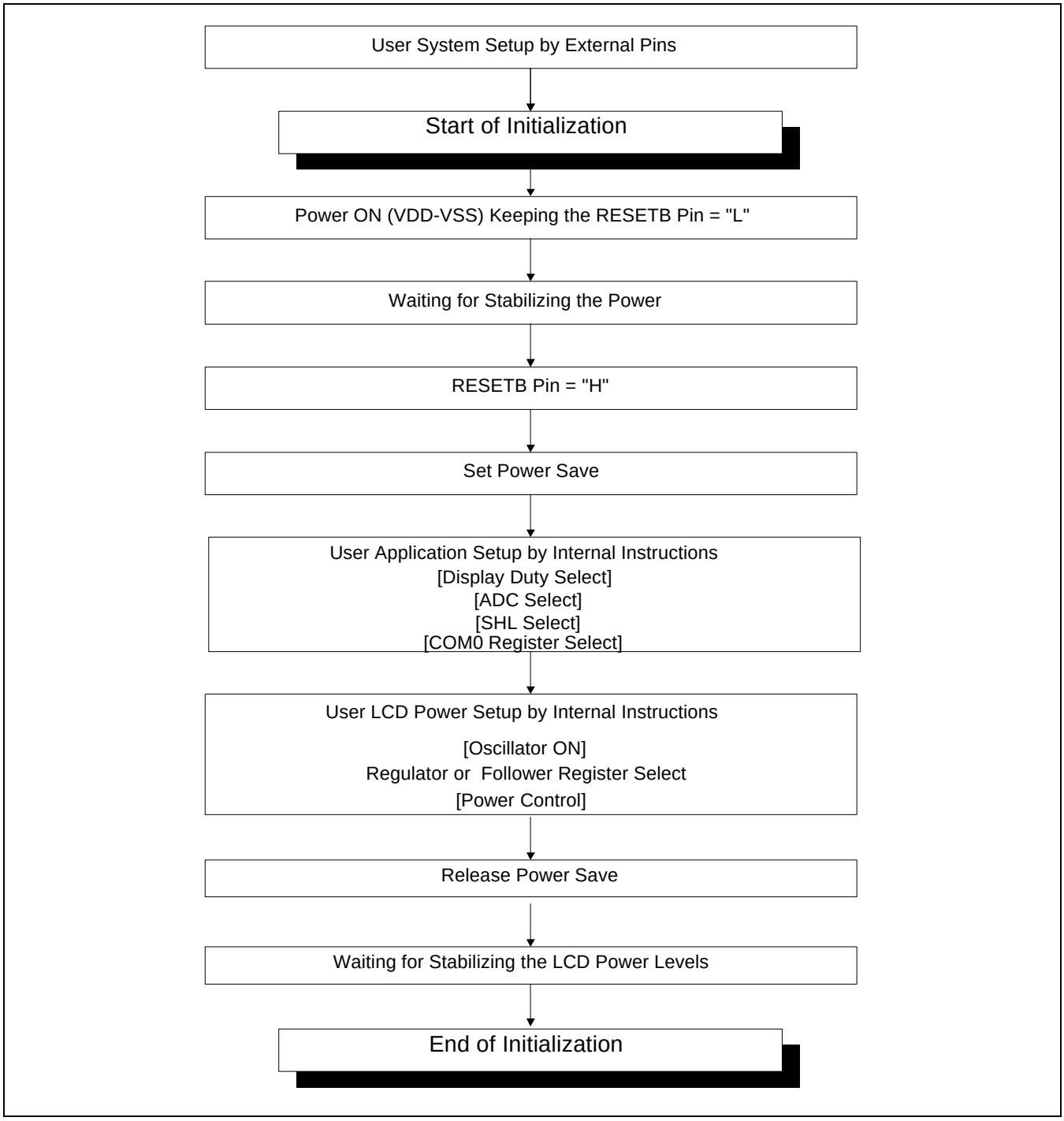

Figure 37. Initializing without the Built-in Power Supply Circuits

Referential Instruction Setup Flow: Data Displaying

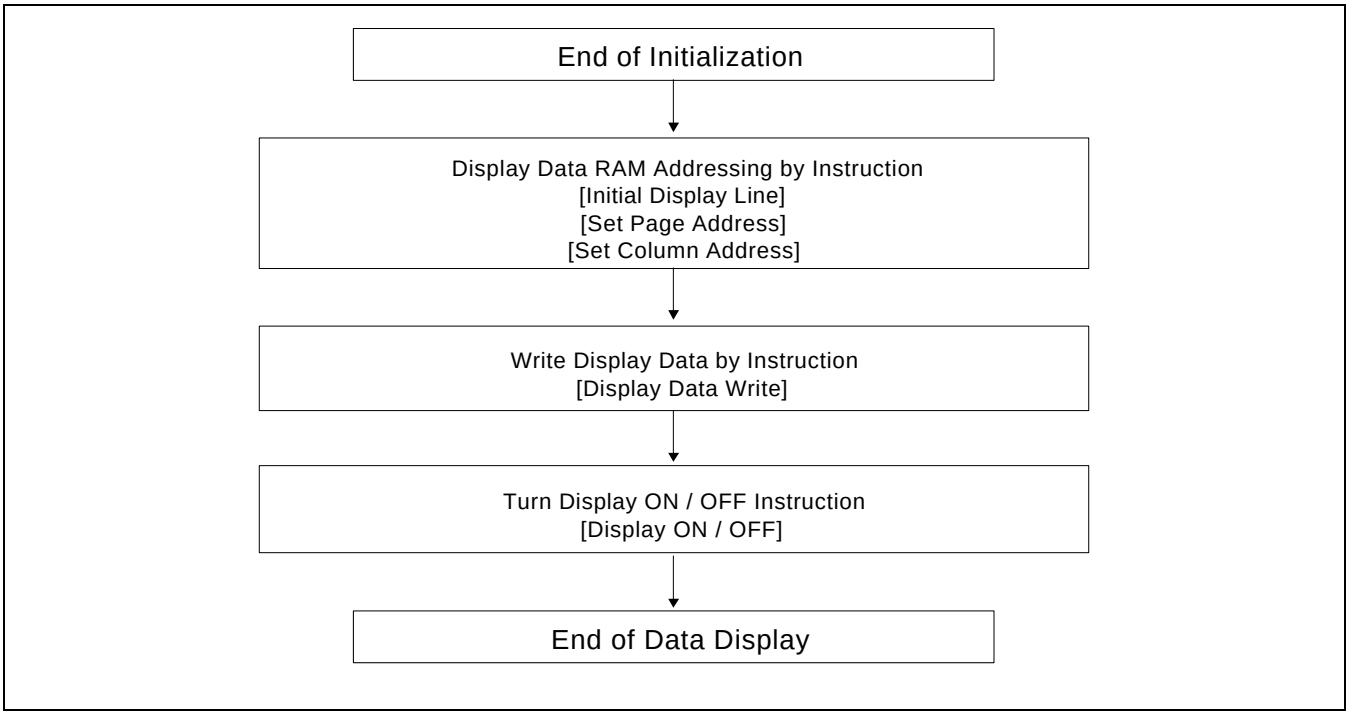

Figure 38. Data Displaying

Referential Instruction Setup Flow: Power OFF

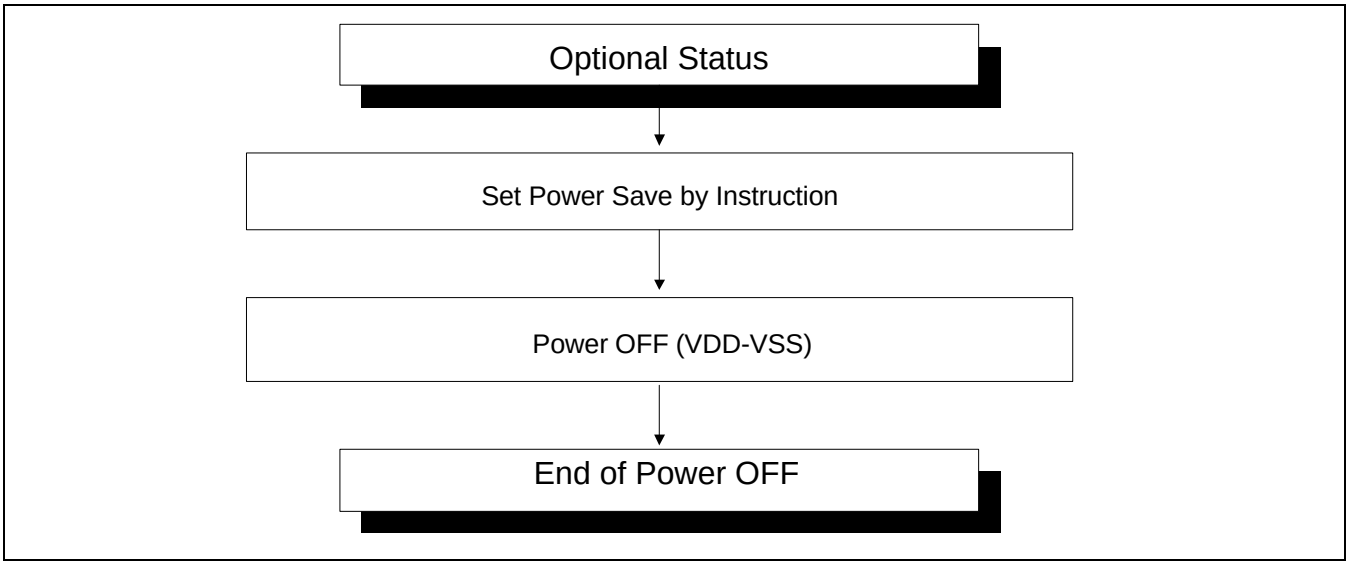

Figure 39. Power OFF

Referential Instruction Setup Flow: Partial Duty Changing

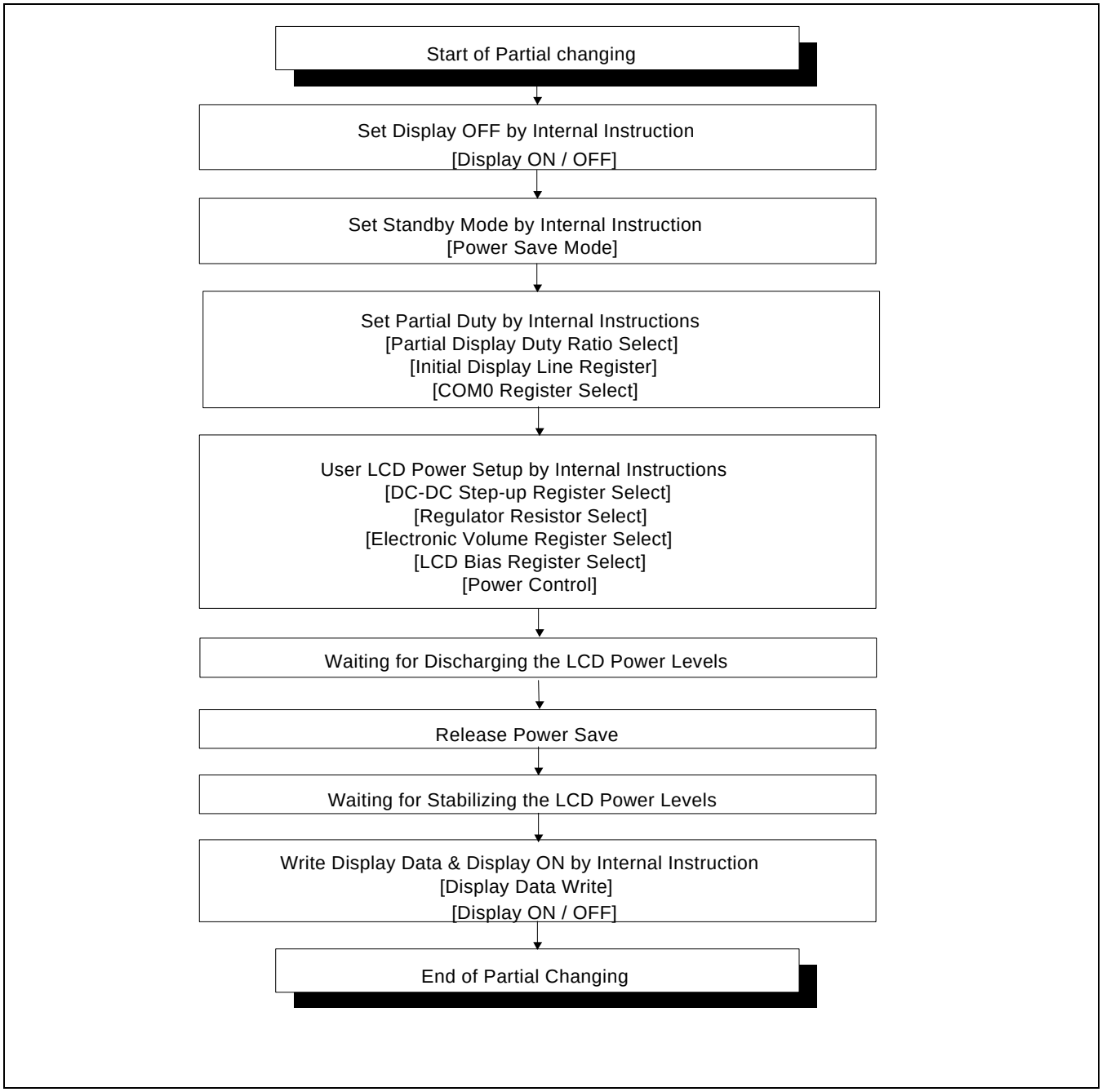

Figure 40. Partial Duty Changing

NOTE:1. Partial COM0 register setting for COM H/W half: [80 – (user duty)] / 2

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Table 16. Absolute Maximum Ratings

(V_{SS} = 0V)

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	- 0.3 ~ + 7.0	V
	V_0, V_{OUT}	+ 0.3 ~ + 17.0	V
	V_1, V_2, V_3, V_4	+ 0.3 ~ V_0	V
External reference voltage	V_{EXT}	+0.3 ~ V_{DD}	
Input voltage range	V_{IN}	- 0.3 ~ V_{DD} + 0.3	V
Operating temperature range	T_{OPR}	- 40 ~ + 85	°C
Storage temperature range	T_{STR}	- 55 ~ + 125	°C

NOTES:

1. VDD, V0, VOUT, V1 to V4, VEXT and VCI are based on VSS = 0V.
2. Voltage VOUT ≥ V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ VSS must always be satisfied.
3. If supply voltage exceeds its absolute maximum range, this LSI may be damaged permanently. It is desirable to use this LSI under electrical characteristic conditions during general operation. Otherwise, this LSI may malfunction or reduced LSI reliability may result.

DC CHARACTERISTICS

Table 17. DC Characteristics

(V_{SS} = 0V, V_{DD} = 1.8~3.3V, Ta=-40~85°C)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Operating voltage (1)		V_{DD}		1.8	-	3.3	V	VDD *1
Operating voltage (2)		V_0		4.0	-	15.0	V	V0, *2
Input voltage	High	V_{IH}		0.7V_{DD}	-	V_{DD}	V	*3
	Low	V_{IL}		V_{SS}	-	0.3V_{DD}		
Output voltage	High	V_{OH}	I_{OH} = -0.5mA	0.8V_{DD}	-	V_{DD}	V	*4
	Low	V_{OL}	I_{OL} = 0.5mA	V_{SS}	-	0.2V_{DD}		
Input leakage current		I_{IL}	V_{IN} = V_{DD} or V_{SS}	- 1.0	-	+ 1.0	µA	*3
Output leakage current		I_{OZ}	V_{IN} = V_{DD} or V_{SS}	- 3.0	-	+ 3.0	µA	*5
LCD driver ON resistance		R_{ON}	Ta = 25°C, V_0 = 8V	-	2.0	3.0	kΩ	SEGn COMn *6
Frame frequency		f_{FR}	Ta = 25°C	70	85	100	Hz	*7

Table 18. DC Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Voltage converter circuit output voltage	V_{OUT}	×3 / ×4 / ×5 / ×6 voltage conversion (no-load)	95	99	-	%	VOUT
Voltage regulator circuit operating voltage	V_{OUT}		5.4	-	15.0	V	VOUT
Voltage follower circuit operating voltage	V_0		4.0	-	15.0	V	V0 *8
Reference voltage	V_{REF}	Ta = 25°C	2.04	2.10	2.16	V	*9

Dynamic Current Consumption (1) when An External Power Supply is used.

Table 19. Dynamic Current 1 (External Power)

(V_{DD} = 3.0V, Ta = 25°C)

Item	Symbol	Condition	Min	Typ	Max	Unit	Pin used
Dynamic current consumption (1)	I_{DD1}	V0-Vss = 12.0V, duty = 1/81 (Display Off)	-	-	TBD	μA	*10
		V0-Vss = 12.0V, duty = 1/81 (Display On , Checker Pattern)	-	-	TBD	μA	*10

Dynamic Current Consumption (2) when The Internal Power Supply is ON

Table 20. . Dynamic Current 2 (Internal Power)

(V_{DD} = 3.0V, Ta = 25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Dynamic current consumption (2)	I_{DD2}	V0 - Vss = 12.0V, x5 boosting, duty = 1/81, normal mode (Display Off)	-	-	TBD	μA	*10
		V0 - Vss = 12.0V, x5 boosting, duty = 1/81, normal mode (Display On , Checker Pattern)	-	-	TBD	μA	*10

Current Consumption during Power Save Mode

Table 21. Power Save Mode Current

(V_{DD} = 3.0V, Ta = 25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Sleep mode current	I_{DDS1}	During sleep	-	-	2	μA	*10

Table 22. The Relationship between Oscillation Frequency and Frame Frequency

Duty ratio	Item	F_{CL}	F_{osc}
1/N	On-chip oscillator circuit is used	$F_{FR} \times N$	$f_{FR} \times 4 \times N$

(f_{OSC}: oscillation frequency, f_{CL}: display clock frequency, f_{FR}: frame frequency, N = 17 to 81)

[* Remark Solves]
*1. Though the wide range of operating voltages is guaranteed, a spike voltage change may affect the voltage assurance during access from the MPU.
*2. In case of external power supply is applied.
*3. CS1B, RS, DB0 to DB7, E_RD, RW_WR, RESETB, PS1, PS0, INTRS, and REF
*4. DB0 to DB7
*5. Applies when the DB0 to DB7 pins are in high impedance.
*6. Resistance value when -0.1[mA] is applied during the ON status of the output pin SEGn or COMn.
RON [kΩ] = ΔV[V] / 0.1[mA] (ΔV : voltage change when -0.1[mA] is applied in the ON status.)
*7. See Table 22 for the relationship between oscillation frequency and frame frequency.
*8. The voltage regulator circuit adjusts V0 within the voltage follower operating voltage range.
*9. On-chip reference voltage source of the voltage regulator circuit to adjust V0.
*10. Applies to the case where the on-chip oscillation circuit is used and no access is made from the MPU.
The current consumption, when the built-in power supply circuit is ON or OFF.
The current flowing through voltage regulation resistors(Rb and Ra) is not included.
It does not include the current of the LCD panel capacity, wiring capacity, etc.

AC CHARACTERISTICS

Read / Write Characteristics (8080-series MP)

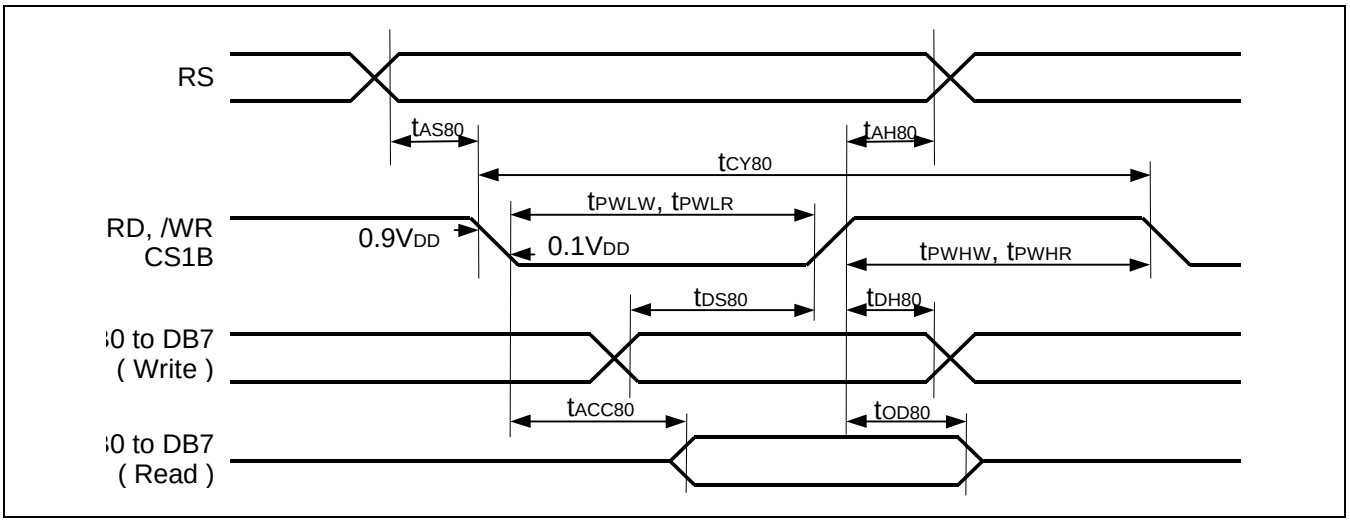

Figure 41. Read / Write Characteristics (8080-series MPU)

Table 23

(V_{DD} = 1.8 ~ 3.3V, Ta = -40 ~ +85°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time Address hold time	RS	t_{AS80} t_{AH80}		0 0	- -	ns
System cycle time		t_{CY80}		1000	-	ns
Pulse width low for write Pulse width high for write	RW_WR (/WR)	t_{PWLW} t_{PWHW}		120 120	- -	ns
Pulse width low for read Pulse width high for read	E_RD (/RD)	t_{PWLR} t_{PWHR}		240 120	- -	ns
Data setup time Data hold time	DB0 to DB7	t_{DS80} t_{DH80}		80 30	- -	ns
Read access time Output disable time		t_{ACC80} t_{OD80}	CL = 100 pF	- 10	280 200	ns

NOTE: *1. The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
(tr + tf) < (t_{CY80} - t_{PWLW} - t_{PWHW}) for write, (tr + tf) < (t_{CY80} - t_{PWLR} - t_{PWHR}) for read

Read / Write Characteristics (6800-series Microprocessor)

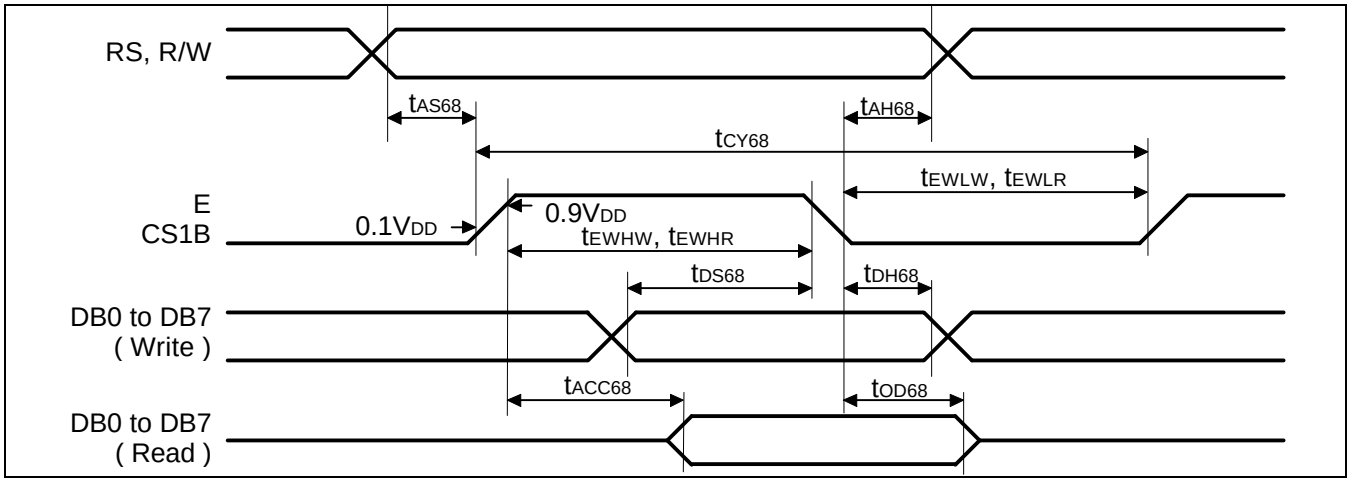

Figure 42. Read / Write Characteristics (6800-series Microprocessor)

Table 24

(V_{DD} = 1.8 ~ 3.3V, Ta = -40 ~ +85°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time Address hold time	RS RW	t_{AS68} t_{AH68}		0 0	- -	ns
System cycle time		t_{CY68}		1000	-	ns
Enable width high for write Enable width low for write	E_RD (E)	t_{EWHW} t_{EWLW}		120 120	- -	ns
Enable width high for read Enable width low for read	E_RD (E)	t_{EWHR} t_{EWLR}		240 120	- -	ns
Data setup time Data hold time	DB0 to DB7	t_{DS68} t_{DH68}		80 30	- -	ns
Read access time Output disable time		t_{ACC68} t_{OD68}	C_L = 100 pF	- 10	280 200	ns

NOTE: *1. The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
(tr + tf) < (tCY68 - tEWHW - tEWLW) for write, (tr + tf) < (tCY68 - tEWHR - tEWLR) for read

Serial Interface Characteristics

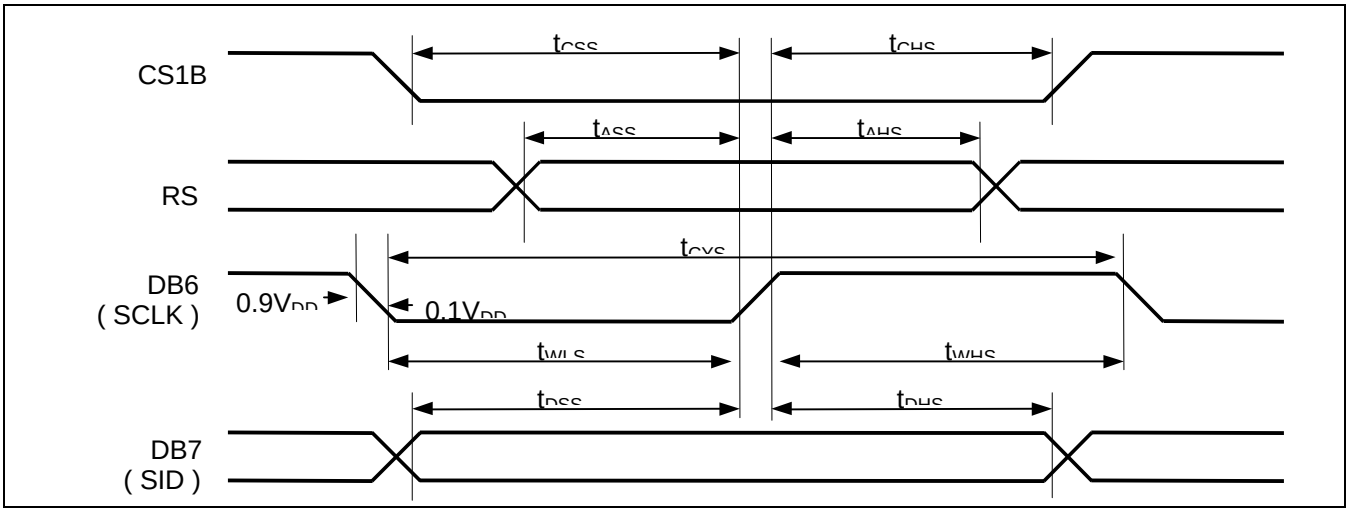

Figure 43

Table 25

(V_{DD} = 1.8 ~ 3.3V, Ta = -40 ~ +85°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock cycle SCLK high pulse width SCLK low pulse width	DB6 (SCLK)	t_{SCY} t_{SHW} t_{SLW}		150 60 60	- - -	ns
Address setup time Address hold time	RS	t_{ASS} t_{AHS}		60 60	- -	ns
Data setup time Data hold time	DB7 (SID)	T_{DSS} t_{DHS}		60 60	- -	ns
CS1B setup time CS1B hold time	CS1B	T_{CSS} t_{CHS}		60 60	- -	ns

NOTE: *1. The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.

Reset Input Timing

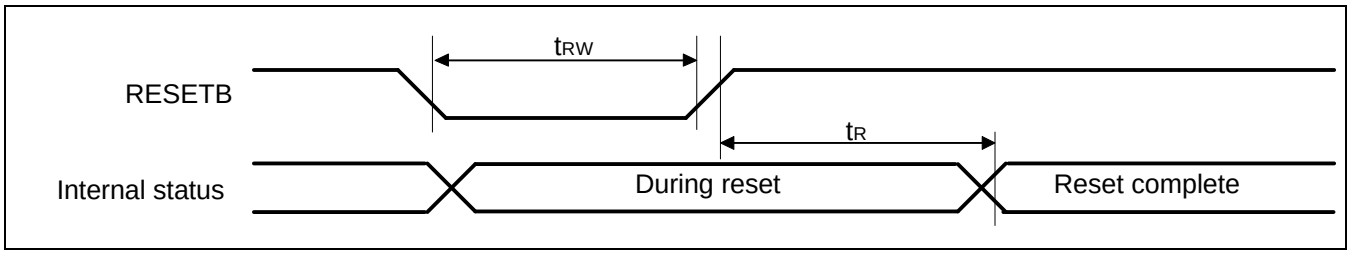

Figure 44

Table 26

(V_{DD} = 1.8 ~ 3.3V, Ta = -40 ~ +85°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Reset low pulse width	RESETB	t_{RW}		2000	-	ns
Reset time	-	t_R		-	2000	ns

REFERENCE APPLICATIONS

MICROPROCESSOR INTERFACE

In Case of Interfacing with 6800-series (PS0 = "H", PS1 = "H")

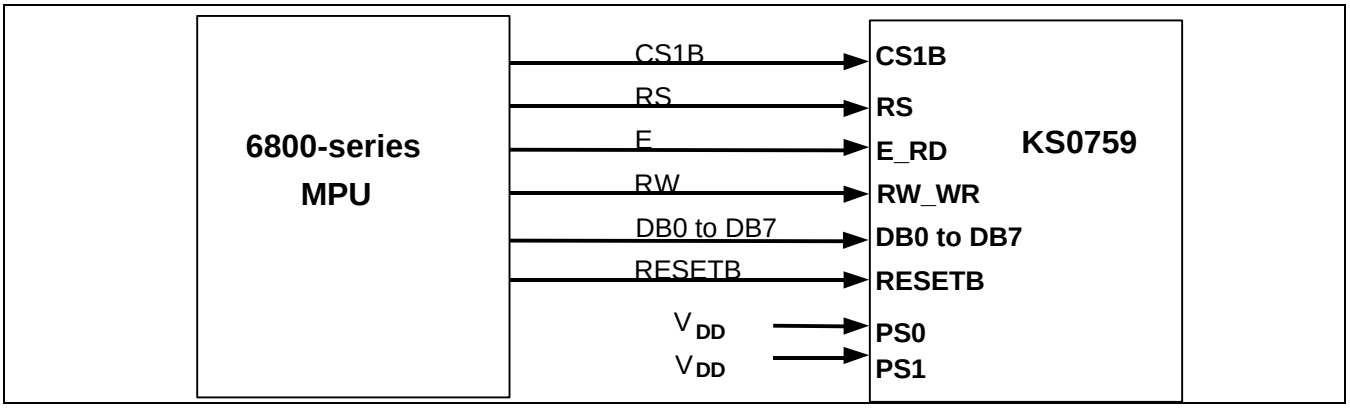

Figure 45. Interfacing with 6800-series

In Case of Interfacing with 8080-series (PS0 = "H" , PS1 = "L")

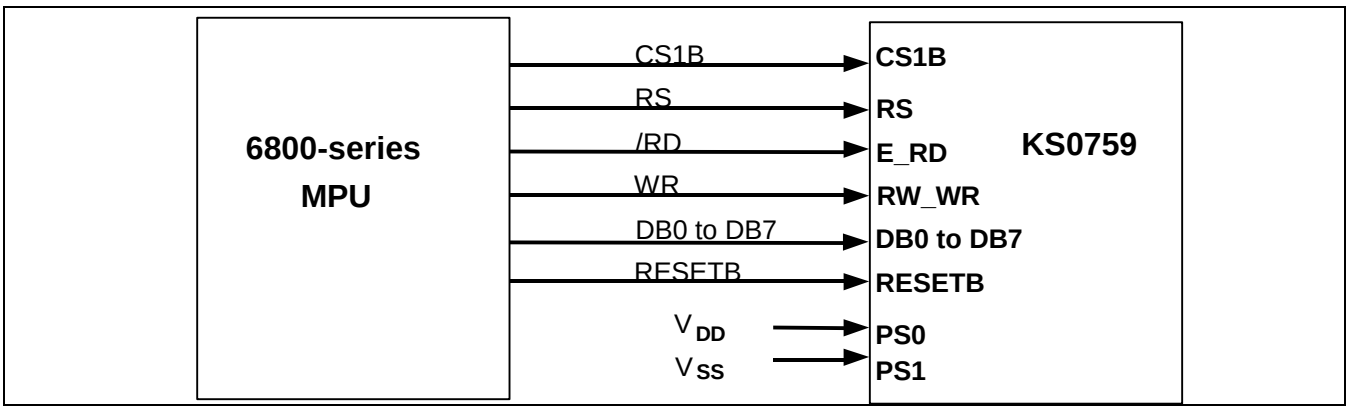

Figure 46. Interfacing with 8080-series

In Case of Serial Peripheral Interface with RS Pin (PS0 = "L" , PS1 = "H")

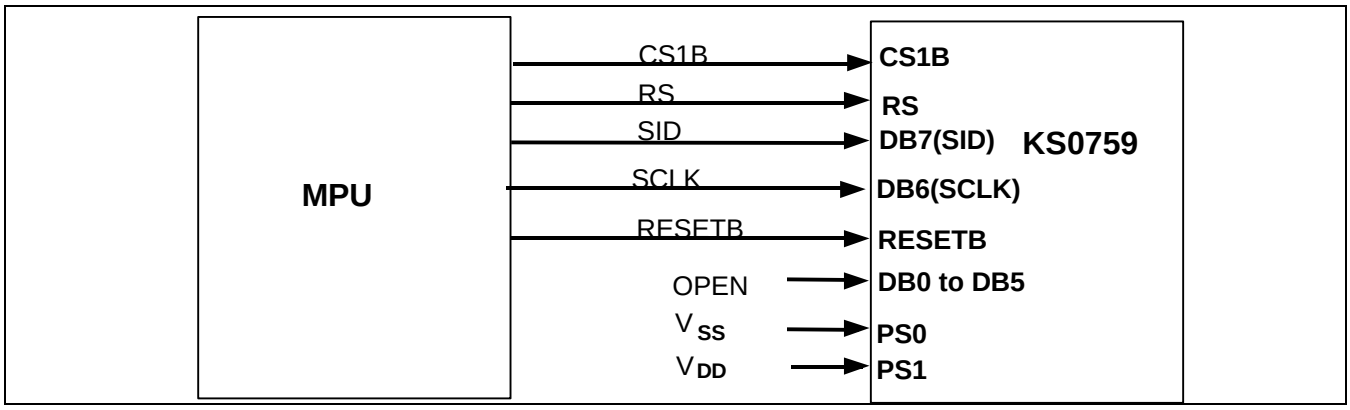

Figure 47. Serial Interface

In Case of Serial Peripheral Interface with software command (PS0 = "L" , PS1 = "L")

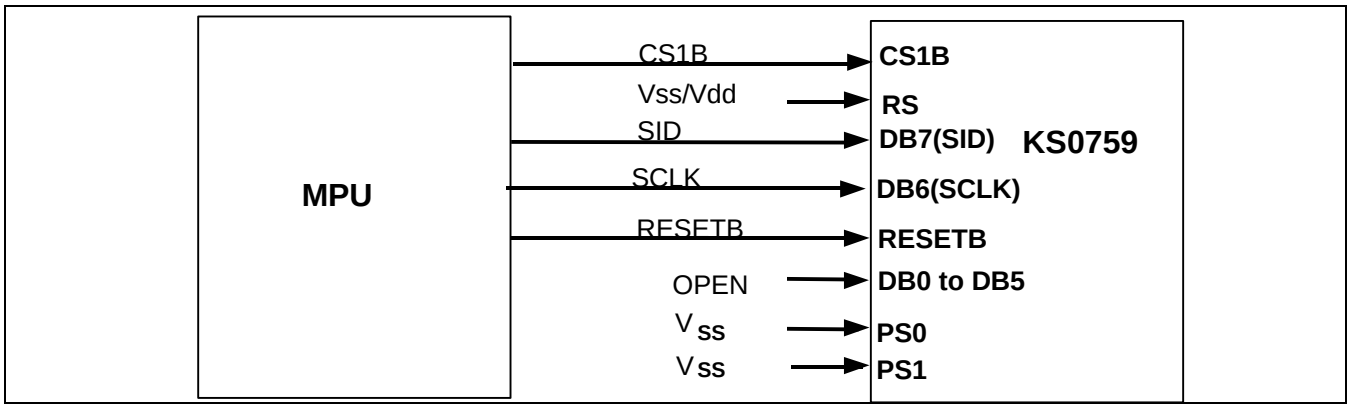

Figure 48. Serial Interface

CONNECTIONS BETWEEN KS0759 AND LCD PANEL

Single Chip Configurations (1/81 Duty)

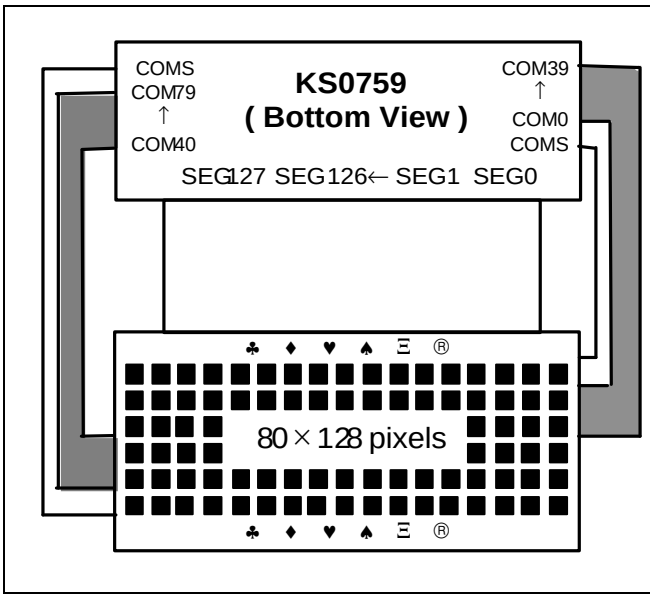

Figure 49. SHL = 0, ADC = 1

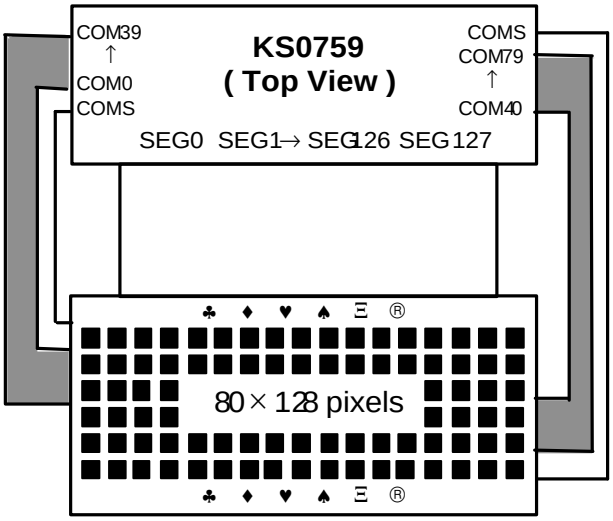

Figure 50. SHL = 0, ADC = 0

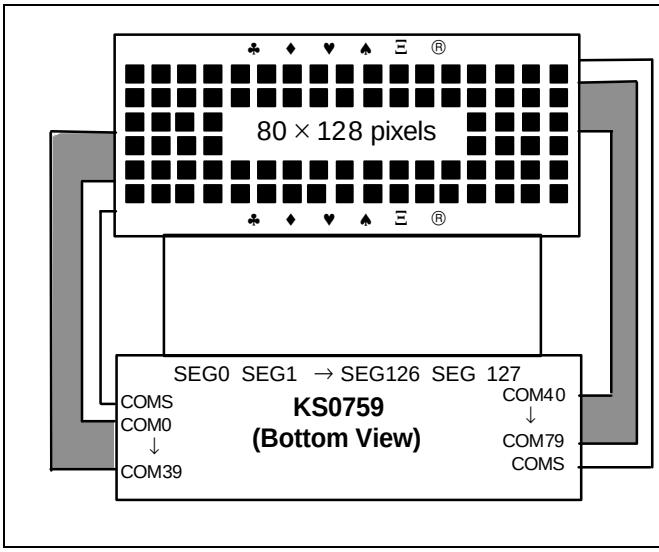

Figure 51. SHL = 1, ADC = 0

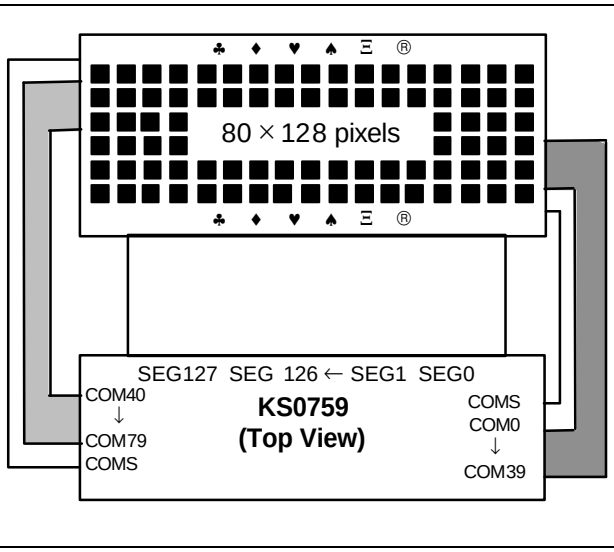

Figure 52. SHL = 1, ADC = 1