HYM5V64214A Z-Series

SO DIMM 2M x 64-bit CMOS DRAM MODULE with EXTENDED DATA OUT

DESCRIPTION

The HYM5V64214A is a 2M x 64-bit EDO mode CMOS DRAM module consisting of eight HY51V17804B in 28/28 pin SOJ or TSOP-II and one 2048 bit EEPROM on a 144 Zig Zag Dual pin glass-epoxy printed circuit board. 0.22μF decoupling capacitor is mounted for each DRAM. The HYM5V64214AZG/ATZG/ASLZG/ASLTZG is Gold plated socket type Dual In-line Memory Modules suitable for easy interchange and addition of 16M byte memory.

FEATURES

- **Low power dissipation**
  Max. self-refresh 8.6mW (SL-part)
  Max. battery back-up 11.5mW (SL-part)
  Max. CMOS standby 5.8mW (SL-part)
  28.8mW
  Max. TTL standby 57.6mW
  Max. operating

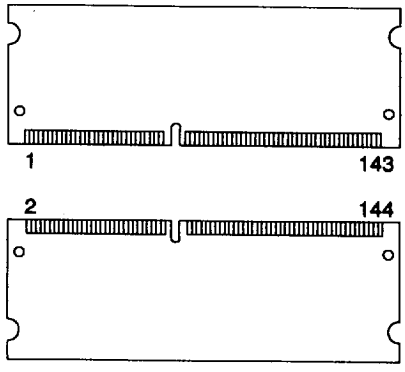
Speed	Power
60	3.46W
70	2.88W
80	2.59W

- **Single power supply of 3.3V± 10%**
- **TTL compatible inputs and outputs**
- **Fast access time**

Speed	tRAC	tCAC	tHPC
60	60ns	15ns	25ns
70	70ns	18ns	30ns
80	80ns	20ns	35ns

- **EDO mode operation**
- **CAS-before-RAS, RAS-only, Hidden refresh and Self-refresh**
- **2048 refresh cycles / 256ms (SL-part)**
  2048 refresh cycles / 32ms
- **Serial Presence Detect**

PIN CONNECTION



PIN DESCRIPTION

$\overline{RAS0}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS7}$	Column Address Strobe
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
A0-A10	Address Input
DQ0-DQ63	Data Input/Output
SLC	Serial PD Clock Input
SDA	Serial PD Data Input/Output
Vcc	Power (+ 3.3V)
Vss	Ground

PIN NAME

#	NAME	#	NAME	#	NAME	#	NAME
1	Vss	2	Vss	73	$\overline{OE}$	74	NC
3	DQ0	4	DQ32	75	Vss	76	Vss
5	DQ1	6	DQ33	77	NC	78	NC
7	DQ2	8	DQ34	79	NC	80	NC
9	DQ3	10	DQ35	81	Vcc	82	Vcc
11	Vcc	12	Vcc	83	DQ16	84	DQ48
13	DQ4	14	DQ36	85	DQ17	86	DQ49
15	DQ5	16	DQ37	87	DQ18	88	DQ50
17	DQ6	18	DQ38	89	DQ19	90	DQ51
19	DQ7	20	DQ39	91	Vss	92	Vss
21	Vss	22	Vss	93	DQ20	94	DQ52
23	$\overline{CAS0}$	24	$\overline{CAS4}$	95	DQ21	96	DQ53
25	$\overline{CAS1}$	26	$\overline{CAS5}$	97	DQ22	98	DQ54
27	Vcc	28	Vcc	99	DQ23	100	DQ55
29	A0	30	A3	101	Vcc	102	Vcc
31	A1	32	A4	103	A6	104	A7
33	A2	34	A5	105	A8	106	NC
35	Vss	36	Vss	107	Vss	108	Vss
37	DQ8	38	DQ40	109	A9	110	NC
39	DQ9	40	DQ41	111	A10	112	NC
41	DQ10	42	DQ42	113	Vcc	114	Vcc
43	DQ11	44	DQ43	115	$\overline{CAS2}$	116	$\overline{CAS6}$
45	Vcc	46	vcc	117	$\overline{CAS3}$	118	$\overline{CAS7}$
47	DQ12	48	DQ44	119	Vss	120	Vss
49	DQ13	50	DQ45	121	DQ24	122	DQ56
51	DQ14	52	DQ46	123	DQ25	124	DQ57
53	DQ15	54	DQ47	125	DQ26	126	DQ58
55	Vss	56	Vss	127	DQ27	128	DQ59
57	NC	58	NC	129	Vcc	130	Vcc
59	NC	60	NC	131	DQ28	132	DQ60
61	NC	62	NC	133	DQ29	134	DQ61
63	Vcc	64	Vcc	135	DQ30	136	DQ62
65	NC	66	NC	137	DQ31	138	DQ63
67	$\overline{WE}$	68	NC	139	Vss	140	Vss
69	$\overline{RAS0}$	70	NC	141	SDA	142	SCL
71	NC	72	NC	143	Vcc	144	Vcc

SERIAL PD BYTE DEFINITION

BYTE NUMBER	FUNCTION DESCRIBED	FUNCTION	VALUE
Byte 0	Number of Byte written during module production	15 Bytes	0Fh
Byte 1	Total Byte of Serial Presence Detect Device	256 Bytes	08h
Byte 2	Memory Type	EDO	02h
Byte 3	Number of ROW Addresses	11	0Bh
Byte 4	Number of COLUMN Addresses	10	0Ah
Byte 5	Number of Banks	1 Bank	01h
Byte 6	Module Data Width	64bit	60h
Byte 7	Module Data Width(Continued)	Not Used	00h
Byte 8	Module Interface Levels	LVTTL	01h
Byte 9	tRAC	60ns 70ns 80ns	3Ch 46h 50h
Byte 10	tCAC	17ns 20ns 20ns	11h 14h 14h
Byte 11	Module Configuration Type	None	00h
Byte 12	Refresh Rate/Type	Normal(15.6μs) SL-Part(125μs)	00h 85h
Byte 13	Primary DRAM Width	x8	08h
Byte 14	Error Checking DRAM Width	None	00h
Byte 15 - 255	Undefined	Undefined	Undefined

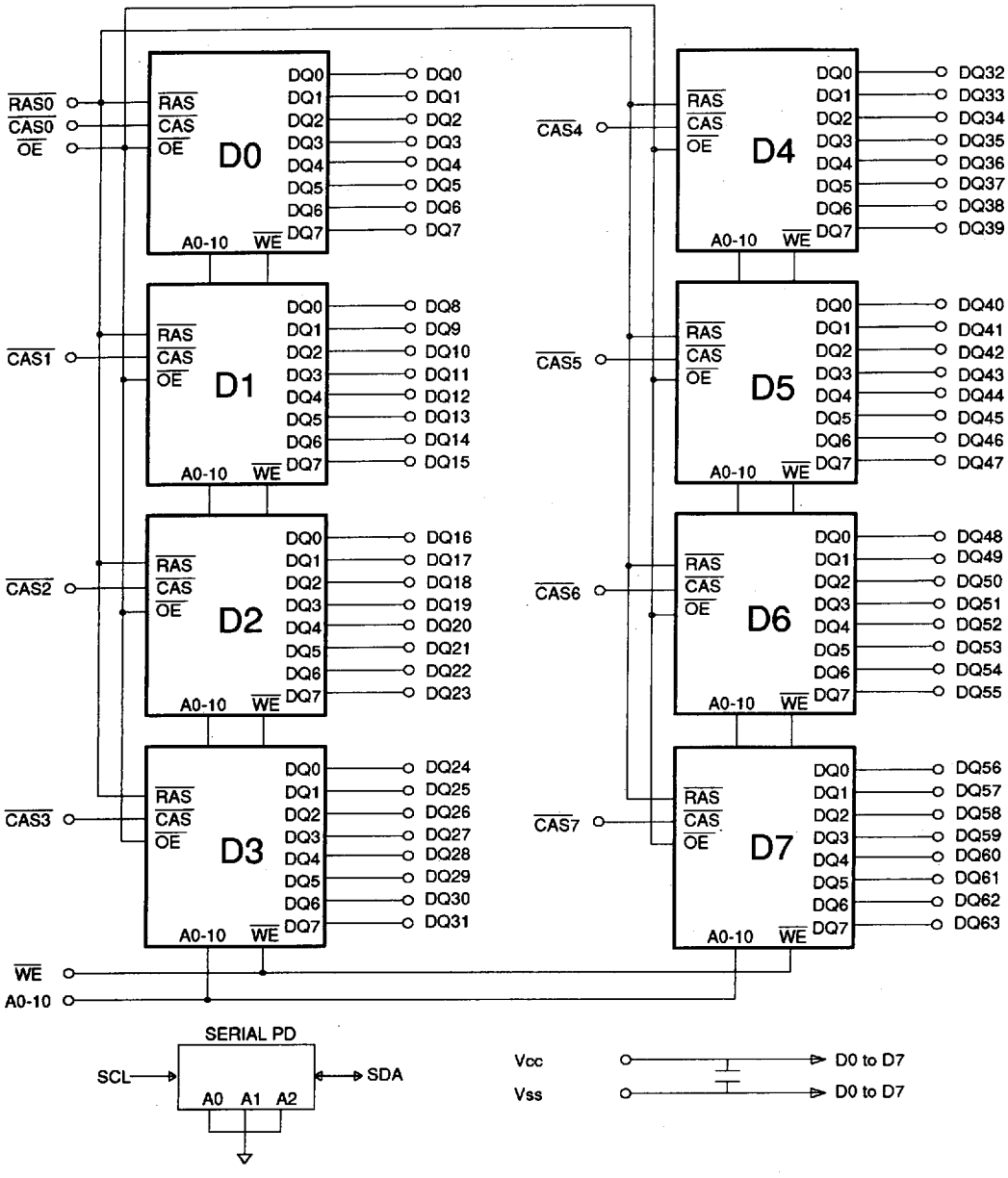
NOTE:
1. Serial PD interface is standard IIC architecture.
2. Pull-up resistors(4.7K typical value) are required on all open collector bus devices (SCL and SDA).
3. Current sink capability on SCL and SDA (I_{OL} max) must be at least 3ma to maintain a valid low level.

IIC BUS INTERFACE

SYMBOL	RATING	NOTE
C_{MAX}	400pF	1
f_{MAX}	80 KHz(3.3V) 100 KHz(5.0V)	2
$I_{OL\,MAX}$	3mA	

NOTE:
1. The maximum number of devices connected on the IIC bus is controlled by the maximum allowable capacitance which is 400pF per line.
2. The maximum IIC system clock frequency depends on Vcc.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Ambient Temperature	0 to 70	°C
T_{STG}	Storage Temperature	–55 to 125	°C
V_{IN}, V_{OUT}	Voltage on Any Pin Relative to V_{SS}	–0.5 to 4.6	V
V_{CC}	Voltage on V_{CC} Relative to V_{SS}	–0.5 to 4.6	V
I_{OS}	Short Circuit Output Current	20	mA
P_D	Power Dissipation	5.6	W

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A= 0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	3.0	3.3	3.6	V
V_{IH}	Input High Voltage	2.0	-	V_{CC}+ 0.3	V
V_{IL}	Input Low Voltage	–0.3	-	0.8	V

NOTE : All voltages are referenced to V_{SS}.

DC CHARACTERISTICS

(TA= 0°C to 70°C, VCC= 3.3V± 10%, VSS= 0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED/ POWER	MIN.	MAX.	UNIT	NOTE
ILI	Input Leakage Current (Any Input Pin)	VSS≤ VIN≤ VCC+ 1.0, other pins not under test= Vss		-80	80	µA	
ILO	Output Leakage Current (High Impedance State)	VSS≤ VOUT≤ VCC, $\overline{RAS}$ & $\overline{CAS}$ at VIH		-10	10	µA	
ICC1	VCC Supply Current, Operating	tRC= tRC (min.)	60 70 80	- - -	960 800 720	mA	1,2,3
ICC2	VCC Supply Current, TTL Standby	$\overline{RAS}$ & $\overline{CAS}$ at VIH, other inputs≥ VSS		-	16	mA	
ICC3	VCC Supply Current, $\overline{RAS}$-only refresh	tRC= tRC (min.)	60 70 80	- - -	960 800 720	mA	1,3
ICC4	VCC Supply Current, EDO mode	tHPC= tHPC (min.)	60 70 80	- - -	960 800 720	mA	1,2,3
ICC5	VCC Supply Current, CMOS Standby	$\overline{RAS}$ & $\overline{CAS}$ ≥ VCC-0.2V	 SL-part	- -	8 1.6	mA	
ICC6	VCC Supply Current, $\overline{CAS}$-before-$\overline{RAS}$ refresh	tRC= tRC (min.)	60 70 80	- - -	960 800 720	mA	1,3
ICC7	VCC Supply Current, Battery Back Up (SL-part only)	tRC= 125µs $\overline{CAS}$= CBR cycling or 0.2V $\overline{WE}$= VCC-0.2V, A0-A10= VCC - 0.2V or 0.2V DQ0-DQ63= VCC - 0.2V, 0.2V or open	tRAS≤ 300ns tRAS≤ 1µs	-	2.4 3.2	mA	1,4,5
ICC8	VCC Supply Current, Self Refresh (SL-part)	$\overline{RAS}$ & $\overline{CAS}$= VIL OE & WE & A0-A10= VCC - 0.2V or 0.2V DQ0-DQ63= VCC - 0.2V, 0.2 or open		-	2.4	mA	5
VOL	Output Low Voltage	IOL= 2.0mA		-	0.4	V	
VOH	Output High Voltage	IOH= -2.0mA		2.4	-	V	

NOTE :

1. ICC1, ICC3, ICC4, ICC6 and ICC7 depend on cycle rate.
2. ICC1, ICC3, ICC4, and ICC6 depend on output loading. Specified values are obtained with the output open.
3. ICC is specified as average current. For ICC1, ICC3 and ICC6, address can be changed maximum two times while $\overline{RAS}$= VIL. For ICC4, address can be changed maximum once while $\overline{CAS}$= VIH.
4. tRAS(max.)= 1µs is only applied to refresh of battery backup but tRAS(max.)= 10µs is applied to normal functonal operatin.
5. ICC5(max.)= 1.6mA, ICC7 and ICC8 are applied to SL-part only (HYM5V64214ASLZG/ASLTZG).

AC CHARACTERISTICS

(TA= 0°C to 70°C, VCC= 3.3V± 10%, VSS = 0V, unless otherwise noted.) NOTE : 1, 2, 3

#	SYMBOL	PARAMETER	HYM5V64214A Z-Series						UNIT	NOTE
			-60		-70		-80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	tRC	Random Read or Write Cycle Time	105	-	125	-	145	-	ns	
2	tRWC	Read-Modify-Write Cycle Time	142	-	167	-	187	-	ns	
3	tHPC	EDO Mode Cycle Time	25	-	30	-	35	-	ns	
4	tHPRWC	EDO Mode Read-Modify-Write Cycle Time	73	-	85	-	100	-	ns	
5	tRAC	Access Time from $\overline{RAS}$	-	60	-	70	-	80	ns	4,9,10
6	tCAC	Access Time from $\overline{CAS}$	-	15	-	20	-	20	ns	4,9
7	tAA	Access Time from Column Address	-	30	-	35	-	40	ns	4,10
8	tCPA	Access Time from $\overline{CAS}$ Precharge	-	35	-	35	-	40	ns	4
9	tCLZ	$\overline{CAS}$ to Output Low Impedance	0	-	0	-	0	-	ns	4
10	tCEZ	Output Buffer Turn-off Delay	0	15	0	15	0	15	ns	5
11	tT	Transition Time (Rise and Fall)	2.5	50	2.5	50	2.5	50	ns	3
12	tRP	$\overline{RAS}$ Precharge Time	40	-	50	-	60	-	ns	
13	tRAS	$\overline{RAS}$ Pulse Width	60	10K	70	10K	80	10K	ns	
14	tRASP	$\overline{RAS}$ Pulse Width (EDO Mode)	60	100K	70	100K	80	100K	ns	
15	tRSH	$\overline{RAS}$ Hold Time	13	-	15	-	20	-	ns	
16	tCSH	$\overline{CAS}$ Hold Time	40	-	50	-	60	-	ns	
17	tCAS	$\overline{CAS}$ Pulse Width	13	10K	15	10K	20	10K	ns	
18	tRCD	$\overline{RAS}$ to $\overline{CAS}$ Delay	20	45	20	50	20	60	ns	9
19	tRAD	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	15	40	ns	10
20	tCRP	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	5	-	5	-	ns	
21	tCP	$\overline{CAS}$ Precharge Time	7	-	10	-	10	-	ns	
22	tASR	Row Address Set-up Time	0	-	0	-	0	-	ns	
23	tRAH	Row Address Hold Time	10	-	10	-	10	-	ns	
24	tASC	Column Address Set-up Time	0	-	0	-	0	-	ns	
25	tCAH	Column Address Hold Time	15	-	15	-	15	-	ns	
26	tAR	Column Address Hold Time from $\overline{RAS}$	30	-	35	-	35	-	ns	
27	tRAL	Column Address to $\overline{RAS}$ Lead Time	30	-	35	-	40	-	ns	
28	tRCS	Read Command Set-up Time	0	-	0	-	0	-	ns	
29	tRCH	Read Command Hold Time Referenced to $\overline{CAS}$	0	-	0	-	0	-	ns	6
30	tRRH	Read Command Hold Time Referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	6
31	tWCH	Write Command Hold Time	10	-	15	-	15	-	ns	
32	tWCR	Write Command Hold Time from $\overline{RAS}$	30	-	35	-	35	-	ns	
33	tWP	Write Command Pulse Width	10	-	10	-	10	-	ns	
34	tRWL	Write Command to $\overline{RAS}$ Lead Time	15	-	15	-	15	-	ns	
35	tCWL	Write Command to $\overline{CAS}$ Lead Time	13	-	15	-	20	-	ns	
36	tDS	Data-In Set-up Time	0	-	0	-	0	-	ns	7
37	tDH	Data-In Hold Time	10	-	15	-	15	-	ns	7
38	tDHR	Data-In Hold Time Referenced to $\overline{RAS}$	30	-	35	-	35	-	ns	
39	tREF	Refresh Period (2048 cycles)	-	32	-	32	-	32	ms	
		SL-part	-	256	-	256	-	256	ms	12
40	tWCS	Write Command Set-up Time	0	-	0	-	0	-	ns	8

AC CHARACTERISTICS

(continued)

#	SYMBOL	PARAMETER	HYM5V64214A Z-Series						UNIT	NOTE
			-60		-70		-80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
41	tCWD	$\overline{CAS}$ to $\overline{WE}$ Delay Time	37	-	45	-	45	-	ns	8
42	tRWD	$\overline{RAS}$ to $\overline{WE}$ Delay Time	80	-	95	-	105	-	ns	8
43	tAWD	Column Address to $\overline{WE}$ Delay Time	50	-	60	-	65	-	ns	8
44	tCSR	$\overline{CAS}$ Set-up Time (CBR Cycle)	5	-	5	-	5	-	ns	
45	tCHR	$\overline{CAS}$ Hold Time (CBR Cycle)	10	-	10	-	10	-	ns	
46	tRPC	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	5	-	5	-	5	-	ns	
47	tCPT	$\overline{CAS}$ Precharge Time (CBR Counter Test)	30	-	35	-	40	-	ns	
48	tROH	$\overline{RAS}$ Hold Time Reference to $\overline{OE}$	10	-	10	-	10	-	ns	
49	tOEA	$\overline{OE}$ Access Time	-	17	-	20	-	20	ns	
50	tOED	$\overline{OE}$ to Data Delay	15	-	20	-	20	-	ns	
51	tOEZ	Output Buffer Turn Off Delay Time from $\overline{OE}$	0	15	0	15	0	15	ns	5
52	tOEH	$\overline{OE}$ Command Hold Time	15	-	20	-	20	-	ns	
53	tCPWD	$\overline{WE}$ Delay Time from $\overline{CAS}$ Precharge	55	-	65	-	75	-	ns	8
54	tRHCP	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	40	-	40	-	50	-	ns	
55	tWRP	$\overline{WE}$ to $\overline{RAS}$ Precharge Time (CBR Cycle)	10	-	10	-	10	-	ns	
56	tWRH	$\overline{WE}$ to $\overline{RAS}$ Hold time (CBR Cycle)	10	-	10	-	10	-	ns	
57	tRASS	$\overline{RAS}$ Pulse Width (Self Refresh Cycle)	100	-	100	-	100	-	µs	
58	tRPS	$\overline{RAS}$ Precharge Time (Self Refresh Cycle)	110	-	130	-	150		ns	
59	tCHS	$\overline{CAS}$ Hold Time (Self Refresh Cycle)	-50	-	-50	-	-50	-	ns	
60	tDOH	Output Data Hold Time	3	-	3	-	3	-	ns	
61	tREZ	Output Buffer Turn-off Delay ($\overline{RAS}$)	0	15	0	15	0	15	ns	5,15
62	tWEZ	Output Buffer Turn-off Delay ($\overline{WE}$)	0	15	0	15	0	15	ns	5
63	tWPE	$\overline{WE}$ Pulse Width for Output Disable	10	-	10	-	10	-	ns	
64	tOEP	$\overline{OE}$ Pulse Width for Output Disable	10	-	10	-	10	-	ns	
65	tOCH	$\overline{OE}$ Low to $\overline{CAS}$ High Delay Time	0	-	0	-	0	-	ns	
66	tCHO	$\overline{CAS}$ High to $\overline{OE}$ High Hold Time	5	-	5	-	5	-	ns	
67	tWED	$\overline{WE}$ to Data Delay Time	15	-	15	-	15	-	ns	

NOTE :

1. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initilization cycles instead of 8 $\overline{RAS}$-only refresh cycles are required. The device should be carefully initialized to be prevented from being entered into multi bit test mode.
2. If $\overline{RAS}$= Vss during power-up, the HYM5V64214A could begin an active cycle. This condition results in higher power-up current than necessary demands from the power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held at a valid V_{IH} in order to minimize the power-up current.
3. Refer to the HY51V17804B data sheet for detailed information.
4. Measured with a load equivalent to 2 TTL loads and 100pF. (V_{OH}= 2.0V,V_{OL}= 0.8V)
5. t_{CEZ}(max.) $t_{OEZ(MAX)}$, $t_{REZ(MAX)}$ and $t_{WEZ(MAX)}$ define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
7. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in late write or read-modify-write cycles.
8. t_{WCS} is not a restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min.)}$, the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle.
9. Operation within the $t_{RCD(max.)}$ limit insures that $t_{RAC(max.)}$ can be met. $t_{RCD(max.)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max.)}$ limit, then access time is controlled by t_{CAC}.
10. Operation within the $t_{RAD(max.)}$ limit insures that $t_{RAC(max.)}$ can be met. $t_{RAD(max.)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max.)}$ limit, then access time is controlled by t_{AA}.
11. Measured with the specified current load and 100pF.
12. A burst of 2048 $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles must be executed within 32ms after exiting self refresh (for SL-part).
13. If $t_{CWD} \geq t_{WCS(MIN.)}$, $t_{RWD} \geq t_{RWD(MIN.)}$, $t_{AWD} \geq t_{AWD(MIN.)}$ and $t_{CPWD} \geq t_{CPWD(MIN.)}$, the cycle is a read modify write cycle and the data output will contain data read from the selected cell. If neither of the above conditions are met, the condition of the data out (at access time and until $\overline{CAS}$ goes bach to V_{IH}) is indeterminated.
14. In $\overline{CAS}$ before $\overline{RAS}$ self refresh mode.
    In case of using distributed $\overline{CAS}$ before $\overline{RAS}$ refresh, refresh 2048 times during a 256ms after reset
    In case of using burst $\overline{CAS}$ before $\overline{RAS}$ refresh, refresh 2048 times during a 32ms after reset
    In case of using $\overline{RAS}$ only refresh, refresh against all refresh address during a 32ms after reset
15. If $\overline{RAS}$ goes to high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes to high before $\overline{RAS}$ high going, the open circuit condition of the output is achieved by $\overline{RAS}$ high going.

CAPACITANCE

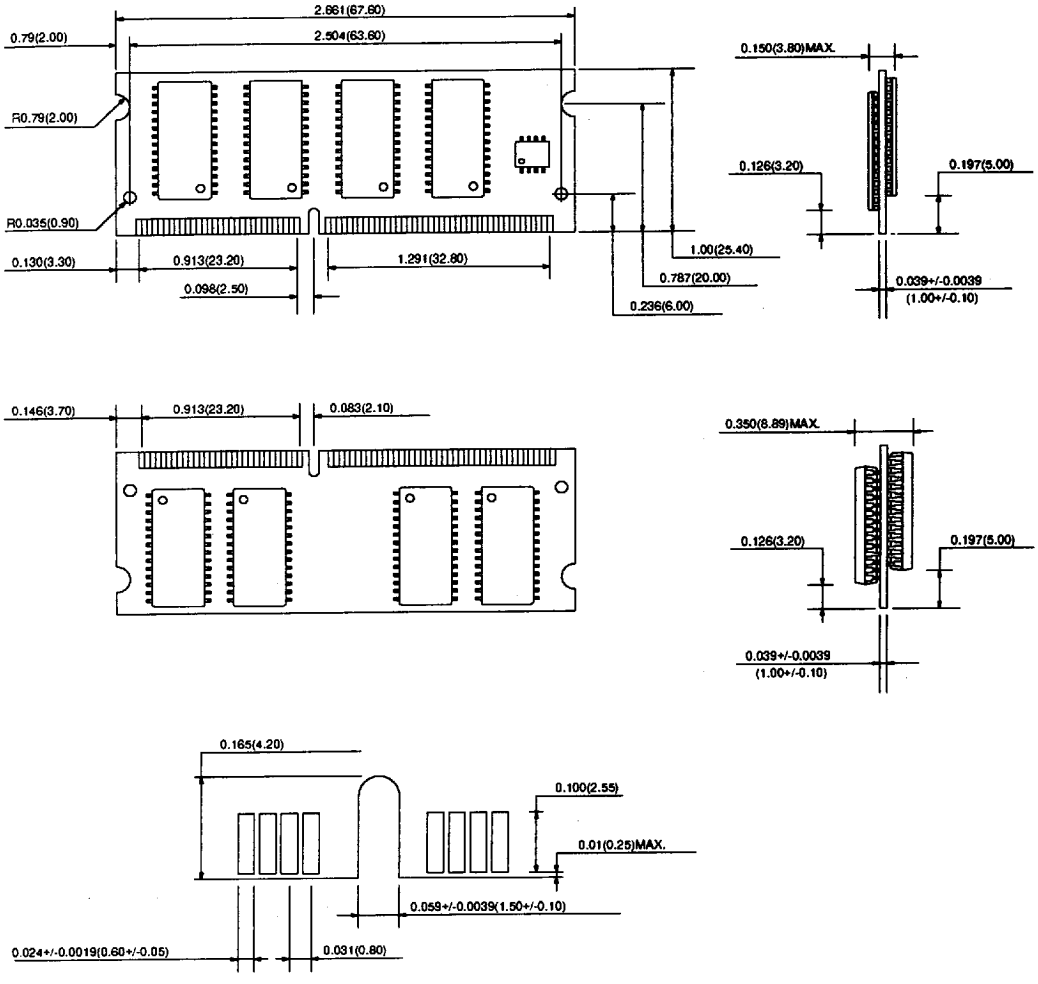
(T_A= 25°C, V_{CC}= 3.3V± 10%, V_{SS}= 0V, f= 1MHz, unless otherwise noted.)

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C_{IN1}	Input Capacitance (A0-A10)	-	54	pF
C_{IN2}	Input Capacitance ($\overline{WE}$,$\overline{OE}$)	-	70	pF
C_{IN3}	Input Capacitance ($\overline{RAS0}$)	-	70	pF
C_{IN4}	Input Capacitance ($\overline{CAS0}$-$\overline{CAS7}$)	-	13	pF
C_{DQ}	Data Input/output Capacitance (DQ0-DQ63)	-	15	pF

PACKAGE INFORMATION

144 pin Small Out-line Dual In-line Memory Module(ZG ; Gold plated)

UNIT : INCH(mm)
TOLERANCE : +/-0.0059(0.15)



ORDERING INFORMATION

PART NUMBER	SPEED	POWER	PACKAGE	PLATING
HYM5V64214AZG	60/70/80		DIMM	Gold
HYM5V64214ASLZG	60/70/80	SL-part	DIMM	Gold
HYM5V64214ATZG	60/70/80		DIMM	Gold
HYM5V64214ASLTZG	60/70/80	SL-part	DIMM	Gold