

Features

- Programmable blocks
 - Highly integrated mouse-on-a-chip with programmable PSoC® microcontroller unit (MCU)
 - 32 KB flash memory
 - 2 KB static RAM (SRAM)
 - Internal 24, 12, or 6 MHz main oscillator (IMO)
 - Internal 32 kHz low-speed oscillator (ILO)
 - 16-bit data report enables simultaneous high-speed and high-resolution tracking
 - CapSense® sensing of up to 26 capacitive elements
- Tracking performance
 - Continuously variable resolution 400 to 3200 counts per inch (CPI), independent of speed
 - High speed with high accuracy tracking
 - Speed up to 75 inches per second (in/s)
 - Acceleration up to 30 g
- Peripheral interface
 - Integrated full-speed USB for wired applications
 - SPI interface to radio for wireless applications
 - Fast or standard mode I²C
- 28 general purpose input/output (GPIO) pins
 - Port 0 – 8 bits
 - Port 1 – 8 bits with high current capability, regulated output voltage, and 5 V input tolerance
 - Port 2 – 8 bits
 - Port 3 – 4 bits
- Power
 - Internal power system enables operation from 5 V USB, battery, or external 2.7 V to 3.6 V supply
 - Battery input voltage of 0.8 V to 3.6 V allows operation from single or dual series cells
 - Automatic switch to USB power when plugged into USB port
 - Automatic switch battery power when removed from USB
 - Self adjusting power saving modes
- On-chip laser
 - Vertical cavity surface emitting laser (VCSEL) integrated within the sensor package
 - No calibration or alignment needed
 - Electrostatic discharge (ESD) immunity: 2000 V human body mode (HBM)
 - Wavelength: 840 - 870 nm
 - IEC 60825-1 Class 1 safety: built-in eye-safe fault tolerant laser drive circuitry
- Snap-on lens
 - Molded optic: Self-aligning snap on molded lens
 - 6 mm distance between the PCB and tracking surface

Description

The CYONS2110 is a member of Cypress Semiconductor's second generation laser navigation System-on-Chip (SoC) family of products. Powered by the high-speed and high-precision OptiCheck™ technology, along with the world-leading PSoC technology, this family integrates the sensor, USB, boost regulator, CapSense, and MCU functions into one chip. Bundled with the VCSEL into one package, the combination forms the market's first true mouse-on-a-chip solution.

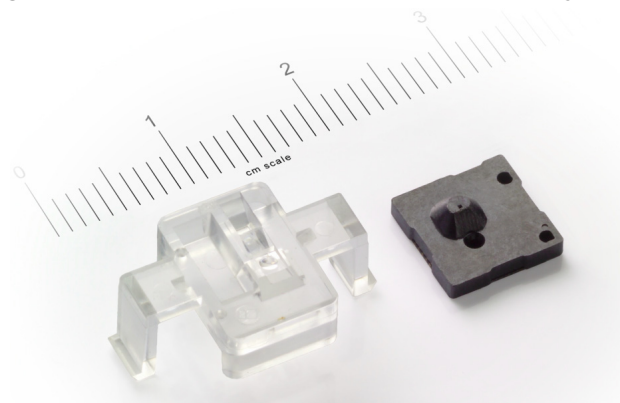
The CYONS2110 is the version that is designed for high-performance applications. Enabled by the Cypress 0.13-micron mixed signal process technology, the device integrates the OptiCheck sensor, full-speed USB, boost power regulator, and CapSense capability into a single silicon chip that allows seamless communication between sensor and MCU/full-speed USB. The sensor provides the best translation of hand motion into true gaming motion on the PC.

This highly integrated solution is programmable. It provides mouse suppliers the ease-of-use to design a single PCB system and customize their product. With the VCSEL integrated in the same package, designers do not need to calibrate the laser power during the manufacturing process. This greatly increases production throughput and reduces manufacturing costs.

The innovative technology of OvationONS™ II provides high-precision, high-speed motion tracking, and low power consumption. Designers can select from a family of integration options, ranging from low-power to high-performance, to target different types of wired and wireless design applications.

The CYONS2110 solutions have a small form factor. Along with the lens, each package forms a complete and compact laser tracking system. This datasheet describes the detailed technology capabilities of the CYONS2110.

Figure 1. CYONS2110/CYONSLENS2000 (2-Piece System)



Contents

| | | | |
|--|-----------|--|-----------|
| OvationONS II Family Performance Table..... | 3 | DC Analog Mux Bus Specifications..... | 18 |
| OvationONS II Family Applications | 3 | DC Low Power Comparator Specifications | 18 |
| OvationONS II Family Functional Description | 3 | DC POR and LVD Specifications | 18 |
| Pin Description | 5 | DC Programming Specifications | 19 |
| Microcontroller System..... | 7 | DC Characteristics - USB Interface..... | 19 |
| Features | 7 | AC Chip Level Specifications | 20 |
| PSoC Functional Overview..... | 8 | AC General Purpose I/O Specifications | 20 |
| The PSoC Core | 8 | AC External Clock Specifications | 21 |
| The CapSense Analog System | 8 | AC Analog Mux Bus Specifications | 21 |
| The Analog Multiplexer System..... | 8 | AC Programming Specifications..... | 21 |
| Additional System Resources | 9 | AC SPI Specifications | 22 |
| Getting Started..... | 9 | AC Comparator Specifications | 25 |
| Application Notes | 9 | AC I2C Specifications..... | 25 |
| Development Kits | 9 | AC USB Specifications..... | 26 |
| Training | 9 | PCB Land Pads and Keepout Zones | 27 |
| CYPros Consultants | 9 | Orientation of Axes..... | 28 |
| Solutions Library..... | 9 | PCB Mounting Height and Thickness..... | 28 |
| Technical Support | 9 | Thermal Impedances | 29 |
| Development Tools | 9 | Solder Reflow Peak Temperature | 29 |
| PSoC Designer Software Subsystems..... | 9 | Laser Safety Considerations | 30 |
| Designing with PSoC Designer | 10 | Laser Output Power | 30 |
| Select User Modules | 10 | Laser Output Power Test Procedure..... | 30 |
| Configure User Modules..... | 10 | Registration Assistance..... | 30 |
| Organize and Connect | 10 | Development Tool Selection | 31 |
| Generate, Verify, and Debug..... | 10 | Software | 31 |
| Power Supply Connections | 11 | Mouse Design Kits | 31 |
| Overview | 11 | Development Kits | 31 |
| Understanding DVDD..... | 11 | Evaluation Tools..... | 31 |
| AVDD, VREGA, and VREGD | 11 | Device Programmers..... | 32 |
| Using USB Power..... | 11 | Third Party Tools..... | 32 |
| Using Battery Power..... | 11 | Package Diagrams..... | 33 |
| Using External Power..... | 11 | Ordering Information..... | 34 |
| Filtering and Grounding..... | 11 | Ordering Code Definition..... | 34 |
| Wired Mouse Application Example..... | 12 | Document Conventions | 35 |
| Wireless Mouse Application Example | 13 | Acronyms Used | 35 |
| Electrical Specifications | 14 | Units of Measure | 35 |
| Absolute Maximum Ratings..... | 14 | Numeric Naming..... | 35 |
| Operating Conditions..... | 14 | Document History Page | 36 |
| | 14 | Worldwide Sales and Design Support..... | 36 |
| Power Consumption | 15 | Products | 36 |
| Power Specifications | 16 | PSoC Solutions | 36 |
| DC General Purpose I/O Specifications | 17 | | |

OvationONS II Family Performance Table

| Parameter | CYONS2000 | CYONS2001 | CYONS2100 | CYONS2101 | CYONS2110 | Unit |
|-------------------------|--|------------------------------|---|---------------------------------|--|-------|
| Variable resolution | 400, 800, 1600 | 400, 800, 1600 | 400–3200 | 400–3200 | 400–3200 | CPI |
| Maximum speed | 30 | 30 | 75 | 75 | 75 | in/s |
| Maximum acceleration | 20 | 20 | 30 | 30 | 30 | g |
| Integrated MCU | Yes | Yes | Yes | Yes | Yes | |
| CapSense | No | No | No | No | 26 inputs | |
| Flash | 16 | 16 | 32 | 32 | 32 | KB |
| SRAM | 2 | 2 | 2 | 2 | 2 | KB |
| Interfaces | Full-speed USB 4-wire SPI up to 28 GPIOs | 4-wire SPI up to 28 GPIOs | Full-speed USB 4-wire SPI up to 28 GPIO | 4-wire SPI up to 28 GPIOs | Full-speed USB 4-wire SPI up to 28 GPIOs | |
| Battery supply voltage | NA | 0.8 to 3.6 | NA | 0.8 to 3.6 | 0.8 to 3.6 | V |
| USB supply voltage | 4.25 to 5.25 | NA | 4.25 to 5.25 | NA | 4.25 to 5.25 | V |
| External supply voltage | 2.7 to 3.6 | 2.7 to 3.6 | 2.7 to 3.6 | 2.7 to 3.6 | 2.7 to 3.6 | V |
| Zero motion | 1 | 1 | 1 | 1 | 1 | Count |

OvationONS II Family Applications

- Wired and wireless laser mice
 - Gaming, graphic design, desktop, and mobile mice
- Optical trackballs
- Battery powered devices
- Motion sensing applications

OvationONS II Family Functional Description

The OvationONS II family is a two-piece laser navigation SoC kit containing the integrated IC package and the molded lens.

The 2-kV ESD-rated IC package integrates the VCSEL and laser sensor SoC. Depending on the product selected, the SoC includes an MCU, flash, SRAM, two internal oscillators, CapSense system, battery boost regulator, power regulator, and full-speed USB.

The molded lens collimates the VCSEL beam and images the light scattered from the tracking surface on to the sensor portion of the laser detector. The lens has features for registration to the package and easily snaps onto the PC board.

At the heart of the system is the OptiCheck laser navigation engine. It supports all functions required for tracking, including laser power control, resolution control, and self-adjusting power reduction, which reduces power consumption when motion stops. The laser output power is pre-calibrated to meet the eye safety requirements of IEC 60825 Class 1.

The navigation engine is accessed and controlled by an integrated PSoC-based MCU. The interface between the two blocks is through a system bus and a collection of navigation engine interrupts. Full details are available in the [OvationONS II Laser Navigation System-on-Chip TRM \(Technical Reference Manual\)](#) or in the PSoC Designer integrated development environment (IDE) software.

In addition to controlling the navigation engine, the PSoC MCU also serves as the main application processor. Based on Cypress's M8C architecture, the PSoC supports a rich instruction set, multiple processor speeds, and flexible GPIOs. Its internal main oscillator requires no external crystal. On-chip Flash and RAM allow entire navigation systems to be implemented with the single SoC.

The OvationONS II family supports a wide range of powering options. Internal regulators minimize the need for external circuitry. Depending on the product selected, the device can be power from a USB 5-V supply, from a single battery, from dual batteries, or from an external supply. The configuration and use of the power blocks are controlled with the integrated PSoC.

Wired sensors include integrated full-speed USB. As with the navigation engine and power system, the USB block is controlled by the integrated PSoC.

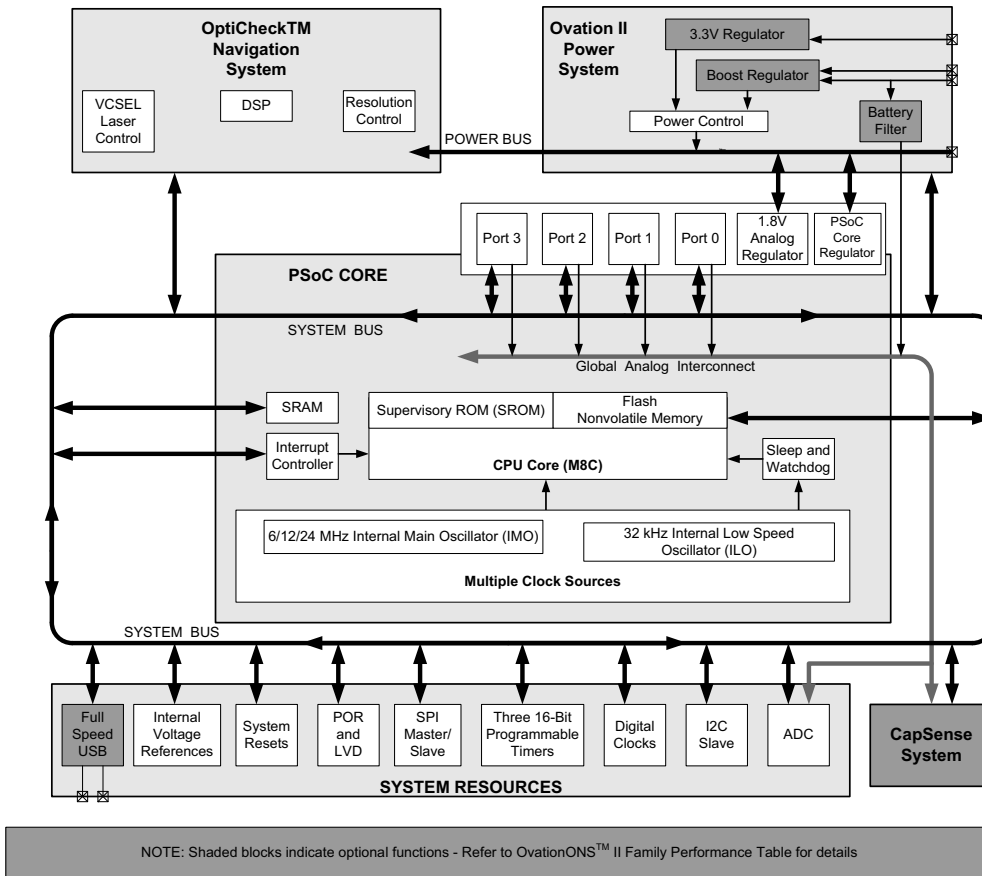
All sensors support a 4-wire SPI interface. A typical use of the SPI interface is to provide access to a radio for wireless applications. An I²C interface is also included with all devices.

The CYONS2110 device also supports CapSense functions, allowing additional features and differentiation in end products.

All features of the OvationONS II family are configured using Cypress's PSoC Designer™ software, allowing fast application development and time to market.

The OvationONS II family block diagram is shown on [Figure 2](#) on page 4. It shows a true SoC solution that enables design cycle reductions along with savings on manufacturing, PCB area, and component inventory management. The packaged solution delivers a fully integrated system that demonstrates tracking performance with efficient power consumption.

Figure 2. Block Diagram



Pin Description

This section describes, lists, and illustrates the CYONS2110 device pins and pinout configurations. The CYONS2110 is available in a 42-pin quad flat no-leads (QFN) package.

Table 1. CYONS2110 Pin Description

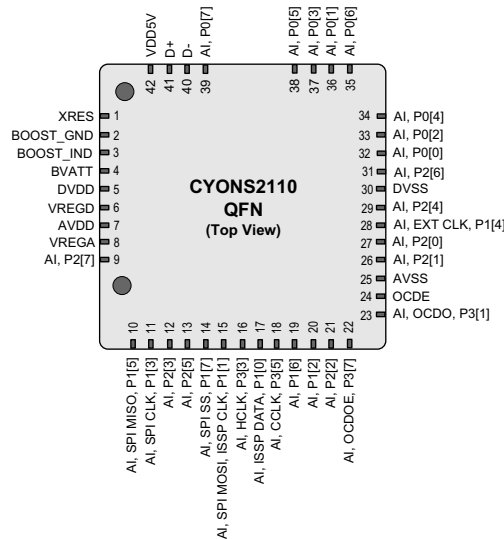
| Pin | Name | Digital | Analog | Description |
|-----|-----------|---------|--------|---|
| 1 | XRES | I | | Active high external reset with internal pull down |
| 2 | BOOST_GND | Power | Power | Boost regulator ground |
| 3 | BOOST_IND | Power | Power | Boost regulator inductor |
| 4 | VBATT | Power | Power | Boost regulator input |
| 5 | DVDD | Power | Power | Digital supply voltage and regulated output (see Power Supply Connections on page 11) |
| 6 | VREGD | Power | Power | Digital VREG |
| 7 | AVDD | Power | Power | Analog supply voltage |
| 8 | VREGA | Power | Power | Analog VREG |
| 9 | P2[7] | I/O | I | GPIO port 2 pin 7 |
| 10 | P1[5] | IOHR | I | SPI MISO, I2C_SDA, GPIO port 1 pin 5 |
| 11 | P1[3] | IOHR | I | SPI CLK, GPIO port 1 pin 3 |
| 12 | P2[3] | I/O | I | GPIO port 2 pin 3 |
| 13 | P2[5] | I/O | I | GPIO port 2 pin 5 |
| 14 | P1[7] | IOHR | I | SPI SS, I2C_SCL, GPIO port 1 pin 7 |
| 15 | P1[1] | IOHR | I | SPI MOSI, ISSP CLK ^[1] , I2C_SCL, GPIO port 1 pin 1 |
| 16 | P3[3] | IOHR | I | HCLK (OCD high speed clock output), GPIO port 3 pin 3 |
| 17 | P1[0] | I/O | I | ISSP DATA ^[1] , I2C_SDA, GPIO port 1 pin 0 |
| 18 | P3[5] | I/O | I | CCLK (OCD CPU clock output), GPIO port 3 pin 5 |
| 19 | P1[6] | IOHR | I | GPIO port 1 pin 6 |
| 20 | P1[2] | IOHR | I | GPIO port 1 pin 2 |
| 21 | P2[2] | I/O | I | GPIO port 2 pin 2 |
| 22 | P3[7] | I/O | I | OCDOE (OCD mode direction pin), GPIO port 3 pin 7 |
| 23 | P3[1] | I/O | I | OCDO (OCD odd data output), GPIO port 3 pin 1 |
| 24 | OCDE | OCD | OCD | OCDE (OCD even data output) |
| 25 | AVSS | Power | Power | Analog ground |
| 26 | P2[1] | I/O | I | GPIO port 2 pin 1 |
| 27 | P2[0] | I/O | I | GPIO port 2 pin 0 |
| 28 | P1[4] | IOHR | I | EXT CLK, GPIO port 1 pin 4 |
| 29 | P2[4] | I/O | I | GPIO port 2 pin 4 |
| 30 | DVSS | Power | Power | Digital ground |
| 31 | P2[6] | I/O | I | GPIO port 2 pin 6 |
| 32 | P0[0] | I/O | I | GPIO port 0 pin 0 |
| 33 | P0[2] | I/O | I | GPIO port 0 pin 2 |
| 34 | P0[4] | I/O | I | GPIO port 0 pin 4 |
| 35 | P0[6] | I/O | I | GPIO port 0 pin 6 |
| 36 | P0[1] | I/O | I | GPIO port 0 pin 1 |

Table 1. CYONS2110 Pin Description (continued)

| Pin | Name | Digital | Analog | Description |
|-----|-------|---------|--------|---|
| 37 | P0[3] | I/O | I | GPIO port 0 pin 3 |
| 38 | P0[5] | I/O | I | GPIO port 0 pin 5 |
| 39 | P0[7] | I/O | I | GPIO port 0 pin 7 |
| 40 | D- | I/O | | USB data |
| 41 | D+ | I/O | | USB data |
| 42 | VDD5V | Power | Power | 5V power |
| CP | DVSS | Power | Power | Center pad (CP) must be connected to digital ground |

Legend: I=Input; O=Output; H=5 mA High Output Drive, R=Regulated Output, OCD=On-Chip Debug

Figure 3. Pin Diagram



Note

1. These are the in-system serial programming (ISSP) pins. Unlike other GPIOs, they are not high-impedance at power-on reset (POR). See the [Technical Reference Manual \(TRM\)](#) at www.cypress.com or in the PSoC Designer development software for more details.

Microcontroller System

Features

- Powerful Harvard-architecture processor
 - M8C processor speed up to 24 MHz
 - Low power at high speed
 - Interrupt controller
 - Operating temperature range: +5°C to +45°C
- Flexible on-chip memory
 - 32 KB flash program storage
50,000 erase and write cycles
 - 2 KB SRAM data storage
 - Partial flash updates
 - Flexible protection modes
 - In-system serial programming (ISSP)
- Full-speed USB (12 Mbps)
 - Eight unidirectional endpoints
 - One bidirectional control endpoint
 - USB 2.0 compliant
 - Dedicated 512-byte buffer
 - Internal 3.3-V output regulator
- Low-power CapSense block
 - Configurable capacitive sensing elements
 - Supports combination of CapSense buttons, sliders, touchpads, touchscreens, and proximity sensors
- Complete development tools
 - Free development tool (PSoC Designer)
 - Full featured in-circuit emulator (ICE) and programmer
 - Full-speed emulation
 - Complex breakpoint structure
 - 128 K trace memory
- Precision programmable clocking
 - Internal $\pm 5.0\%$ 6-, 12-, 24-MHz main oscillator
 - Internal 32-kHz low speed oscillator
 - Support for optional external 32-kHz crystal
 - 0.25% accuracy for USB with no external crystal
- Programmable pin configurations
 - 25-mA sink current on all GPIOs
 - Pull-up, high-Z, open drain, or strong drive modes on all GPIOs
 - Up to 28 analog inputs on GPIO
 - Configurable inputs on all GPIOs
 - Selectable, regulated digital I/O on port 1
 - 3.3-, 2.5-, or 1.8-V output
 - 3.0 V, 20 mA total port 1 source current
 - 5-mA source current mode on ports 0 and 1
 - Hot swap capable
- Versatile analog mux
 - Common internal analog bus
 - Simultaneous connection of I/O combinations
 - High power supply rejection ratio (PSRR) comparator
 - Low dropout voltage regulator for the analog array
- Additional system resources
 - SPI master and SPI slave
 - Clock speed up to 12 MHz
 - Three 16-bit timers
 - Watchdog and sleep timers
 - Internal voltage reference
 - Integrated supervisory circuit
 - Analog-to-digital converter (ADC)
 - I²C slave

PSoC Functional Overview

Cypress's programmable system-on-chip (PSoC) on-chip controllers combine dynamic, configurable analog and digital blocks and an 8-bit MCU on a single chip, replacing multiple discrete components while delivering advanced flexibility and functionality. A PSoC device includes configurable analog and digital blocks, and programmable interconnect. This architecture enables the creation of customized peripheral configurations, to match the requirements of each individual application. Additionally, a fast CPU, flash program memory, SRAM data memory, and configurable I/O are included in a range of convenient pinouts.

The architecture for this device family, as shown in Figure 2 on page 4, contains: the core, the sensor, the CapSense analog system, and the system resources (including a full-speed USB port). A common, versatile bus enables connection between I/O and the analog system. Each PSoC device includes a dedicated CapSense block that provides sensing and scanning control circuitry for capacitive sensing applications. GPIO is also included. The GPIO provides access to the MCU and analog mux.

The PSoC Core

The PSoC core is a powerful engine that supports a rich instruction set. The PSoC core encompasses SRAM for data storage, an interrupt controller, Sleep and Watchdog timers, an IMO, and an ILO. The CPU core, called the M8C, is a powerful processor with speeds up to 24 MHz. The M8C is a 4 MIPS, 8-bit Harvard-architecture microprocessor.

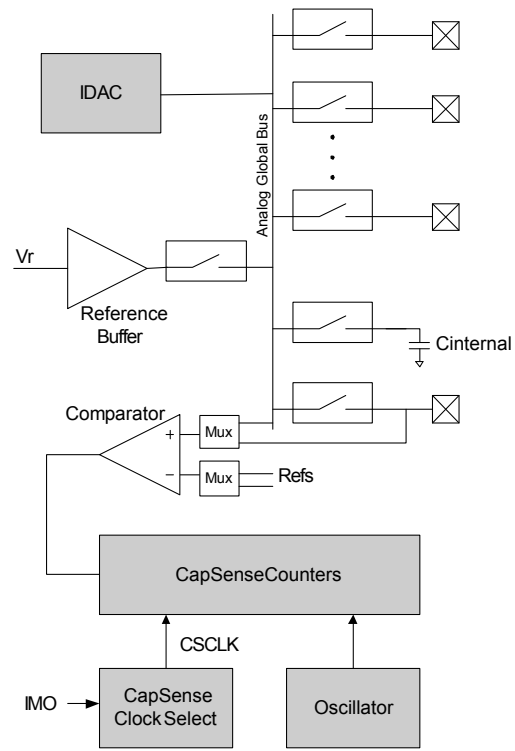
System resources provide additional capability, such as configurable USB and SPI master-slave communication interface, three 16-bit programmable timers, and various system resets supported by the M8C.

The analog system is composed of the CapSense PSoC block and an internal 1.8 V analog reference, which together support capacitive sensing of up to 26 inputs.

The CapSense Analog System

The analog system contains the capacitive sensing hardware. Several hardware algorithms are supported. This hardware performs capacitive sensing and scanning without requiring external components. Capacitive sensing is configurable on each GPIO pin. Scanning of enabled CapSense pins are completed quickly and easily across multiple ports.

Figure 4. Analog System Block Diagram



The Analog Multiplexer System

The analog mux bus connects to every GPIO pin. Pins are connected to the bus individually or in any combination. The bus also connects to the analog system for analysis with the CapSense block comparator.

Switch control logic enables selected pins to precharge continuously under hardware control. This enables capacitive measurement for applications such as touch sensing. Other multiplexer applications include:

- Complex capacitive sensing interfaces, such as sliders and touchpads
- Chip-wide mux that enables analog input from any I/O pin
- Crosspoint connection between any I/O pin combinations

When designing capacitive sensing applications, refer to the latest signal-to-noise signal level requirements application notes, which are at <http://www.cypress.com>. In general, and unless otherwise noted in the relevant application notes, the minimum signal-to-noise ratio (SNR) for CapSense applications is 5:1.

Additional System Resources

System resources, some previously listed, provide additional capability useful to complete systems. Additional resources include low voltage detection (LVD) and power-on reset (POR). Brief statements describing the merits of each system resource follows.

- The SPI master/slave module
 - Provides communication over three or four wires.
 - Runs at speeds of 46.9 kHz to 3 MHz (lower for a slower system clock).
- An I²C slave module
- LVD interrupts can signal the application of falling voltage levels, while the advanced POR circuit eliminates the need for a system supervisor.
- An internal reference provides an absolute reference for capacitive sensing.

Getting Started

For in depth information, along with detailed programming details, see the *PSoC[®] Technical Reference Manual*.

For up-to-date ordering, packaging, and electrical specification information, see the latest [PSoC device datasheets](#) on the web.

Application Notes

[Cypress application notes](#) are an excellent introduction to the wide variety of possible PSoC designs.

Development Kits

[PSoC Development Kits](#) are available online from and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

Training

[Free PSoC technical training](#) (on demand, webinars, and workshops), which is available online via www.cypress.com, covers a wide variety of topics and skill levels to assist you in your designs.

CYPros Consultants

Certified PSoC Consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC Consultant go to the [CYPros Consultants](#) web site.

Solutions Library

Visit our growing [library of solution focused designs](#). Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

Technical Support

[Technical support](#) – including a searchable Knowledge Base articles and technical forums – is also available online. If you cannot find an answer to your question, call our Technical Support hotline at 1-800-541-4736.

Development Tools

PSoC Designer™ is the revolutionary Integrated Design Environment (IDE) that you can use to customize PSoC to meet your specific application requirements. PSoC Designer software accelerates system design and time-to-market. Develop your applications using a library of precharacterized analog and digital peripherals (called User Modules) in a drag-and-drop design environment. Then, customize your design by leveraging the dynamically generated application programming interface (API) libraries of code. Finally, debug and test your designs with the integrated debug environment including in-circuit emulation (ICE) and standard software debug features. PSoC Designer includes:

- Application Editor GUI for device and [User Module](#) configuration and dynamic reconfiguration
- Extensive [User Module](#) catalog
- Integrated source code editor (C and Assembly)
- Free C compiler with no size restrictions or time limits
- Built in debugger
- Integrated Circuit Emulation (ICE)
- Built-in Support for Communication Interfaces:
 - Hardware and software I²C slaves and masters
 - Full-speed USB 2.0
 - Up to 4 full-duplex UARTs, SPI master and slave, and Wireless

PSoC Designer supports the entire library of PSoC 1 devices and runs on Windows XP, Windows Vista, and Windows 7.

PSoC Designer Software Subsystems

Design Entry

In the chip-level view you choose a base device to work with and then select different onboard analog and digital components called user modules that use the PSoC blocks. Examples of user modules are ADCs, DACs, amplifiers, and filters. You configure the user modules for your chosen application and connect them to each other and to the proper pins. Then you generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The tool also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration allows for changing configurations at run time. In essence, this allows you to use more than 100% of PSoC's resources for a given application.

Code Generation Tools

The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. You can develop your design in C, assembly, or a combination of the two - the choice is yours.

Assemblers. The assemblers allow you to merge assembly code seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and linked with other software modules to get absolute addressing.

C Language Compilers. C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices. The optimizing C compilers provide all the features of C tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

PSoC Designer has a debug environment that provides hardware in-circuit emulation (ICE), allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow a designer to read and program and read and write data memory, read and write I/O registers, read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows the designer to create a trace buffer of registers and memory locations of interest.

Online Help System

The online help system displays online, context-sensitive help. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer.

In-Circuit Emulator

A low cost, high functionality In-Circuit Emulator (ICE) is available for development support. This hardware has the capability to program single devices.

The emulator consists of a base unit that connects to the PC using a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full speed (24 MHz) operation.

Designing with PSoC Designer

The development process for the PSoC® device differs from that of a traditional fixed function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and by lowering inventory costs. These configurable resources, called PSoC Blocks, have the ability to implement a wide variety of user-selectable functions. The PSoC development process is summarized in four steps:

1. Select [User Modules](#).
2. Configure user modules.
3. Organize and connect.
4. Generate, verify, and debug.

Select User Modules

PSoC Designer provides a library of prebuilt, pretested hardware peripheral components called “user modules.” User modules make selecting and implementing peripheral devices, both analog and digital, simple.

Configure User Modules

Each user module that you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a pulse width modulator (PWM) User Module configures one or more digital PSoC blocks, one for each 8 bits of resolution. The user module parameters permit you to establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus. All the user modules are documented in datasheets that may be viewed directly in PSoC Designer or on the Cypress website. These [user module datasheets](#) explain the internal operation of the user module and provide performance specifications. Each datasheet describes the use of each user module parameter, and other information you may need to successfully implement your design.

Organize and Connect

You build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. You perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

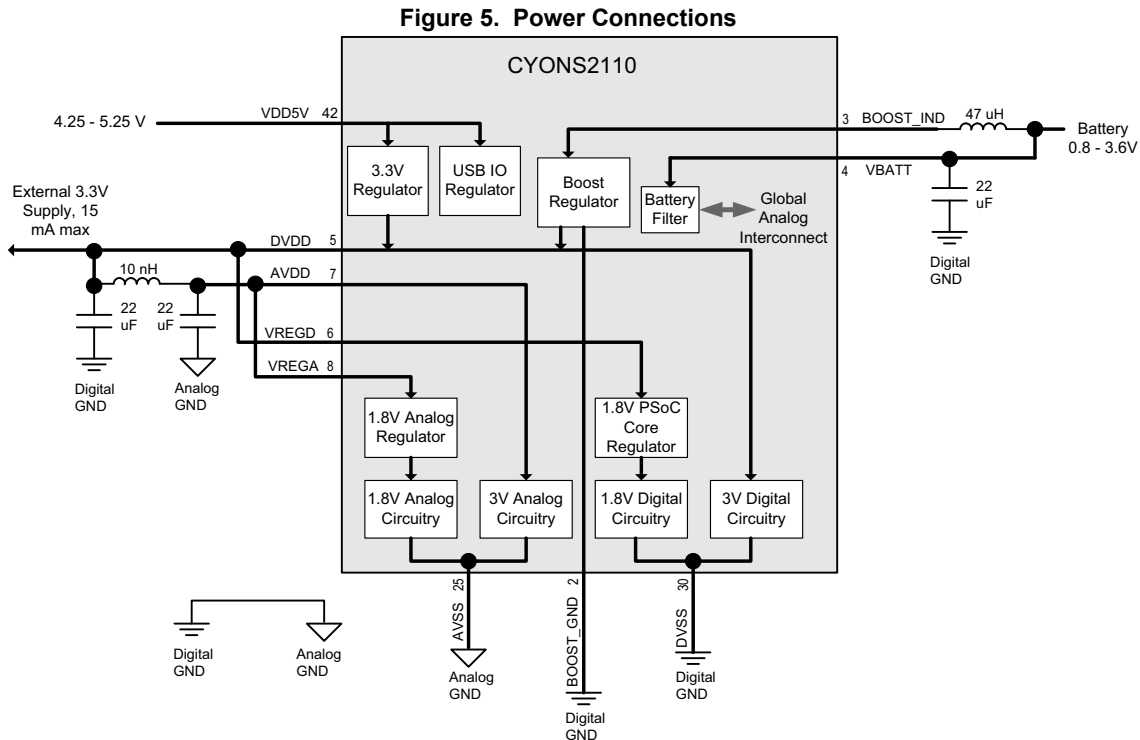
Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, you perform the “Generate Configuration Files” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides APIs with high-level functions to control and respond to hardware events at run time and interrupt service routines that you can adapt as needed.

A complete code development environment allows you to develop and customize your applications in either C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer’s debugger (access by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint and watch-variable features, the debug interface provides a large trace buffer and allows you to define complex breakpoint events that include monitoring address and data bus values, memory locations and external signals.

Power Supply Connections



Overview

The CYONS2110 incorporates a powerful and flexible powering system. It can be powered from one of three sources: a 5V supply (typically from the USB VBUS line), a battery, or an external 3.3V supply. Additionally, the CYONS2110's internal regulators can supply current to external devices. This section describes the capabilities and usage of the power system. Refer to [Figure 5](#) for a block diagram of the CYONS2110's power system.

Understanding DVDD

DVDD is a unique pin because it serves as either an input or an output. When the device is powered from USB (using the 3.3-V regulator) or battery (using the Boost Regulator), DVDD acts as an output, providing a 3.3-V voltage that can be used to power AVDD, VREGD, VREGA, and external parts. When the device is powered from an external 3.3-V supply, DVDD acts as an input only.

AVDD, VREGA, and VREGD

As with DVDD, these signals power the internal circuitry of the device. Unlike DVDD, these are always inputs. They should be connected as shown in [Figure 5](#).

Using USB Power

For most USB applications, the device is powered from the USB VBUS signal. In this case, the 5-V VBUS signal should be connected directly to the CYONS2110's VDD5V pin. Pins VBATT and BOOST_GND should be connected to DVSS, and BOOST_IND should be left unconnected.

Using Battery Power

For wireless applications, the device may be powered by the boost regulator. In this configuration, BOOST_GND should be connected to DVSS, BOOST_IND and VBATT pins should be connected as shown in [Figure 5](#), and VDD5V should be left unconnected. Do not run the device without the appropriate bypass capacitors, or excessive voltage may be generated across the inductor.

VBATT connects to an internal low-pass filter. The filter output can be routed through the global analog interconnect to the device's ADC, enabling the battery voltage to be monitored.

For designs using two series batteries, an option is to drive VREGA directly from the battery output. Doing so reduces the conversion loss in the boost regulator. However, care must be taken to ensure that the battery voltage does not fall below 1.71 V.

Using External Power

The CYONS2110 can also be powered from an external source. In this case, BOOST_GND should be connected to DVSS, VDD5V and BOOST_IND should be left unconnected, and the external 3.3V source should connect to DVDD. VBATT can be connected to DVSS or left unconnected.

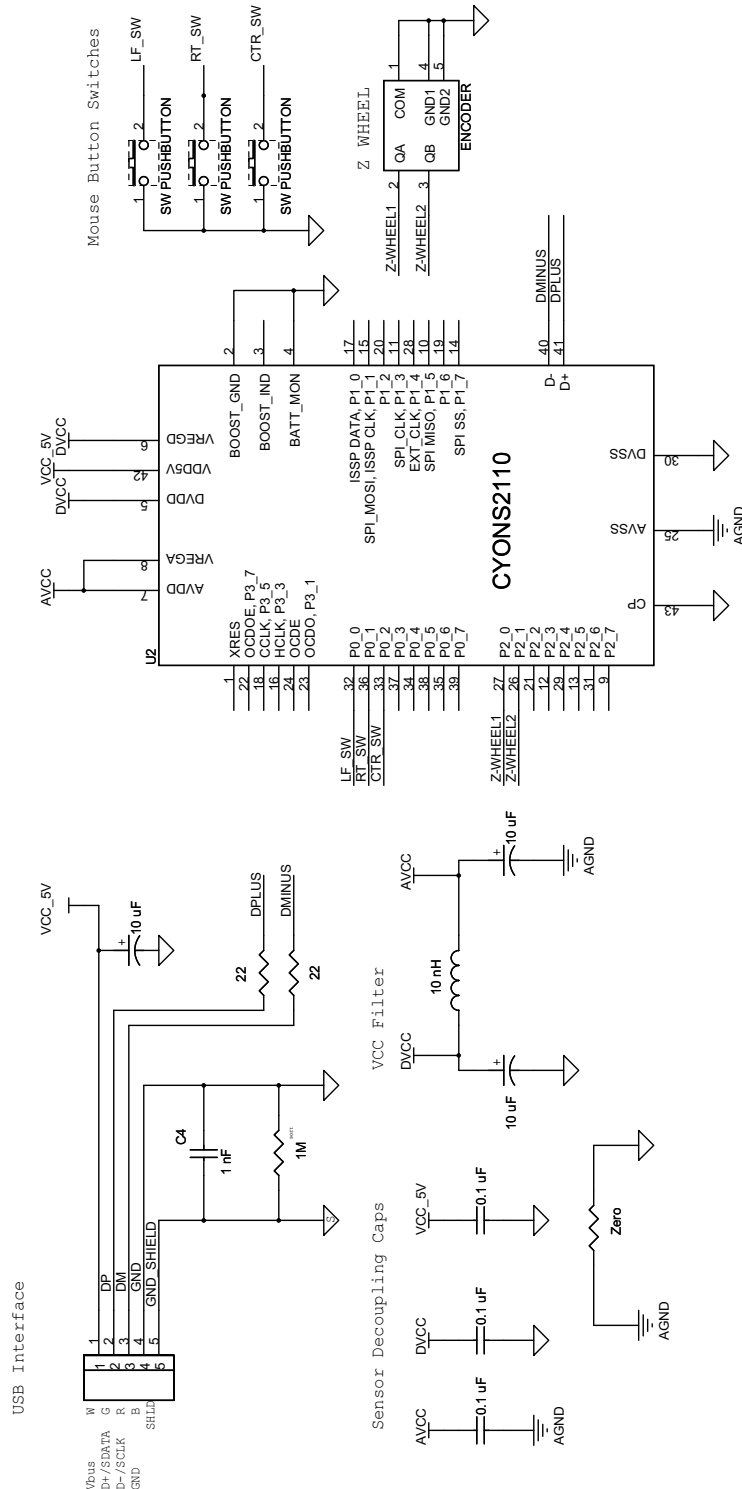
Filtering and Grounding

For all designs, it is important to provide proper grounding and isolation between the analog and digital power supplies. The analog and digital grounds should be isolated, except for a single connection point that is placed as close as possible to the device. On the supply side, an L-C filter should be placed between AVDD and DVDD, as shown in [Figure 5](#).

Wired Mouse Application Example

Figure 6 shows an implementation of a wired mouse. For complete details, refer to the [CY4631 - OvationONS™ II Laser Gaming Mouse Reference Design Kit](#).

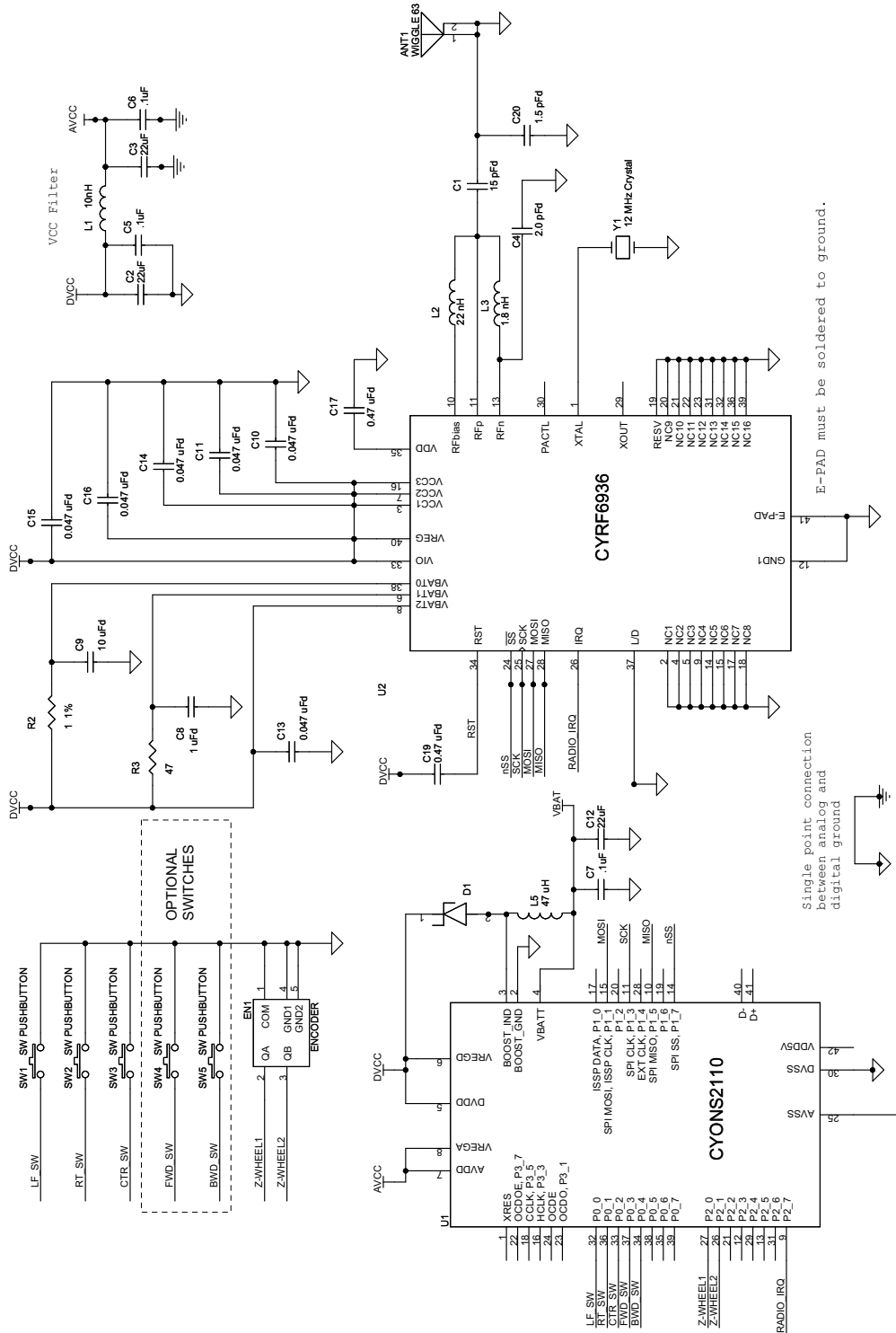
Figure 6. Wired Mouse



Wireless Mouse Application Example

Figure 7 shows an implementation of a wireless mouse.

Figure 7. Wireless Mouse



Single point connection between analog and digital ground.

E-PAD must be soldered to ground.

Electrical Specifications

This section presents the DC and AC electrical specifications of the CYONS2110 device. For the most up-to-date electrical specifications, confirm that you have the most recent datasheet by visiting <http://www.cypress.com>.

Absolute Maximum Ratings

| Parameter | Min | Typ | Max | Unit | Conditions |
|--|------|-----|------------|------|-------------------------------------|
| Storage temperature ^[2] | -40 | 25 | 65 | °C | Case temperature |
| Operating temperature | -15 | - | 55 | °C | Case temperature |
| Lead solder temperature | - | - | 260 | °C | 10 seconds |
| Supply voltage, DVDD, AVDD, VREGA, and VREGD relative to DVSS) | - | - | 3.6 | V | |
| Supply voltage, VDD5V relative to DVSS | - | - | 5.5 | V | |
| Supply voltage, VBATT relative to DVSS | - | - | 3.6 | V | |
| ESD | - | - | 2.0 | kV | All pins, HBM MIL 883 method 3015 |
| I/O voltage relative to DVSS | -0.5 | - | DVDD + 0.5 | V | GPIO ports 0, 2, and 3 |
| I/O voltage relative to DVSS | - | - | 5.5 | V | GPIO port 1 |
| Latch-up current | - | - | 100 | mA | In accordance with JESD78 standard. |
| Maximum current into any GPIO pin | -25 | - | +50 | mA | |

Operating Conditions

| Parameter | Min | Typ | Max | Unit | Conditions |
|---------------------------------------|------|-----|------|-------|-------------------------------|
| Operating temperature | 5 | - | 45 | °C | Ambient air temperature |
| Power supply voltage | | | | V | |
| VDD5V | 4.35 | - | 5.25 | | |
| DVDD, AVDD, VREGD | 2.70 | | 3.60 | | |
| VREGA | 1.71 | | 3.60 | | |
| VBATT | 0.80 | | 3.60 | | |
| Power supply rise time | 100 | - | - | µs | DVDD, AVDD, VREGD, VREGA |
| Supply noise – AVDD (sinusoidal) | - | - | 25 | mV pp | 10 kHz to 50 MHz |
| Supply noise – VDD, DVDD (sinusoidal) | - | - | 100 | mV pp | 10 kHz to 50 MHz |
| Distance from PCB to tracking surface | 5.80 | 6 | 6.20 | mm | See Figure 17 |
| PCB thickness | 1.54 | - | 1.79 | mm | See Figure 17 |

Note

- High storage temperature reduces flash data retention time specified in [Table 7](#) on page 19. Recommended storage temperature is 25 ± 25°C. Extended duration above 65°C can degrade reliability.

Power Consumption

Introduction

As described in [Overview](#) on page 11, the CYONS2110 has a highly advanced power system, which can be used to develop very low power applications. This section describes and specifies the power consumption performance of the device.

Enabling Low-Power Modes

In some cases, designers may wish to develop “always-on” applications, with no power-saving modes, and consequently no wakeup latency in performance. In other applications, conserving power is crucial and power saving modes are a firm requirement. The CYONS2110 allows low power modes to be enabled or disabled in firmware, either through register writes or through the application programming interface in Cypress’s PSoC Designer development software. The remainder of this section applies to applications requiring power saving modes.

Operating Modes

From a power consumption standpoint, consider these three operating modes.

- **Tracking mode:** In this mode, the device is actively tracking on a surface. It is the highest power mode of the device. The current consumption has a slight dependence on speed and surface. The current, however, is independent of resolution.
- **Inactive mode:** In this mode, the device is in its lowest power state. In inactive mode, the device cannot sense motion, but a timer is running. The timer can generate an interrupt that can wake the rest of the device and start tracking motion.
- **Sleep mode:** In sleep mode, the device self-transitions between tracking mode and inactive mode. The typical use of sleep modes is when the device is at rest, but might still be moved. In sleep mode, the CYONS2110 stays in inactive mode for a fixed time, then wakes up and checks for motion. If motion is detected, the device fully wakes up and begins tracking. If no motion is detected, the device can go back to sleep mode.

Power Management Through Sleep Mode Control

Power management for the CYONS2110 consists of setting the parameters that define the sleep modes. The device is equipped

with four sets of sleep mode settings, allowing four levels of sleep. By controlling the parameters of these four sleep modes, the designer can tailor the solution to make appropriate tradeoffs between power consumption and wakeup latency.

The transition between sleep modes is under the control of the CYONS2110’s digital signal processor (DSP) – no firmware needs to be written to manage the transition between modes.

Each of the four available sleep modes is defined by three parameters. These parameters are defined as registers that can be controlled by firmware, either through direct register writes or by using the NAV User Module in PSoC Designer.

- **Sleep time:** This is the amount of time that the device is in its low power inactive state.
- **Motion threshold:** This is the amount of motion that is required to bring the device out of sleep.
- **Sleep mode time:** This is the amount of time that the device stays in a particular sleep mode before transitioning to the next lowest sleep mode. Longer sleep times saves power but have higher wakeup latency.

[Figure 8](#) shows the flowchart for a particular sleep mode, showing how the three parameters affect behavior.

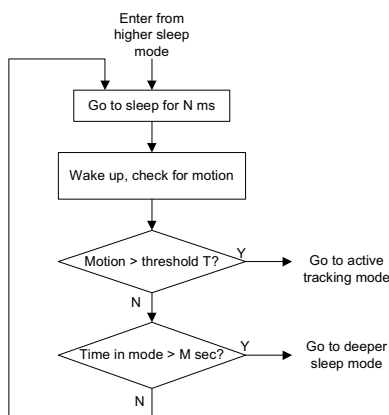
Calculating Power for Sleep Mode

The power consumption in sleep mode can be found by using a duty cycle calculation. The sleep mode current is determined by the tracking mode current, the inactive current, the time required to check for motion (typically 2.9 ms), and the time between check-for-motion events. The expected current consumption is given by the formula

$$I_{SLEEP} = \frac{I_{TRACK} \times 2.9 + I_{INACT} \times T_{SLEEP}}{2.9 + T_{SLEEP}}$$

where I_{SLEEP} is the sleep current, I_{TRACK} is the tracking current, I_{INACT} is the inactive current, and T_{SLEEP} is the time (in ms) in the low power state. As an example, if the tracking current is 8.5 mA, the inactive current is 7.5 μ A and the sleep time is 100 ms, then the expected sleep current is 0.25 mA.

Figure 8. Sleep Mode Flowchart.



Power Specifications

There are three ways to power the CYONS2110 – external powering, battery powering, and USB powering. [Table 4](#) provides the current consumption values for each mode.

With external powering, a 3-V supply is connected to DVDD, AVDD, VREGD, and VREGA, and the internal regulators are turned off. In this case, the current consumption during tracking is I_{TRACK_EXT} , and the consumption during sleep is I_{SLEEP} .

With battery powering, the device is powered by the internal boost regulator. The 5-V USB regulator is turned off. Total tracking current must include the current consumed by the regulator itself, and is given by the sum of I_{TRACK} and $I_{REGBOOST}$. Sleep current is likewise given by the sum of I_{SLEEP} and $I_{REGBOOST}$. In both cases, the current drawn from the battery must be adjusted by the voltage conversion ratio and the boost regulator efficiency η_{TRACK} and η_{INACT} .

With USB powering, the 5-V USB supply is connected to VDD5V, and DVDD, AVDD, VREGD, and VREGA are driven by the internal 5-V USB regulator. The boost regulator is turned off. Tracking current in this case is specified by I_{TRACK_USB} . Sleep current must include the current consumption of the regulator itself, and is specified by the sum of I_{SLEEP} and I_{REG5V} . For designs using the CYONS2110, low power operation is often only needed to support USB Suspend. Reference code for this is available in the [CY4631 - OvationONS™ II Laser Gaming Mouse Reference Design Kit](#).

Sleep current is achieved by activating “Navigation Sleep Modes” in Cypress’s PSoC Designer development environment. Doing so enables the sleep mode progressions described earlier. If sleep modes are not activated, the device current stays at tracking levels, even when the device is not sensing motion.

I_{SB} is the current in the lowest-power mode of the device. In this mode, the CPU is halted and operation can only be restarted with an external reset at the XRES pin.

Table 2. Power Specifications

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|-------------------|---|---|--|------|------|-------|
| I_{TRACK_EXT} | Tracking current into DVDD, AVDD, VREGD, VREGA | 3.0 V, 25 °C, 5 inch/second, 24 MHz IMO, 6 MHz CPU clock, white surface, nominal tracking height | – | 9 | 12.5 | mA |
| I_{TRACK_USB} | Tracking current into VDD5V | 5.25 V, 25 °C, 5 inch/second, 24 MHz IMO, 6 MHz CPU clock, white surface, nominal tracking height, DVDD, AVDD, VREGD, and VREGA powered by internal regulator | – | 12.5 | 16 | mA |
| I_{INACT} | Inactive current into DVDD, AVDD, VREGD, VREGA | 3.0 V, 25 °C, CPU in sleep state | – | 7 | 14 | µA |
| I_{SLEEP} | Sleep current into DVDD, AVDD, VREGD, VREGA | 3.0 V, 25 °C | See Calculating Power for Sleep Mode on page 15 for equation | | | |
| I_{REG5V} | 5 V-to-3 V regulator current consumption | VDD5V = 5.25 V, regulator active | – | 250 | – | µA |
| $I_{REGBOOST}$ | Boost regulator current consumption | 3.0 V at VBATT, 25 °C | – | 20 | – | µA |
| η_{TRACK} | Boost converter efficiency, tracking mode | 1.2 V VBATT input, 47 µH inductor, 10 mA load, 400 kHz switching frequency | – | 90 | – | % |
| η_{INACT} | Boost converter efficiency, inactive mode | 1.2 V VBATT input, 47 µH inductor | – | 70 | – | % |
| V_{BOOST_SET} | Boost converter nominal output | Programmed using PSoC Designer user module calibration feature | 2.7 | – | 3.3 | V |
| $V_{BOOST}^{[3]}$ | Boost converter accuracy | Offset from set point | –10 | | +10 | % |
| I_{SB} | Shutdown current into DVDD, AVDD, VREGD, VREGA, all blocks off | 3.0 V, 25 °C, 5 V supply not present | – | 4 | 11 | µA |
| I_{SB_USB} | Shutdown current, all blocks off, into VDD5V | 5.25 V, 25C, DVDD, AVDD, VREGA, VREGD powered by internal 5 V-to-3 V regulator in standby | – | 80 | – | µA |
| $I_{SB_DUALUSB}$ | Shutdown current, all blocks off, into DVDD, AVDD, VREGD, VREGA | 25 °C, dual mode trip circuit active, 5V supply present | – | 16.5 | – | µA |

Note

3. Boost output specification requires use of calibrated user module in PSoC Designer version 5.0 Service Pack 6 or later.

DC General Purpose I/O Specifications

GPIOs are arranged into four ports. Ports 0, 1, and 2 have eight GPIO pins and Port 3 has four GPIO pins. Port 1 has an optional low drop out (LDO) regulator that adjusts the port's output voltage to 1.8, 2.5, or 3.0 volts. Additionally, each GPIO pin can be independently set to one of four drive modes: strong drive, open drain, pull-up, or Hi-Z analog.

Rise and fall times are specified for 10% and 90% voltage values.

The following tables list guaranteed maximum and minimum specifications for the voltage range of 2.7 V to 3.6 V at the DVDD pin, and over the temperature range $5\text{ }^{\circ}\text{C} \leq T_A \leq 45\text{ }^{\circ}\text{C}$. Typical parameters apply to 3.3 V at 25 °C and are for design guidance only.

Table 3. 2.7V to 3.6V DC GPIO Specifications

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|-------------------|--|--|------------|------|------|-------|
| R _{PU} | Pull-up resistor | Pin configured for pull-up mode. | 4.0 | 5.6 | 8.0 | kΩ |
| V _{OH1} | High output voltage Port 2 or 3 Pins | I _{OH} ≤ 10 μA, maximum of 10 mA source current in all I/Os. | DVDD - 0.2 | – | – | V |
| V _{OH2} | High output voltage Port 2 or 3 Pins | I _{OH} = 1 mA, maximum of 20 mA source current in all I/Os. | DVDD - 0.9 | – | – | V |
| V _{OH3} | High output voltage Port 0 or 1 Pins with LDO Regulator Disabled for Port 1 | I _{OH} < 10 μA, maximum of 10 mA source current in all I/Os. | DVDD - 0.2 | – | – | V |
| V _{OH4} | High output voltage Port 0 or 1 Pins with LDO Regulator Disabled for Port 1 | I _{OH} = 5 mA, maximum of 20 mA source current in all I/Os. | DVDD - 0.9 | – | – | V |
| V _{OH5} | High output voltage Port 1 Pins with LDO Regulator Enabled for 3V Out | I _{OH} < 10 μA, DVDD > 3.1V, maximum of 4 I/Os all sourcing 5 mA. | 2.85 | 3.00 | 3.30 | V |
| V _{OH6} | High output voltage Port 1 Pins with LDO Regulator Enabled for 3V Out | I _{OH} = 5 mA, DVDD > 3.1V, maximum of 20 mA source current in all I/Os. | 2.20 | – | – | V |
| V _{OH7} | High output voltage Port 1 Pins with LDO Enabled for 2.5V Out | I _{OH} < 10 μA, DVDD > 2.7V, maximum of 20 mA source current in all I/Os. | 2.35 | 2.50 | 2.75 | V |
| V _{OH8} | High output voltage Port 1 Pins with LDO Enabled for 2.5V Out | I _{OH} = 2 mA, DVDD > 2.7V, maximum of 20 mA source current in all I/Os. | 1.90 | – | – | V |
| V _{OH9} | High output voltage Port 1 Pins with LDO Enabled for 1.8V Out | I _{OH} < 10 μA, DVDD > 2.7V, maximum of 20 mA source current in all I/Os. | 1.60 | 1.80 | 2.10 | V |
| V _{OH10} | High output voltage Port 1 Pins with LDO Enabled for 1.8V Out | I _{OH} = 1 mA, DVDD > 2.7V, maximum of 20 mA source current in all I/Os. | 1.20 | – | – | V |
| V _{OL} | Low output voltage | I _{OL} = 25 mA, DVDD > 3.3V, maximum of 60 mA sink current on even port pins (for example, P0[2] and P1[4]) and 60 mA sink current on odd port pins (for example, P0[3] and P1[5]). | – | – | 0.75 | V |
| V _{IL} | Input low voltage | | – | – | 0.80 | V |
| V _{IH} | Input high voltage | | 2.00 | – | – | V |
| V _H | Input hysteresis voltage | | – | 80 | – | mV |
| I _{IL} | Input leakage (absolute value) | Gross tested to 1 μA. | – | 0.5 | 1.0 | μA |
| C _{PIN} | Pin capacitance | Temp = 25 °C. | 0.5 | 1.7 | 8.0 | pF |

DC Analog Mux Bus Specifications

The analog mux bus can connect signals from GPIOs to and from internal analog blocks and other GPIOs. [Table 4](#) lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 4. DC Analog Mux Bus Specifications

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|------------------|---|---------------------|-----|-----|-----|------|
| R _{SW} | Switch resistance to common analog bus | Pin voltage < 1.8 V | – | – | 800 | Ω |
| R _{GND} | Resistance of initialization switch to DVSS | Pin voltage < 1.8 V | – | – | 800 | Ω |

DC Low Power Comparator Specifications

The device includes two general-purpose comparators, using internal or external signals from the analog mux bus. [Table 5](#) lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 5. DC Comparator Specifications

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|--------------------|--|----------------------------------|-----|-----|-----|------|
| V _{LPC} | Low power comparator (LPC) common mode | Maximum voltage limited to DVDD. | 0.0 | – | 1.8 | V |
| I _{LPC} | LPC supply current | | – | 10 | 40 | μA |
| V _{OSLPC} | LPC voltage offset | | – | 2.5 | 30 | mV |

DC POR and LVD Specifications

The device features two mechanisms for dealing with low power supply voltages. Both POR and LVD events occur when DVDD falls below a threshold. A POR completely resets the device. An LVD generates an interrupt to the MCU, allowing the application developer to better manage power supply drops.

The POR threshold is defined by bits 7 (HPOR) and 5:4 (PORLEV) and of the VLT_CR register at address E3h in register bank 1. The LVD threshold is defined by bits 2:0 (VM) of the same register. Refer to the [technical reference manual](#) for more details.

[Table 6](#) lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 6. DC POR and LVD Specifications

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|-------------------|--|--|---------------------|------|------|------|
| V _{POR0} | DVDD value for POR trip PORLEV[1:0] = 00b, HPOR = 0 | DVDD must be greater than or equal to 1.71V during startup, reset from the XRES pin, or reset from watchdog. | 1.61 | 1.66 | 1.71 | V |
| V _{POR1} | PORLEV[1:0] = 00b, HPOR = 1 | | – | 2.36 | 2.40 | V |
| V _{POR2} | PORLEV[1:0] = 01b, HPOR = 1 | | – | 2.60 | 2.65 | V |
| V _{POR3} | PORLEV[1:0] = 10b, HPOR = 1 | | – | 2.82 | 2.95 | V |
| V _{LVD0} | DVDD value for LVD trip VM[2:0] = 000b | | 2.40 ^[4] | 2.45 | 2.51 | V |
| V _{LVD1} | VM[2:0] = 001b | | 2.64 ^[5] | 2.71 | 2.78 | V |
| V _{LVD2} | VM[2:0] = 010b | | 2.85 ^[6] | 2.92 | 2.99 | V |
| V _{LVD3} | VM[2:0] = 011b | | 2.95 | 3.02 | 3.09 | V |
| V _{LVD4} | VM[2:0] = 100b | | 3.06 | 3.13 | 3.20 | V |
| V _{LVD5} | VM[2:0] = 101b | | 1.84 | 1.90 | 1.96 | V |
| V _{LVD6} | VM[2:0] = 110b | | 1.75 ^[7] | 1.80 | 1.84 | V |

Notes

4. Always greater than 50 mV above V_{POR1} voltage for falling supply.
5. Always greater than 50 mV above V_{POR2} voltage for falling supply.
6. Always greater than 50 mV above V_{POR3} voltage for falling supply.
7. Always greater than 50 mV above V_{POR0} voltage for falling supply.

DC Programming Specifications

Table 7 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

The CYONS2110 must be properly powered for flash programming, with DVDD, AVDD, VREGD, and VREGA all held within the specified range. A suitable option for in-circuit programming USB designs is to apply 5 V to the VDD5V pin, and use the internal regulator to drive DVDD, AVDD, VREGD, and VREGA. This enables direct connection to Cypress's CY3210-Miniprogram. For in-circuit programming of battery or externally-powered designs, the designer must include provisions for supplying DVDD, AVDD, VREGD, and VREGA externally.

Table 7. DC Programming Specifications

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|-----------------------|--|--|-----------------|-----|-----------------|--------|
| V _{IW} | Supply voltage for flash write operations | V _{IW} applied to DVDD, AVDD, VREGD, and VREGA | 2.7 | – | 3.6 | V |
| I _{DDP} | Supply current during programming or verify | | – | 5 | 25 | mA |
| V _{ILP} | Input low voltage during programming or verify | See DC General Purpose I/O Specifications on page 17. | – | – | V _{IL} | V |
| V _{IHP} | Input high voltage during programming or verify | See DC General Purpose I/O Specifications on page 17. | V _{IH} | – | – | V |
| I _{ILP} | Input current when applying V _{ILP} to ISSP CLK and ISSP DATA pins during programming or verify | Driving internal pull-down resistor. | – | – | 0.2 | mA |
| I _{IHP} | Input current when applying V _{IHP} to ISSP CLK and ISSP DATA pins during programming or verify | Driving internal pull-down resistor. | – | – | 1.5 | mA |
| V _{OLP} | Output low voltage during programming or verify | | – | – | DVSS + 0.75 | V |
| V _{OHP} | Output high voltage during programming or verify | DC General Purpose I/O Specifications on page 17. For DVDD > 3V use the value with I _{OH} = 5 mA. | V _{OH} | – | DVDD | V |
| Flash _{ENPB} | Flash write endurance | Erase/write cycles by block. | 50,000 | – | – | Cycles |
| Flash _{DR} | Flash data retention | Following maximum flash write cycles at ambient temp of 45°C. | 5 | 10 | – | Years |

DC Characteristics - USB Interface

The device includes an integrated full-speed USB block. Table 8 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 8. DC USB Characteristics

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|--------|--------------------------------------|-----------------------------|-------|-----|-------|-------|
| Rusbi | USB D+ pull-up resistance | With idle bus | 0.900 | – | 1.575 | kΩ |
| Rusba | USB D+ pull-up resistance | While receiving traffic | 1.425 | – | 3.090 | kΩ |
| Vohusb | Static output high | | 2.8 | – | 3.6 | V |
| Volusb | Static output low | | – | – | 0.3 | V |
| Vdi | Differential input sensitivity | | 0.2 | – | – | V |
| Vcm | Differential input common mode range | | 0.8 | – | 2.5 | V |
| Vse | Single-ended receiver threshold | | 0.8 | – | 2.0 | V |
| Cin | Transceiver capacitance | | | – | 50 | pF |
| Iio | High-Z state data line leakage | On D+ or D- line | –10 | – | 10 | μA |
| Rps2 | PS/2 pull-up resistance | | 3 | 5 | 7 | kΩ |
| Rext | External USB series resistor | In series with each USB pin | 21.78 | 22 | 22.22 | Ω |

AC Chip Level Specifications

The device has two internal oscillators. The IMO controls the clock speeds for the CPU. A programmable frequency divider allows the CPU to run at lower speeds than the IMO. The ILO is typically active in sleep modes, clocking sleep, and watchdog timers. Other internal timers can be clocked by either the CPU clock or the ILO.

Table 9 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 9. AC Specifications

| Parameter | Description | Min | Typ | Max | Unit |
|--------------------|--|------------------------|-----|------------------|------|
| F _{IMO24} | IMO frequency for 24 MHz setting | 22.8 | 24 | 25.2 | MHz |
| F _{IMO12} | IMO frequency for 12 MHz setting | 11.4 | 12 | 12.6 | MHz |
| F _{IMO6} | IMO frequency for 6 MHz setting | 5.7 | 6.0 | 6.3 | MHz |
| DC _{IMO} | IMO output duty cycle at 6 and 12 MHz setting ^[8] | 40 | 50 | 60 | % |
| F _{CPU} | CPU frequency ^[9] | F _{IMO} / 256 | – | F _{IMO} | MHz |
| F _{32K1} | ILO frequency ^[10] | 19 | 32 | 50 | kHz |
| T _{RAMP} | Supply ramp time | 20 | – | – | μs |
| TXRST | External reset pulse width at power-up | 1 | – | – | ms |
| TXRST2 | External reset pulse width after power-up | 10 | – | – | μs |
| TMOT | Motion delay from reset to valid tracking data ^[11] | – | – | 30 | ms |

AC General Purpose I/O Specifications

GPIOs are arranged into ports. Ports 0, 1, and 2 have eight GPIO pins and Port 3 has four GPIO pins. Port 1 has an optional LDO regulator that adjusts the port's output voltage to 1.8, 2.5, or 3.0 volts. Additionally, each GPIO pin can be independently set to one of four drive modes: strong drive, open drain, pull-up, or high-Z analog.

Rise and fall times are specified for 10% and 90% voltage values.

Specifications are for the entire operating temperature range.

Table 10. AC GPIO Specs

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---------------------------|------------------------------------|---|-----|-----|-----|-------|
| F _{GPIO} | GPIO operating frequency | Strong drive | 0 | – | 12 | MHz |
| T _{RISE_01} | Rise time, ports 0 -1 | Strong drive, C _{LOAD} = 50 pF, DVDD = 3.0 - 3.6 | – | – | 50 | ns |
| T _{RISE_01_L} | Rise time, ports 0 -1, low supply | Strong drive, C _{LOAD} = 50 pF, DVDD = 2.7 - 3.0 | – | – | 70 | ns |
| T _{RISE_LDO_3} | Rise time, port 1, 3V LDO enabled | Strong drive, C _{LOAD} = 50 pF, DVDD > 3.1V | – | – | 50 | ns |
| T _{RISE_LDO_2.5} | Rise time, port 1, 2.5 LDO enabled | Strong drive, C _{LOAD} = 50 pF, DVDD > 2.7V | – | – | 70 | ns |
| T _{RISE_LDO_1.8} | Rise time, port 1, 1.8 LDO enabled | Strong drive, C _{LOAD} = 50 pF, DVDD > 2.7V | – | – | 100 | ns |
| T _{RISE_23} | Rise time, ports 2 - 3 | Strong drive, C _{LOAD} = 50 pF, DVDD = 2.7 - 3.6 | – | – | 80 | ns |
| T _{FALL} | Fall time, all ports | Strong drive, C _{LOAD} = 50 pF, DVDD = 3.0 - 3.6 | – | – | 50 | ns |
| T _{FALL_L} | Fall time, all ports, low supply | Strong drive, C _{LOAD} = 50 pF, DVDD = 2.7 - 3.0 | – | – | 70 | ns |
| T _{FALL_LDO_3} | Fall time, port 1, 3V LDO enabled | Strong drive, C _{LOAD} = 50 pF, DVDD > 3.1V | – | – | 50 | ns |
| T _{FALL_LDO_2.5} | Fall time, port 1, 2.5 LDO enabled | Strong drive, C _{LOAD} = 50 pF, DVDD > 2.7V | – | – | 70 | ns |
| T _{FALL_LDO_1.8} | Fall time, port 1, 1.8 LDO enabled | Strong drive, C _{LOAD} = 50 pF, DVDD > 2.7V | – | – | 80 | ns |

Notes

8. IMO can be output from chip by routing to GPIO. Maximum GPIO output frequency is 12 MHz, so duty cycle at 24 MHz is not defined. See Technical Reference Manual at www.cypress.com or in Cypress's PSoC Designer software for details on routing IMO to GPIO pin.

9. Available frequency divisors are 1, 2, 4, 8, 16, 32, 128, and 256.

10. 32 kHz oscillator can be locked to external crystal. See technical reference manual available at www.cypress.com or in Cypress' PSoC Designer software.

11. Value provided represents maximum startup time for typical application. Applications requiring additional startup code, processing, or delay may increase TMOT.

AC External Clock Specifications

The IMO can be replaced with an external clock at the EXT CLK / P[1]4 pin. Refer to the [technical reference manual](#) for more details. [Table 11](#) lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 11. AC External Clock Specifications

| Parameter | Description | Min | Typ | Max | Unit |
|---------------------|--|-------|-----|------|------|
| F _{OSCEXT} | Frequency | 0.750 | – | 25.2 | MHz |
| – | High period | 20.6 | – | 5300 | ns |
| – | Low period | 20.6 | – | – | ns |
| – | Required time to run from IMO before switching to external clock | 150 | – | – | μs |

AC Analog Mux Bus Specifications

The analog mux bus can connect signals from GPIOs to and from internal analog blocks and other GPIOs. [Table 12](#) lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 12. AC Analog Mux Bus Specifications

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|-----------------|-------------|---------------------|-----|-----|-----|------|
| F _{SW} | Switch rate | Pin voltage < 1.8 V | – | – | 6.3 | MHz |

AC Programming Specifications

[Table 13](#) lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 13. AC Programming Specifications

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---------------------|--|------------------|-----|-----|-----|-------|
| T _{RSCLK} | Rise time of ISSP CLK | | 1 | – | 20 | ns |
| T _{FSCLK} | Fall time of ISSP CLK | | 1 | – | 20 | ns |
| T _{SSCLK} | Data setup time to falling edge of ISSP CLK | | 40 | – | – | ns |
| T _{HSCLK} | Data hold time from falling edge of ISSP CLK | | 40 | – | – | ns |
| F _{SCLK} | Frequency of ISSP CLK | | 0 | – | 8 | MHz |
| T _{ERASEB} | Flash erase time (Block) | | – | – | 18 | ms |
| T _{WRITE} | Flash block write time | | – | – | 25 | ms |
| T _{DSCLK2} | Data out delay from falling edge of ISSP CLK | 3.0 ≤ DVDD ≤ 3.6 | – | – | 85 | ns |

AC SPI Specifications

Table 14 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 14. AC SPI Master Specifications

| Parameter | Description | Min | Typ | Max | Unit |
|---------------------|-----------------------------------|-----|-----|---------------------|------|
| f _{SCLK} | SPI CLK frequency ^[12] | – | – | F _{IMO} /2 | MHz |
| t _{SETUP} | SPI MISO to SPI CLK setup time | 60 | – | – | ns |
| t _{HOLD} | SPI CLK to SPI MISO hold time | 40 | – | – | ns |
| t _{OUT_SU} | SPI MOSI to SPI CLK setup time | 40 | – | – | ns |
| t _{OUT_H} | SPI CLK to SPI MOSI hold time | 40 | – | – | ns |

Table 15. AC SPI Slave Specifications

| Parameter | Description | Min | Typ | Max | Unit |
|------------------------|--|-------|-----|-----|------|
| f _{SCLK} | SPI CLK frequency ^[12] | – | – | 12 | MHz |
| t _{LOW} | Minimum SPI CLK low width ^[13] | 41.67 | – | – | ns |
| t _{HIGH} | Minimum SPI CLK high width ^[13] | 41.67 | – | – | ns |
| t _{SETUP} | SPI MOSI to SPI CLK setup time | 25 | – | – | ns |
| t _{HOLD} | SPI CLK to SPI MOSI hold time | 25 | – | – | ns |
| t _{OUT_H} | SPI CLK to SPI MISO hold time | 35 | – | – | ns |
| t _{SS_MISO} | SPI SS to SPI MISO valid | – | – | 100 | ns |
| t _{SCLK_MISO} | SPI CLK to SPI MISO valid | – | – | 140 | ns |
| t _{SS_HIGH} | Minimum SPI SS high width | – | – | 35 | ns |
| t _{SS_CLK} | Time from SPI SS low to first SPI CLK | – | – | 20 | ns |
| t _{CLK_SS} | Time from last SPI CLK to SPI SS high | – | – | 25 | ns |

Notes

12. Clock frequency is half of clock input to SPI block.

13. Value corresponds to 50% duty cycle at 12 MHz.

Figure 9. SPI Master Timing Diagram, Modes 0 and 2

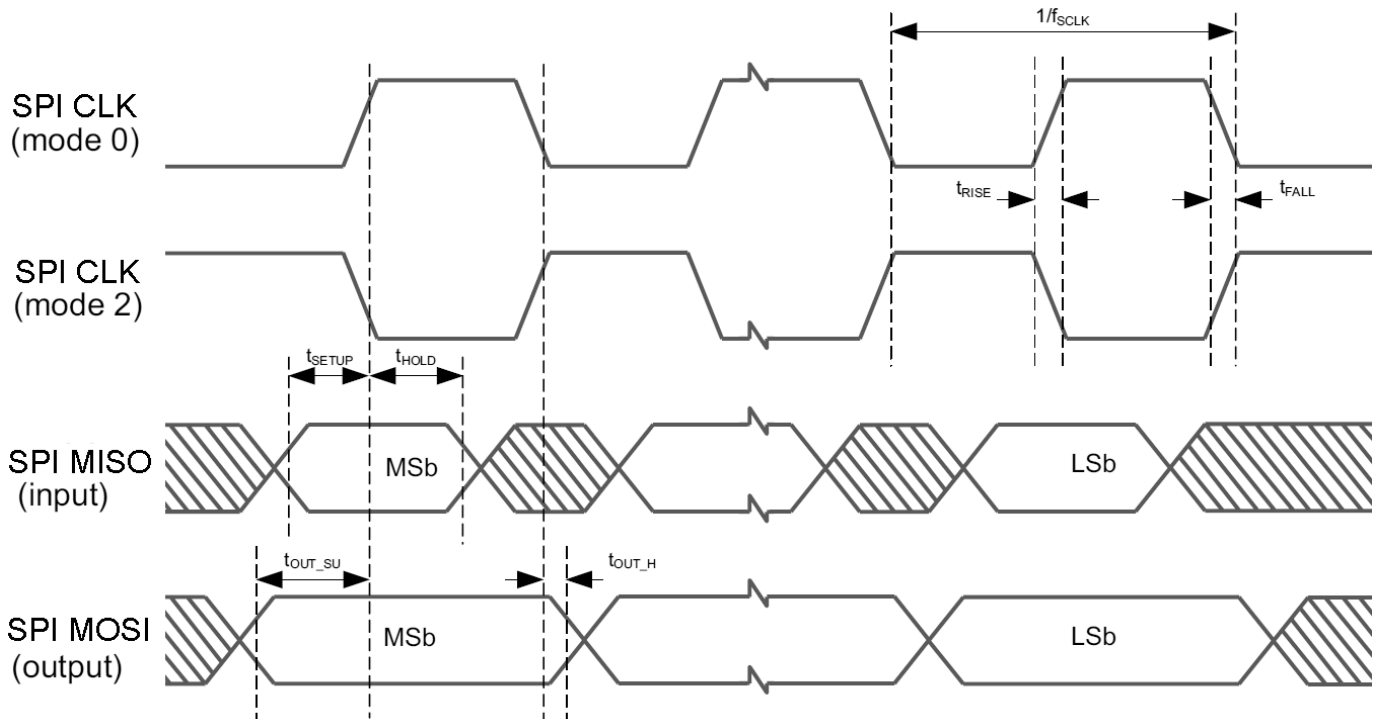


Figure 10. SPI Master Timing Diagram, Modes 1 and 3

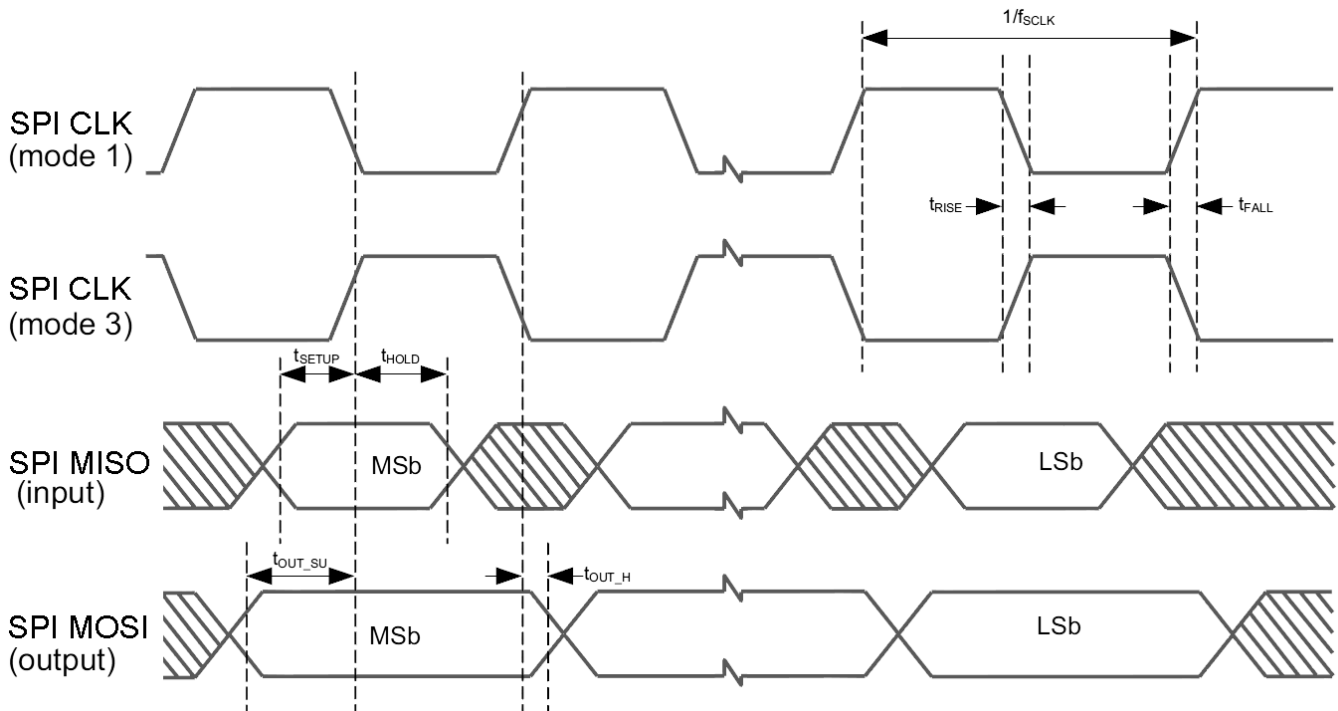


Figure 11. SPI Slave Timing Diagram, Modes 0 and 2

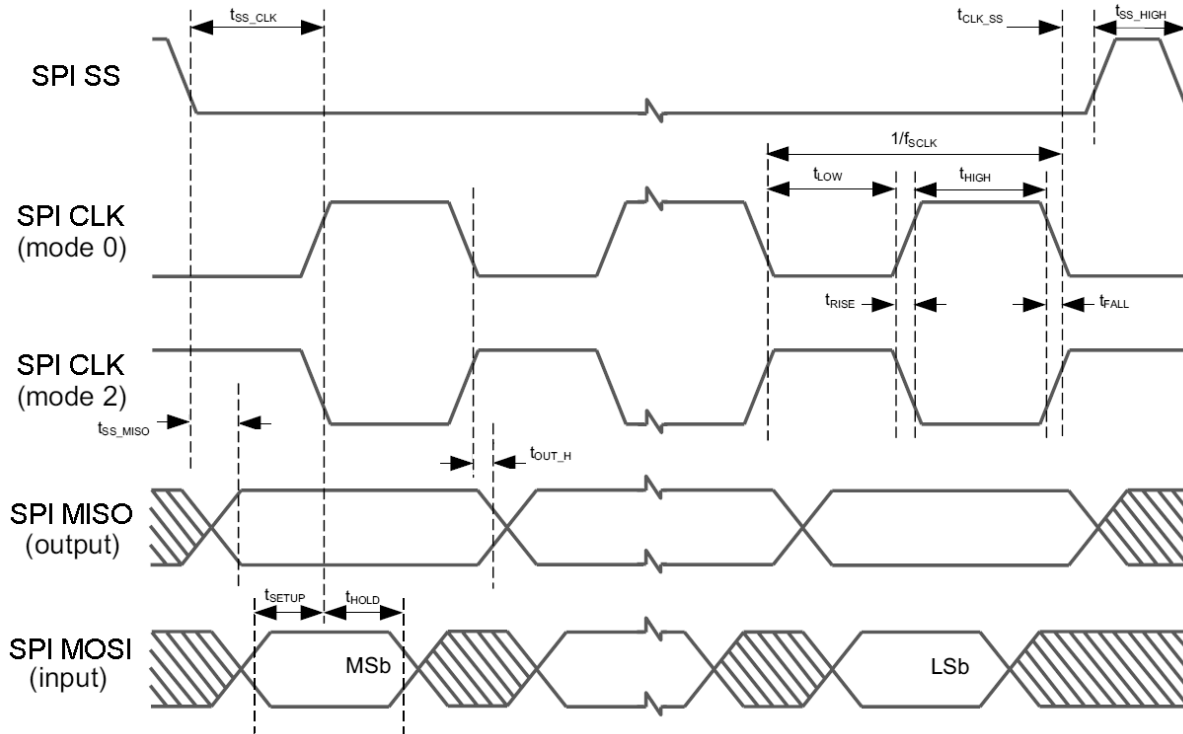
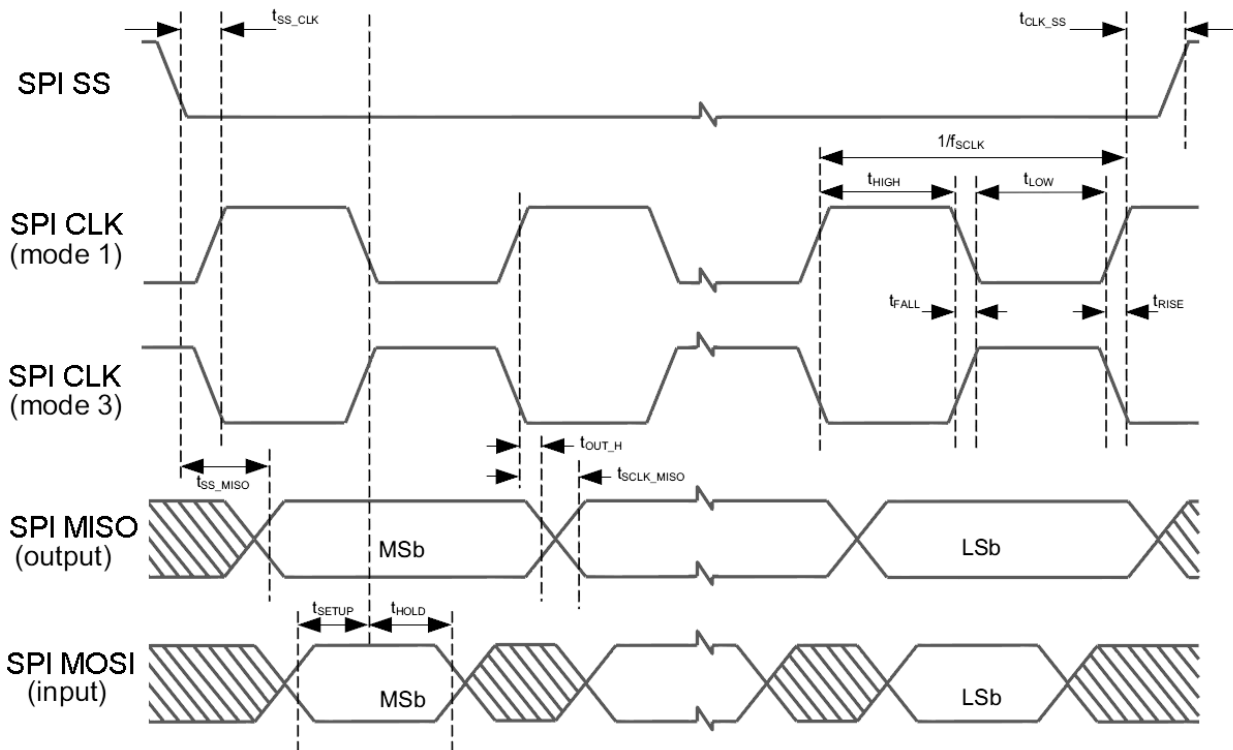


Figure 12. SPI Slave Timing Diagram, Modes 1 and 3



AC Comparator Specifications

The device includes two general purpose comparators, using internal or external signals from the analog mux bus. Table 16 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 16. AC Low Power Comparator Specifications

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|------------------|---|--|-----|-----|-----|-------|
| T _{LPC} | Comparator response time, 50 mV overdrive | 50 mV overdrive does not include offset voltage. | – | – | 100 | ns |

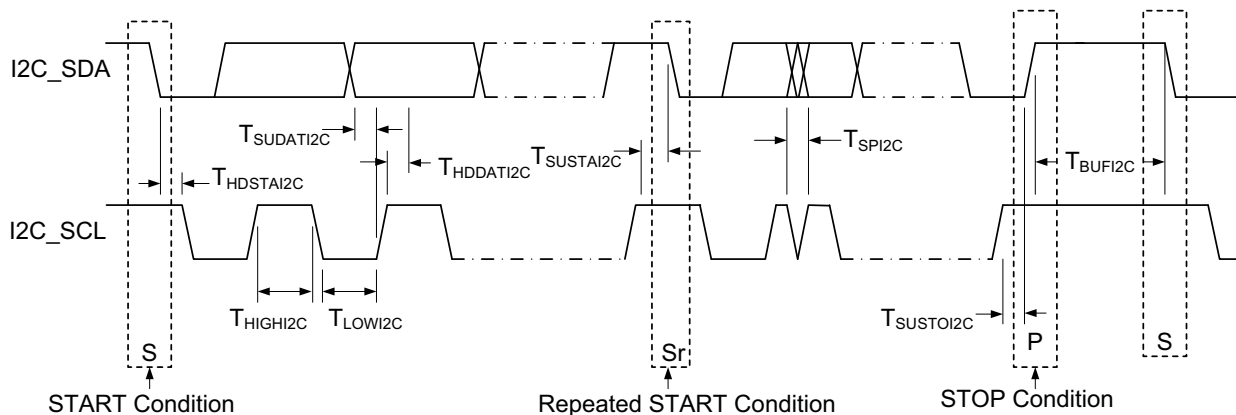
AC I²C Specifications

The device includes an I²C slave block with an input filter that suppresses spikes and glitches on the clock and data lines. The block can be configured for standard or fast mode. Table 17 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 17. AC Characteristics of the I²C SDA and SCL Pins

| Symbol | Description | Standard Mode | | Fast Mode | | Units |
|------------------------|---|---------------|-----|---------------------|-----|-------|
| | | Min | Max | Min | Max | |
| F _{SCL I2C} | I2C_SCL clock frequency | 0 | 100 | 0 | 400 | kHz |
| T _{HDSTAI2C} | Hold time for START and Repeated START condition | 4.0 | – | 0.6 | – | μs |
| T _{LOWI2C} | LOW period of the I2C_SCL clock | 4.7 | – | 1.3 | – | μs |
| T _{HIGHI2C} | HIGH period of I2C_SCL clock | 4.0 | – | 0.6 | – | μs |
| T _{SUSTA I2C} | Setup time for a START and Repeated START condition | 4.7 | – | 0.6 | – | μs |
| T _{HDDAT I2C} | Data hold time | 0 | – | 0 | – | μs |
| T _{SUDAT I2C} | Data setup time | 250 | – | 100 ^[14] | – | ns |
| T _{SUSTO I2C} | Setup time for STOP condition | 4.0 | – | 0.6 | – | μs |
| T _{BUFI2C} | Bus free time between a STOP and START condition | 4.7 | – | 1.3 | – | μs |
| T _{SPI2C} | Pulse width of spikes that are suppressed by the input filter | – | – | 0 | 50 | ns |

Figure 13. Timing for Fast/Standard Mode on the I²C Bus



Note

14. A Fast-Mode I2C-bus device can be used in a Standard Mode I2C-bus system, but the requirement $t_{SUDAT I2C} \geq 250$ ns must then be met. This automatically is the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SUDAT I2C} = 1000 + 250 = 1250$ ns (according to the Standard-Mode I2C-bus specification) before the SCL line is released.

AC USB Specifications

The device includes an integrated full-speed USB block. [Table 18](#) lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 18. AC Characteristics – USB Data Timing Specifications

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|--------|--|--------------------|----------|-----|-----------|-------|
| Tdrate | Full-speed data rate | Average bit rate | 12–0.25% | 12 | 12 + 0.25 | MHz |
| Tdjr1 | Receiver data jitter tolerance | To next transition | –18.5 | 0 | 18.5 | ns |
| Tdjr2 | Receiver data jitter tolerance | To pair transition | –9 | – | 9 | ns |
| Tudj1 | Driver differential jitter | To next transition | –3.5 | – | 3.5 | ns |
| Tudj2 | Driver differential jitter | To pair transition | –4.0 | – | 4.0 | ns |
| Tfdeop | Source jitter for differential transition | To SE0 transition | –2 | – | 5 | ns |
| Tfeopt | Source SE0 interval of EOP | | 160 | – | 175 | ns |
| Tfeopr | Receiver SE0 interval of EOP | | 82 | – | – | ns |
| Tfst | Width of SE0 interval during differential transition | | – | – | 14 | ns |

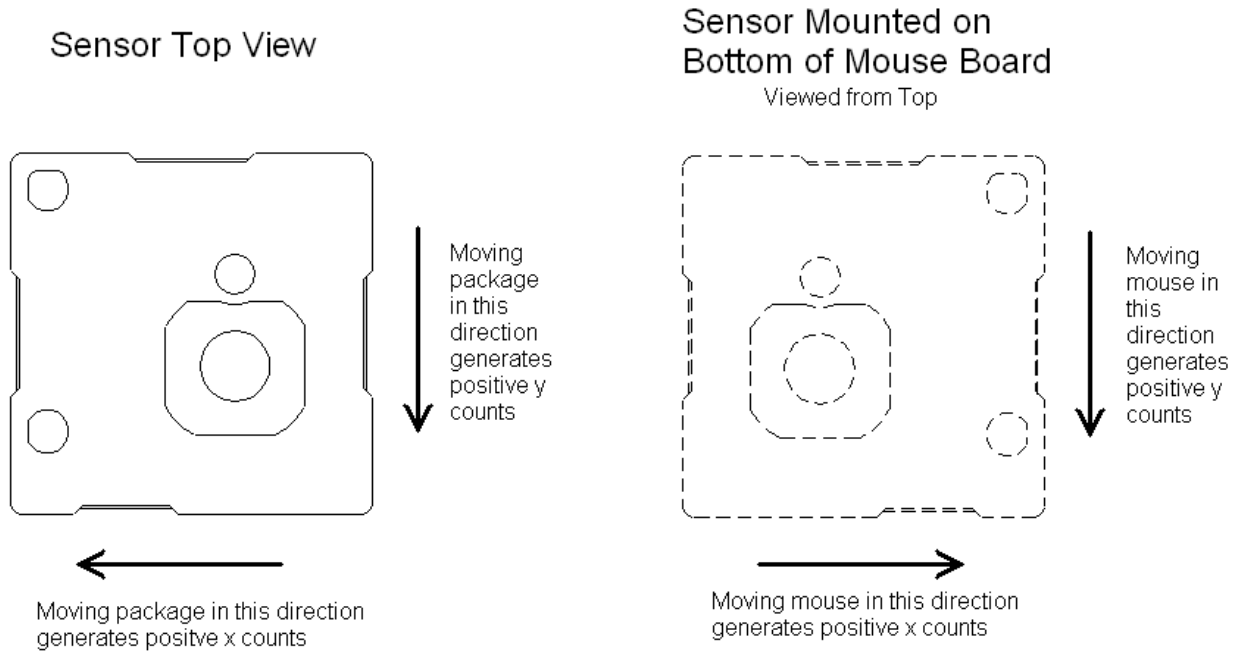
Table 19. AC Characteristics – USB Driver

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|--------|---------------------------------|-------------|-----|-----|-----|-------|
| Tr | Transition rise time | 50 pF | 4 | – | 20 | ns |
| Tf | Transition fall time | 50 pF | 4 | – | 20 | ns |
| TR | Rise/fall time matching | 0.8V - 2.5V | 90 | – | 111 | % |
| Vcrs | Output signal crossover voltage | | 1.3 | – | 2.0 | V |

Orientation of Axes

Figure 16 describes the relationship between the package and the x/y axes when using the API provided by Cypress's PSoC Designer software. Note that there is a 90-degree rotation between the orientation below and the orientation described in the register section of the [Technical Reference Manual](#). If PSoC Designer is not used, the application firmware should read and invert the Y count register for X data, and read the X count register for Y data.

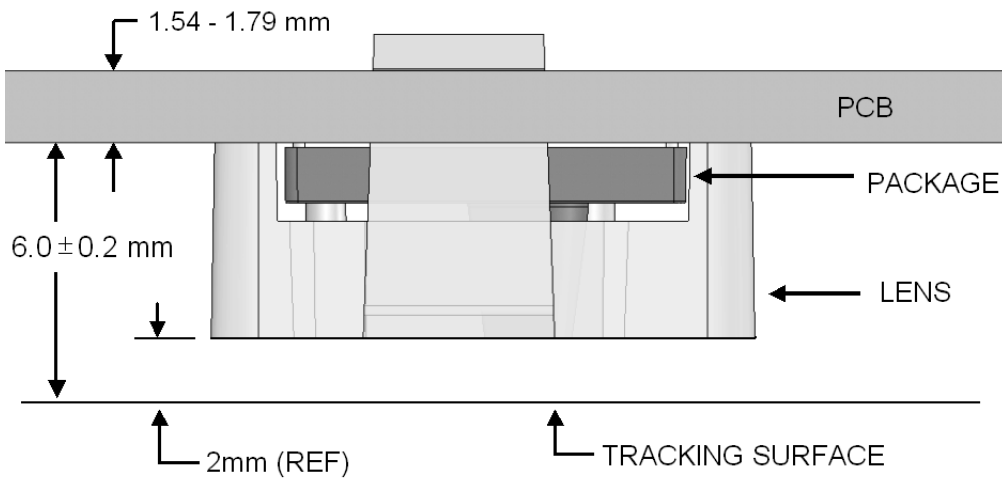
Figure 16. Sensor Orientation



PCB Mounting Height and Thickness

Figure 17 shows the recommended thickness and mounting height of the PCB above the tracking surface.

Figure 17. PCB Height and Thickness



Thermal Impedances

Table 20. Thermal Impedances per Package

| Package | Typical θ_{JA} ^[15] |
|-------------------------|---------------------------------------|
| 42 PQFN ^[16] | 24 °C/W |

Solder Reflow Peak Temperature

Following is the minimum solder reflow peak temperature to achieve good solderability.

Table 21. Solder Reflow Peak Temperature

| Package | Minimum Peak Temperature ^[17] | Maximum Peak Temperature |
|---------|--|--------------------------|
| 42 PQFN | 240°C | 260°C |

Notes

15. $T_J = T_A + \text{Power} \times \theta_{JA}$.

16. To achieve the thermal impedance specified for the QFN package, the center thermal pad must be soldered to the PCB ground plane.

17. Higher temperatures may be required based on the solder melting point. Typical temperatures for solder are $220 \pm 5^\circ\text{C}$ with Sn-Pb or $245 \pm 5^\circ\text{C}$ with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications. For a recommended soldering profile, refer to Application Note 49035, *Manufacturing Considerations for the Ovation-ONS™ Laser Navigation System-on-Chip*.

Laser Safety Considerations

The CYONS2110 laser navigation SoC and the CYONSLENS2000 lens are designed and tested to enable manufacturers to achieve eye safety certification with minimal effort. This section provides guidelines for complying with the Class 1 emission requirements of IEC/EN 60825-1.

When installed and operated in accordance with all requirements in this datasheet, the kit consisting of the CYONS2110 Laser Navigation SoC and CYONSLENS2000 satisfies CDRH 21 CFR 1040 per Laser Notice #50 and IEC/EN 60825-1 Class 1.

Laser Output Power

The CYONS2110 sensor package contains an integrated VCSEL and drive circuitry. Before shipping, Cypress adjusts the laser output power to eye-safe levels, taking into account specified variations in supply voltage, temperature, lens transmission, and VCSEL polarization, and factors such as VCSEL aging and test equipment accuracy. The output remains within eye-safe limits under reasonably foreseeable single-faults, as required by the IEC standard.

From the perspective of a manufacturer, laser emission remains within the Class 1 limit, as defined in IEC 60825-1, Edition 2, 2007, provided the following requirements are met.

- The supply voltage applied to pins DVDD and AVDD of the SoC must be in the range of 2.7 to 3.6V.
- The operating temperature must be between 5 and 45 °C.
- The laser output power must not be increased by any means, including but not limited to firmware, hardware, or mechanical modifications to the sensor or lens.
- The mechanical housing must be designed such that the CYONSLENS2000 cannot be removed by the user.
- The device firmware must initialize the VCSEL driver as described in the “VCSEL Driver” chapter of the [OvationONS II technical reference manual](#) or by using the NAV or LaserNAV User Modules in Cypress’s PSoC Designer software.

The manufacturer must ensure these conditions are always met and demonstrate end-product compliance to the appropriate regulatory standards.

Laser Output Power Test Procedure

To verify the laser output level, follow the steps shown in the “VCSEL Power Calibration and Verification” section of the [technical reference manual](#).

Registration Assistance

The mouse or end-product supplier is responsible for certifying the end-use product with respect to the drive voltage, manuals and labels, and operating temperature specifications. Additionally, for products sold in the US, a CDRH report must be filed for each model produced, and test and inspection of the product’s characteristics as they relate to laser safety and the CDRH requirements must be performed.

When filing a report with the CDRH, the supplier can refer to the product report filed by Cypress for the CYONS2xxx family of products. The Cypress report is based on the previously-noted limits for voltage and temperature, and describes how the sensor design includes consideration of drive circuit failures, laser output variation with temperature, drive circuit variation with temperature and voltage, polarization sensitivity of molded optics, and measurement uncertainties.

Cypress can provide assistance to customers who wish to obtain registration. Supporting documentation, including a verification test procedure to demonstrate end-product compliance with IEC and CDRH requirements is available. For further information, contact a Cypress representative.

Development Tool Selection

This section presents the development tools available for all current PSoC device families including the CYONS2110.

Software

PSoC Designer

At the core of the PSoC development software suite is PSoC Designer, used to generate PSoC firmware applications. PSoC Designer is available free of charge at <http://www.cypress.com/psocdesigner> and includes a free C compiler with version Service Pack 4.5 or later.

PSoC Programmer

Flexible enough to be used on the bench in development, yet suitable for factory programming, PSoC Programmer works either as a standalone programming application or it can operate directly from PSoC Designer. PSoC Programmer software is compatible with both PSoC ICE-Cube In-Circuit Emulator and PSoC MiniProg. PSoC programmer is available free of charge at <http://www.cypress.com/psocprogrammer>.

Mouse Design Kits

Two kits featuring the OvationONS II family of products are available. The reference design kit provides a complete hardware, firmware, and software solution, ready for production. The demonstration kit provides tested hardware and firmware that demonstrate the capabilities of the OvationONS II device.

- CY4631 Wired Mouse Reference Design Kit
- Wireless Mouse Demonstration Kit

Development Kits

You can purchase the development kits from the Cypress Online Store.

CY3215-DK Basic Development Kit

The [CY3215-DK](#) kit enables prototyping and development with PSoC Designer. This kit supports in-circuit emulation and the software interface enables users to run, halt, and single step the processor and view the content of specific memory locations. Advanced emulation features are also supported through PSoC Designer. The kit includes:

- PSoC Designer software CD
- ICE-Cube In-Circuit Emulator
- ICE Flex-Pod for CY8C29x66 family
- Cat-5 adapter
- Mini-Eval programming board
- 110 ~ 240 V power supply, Euro-Plug adapter
- iMAGEcraft C compiler (registration required)
- ISSP cable
- USB 2.0 cable and Blue Cat-5 cable
- Two CY8C29466-24PXI 28-PDIP chip samples

Evaluation Tools

You can purchase the evaluation tools from the Cypress Online Store.

CY3210-MiniProg1

The [CY3210-MiniProg1 kit](#) enables a user to program PSoC devices using the MiniProg1 programming unit. The MiniProg1 is a small, compact prototyping programmer that connects to the PC via a provided USB 2.0 cable. The kit includes:

- MiniProg programming unit
- MiniEval socket programming and evaluation board
- 28-pin CY8C29466-24PXI PDIP PSoC device sample
- 28-pin CY8C27443-24PXI PDIP PSoC device sample
- PSoC Designer software CD
- Getting Started guide
- USB 2.0 cable

CY3210-PSoCEval1

The [CY3210-PSoCEval1 kit](#) features an evaluation board and the MiniProg1 programming unit. The evaluation board includes an LCD module, potentiometer, LEDs, and plenty of bread-boarding space to meet all of your evaluation needs. The kit includes:

- Evaluation board with LCD module
- MiniProg programming unit
- 28-pin CY8C29466-24PXI PDIP PSoC device sample (2)
- PSoC Designer software CD
- Getting Started guide
- USB 2.0 cable

CY3214-PSoCEvalUSB

The [CY3214-PSoCEvalUSB evaluation kit](#) features a development board for the CY8C24794-24LFXI PSoC device. Special features of the board include both USB and capacitive sensing development and debugging support. This evaluation board also includes an LCD module, potentiometer, LEDs, an annunciator and plenty of bread boarding space to meet all of your evaluation needs. The kit includes:

- PSoCEvalUSB board
- LCD module
- MiniProg programming unit
- Mini USB cable
- PSoC Designer and example projects CD
- Getting Started guide
- Wire pack

Device Programmers

You can purchase the device programmers from the Cypress Online Store.

CY3216 Modular Programmer

The [CY3216 Modular Programmer kit](#) features a modular programmer and the MiniProg1 programming unit. The modular programmer includes three programming module cards and supports multiple Cypress products. The kit includes:

- Modular programmer base
- Three programming module cards
- MiniProg programming unit
- PSoC Designer software CD
- Getting Started guide
- USB 2.0 cable

CY3207ISSP In-System Serial Programmer (ISSP)

The [CY3207ISSP](#) is a production programmer. It includes protection circuitry and an industrial case that is more robust than the MiniProg in a production-programming environment.

Note CY3207ISSP needs special software and is not compatible with PSoC Programmer.

The kit includes:

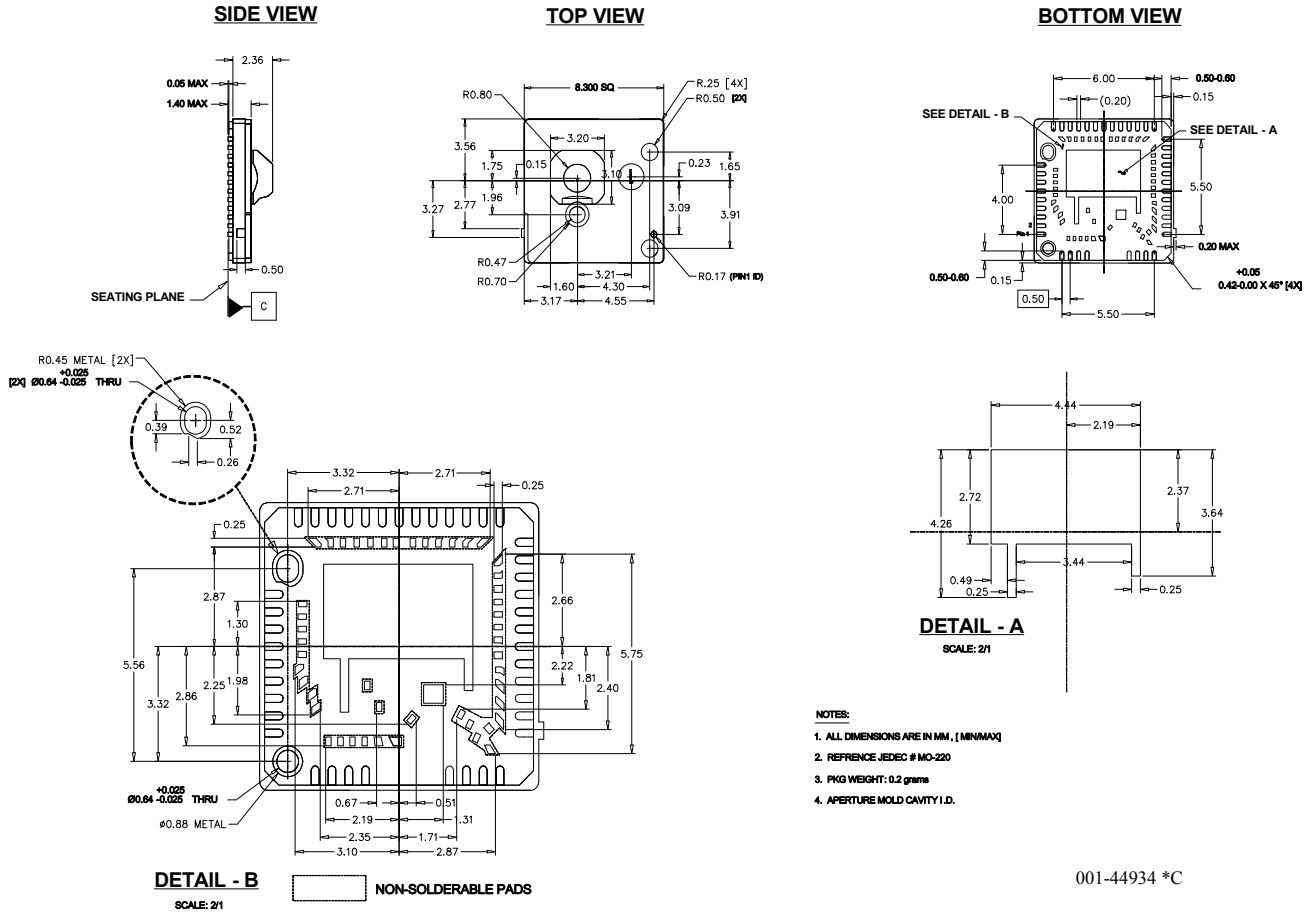
- CY3207 programmer unit
- PSoC ISSP software CD
- 110 ~ 240 V power supply, Euro-Plug adapter
- USB 2.0 cable

Third Party Tools

Several tools have been specially designed by third-party vendors to accompany PSoC devices during development and production. Specific details for each of these tools are found at <http://www.cypress.com>.

Package Diagrams

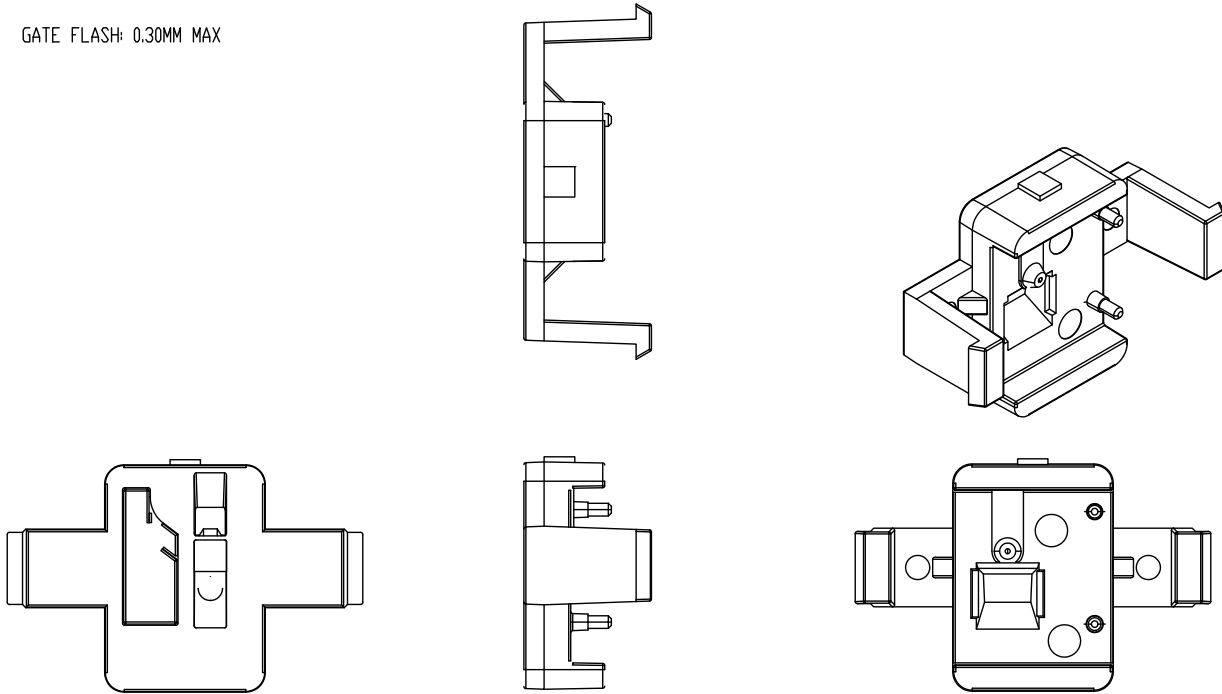
Figure 18. QFN Package



001-44934 *C

Figure 19. Lens

GATE FLASH: 0.30MM MAX



001-44677 *B

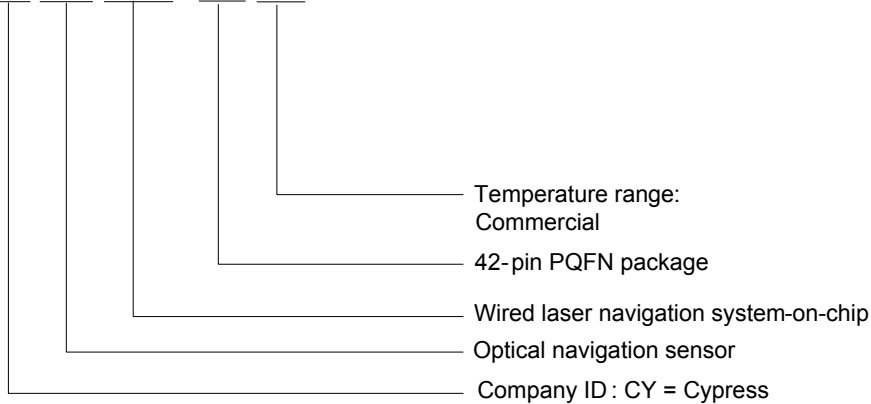
Ordering Information

The CYONS2110 and CYONSLENS2000 are sold separately. When placing orders, order both part numbers

| Part Number | Package | Application |
|-----------------|--------------------|-------------------------------------|
| CYONS2110-LBXC | 42 Pin PQFN | High Performance wired and wireless |
| CYONSLENS2000-C | Lens - 4 mm height | Molded optic |

Ordering Code Definition

CYONS XXXX-XXX C



Document Conventions

Acronyms Used

Table 22 lists the acronyms used in this document.

Units of Measure

The units of measure in Table 23 lists the abbreviations used to measure the devices.

Numeric Naming

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase 'h' (for example, '14h' or '3Ah'). Hexadecimal numbers may also be represented by a '0x' prefix, the C coding convention. Binary numbers have an appended lowercase 'b' (for example, '01010100b' or '01000011b'). Numbers not indicated by an 'h', 'b', or '0x' are decimal.

Table 22. Acronyms

| Acronym | Description | Acronym | Description |
|------------------|--|---------|--|
| AC | Alternating Current | LDO | Low Drop Out (regulator) |
| ADC | Analog to Digital Converter | LED | Light Emitting Diode |
| API | Application Programming Interface | LPC | Low Power Comparator |
| CDRH | Center for Devices and Radiological Health | LSb | Least-significant Bit |
| CPI | Counts per Inch | LVD | Low Voltage Detect |
| CPU | Central Processing Unit | M8C | Cypress' 8-bit CPU Core |
| DAC | Digital to Analog Converter | MCU | Microcontroller Unit |
| DC | Direct Current | MIPS | Million Instructions per Second |
| DSP | Digital Signal Processor | MSb | Most-significant Bit |
| ESD | Electrostatic Discharge | MUX | Multiplexer |
| GND | Ground | PC, PCB | Printed Circuit, Printed Circuit Board |
| GPIO | General Purpose I/O | PDIP | Plastic Dual In-Line Package |
| HEX | Hexadecimal | PGA | Programmable Gain Amplifier |
| Hi-Z | High Impedance | POR | Power On Reset |
| I ² C | Inter-Integrated Circuit (bus) | PQFN | Plastic Quad Flat No-Leads (package) |
| ICE | In-circuit Emulator | PSoC | Programmable System-on-Chip |
| IDAC | DAC-Controlled Current Source | PSRR | Power Supply Rejection Ratio |
| IDE | Integrated Development Environment | PWM | Pulse Width Modulator |
| IEC | International Electrotechnical Commission | QFN | Quad Flat No-Leads (package) |
| ILO | Internal Low Speed Oscillator | SoC | System on Chip |
| IMO | Internal Main Oscillator | SPI | Serial Peripheral Interface (bus) |
| I/O | Input/Output | SRAM | Static Random Access Memory |
| JEDEC | Joint Electron Devices Engineering Council | USB | Universal Serial Bus |
| LCD | Liquid Crystal Display | VCSEL | Vertical Cavity Surface Emitting Laser |

Table 23. Units of Measure

| Symbol | Unit of Measure | Symbol | Unit of Measure |
|--------|-------------------------|--------|-----------------|
| °C | degree Celsius | μV | microvolts |
| g | acceleration of gravity | mA | milliampere |
| KB | 1024 bytes | ms | millisecond |
| in/s | inches per second | mV | millivolt |
| kHz | kilohertz | nH | nanohenry |
| kΩ | kilohm | nm | nanometer |
| kV | kilovolt | ns | nanosecond |
| MHz | megahertz | Ω | ohm |
| μA | microampere | pF | picofarad |
| μF | microfarad | pp | peak-to-peak |
| μH | microhenry | V | volt |
| μs | microsecond | W | watt |

Document History Page

| Document Title: CYONS2110 OvationONS™ II Wired / Wireless Laser Navigation System-on-Chip | | | | |
|---|---------|-----------------|-----------------|--|
| Document Number: 001-44048 | | | | |
| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
| ** | 2261927 | FJZ | See ECN | CYONS2110 New Data Sheet. |
| *A | 2580125 | FJZ | 10/07/08 | Extensive Updates |
| *B | 2769396 | FJZ/AESA | 25/09/09 | Updated Getting Started and Development Tools sections Updated thermal impedance, wireless kit info, Flash specs, storage temperature, I2C footnote, external mode powering, reference schematic, power specifications, pin table, and c compiler information. |
| *C | 2889331 | FJZ | 03/09/10 | Added Table of Contents. Updated package diagram and sales links. |
| *D | 2903558 | FJZ | 04/20/10 | Update LVD, USB, SPI Master and SPI Slave specs, numerous minor updates for improved clarity and consistency |
| *E | 2936335 | MMCY | 05/24/2010 | Updated content to match the new template and style guide. No technical updates. |
| *F | 3092209 | FJZ | 11/22/2010 | Corrected error in Pin Description . Removed invalid reference to application note in Registration Assistance . |
| *G | 3126503 | FJZ | 01/03/2011 | Updated Figure 19 . Changed posting to external web |

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer’s representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

- Automotive cypress.com/go/automotive
- Clocks & Buffers cypress.com/go/clocks
- Interface cypress.com/go/interface
- Lighting & Power Control cypress.com/go/powerpsoc
cypress.com/go/plc
- Memory cypress.com/go/memory
- Optical & Image Sensing cypress.com/go/image
- PSoC cypress.com/go/psoc
- Touch Sensing cypress.com/go/touch
- USB Controllers cypress.com/go/USB
- Wireless/RF cypress.com/go/wireless

PSoC Solutions

- psoc.cypress.com/solutions
- PSoC 1 | PSoC 3 | PSoC 5

© Cypress Semiconductor Corporation, 2008-2011. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and/or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.