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APPLICATION INFORMATION for KA8514

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APPLICATION Eng.

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/. General Information

This application note describes the KA8514 information required for the pager design. The KA8514 is especially designed for FM IF receiver with RSSI function.

//. IF Detector Description

The KA8514 consists of 2nd mixer, discriminator, low-pass filter, data comparator, battery saving circuit, low battery detector , voltage regulator and RSSI function. AF signal extracted from the discriminatorpart, goes to the low-pass filter and FSK signal extracted by the comparator, goes to decoder.

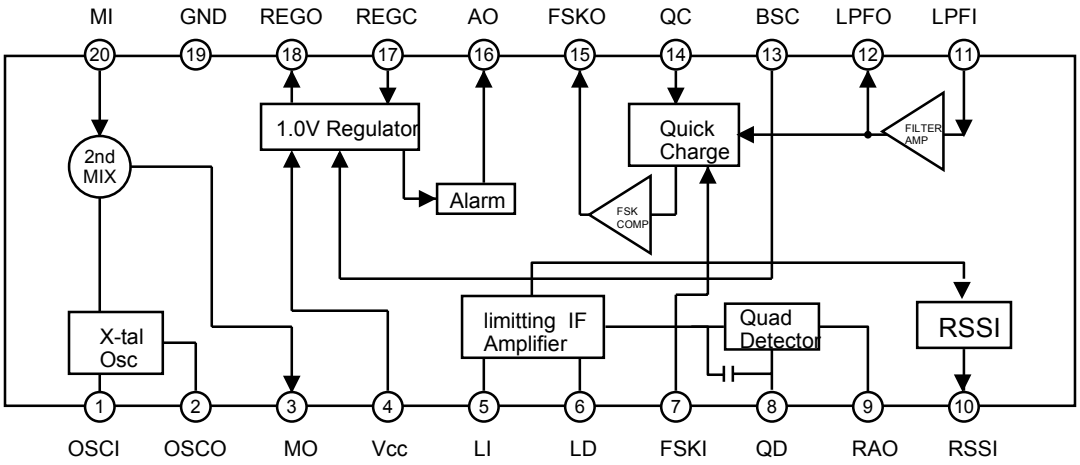


Fig 1. KA8514 Block Diagram

///. Internal Circuit & Function Description

1. Mixer input Circuit

2nd Mixer operating frequency is 10 ~ 50MHz , but 21.4MHz is used for Mixer input. Local oscillation circuit is colpitts type. 455KHz signal is made from the 2nd Mixer outputs to the pin 3 (M0). Conversion gain of 2nd Mixer is 13dB. Because Mixer output impedance is 2kΩ, it should be used the same impedance 455KHz filter.

To improve the receiving sensitivity, filter impedance matching is important. Also, KA8514 includes the 22kΩ bias resistor, so no need the external resistor between the pin 1 and pin 18 (REGO).

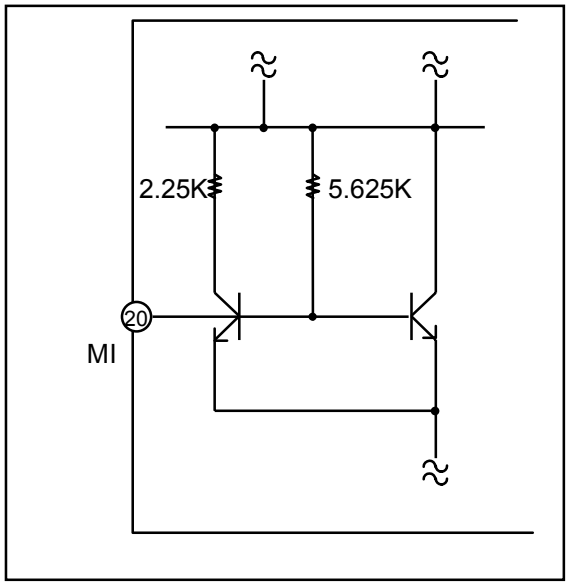


Fig 2. Mixer Input Internal Circuit

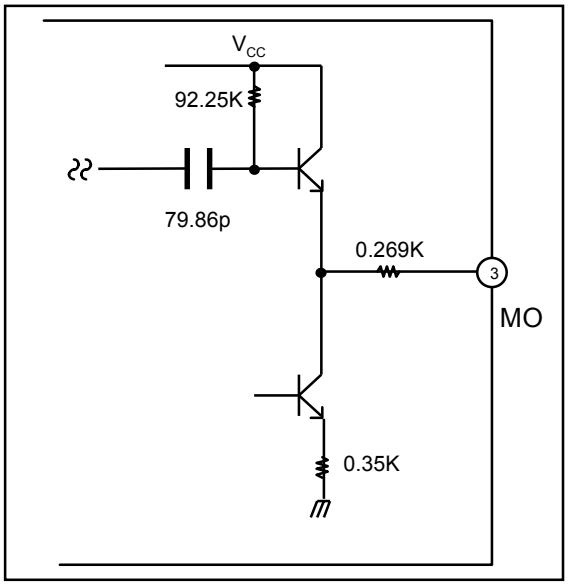


Fig 3. Mixer Output Circuit

* Mixer output impedance

Ro(mix) = (92.25K/ β) + re + 0.269K = 1.8Kohm

2. limitting IF Amp

The output of 2nd Mixer conversion gain is ≒ 12.8dB. The 2nd mixer output signal goes to IF amp (pin 5) after passing through the 455KHz ceramic filter. The voltage gain of limitting amp is 76.48dB.

The limitter Amp input impedance is approximately 2kΩ. The voltage of the pin 5 & pin 6 becomes the same level because of differential amplifier.

3. Quadrature Detector (pin 8)

The detector is a quadrature type. The 455KHz discriminator circuit must be provided externally. Damping resistor determines the peak separation of detector and the audio sensitivity.

4. Battery - Saving Function

This pin can be used to battery saving to conserve the power. Because BSC (pin 13) is the base of the NPN TR , it can be driven by the CMOS output.

BSC state	IC Operation	Current Consumption
High	Normal Operation	1.1mA
Low	Operation Stop	0.01㎂

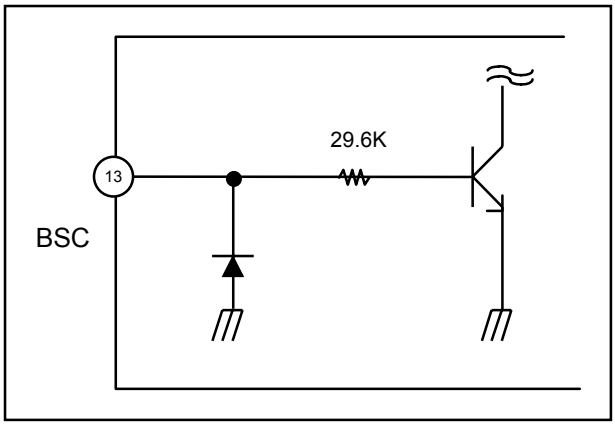


Fig 4. Battery Saving Circuit

5. Low Battery Dectection

The low battery detection circuit is composed of NPN open collector output. When the Vcc voltage drops below 1.05V, this pin becomes the high level. Typically, this pin should be connected with pull-up resistor 100kΩ.

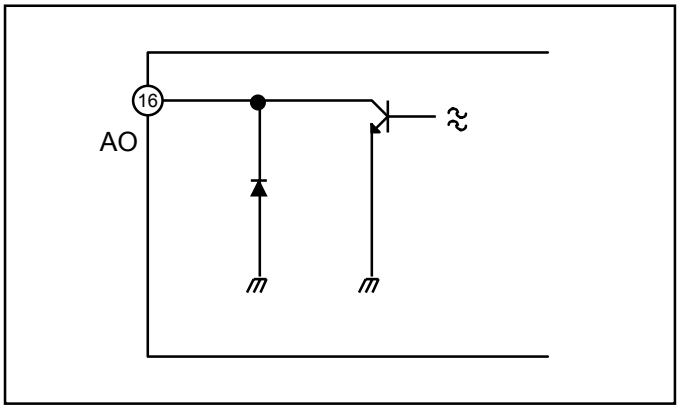


Fig 5. Low Battery Detector Circuit

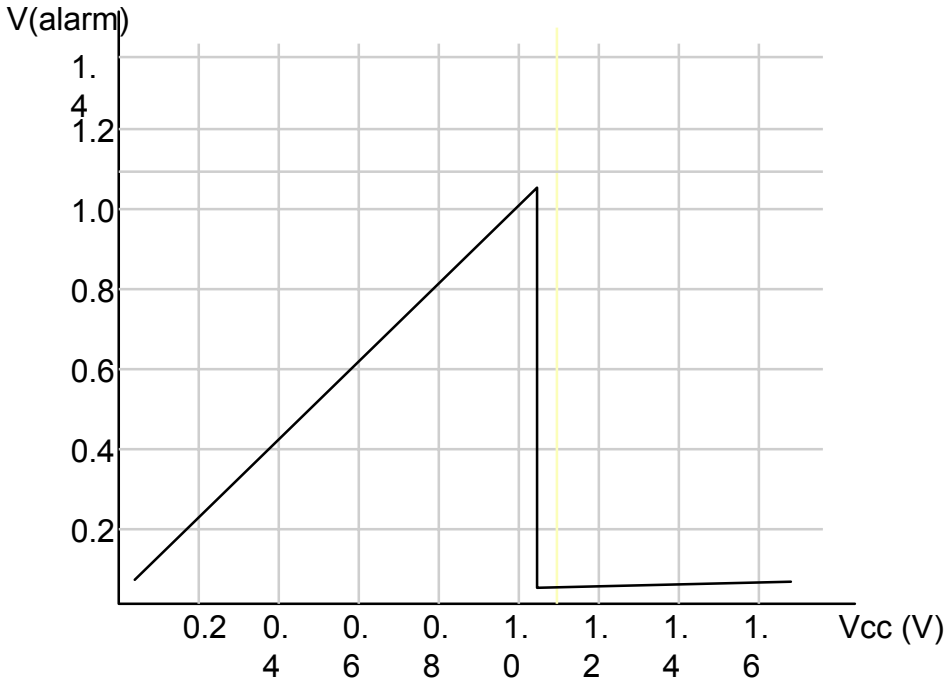


Fig 6. Vcc Vs Low Battery Detection Graph

6. Local Oscillator Circuit

This circuit is operating by the 20.945MHz crystal oscillator connected between pin 1 and pin 2. The oscillator bias voltage is provided by internal resistor (22kΩ). There is no need to using a external resistor (22kΩ) between pin 1 and pin 18 (REGO). On the contrary, in case of Competitor, it must use the external resistor (22kΩ) to operate this oscillation block.

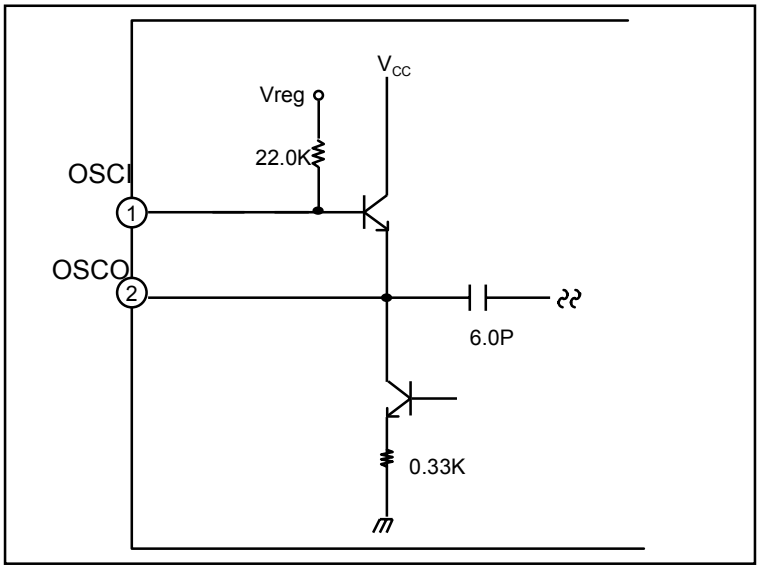


Fig 7. Crystal Oscillator circuit

7. 455KHz Ceramic Filter

The output impedance of pin 3 (Mix out) is ≒ 2kΩ, and input impedance of pin 5 (Limiting input) is ≒ 2kΩ. When use the ceramic filter, impedance matching is most important to obtain the high receiving sensitivity. According to the test, during the soldering the ceramic filter, we found that irregular spark voltage might be happen at the filters I/O pin. So the user should be aware of this , how to prevent it

When you select a filters maker, we would like to recommend the credible filter such as MURATA (vendor). And the following graph shows the testing method and result.

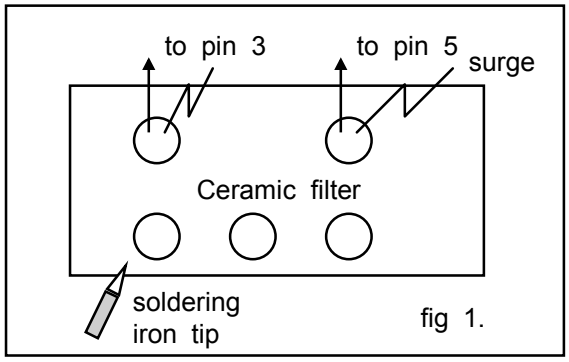
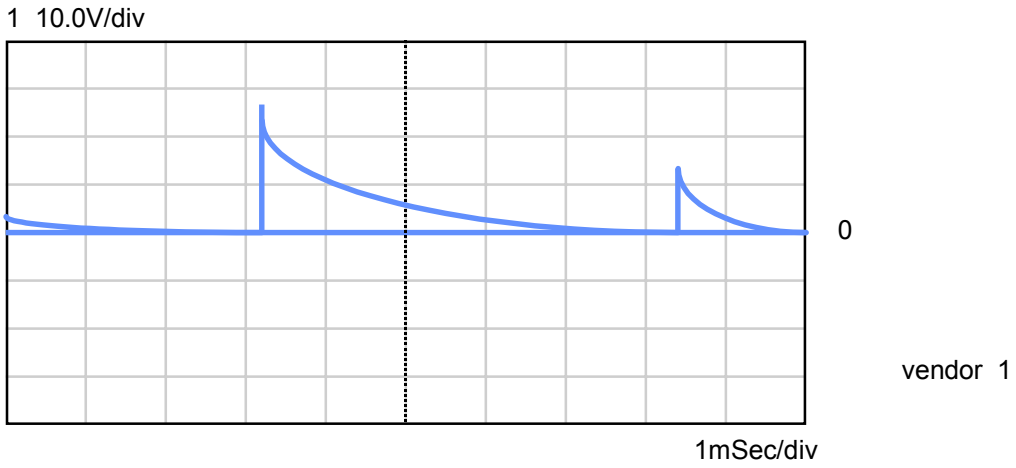


Fig 8. 455KHz Ceramic Filter Soldering



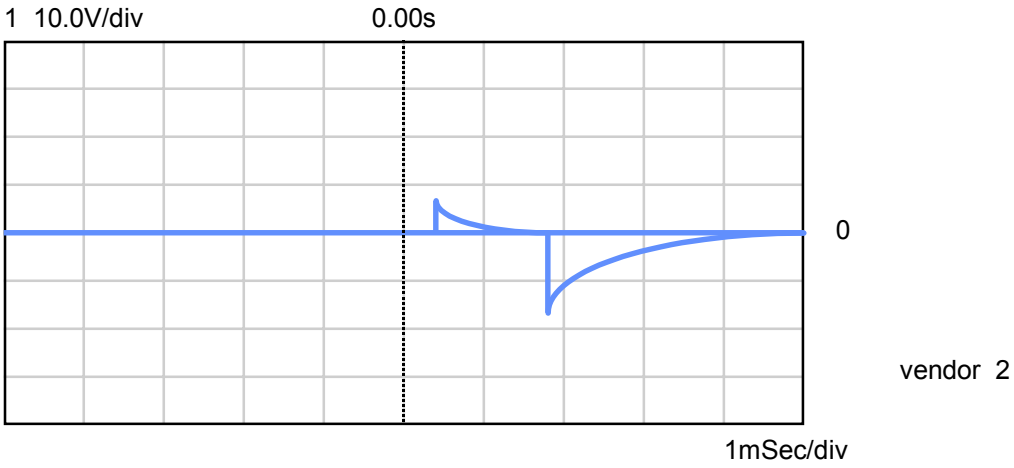


Fig 9. Surge voltage graph from the filter

8. RSSI (Received Signal Strength Indicator)

The DC level of this pin is determined by the value of RF input level. The signal strength output is derived from the summed stage current of the limitting amplifiers.

The RSSI pin may be used many ways, such as : AGC, level meter and triggering of the comparator block. The output DC level can be adjust by the external resistor connected to the GND.

The DC level adjusting range is 0.10V ~ 1.16V at the -110dBm ~ 20dBm (RF input level). The input resistance is ≒ 100kΩ.

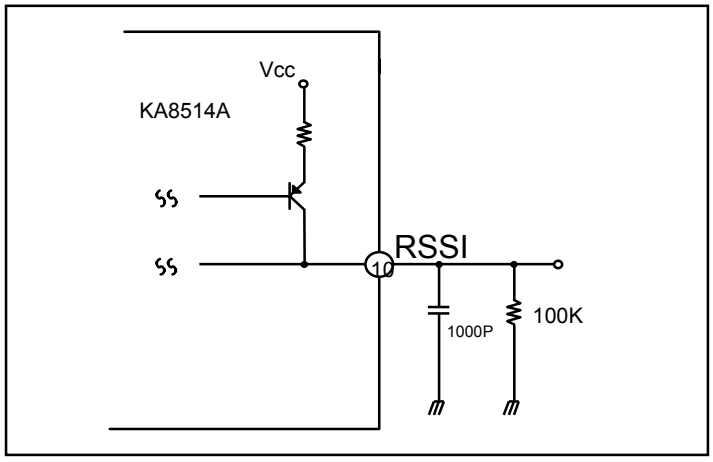


Fig 10. RSSI Circuit

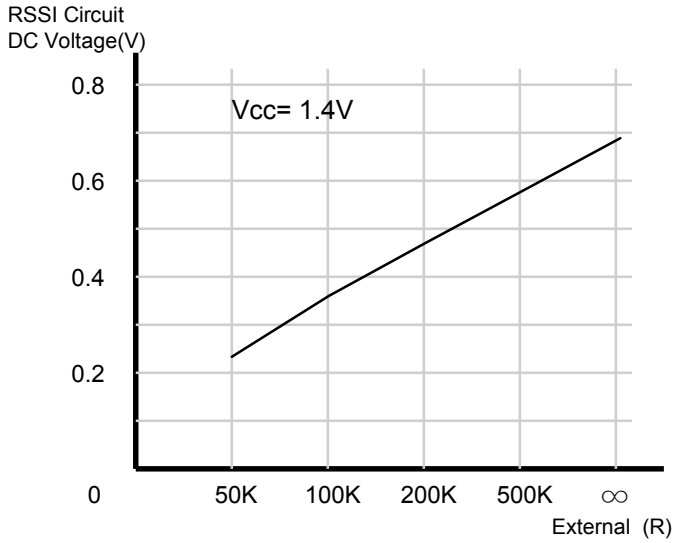


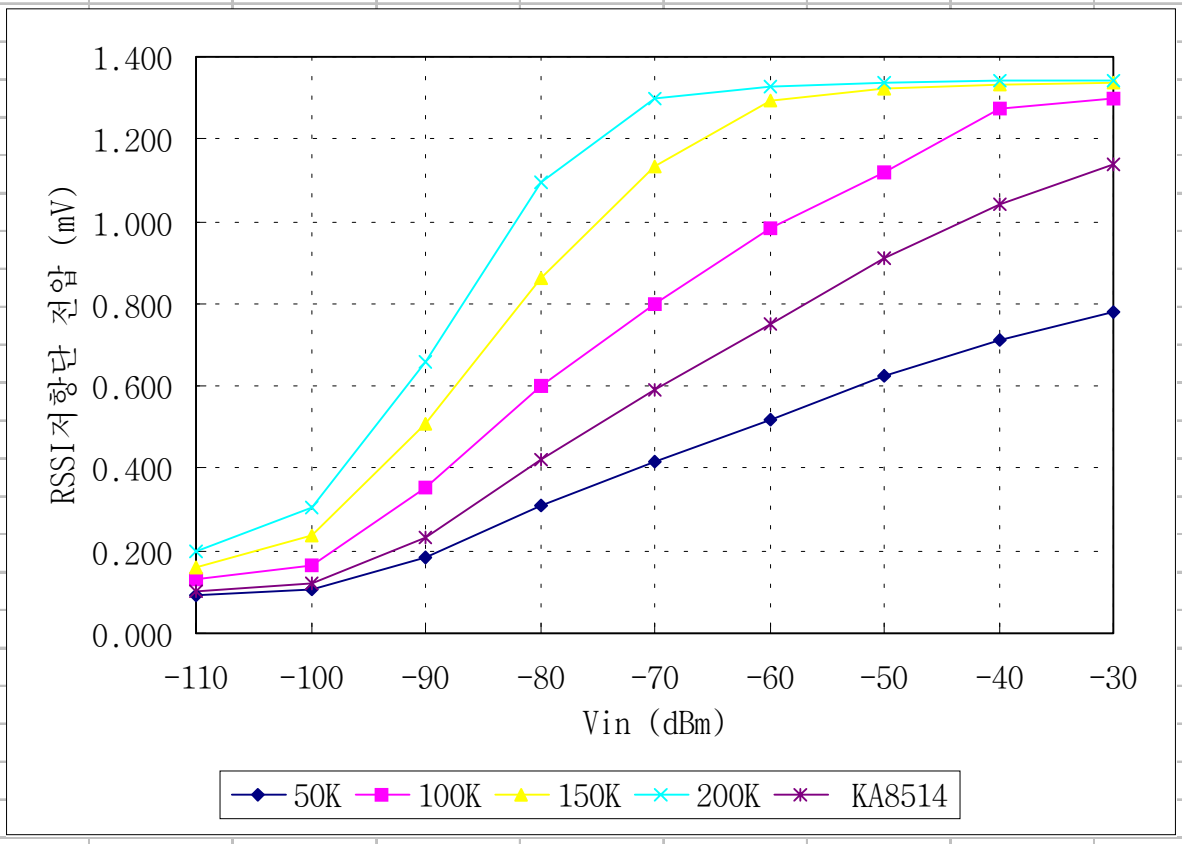
Fig 11. RSSI DC level Vs external resistor at -60dBm.

■ KA8514/14A RSSI Characteristic

(Test condition : Fin = 21.4 MHz , Vcc = 1.4V)

(Unit:mV)

Vin	KA8514A (RSSI Resistor Value)				
(dBm)	50K	100K	150K	200K	KA8514
-110	0.093	0.129	0.162	0.200	0.102
-100	0.108	0.167	0.236	0.306	0.120
-90	0.184	0.352	0.510	0.658	0.232
-80	0.312	0.599	0.860	1.095	0.421
-70	0.418	0.797	1.132	1.299	0.590
-60	0.520	0.984	1.292	1.326	0.753
-50	0.627	1.117	1.321	1.337	0.911
-40	0.714	1.275	1.330	1.341	1.041
-30	0.780	1.300	1.335	1.343	1.139



9. Voltage Regulator

This regulator (pin 18) supplies a typical 1.0 volts for external RF circuit, and/or other circuitry such as PLL. In the normal operation mode, the output current capability at pin 18 is typically ≒ 5 mA .

The KA8514 has the internal PNP transistor.

So, there is no need to use the extra PNP TR. However, if the current driving capability is not enough, only added a external PNP transistor as below fig 13. By the external resistor connected between pin 18 and TR collector, regulator voltage can be changed (1.0 V ~ 1.2 V) as below fig 14. At the battery saving mode, voltage regulator output becomes off.

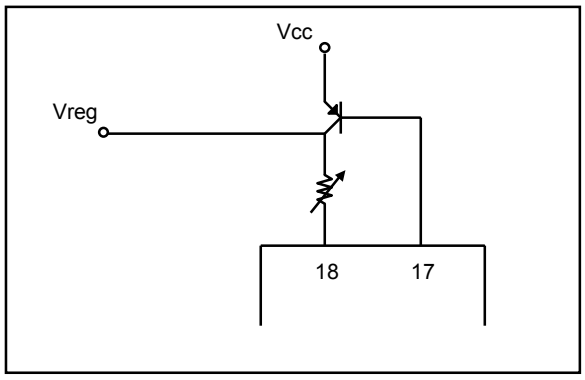


Fig 12. The circuit when use the external R & TR

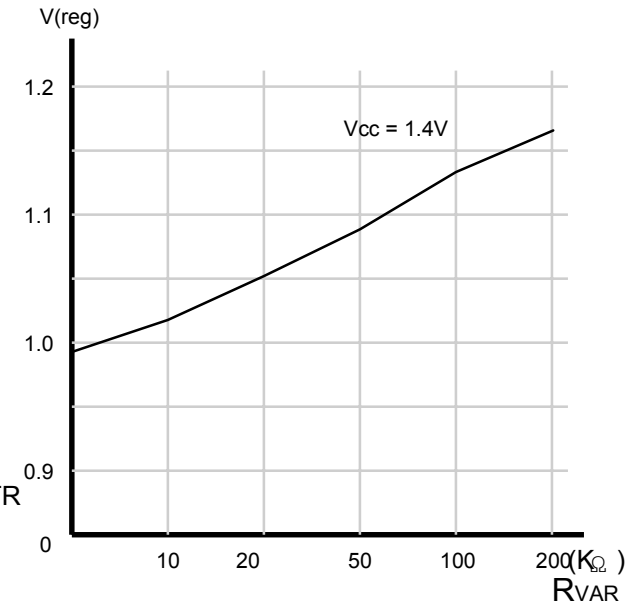


Fig 13. The graph of Vreg Vs external resistor

10. Quick charge Circuit

When the Quick charge (pin 14) goes to High level, the Quick charge circuit becomes active status. To prevent the error of FSK waveform , this circuit is very important. When this pin goes to low level , if the data is inputted, the time delay may occurs because of external capacitor and resistor.

In case of this , the waveform of initialization data can be distorted. To improve the shape of FSK data , this Quick charge pin should be High When Quick-charge pin goes to High level , the voltage of pin 7 and pin 12 becomes the same voltage.

In this case, FSK waveform error will be prevented. According to the test, on the pager set, it is need to short the port BS (pin 13)and QC (pin 14) pin simultaneously.

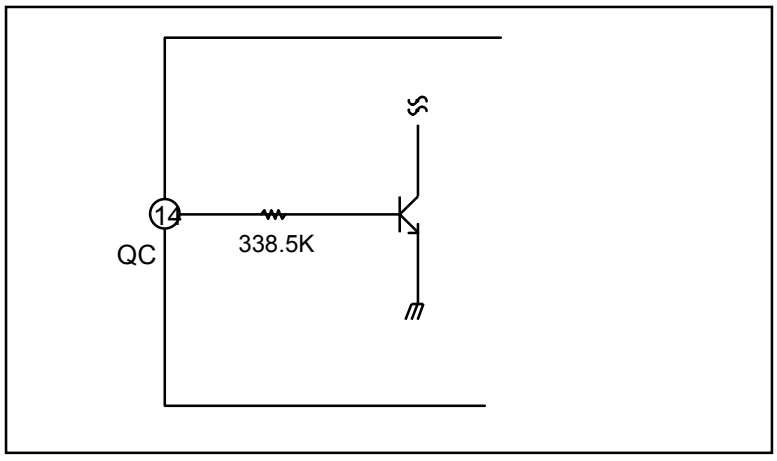


Fig 14. Quick Charge Circuit

11. FSK out Circuit

FSK demodulation can be accomplished by the internal comparator. The output of the comparator will be the logical output. The comparator is a non-inverting type with an open collector output. Typically the pull-up resistor needs 100kΩ between pin 15 and Vcc.

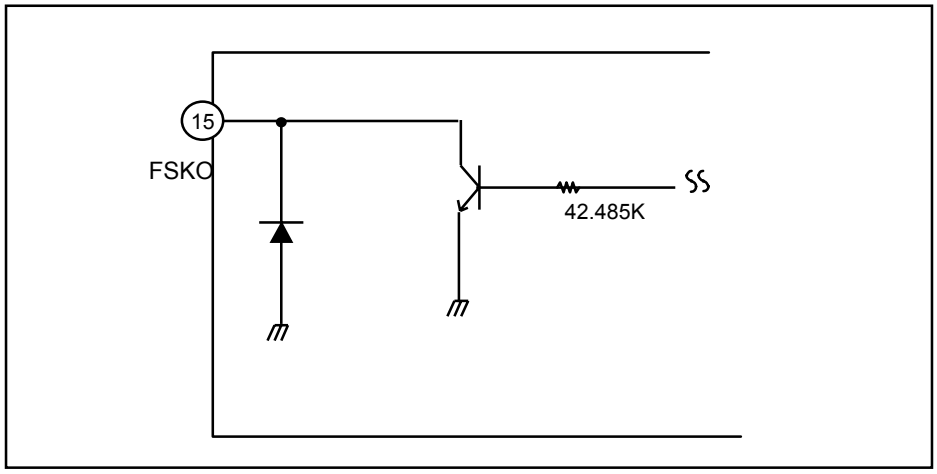


Fig 15. FSK output circuit

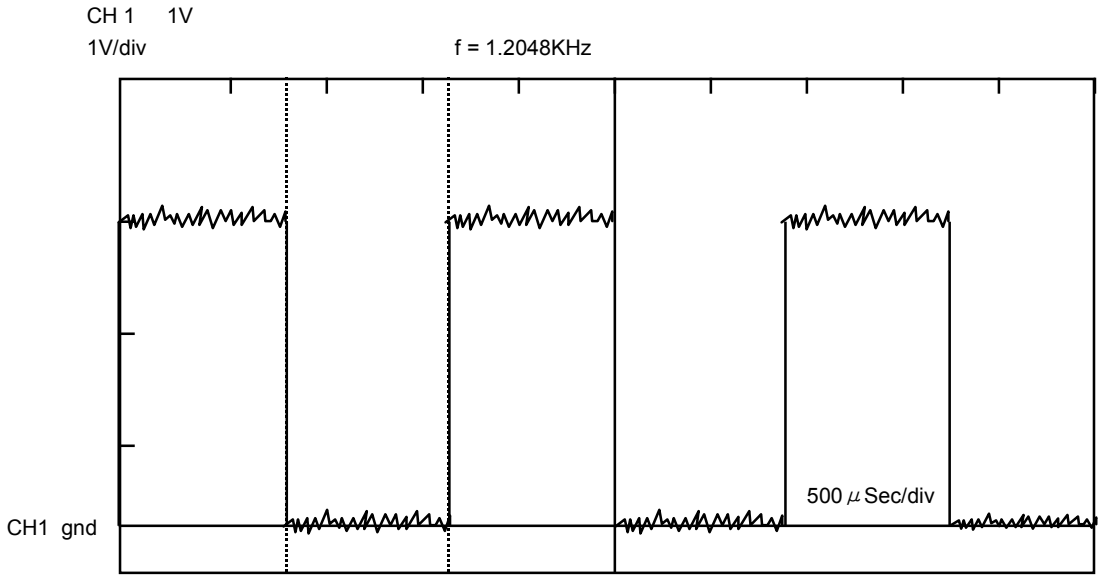


Fig 16. FSK 파형

12. CHARACTERISTIC CURVE

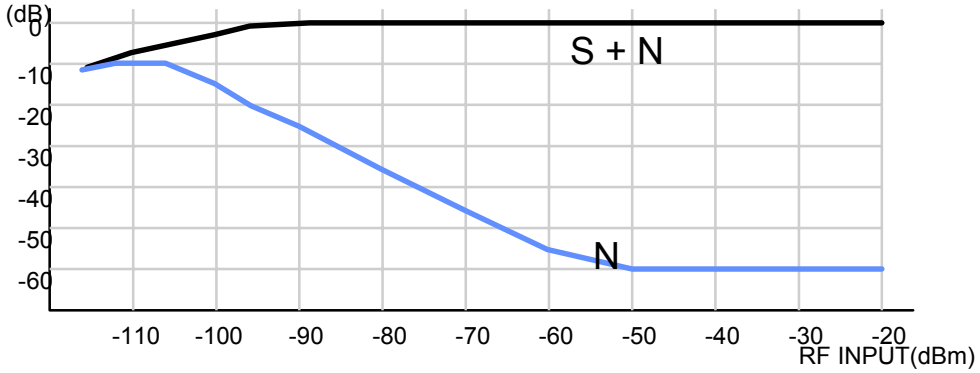


Fig 17. INPUT Level 에 따른 S+N / N 특성

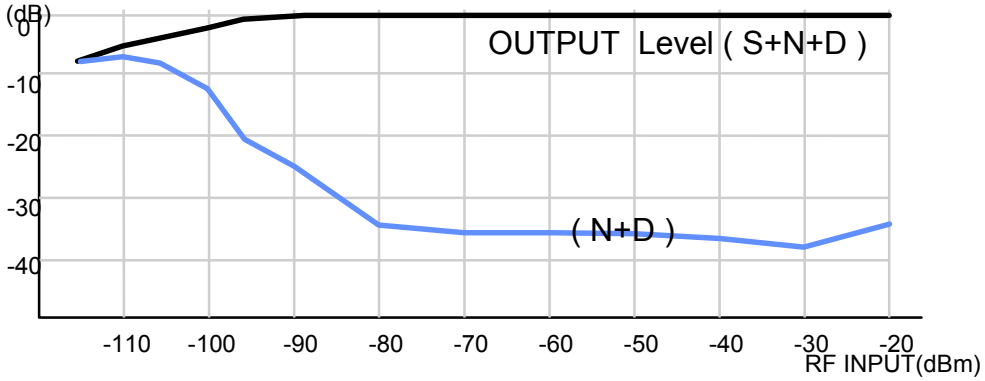


Fig 18. INPUT Level 에 따른 SINAD 특성

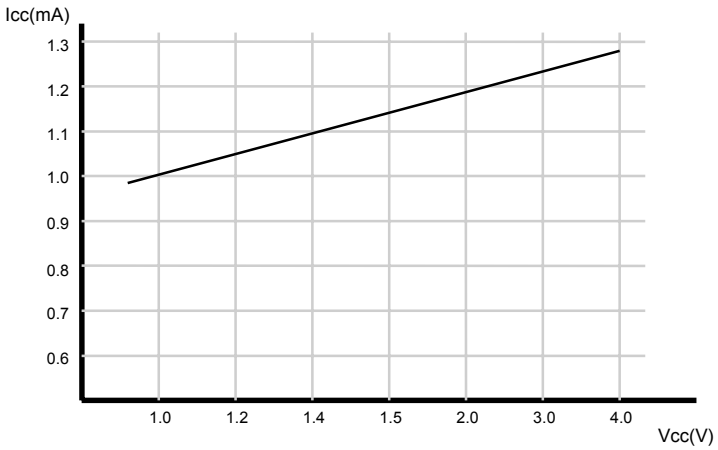


Fig 19. Icc 와 Vcc 와의 특성 Graph

Ⅴ. APPLICATION CIRCUIT