3.3V 1:10 LVCMOS PLL Clock Generator

Features

- 1:10 PLL based low-voltage clock generator
- Supports zero-delay operation
- 3.3V power supply
- Generates clock signals up to 250MHz
- Maximum output skew of 120pS
- Differential LVPECL reference clock input
- External PLL feedback
- Drives up to 20 clock lines
- 32 lead LQFP & TQFP Packages
- Pin and function compatible to the MPC958 and MPC9658

Functional Description

The PCS5I9658 is a 3.3V compatible, 1:10 PLL based clock generator and zero-delay buffer targeted for high performance low-skew clock distribution in mid-range to high-performance telecom, networking and computing applications. With output frequencies up to 250MHz and output skews less than 120pS the device meets the needs of the most demanding clock applications. The PCS5I9658 is specified for the temperature range of 0°C to +70°C.

The PCS5I9658 utilizes PLL technology to frequency lock its outputs onto an input reference clock. Normal operation of the PCS5I9658 requires the connection of the QFB output to the feedback input to close the PLL feedback path (external feedback). With the PLL locked, the output frequency is equal to the reference frequency of the device and VCO_SEL selects the operating frequency range of 50 to 125MHz or 100 to 250MHz. The two available post-PLL dividers selected by VCO_SEL (divide-by-2 or divide-by-4) and the reference clock frequency determines the VCO frequency. Both must be selected to match the VCO frequency range. The internal VCO of the PCS5I9658 is running at either 2x or 4x of the reference clock frequency.

The PCS5I9658 has a differential LVPECL reference input along with an external feedback input. The PCS5I9658 is ideal for use as a zero delay, low skew fanout buffer. The device performance has been tuned and optimized for zero delay performance.

The PLL_EN and $\overline{\text{BYPASS}}$ controls select the PLL bypass configuration for test and diagnosis. In this configuration, the selected input reference clock is bypassing the PLL and routed either to the output dividers or directly to the outputs. The PLL bypass configurations are fully static and the minimum clock frequency specification and all other PLL characteristics do not apply. The outputs can be disabled (high-impedance) and the device reset by asserting the MR/$\overline{\text{OE}}$ pin. Asserting MR/$\overline{\text{OE}}$ also causes the PLL to loose lock due to missing feedback signal presence at FB_IN. Deasserting MR/$\overline{\text{OE}}$ will enable the outputs and close the phase locked loop, enabling the PLL to recover to normal operation.

The PCS5I9658 is fully 3.3V compatible and requires no external loop filter components. The inputs (except PCLK) accept LVCMOS except signals while the outputs provide LVCMOS compatible levels with the capability to drive terminated 50Ω transmission lines. For series terminated transmission lines, each of the PCS5I9658 outputs can drive one or two traces giving the devices an effective fanout of 1:16. The device is packaged in a 7x7 mm^2 32-lead LQFP & TQFP Packages.

PulseCore Semiconductor Corporation
1715 S. Bascom Ave Suite 200, Campbell, CA 95008 • Tel: 408-879-9077 • Fax: 408-879-9018
www.pulsecoresemi.com

Block Diagram

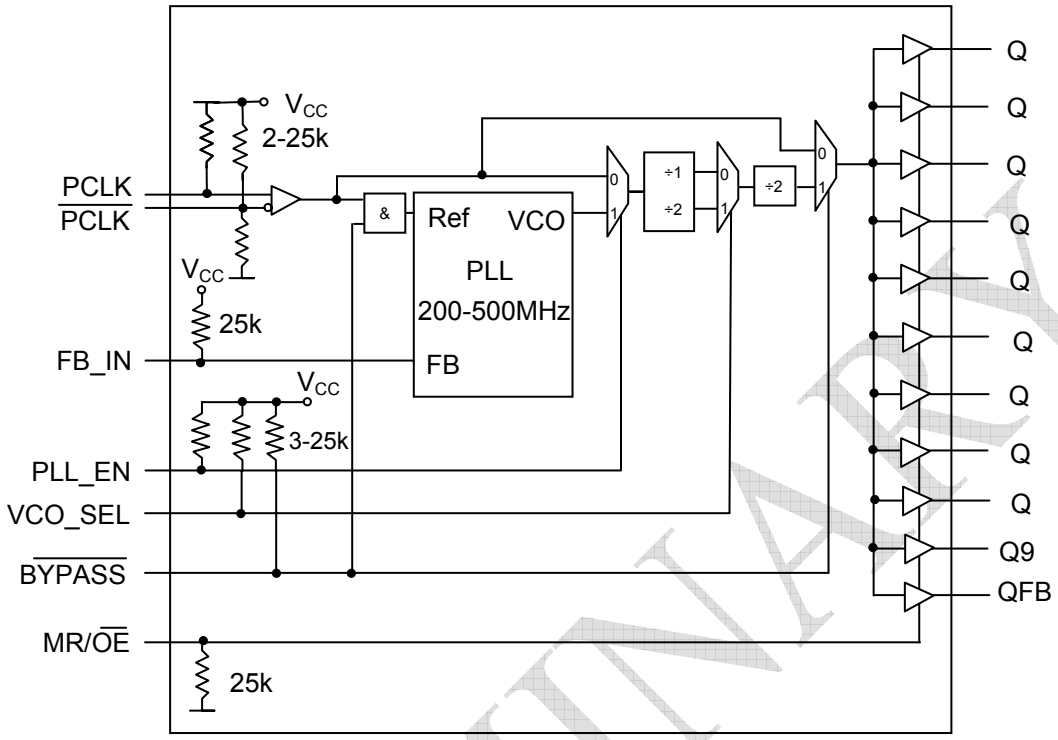

Figure 1. PCS5I9658 Logic Diagram

Pin Configuration

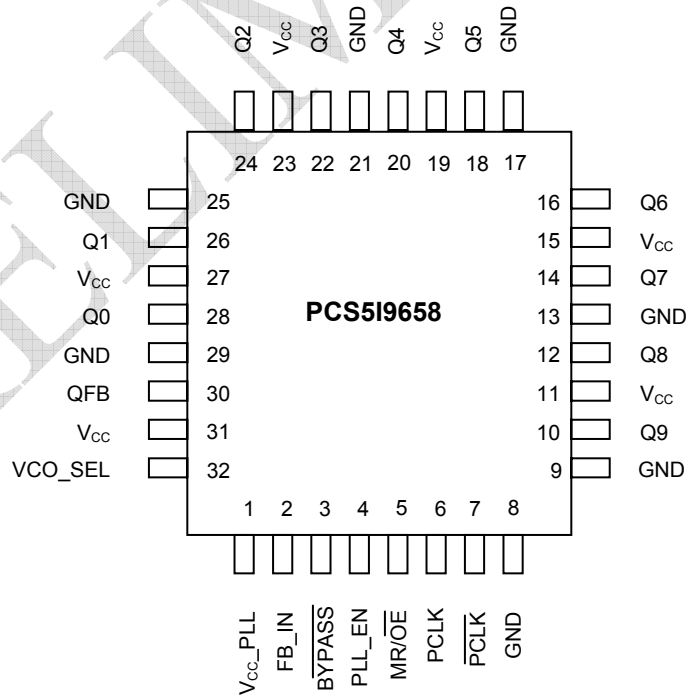

Figure 2. PCS5I9658 32-Lead Package Pinout (Top View)

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Table 1: Pin Configuration

Pin #	Pin Name	I/O	Type	Function
6 7	PCLK, $\overline{PCLK}$	Input	LVPECL	LVPECL reference clock signal
2	FB_IN	Input	LVCMOS	PLL feedback signal input, connect to QFB
32	VCO_SEL	Input	LVCMOS	Operating frequency range select
3	$\overline{BYPASS}$	Input	LVCMOS	PLL and output divider bypass select
4	PLL_EN	Input	LVCMOS	PLL enable/disable
5	MR/$\overline{OE}$	Input	LVCMOS	Output enable/disable (high-impedance tristate) and device reset
28,26,24, 22,20,18, 16,14,12, 10	Q0-9	Output	LVCMOS	Clock outputs
30	QFB	Output	LVCMOS	Clock output for PLL feedback, connect to FB_IN
8,9,13,17 21,25,29	GND	Supply	Ground	Negative power supply (GND)
1	VCC_PLL	Supply	VCC	PLL positive power supply (analog power supply). It is recommended to use an external RC filter for the analog power supply pin V_{CC_PLL}. Please see applications section for details.
11,15,19, 23,27,31	VCC	Supply	VCC	Positive power supply for I/O and core. All V_{CC} pins must be connected to the positive power supply for correct operation

Table 2: Function Table

Control	Default	0	1
PLL_EN	1	Test mode with PLL bypassed. The reference clock (PCLK) is substituted for the internal VCO output. PCS59658 is fully static and no minimum frequency limit applies. All PLL related AC characteristics are not applicable.	Selects the VCO output[1]
$\overline{BYPASS}$	1	Test mode with PLL and output dividers bypassed. The reference clock (PCLK) is directly routed to the outputs. PCS59658 is fully static and no minimum frequency limit applies. All PLL related AC characteristics are not applicable.	Selects the output dividers.
VCO_SEL	1	VCO ÷ 1 (High frequency range). $f_{REF} = f_{Q0-9} = 2. f_{VCO}$	V_{CO} ÷ 2 (Low frequency range). $f_{REF} = f_{Q0-9} = 4.f_{VCO}$
MR/$\overline{OE}$	0	Outputs enabled (active)	Outputs disabled (high-impedance state) and reset of the device. During reset the PLL feedback loop is open. The VCO is tied to its lowest frequency. The length of the reset pulse should be greater than one reference clock cycle (PCLK).

Note: 1 PLL operation requires BYPASS=1 and PLL_EN=1.

Table 3: Absolute Maximum Ratings[1]

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	-0.3	3.9	V	
V_{IN}	DC Input Voltage	-0.3	V_{CC}+0.3	V	
V_{OUT}	DC Output Voltage	-0.3	V_{CC}+0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage Temperature	-65	125	°C	

Note: 1 These are stress ratings only and are not implied for functional use. Exposure to absolute maximum ratings for prolonged periods of time may affect device reliability.

Table 4: GENERAL SPECIFICATIONS

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage		V_{CC}÷2		V	
MM	ESD Protection (Machine Model)	200			V	
HBM	ESD Protection (Human Body Model)	2000			V	
LU	Latch-Up Immunity	200			mA	
C_{PD}	Power Dissipation Capacitance		10		pF	Per output
C_{IN}	Input Capacitance		4.0		pF	Inputs
θ_{JA}	LQFP 32 Thermal resistance junction to ambient JESD 51-3, single layer test board		83.1	86.0	°C/W	Natural convection
			73.3	75.4	°C/W	100 ft/min
			68.9	70.9	°C/W	200 ft/min
			63.8	65.3	°C/W	400 ft/min
			57.4	59.6	°C/W	800 ft/min
	JESD 51-6, 2S2P multilayer test board		59.0	60.6	°C/W	Natural convection
			54.4	55.7	°C/W	100 ft/min
			52.5	53.8	°C/W	200 ft/min
			50.4	51.5	°C/W	400 ft/min
			47.8	48.8	°C/W	800 ft/min
θ_{JC}	LQFP 32 Thermal resistance junction to case		23.0	26.3	°C/W	MIL-SPEC 883E Method 1012.1

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Table 5: DC Characteristics (V_{CC} = 3.3V ± 5%, T_A = -40°C to +85°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{IH}	Input high voltage	2.0		V_{CC} +0.3	V	LVCMOS
V_{IL}	Input low voltage			0.8	V	LVCMOS
V_{PP}	Peak-to-peak input voltage (PCLK)	250			mV	LVPECL
V_{CMR}[1]	Common Mode Range (PCLK)	1.0		V_{CC}-0.6	V	LVPECL
V_{OH}	Output High Voltage	2.4			V	I_{OH}=-24 mA[2]
V_{OL}	Output Low Voltage[3]			0.55 0.30	V V	I_{OL}=24mA I_{OL}=12mA
Z_{OUT}	Output impedance		14 -17		Ω	
I_{IN}	Input Current[4]			±200	µA	V_{IN}=V_{CC} or GND
I_{CC_PLL}	Maximum PLL Supply Current		12	15	mA	V_{CC_PLL} Pin
I_{CCQ}	Maximum Quiescent Supply Current		13	15	mA	All V_{CC} Pins

Note: 1. V_{CMR} (DC) is the cross point of the differential input signal. Functional operation is obtained ,when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (DC) specification.
2. The PCS5I9658 is capable of driving 50Ωtransmission lines on the incident edge. Each output drives one 50Ωparallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up to two 50Ωseries terminated transmission lines.
3. The PCS5I9658 output levels are compatible to the MPC958 output levels.
4. Inputs have pull-down or pull-up resistors affecting the input current.

Table 6: AC Characteristics (V_{CC} = 3.3V ± 5%, T_A = -40°C to +85°C)[1]

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
f_{REF}	Input reference frequency ÷2 feedback[2] PLL mode, external feedback ÷4 feedback[3] Input reference frequency in PLL bypass mode[4]	100 50 0		250 125 250	MHz MHz MHz	PLL locked PLL locked
f_{VCO}	VCO operating frequency range[5]	200		500	MHz	
f_{MAX}	Output Frequency ÷2 feedback[3] ÷4 feedback[4]	100 50		250 125	MHz MHz	PLL locked PLL locked
V_{PP}	Peak-to-peak input voltage PCLK	500		1000	mV	LVPECL
V_{CMR}[6]	Common Mode Range PCLK	1.2		VCC-0.9	V	LVPECL
$t_{PW,MIN}$	Input Reference Pulse Width[7]	2.0			nS	
$t_{(Ø)}$	Propagation Delay (static phase offset)[8] PCLK to FB_IN f_{REF}=100MHz any frequency	-70 -125		+80 +125	pS pS	PLL locked
t_{PD}	Propagation Delay PLL and divider bypass, PCLK to Q0-9	1.0		4.0	nS	
$t_{sk(O)}$	Output-to-output Skew[9]			120	pS	
DC	Output duty cycle[10]	(T÷2) -400	T÷2	(T÷2) +400	pS	
t_R ,t_F	Output Rise/Fall Time	0.1		1.0	nS	0.55 to 2.4V
$t_{PLZ, HZ}$	Output Disable Time			7.0	nS	
$t_{PZL, LZ}$	Output Enable Time			6.0	nS	
$t_{JIT(CC)}$	Cycle-to-cycle jitter			80	pS	
$t_{JIT(PER)}$	Period Jitter			80	pS	
$t_{JIT(Ø)}$	I/O Phase Jitter f_{VCO}=500MHz and ÷ 2 feedback, RMS (1σ)[11] f_{VCO}=500MHz and ÷ 4 feedback, RMS (1σ)			5.5 6.5	pS pS	
BW	PLL closed loop bandwidth[12] ÷2 feedback[3] PLL mode, external feedback ÷4 feedback[4]		6-20 2 - 8		MHz MHz	
t_{LOCK}	Maximum PLL Lock Time			10	mS	

Note:1. AC characteristics apply for parallel output termination of 50Ω to V_{TT}.
2. ÷2 PLL feedback (high frequency range) requires VCO_SEL=0, PLL_EN=1, BYPASS=1 and MR/OE=0.
3.÷4 PLL feedback (low frequency range) requires VCO_SEL=1, PLL_EN=1, BYPASS=1 and MR/OE=0.
4.In bypass mode, the PCS5I9658 divides the input reference clock.
5.The input frequency f_{REF} must match the VCO frequency range divided by the feedback divider ratio FB: $f_{REF} = f_{VCO} \div FB$.
6.V_{CMR} (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} or V_{PP} impacts static phase offset t(Ø).
7.Calculation of reference duty cycle limits: $DC_{REF,MIN} = t_{PW,MIN} \cdot f_{REF}$. 100% and $DC_{REF,MAX}$ = 100% - $DC_{REF,MIN}$.
8.Valid for f_{REF}=50MHz and FB=÷8 (VCO_SEL=1). For other reference frequencies: t(Ø) [pS] = 50 pS ± (1÷(120 . f_{REF})).
9.See application section for part-to-part skew calculation in PLL zero-delay mode.
10.Output duty cycle is DC = (0.5 ± 400pS. f_{OUT}) V 100%. E.g. the DC range at f_{OUT}=100MHz is 46%<DC<54%. T = output period.
11.See application section for a jitter calculation for other confidence factors than 1 and a characteristic for other VCO frequencies.
12.-3 dB point of PLL transfer characteristics.

Applications Information

Driving Transmission Lines

The PCS5I9658 supports output clock frequencies from 50 to 250MHz. Two different feedback divider configurations can be used to achieve the desired frequency operation range. The feedback divider (VCO_SEL) should be used to situate the VCO in the frequency lock range between 200 and 500MHz for stable and optimal operation. Two operating frequency ranges are supported: 50 to 125MHz and 100 to 250 MHz. Table 7 illustrates the configurations supported by the PCS5I9658. PLL zero-delay is supported if $\overline{\text{BYPASS}}$=1, PLL_EN=1 and the input frequency is within the specified PLL reference frequency range.

Table 7: PCS5I9658 Configurations (QFB connected to FB_IN)

BYPASS	PLL_EN	VCO_SEL	Operation	Frequency		
				Ratio	Output range (fQ0-7)	VCO
0	X	X	Test mode: PLL and divider bypass	$f_{Q0-9} = f_{REF}$	0-250MHz	n/a
1	0	0	Test mode: PLL bypass	$f_{Q0-9} = f_{REF} \div 2$	0-125MHz	n/a
1	0	1	Test mode: PLL bypass	$f_{Q0-9} = f_{REF} \div 4$	0-62.5MHz	n/a
1	1	0	PLL mode (high frequency range)	$f_{Q0-9} = f_{REF}$	100 to 250MHz	$f_{VCO} = f_{REF} . 2$
1	1	1	PLL mode (low frequency range)	$f_{Q0-9} = f_{REF}$	50 to 125MHz	$f_{VCO} = f_{REF} . 4$

Power Supply Filtering

The PCS5I9658 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Random noise on the V_{CCA_PLL} power supply impacts the device characteristics, for instance I/O jitter. The PCS5I9658 provides separate power supplies for the output buffers (V_{CC}) and the phase-locked loop (V_{CCA_PLL}) of the device. The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simple but effective form of isolation is a power supply filter on the V_{CC_PLL} pin for the PCS5I9658. Figure 3. illustrates a typical power supply filter scheme. The PCS5I9658 frequency and phase stability is most susceptible to noise with spectral content in the 100KHz to 20MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop across the series filter resistor R_F. From the data sheet the I_{CC_PLL} current (the current sourced through the V_{CC_PLL} pin) is typically 12mA (20 mA maximum), assuming that a minimum of 2.835V must be maintained on the V_{CC_PLL} pin.

The minimum values for R_F and the filter capacitor C_F are defined by the required filter characteristics: the RC filter should provide attenuation greater than 40 dB for

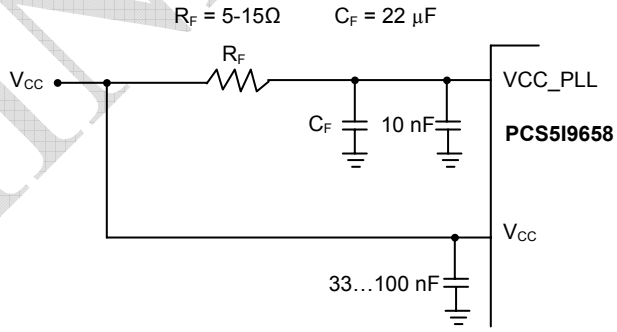


Figure 3. V_{CC_PLL} Power Supply Filter

noise whose spectral content is above 100KHz. In the example RC filter shown in Figure 3."V_{CC_PLL} Power Supply Filter", the filter cut-off frequency is around 3-5KHz and the noise attenuation at 100KHz is better than 42dB.

As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Although the PCS5I9658 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed

in this section should be adequate to eliminate power supply noise related problems in most designs.

Using the PCS5I9658 in zero-delay applications

Nested clock trees are typical applications for the PCS5I9658. Designs using the PCS5I9658, as LVCMOS PLL fanout buffer with zero insertion delay will show significantly lower clock skew than clock distributions developed from CMOS fanout buffers. The external feedback option of the PCS59658 clock driver allows for its use as a zero delay buffer. The PLL aligns the feedback clock output edge with the clock input reference edge resulting a near zero delay through the device (the propagation delay through the device is virtually eliminated). The maximum insertion delay of the device in zero-delay applications is measured between the reference clock input and any output. This effective delay consists of the static phase offset, I/O jitter (phase or long-term jitter), feedback path delay and the output-to-output skew error relative to the feedback output.

Calculation of part-to-part skew

The PCS5I9658 zero delay buffer supports applications where critical clock signal timing can be maintained across several devices. If the reference clock inputs of two or more PCS5I9658 are connected together, the maximum overall timing uncertainty from the common PCLK input to any output is:

$t_{SK(PP)} = t_{(\varphi)} + t_{SK(O)} + t_{PD}$, LINE(FB) + $t_{JIT(\varphi)}$ .CF

This maximum timing uncertainty consist of 4 components: static phase offset, output skew, feedback board trace delay and I/O (phase) jitter:

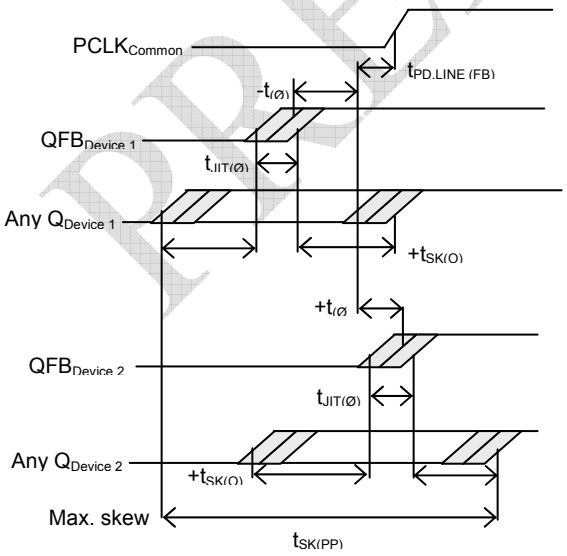


Figure 4. PCS5I9658 max device-to-device skew

Due to the statistical nature of I/O jitter a RMS value (1σ) is specified. I/O jitter numbers for other confidence factors (CF) can be derived from Table 8.

Table 8: Confidence Factor CF

CF	Probability of clock edge within the distribution
± 1σ	0.68268948
± 2σ	0.95449988
± 3σ	0.99730007
± 4σ	0.99993663
± 5σ	0.99999943
± 6σ	0.99999999

The feedback trace delay is determined by the board layout and can be used to fine-tune the effective delay through each device. In the following example calculation a I/O jitter confidence factor of 99.7% (±3σ) is assumed, resulting in a worst case timing uncertainty from input to any output of -214pS to 224pS relative to PCLK

(f_{REF} = 100MHz, FB=÷4, $t_{jit(\varphi)}$=8pS RMS at f_{VCO} = 400MHz):

$t_{SK(PP)}$ = [–70pS...80pS] + [–120pS...120pS] +

[(8Ps . –3)...(8pS . 3)] + t_{PD}, LINE(FB)

$t_{SK(PP)}$ = [–214pS...224pS] + t_{PD}, LINE(FB)

Due to the frequency dependence of the I/O jitter, Figure 5. can be used for a more precise timing performance analysis.

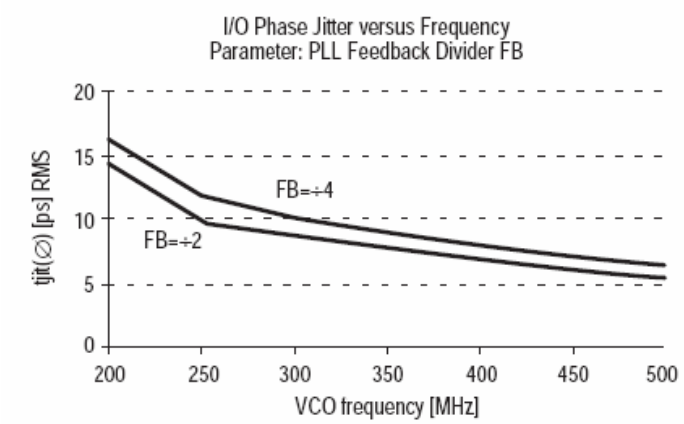


Figure 5. Maximum I/O Jitter versus frequency

Driving Transmission Lines

The PCS5I9658 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20Ω the drivers can drive either parallel or series terminated transmission lines. In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to V_{CC}÷2.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the PCS59658 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 6. “Single versus Dual Transmission Lines” illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme the fanout of the PCS5I9658 clock driver is effectively doubled due to its capability to drive multiple lines.

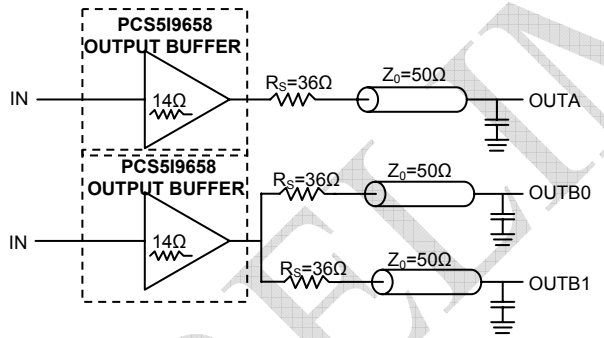


Figure 6. Single versus Dual Transmission Lines

The waveform plots in Figure 7. “Single versus Dual Line Termination Waveforms” show the simulation results of an output driving a single line versus two lines. In both cases the drive capability of the PCS5I9658 output buffer is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43pS exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the PCS5I9658. The output waveform in Figure 7. “Single versus Dual Line Termination Waveforms” shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$V_L = V_S (Z_0 ÷(R_S+R_0 +Z_0))$

$Z_0 = 50Ω || 50Ω$

$R_S = 36 Ω || 36Ω$

$R_0 = 14Ω$

$V_L = 3.0 (25 ÷(18+14+25))$

$= 1.31V$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.6V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0nS).

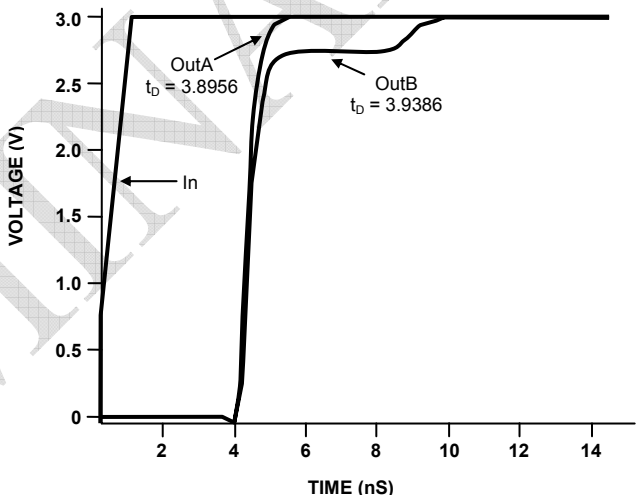
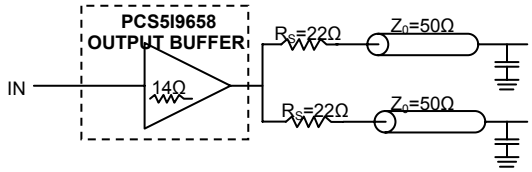


Figure 7. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 8. “Optimized Dual Line Termination” should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.



14Ω + 22Ω || 22Ω = 50Ω || 50Ω
25Ω = 25Ω

Figure 8. Optimized Dual Line Termination

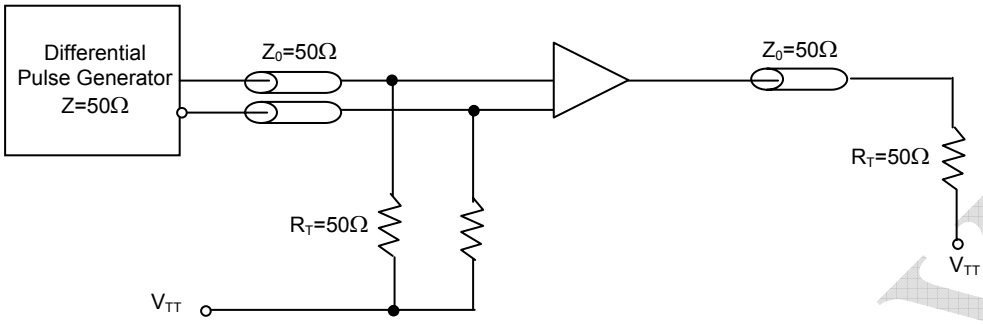
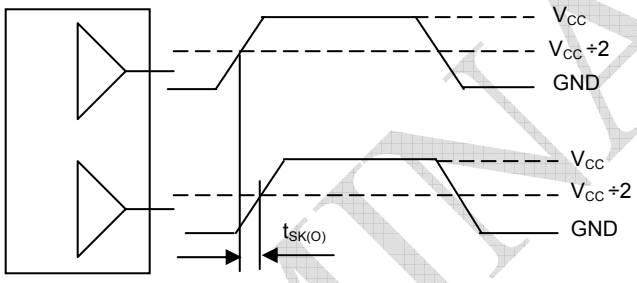


Figure 9. PCLK PCS5I958 AC test reference



The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

Figure 10. Output–to–Output Skew $t_{SK(O)}$

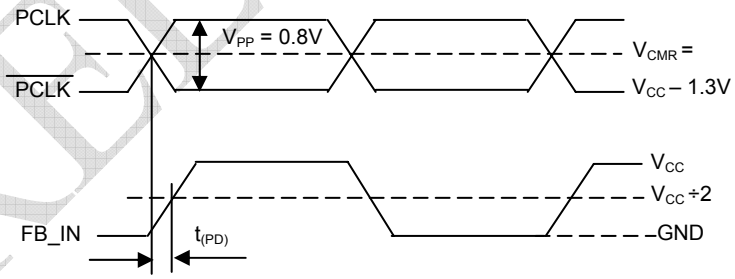
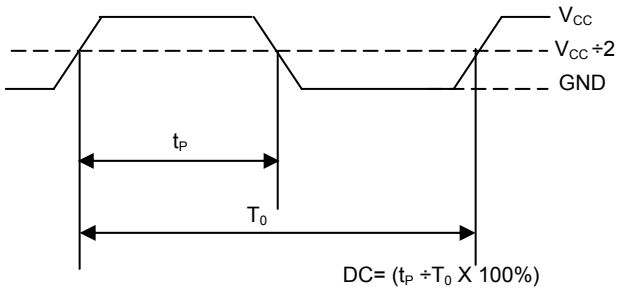
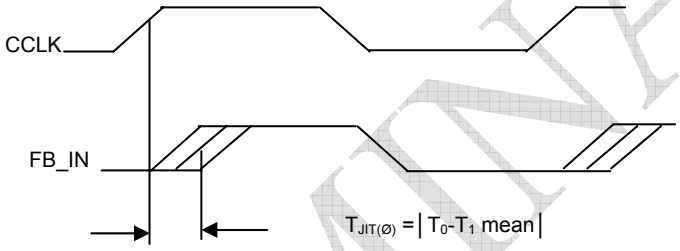


Figure 11. Propagation Delay ($t_{(PD)}$). Static phase offset test reference



The time from the PLL controlled edge to the non-controlled edge, divided by the time between PLL controlled edges, expressed as a percentage.

Figure 12. Output Duty Cycle (DC)

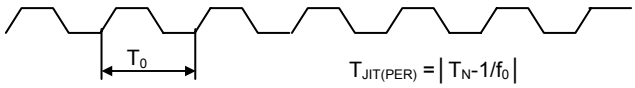


The deviation in t_0 for a controlled edge with respect to a t_0 mean in a random sample of cycles

Figure 13.I/O Jitter

The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

Figure 14. Cycle-to-cycle Jitter



The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

Figure 15. Period Jitter

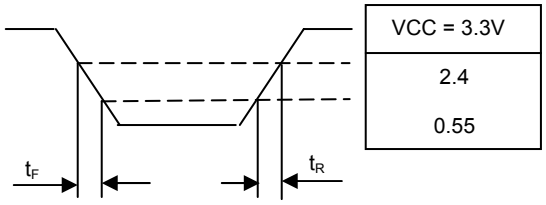
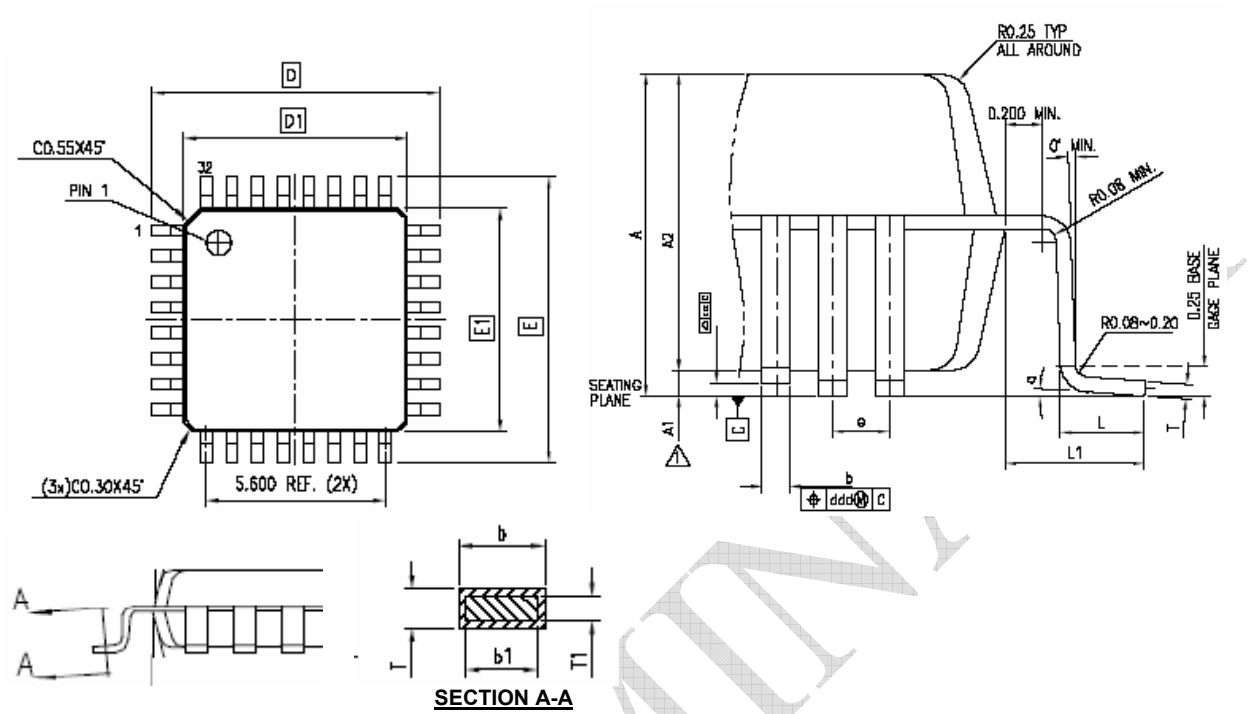


Figure 16. Output Transition Time Test Reference

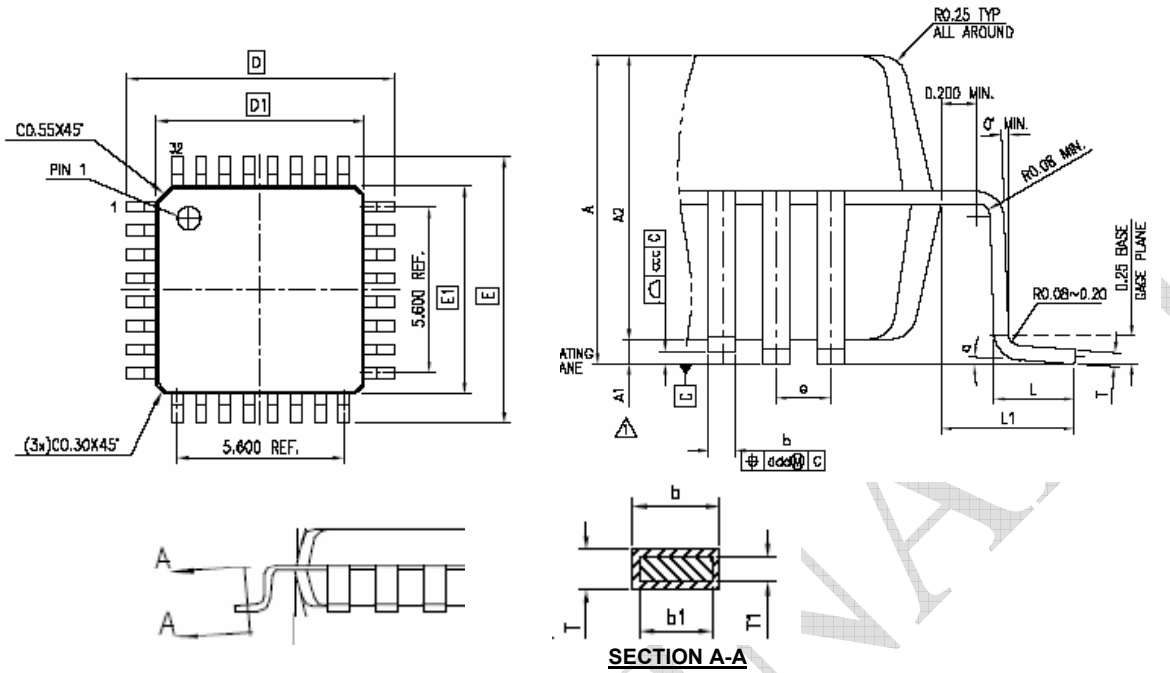
Package Information

32-lead TQFP



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	….	0.0472	…	1.2
A1	0.0020	0.0059	0.05	0.15
A2	0.0374	0.0413	0.95	1.05
D	0.3465	0.3622	8.8	9.2
D1	0.2717	0.2795	6.9	7.1
E	0.3465	0.3622	8.8	9.2
E1	0.2717	0.2795	6.9	7.1
L	0.0177	0.0295	0.45	0.75
L1	0.03937 REF		1.00 REF	
T	0.0035	0.0079	0.09	0.2
T1	0.0038	0.0062	0.097	0.157
b	0.0118	0.0177	0.30	0.45
b1	0.0118	0.0157	0.30	0.40
R0	0.0031	0.0079	0.08	0.2
a	0°	7°	0°	7°
e	0.031 BASE		0.8 BASE	

32-lead LQFP



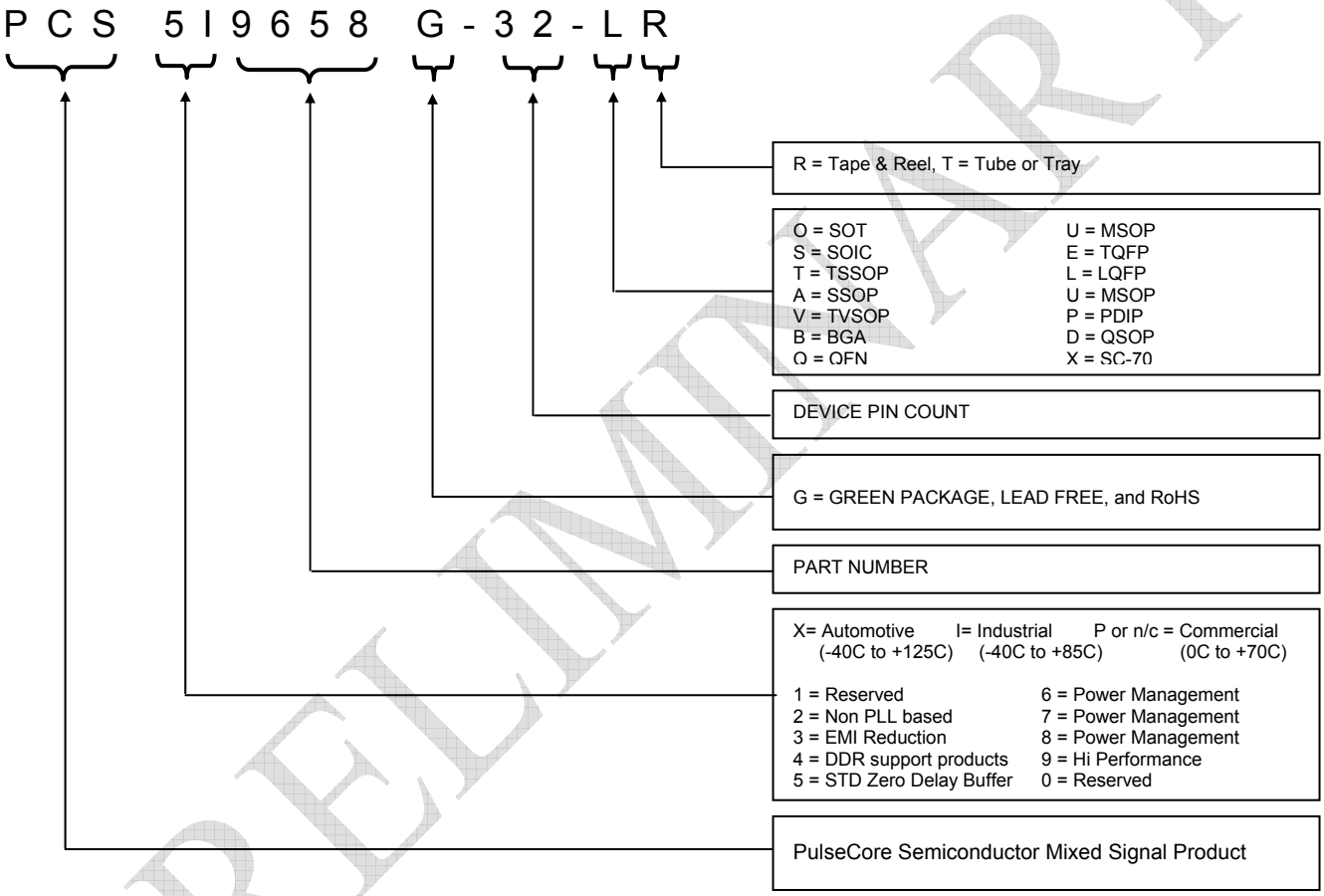
SECTION A-A

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	....	0.0630	...	1.6
A1	0.0020	0.0059	0.05	0.15
A2	0.0531	0.0571	1.35	1.45
D	0.3465	0.3622	8.8	9.2
D1	0.2717	0.2795	6.9	7.1
E	0.3465	0.3622	8.8	9.2
E1	0.2717	0.2795	6.9	7.1
L	0.0177	0.0295	0.45	0.75
L1	0.03937 REF		1.00 REF	
T	0.0035	0.0079	0.09	0.2
T1	0.0038	0.0062	0.097	0.157
b	0.0118	0.0177	0.30	0.45
b1	0.0118	0.0157	0.30	0.40
R0	0.0031	0.0079	0.08	0.20
e	0.031 BASE		0.8 BASE	
a	0°	7°	0°	7°

Ordering Information

Part Number	Marking	Package Type	Operating Range
PCS5I9658G-32-ER	PCS5I9658G	32-pin TQFP, Green	Industrial
PCS5I9658G-32-LR	PCS5I9658G	32-pin LQFP –Tape and Reel, Green	Industrial

Device Ordering Information



PulseCore Semiconductor Corporation
1715 S. Bascom Ave Suite 200
Campbell, CA 95008
Tel: 408-879-9077
Fax: 408-879-9018
www.pulsecoresemi.com

Note: This product utilizes US Patent # 6,646,463 Impedance Emulator Patent issued to PulseCore Semiconductor, dated 11-11-2003