SiPHY™ OC-192/STM-64 SONET/SDH RECEIVER

Features

Complete low power, high speed, receiver with integrated limiting amplifier, clock and data recovery (CDR), and 1:16 demultiplexer:

- Data Rates Supported: OC-192/STM-64, 10GbE, 10.7 Gbps FEC
- Low Power Operation 0.6 W (typ)
- Small Footprint 99-Pin BGA Package (11 x 11 mm)
- Integrated Limiting Amplifier
- Programmable Slicing Level and Sampling Phase
- SFI-4 Compliant LVDS Low Speed Interface
- Loss-of-Signal and Loss-of-Lock Detection
- Lock-to-Reference Control
- Optional 3.3 V Supply Pin for LVTTL Compatible Outputs
- Single 1.8 V Supply Operation

Applications

- Sonet/SDH/ATM Routers
- Add/Drop Multiplexers
- Digital Cross Connects
- Optical Transceiver Modules
- Sonet/SDH Test Equipment

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Bottom View

Ordering Information:
See page 16.

Description

The Si5530 is a fully integrated low-power receiver for high-speed serial communication systems. It combines post amplification, clock and data recovery, and a 1:16 deserialization as required in OC-192/STM-64 applications. Support for data streams up to 10.7 Gbps is also provided for applications that employ forward error correction (FEC). A fully integrated clock and data recovery unit with integrated loop filter ensures optimal jitter performance while reducing design complexity.

The Si5530 represents a new standard in low power and small size for high-speed serial receivers. It operates from a single 1.8 V supply over the industrial temperature range (–40°C to 85°C).
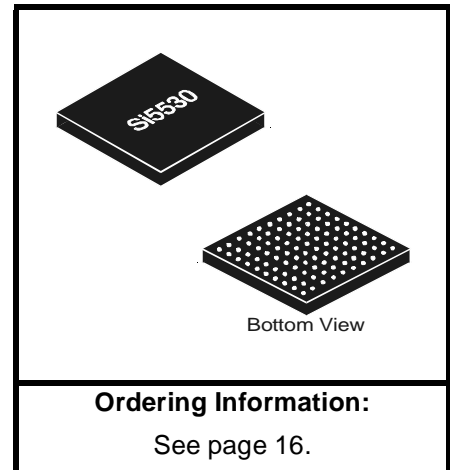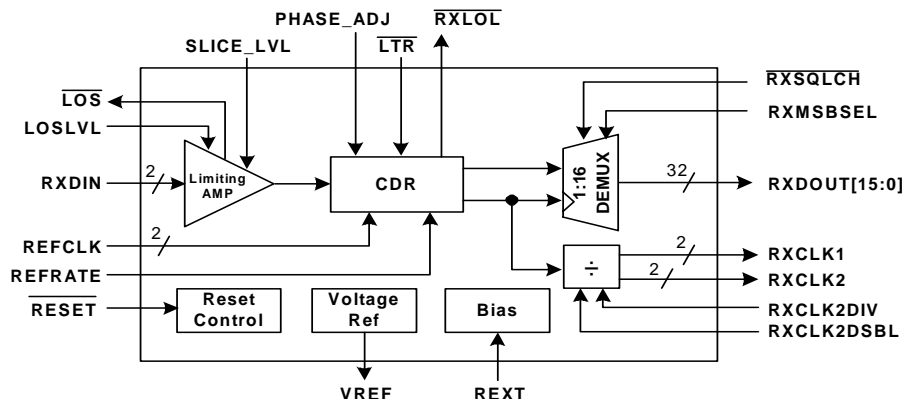
Functional Block Diagram

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Electrical Specifications

Table 1. Recommended Operating Conditions

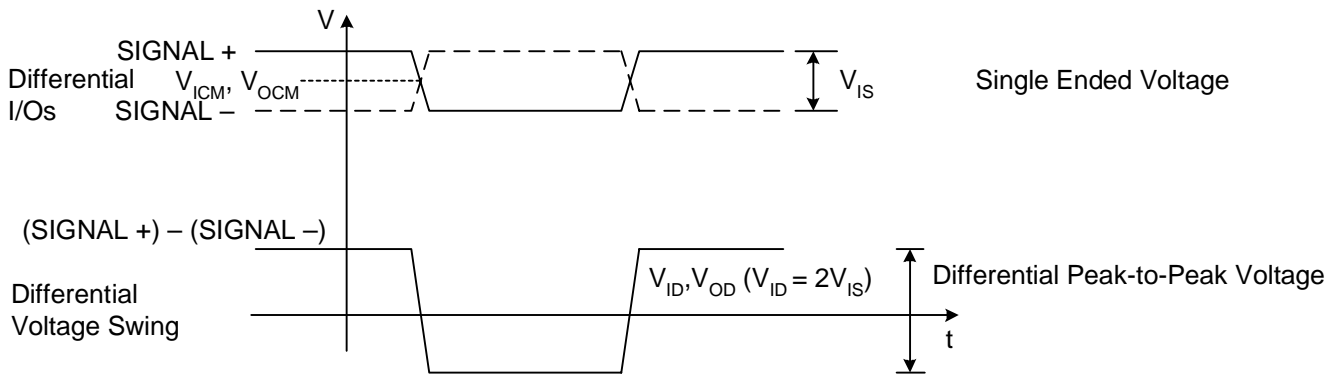| Parameter	Symbol	Test Condition	Min[*]	Typ	Max[*]	Unit
Ambient Temperature	T_A		–40	25	85	°C
LVTTL Output Supply Voltage	V_{DD33}		1.71	—	3.47	V
Si5530 Supply Voltage	V_{DD}		1.71	1.8	1.89	V
*Note: All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25°C unless otherwise stated.						

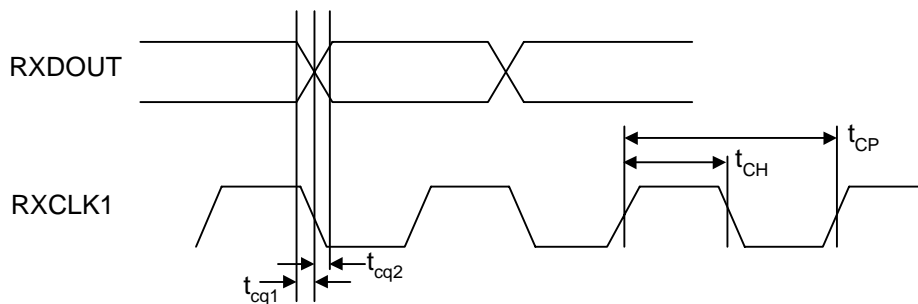**Figure 1. Differential Voltage Measurement (RXDIN, RXDOUT, RXCLK1, RXCLK2)**
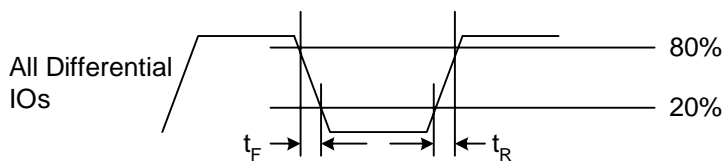

Figure 2. Data to Clock Delay

Figure 3. Rise/Fall Time Measurement

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Table 2. DC Characteristics

(V_{DD} = 1.8 V ±5%, T_A = −40°C to 85°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Current	I_{DD}		—	278	TBD	mA
Power Dissipation	P_D		—	0.5	TBD	W
Voltage Reference (VREF)	V_{REF}	VREF driving 10 kΩ load	1.21	1.25	1.29	V
Common Mode Input Voltage (RXDIN)	V_{ICM}		TBD	0.1	TBD	V
Differential Input Voltage Swing (RXDIN)	V_{ID}	See Figure 1	20	—	1.0	mV (pk-pk)
LVPECL Input Voltage HIGH (REFCLK)	V_{IH}		1.975	2.3	2.59	V
LVPECL Input Voltage LOW (REFCLK)	V_{IL}		1.32	1.6	1.99	V
LVPECL Input Voltage Swing, Differential pk-pk (REFCLK)	V_{ID}	Figure 1	250	—	2400	mV (pk-pk)
LVPECL Internally Generated Input Bias (REFCLK)	V_{IB}		1.65	1.95	2.3	V
LVDS Output High Voltage (RXDOUT, RXCLK1, RXCLK2)	V_{OH1}	100 Ω Load Line-to-Line	TBD	—	1.475	mV
LVDS Output Low Voltage (RXDOUT, RXCLK1, RXCLK2)	V_{OL1}	100 Ω Load Line-to-Line	0.925	—	TBD	V
LVDS Output Voltage, Differential pk-pk (RXDOUT, RXCLK1, RXCLK2)	V_{OSE}	100 Ω Load Line-to-Line, Figure 1	500	—	800	mV (pk-pk)
LVDS Common Mode Voltage (RXDOUT, RXCLK1, RXCLK2)	V_{CM}		1.125	—	1.275	V
Output Short to GND (RXDOUT, RXCLK1, RXCLK2)	$I_{SC(−)}$		—	25	TBD	mA
Output Short to V_{DD} (RXDOUT, RXCLK1, RXCLK2)	$I_{SC(+)}$		TBD	−100	—	µA
LVTTL Input Voltage Low (RXMSBSEL, RXCLK2DIV, RXCLK2DSBL, RXSQLCH, REFSEL, LTR, RESET)	V_{IL2}	VDD33 = 3.3 V	—	—	0.8	V
		VDD33 = 1.8 V	—	—	0.7	
LVTTL Input Voltage High (RXMSBSEL, RXCLK2DIV, RXCLK2DSBL, RXSQLCH, REFSEL, LTR, RESET)	V_{IH2}	VDD33 = 3.3 V	2.0	—	—	V
		VDD33 = 1.8 V	1.7	—	—	
LVTTL Input Low Current (RXMSBSEL, RXCLK2DIV, RXCLK2DSBL, RXSQLCH, REFSEL, LTR, RESET)	I_{IL}		—	—	10	µA
LVTTL Input High Current (RXMSBSEL, RXCLK2DIV, RXCLK2DSBL, RXSQLCH, REFSEL, LTR, RESET)	I_{IH}		—	—	10	µA

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Table 2. DC Characteristics (Continued)
(V_{DD} = 1.8 V ±5%, T_A = –40°C to 85°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
LVTTL Input Impedance (RXMSBSEL, RXCLK2DIV, RXCLK2DSBL, RXSQLCH, REFSEL, LTR, RESET)	R_{IN}		10	—	—	kΩ
LVTTL Output Voltage Low (LOS, RXLOL)	V_{OL2}	VDD33 = 1.8 V	—	—	0.4	V
		VDD33 = 3.3 V	—	—	0.4	
LVTTL Output Voltage High (LOS, RXLOL)	V_{OH2}	VDD33 = 1.8 V	1.4	—	—	V
		VDD33 = 3.3 V	2.4	—	—	

Table 3. AC Characteristics (RXDIN, RXDOUT, RXCLK1, RXCLK2)
(V_{DD} = 1.8 V ±5%, T_A = –40°C to 85°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Clock Frequency (RXCLK1)	f_{clkout}	See Figure 2	—	622.08	667	MHz
Duty Cycle (RXCLK1, RXCLK2)		tch/tcp, Figure 2	45	—	55	%
Output Rise and Fall Times (RXCLK1, RXCLK2,RXDOUT)	t_R,t_F	Figure 3	—	50	—	ps
Data Invalid Prior to RXCLK1	t_{cq1}	Figure 2	—	—	200	ps
Data Invalid After RXCLK1	t_{cq2}	Figure 2	—	—	200	ps
Input Return Loss (RXIN)		400 kHz–10.0 GHz 10.0 GHz–16.0 GHz	18.7 TBD	— —	— —	dB dB
Slicing Adjust Dynamic Range		SLICELVL = 200–800 mV	–20	—	20	mV
Slicing Level Offset[1] (referred to RXDIN)		SLICELVL = 200–800 mV	–500	—	500	μV
Slicing Level Accuracy		VSLICE	–5	—	5	%
Sampling Phase Adjustment[2]		PHASEADJ = 200–800 mV	-45°	—	45°	
LOS Threshold Dynamic Range		LOSLVL = 200–800 mV	10	—	50	mV pk-pk
LOS Threshold Offset[3] (referred to RXDIN)		LOSLVL = 200–800 mV	–500	—	500	μV
LOS Threshold Accuracy		VLOS	–5	—	5	%

Note:
1. Slice level (referred to RXDIN) is calculated as follows: VSLICE = (SLICE_LVL – 0.4 · VREF)/15.
2. Sample Phase Offset is calculated as follows: PHASE OFFSET = 45° (PHASEADJ – 0.4 · VREF)/0.3
3. LOS Threshold voltage (referred to RXDIN) is calculated as follows: VLOS = 30mV + (LOS_LVL – 0.4 · VREF)/15.

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Table 4. AC Characteristics (PLL Characteristics)

(V_{DD} = 1.8 V ± 5%, T_A = −40°C to 85°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Jitter Tolerance	$J_{TOL(PP)}$	f = 2.4 kHz	15	30	—	UI_{PP}
		f = 24 kHz	1.5	3.0	—	UI_{PP}
		f = 400 kHz	1.5	3.0	—	UI_{PP}
		f = 4 MHz	0.15	0.3	—	UI_{PP}
Acquisition Time	T_{AQ}		—	—	20	µs
Input Reference Clock Frequency	RC_{FREQ}	REFRATE = 1	—	622	667	MHz
		REFRATE = 0	—	155	167	MHz
Reference Clock Duty Cycle	RC_{DUTY}		40	50	60	%
Reference Clock Frequency Tolerance	RC_{TOL}		−100	—	100	ppm
Frequency Difference at which Receive PLL goes out of Lock (REFCLK compared to the divided down VCO clock)	LOL		TBD	600	1000	ppm
Frequency Difference at which Receive PLL goes into Lock (REFCLK compared to the divided down VCO clock)	LOCK		TBD	300	TBD	ppm
Note: Bellcore specifications: GR-1377-CORE, Issue 5, December 1998.						

Table 5. Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to TBD	V
LVTTL Input Voltage	V_{DD33}	−0.5 to 3.6	V
Differential Input Voltages	V_{DIF}	−0.3 to (V_{DD}+ 0.3)	V
Maximum Current any output PIN		±50	mA
Operating Junction Temperature	T_{JCT}	−55 to 150	°C
Storage Temperature Range	T_{STG}	−55 to 150	°C
Package Temperature (soldering 10 seconds)		275	°C
ESD HBM Tolerance (100 pf, 1.5 kΩ)		TBD	V
Note: Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.			

Table 6. Thermal Characteristics

Parameter	Symbol	Test Condition	Value	Unit
Thermal Resistance Junction to Ambient	φ_{JA}	Still Air	38	°C/W

Functional Description

The Si5530 is a high performance, low power, fully integrated receiver for SONET/SDH applications operating at OC-192/STM-64 data rates. It saves board space by integrating a limiting amplifier, clock and data recovery unit, and a demultiplexer into a small 99-pin BGA package. Further space savings are realized because no external loop filter components are required to support CDR operation. The Si5530 also provides a low-speed LVDS interface that is compliant to the Optical Interface Forums SFI-4 standard.

To support long haul transmission applications, operation at data rates up to 10.7 Gbps is supported to accommodate forward error correction (FEC). In addition, programmable data slicing and sampling phase adjustment are provided to support bit-error-rate (BER) optimization.

Limiting Amplifier

The Si5530 incorporates a high sensitivity limiting amplifier with sufficient gain to directly accept the output of transimpedance amplifiers. High sensitivity is achieved by using a digital calibration algorithm to cancel out amplifier offsets. This algorithm achieves superior offset cancellation by using statistical averaging to remove noise that can degrade more traditional calibration routines.

The limiting amplifier provides sufficient gain to fully saturate with input signals that are less than 20 mV peak-to-peak differential. In addition, input signals that exceed 1 V peak-to-peak differential will not cause any performance degradation.

Loss-of-Signal Detection

The limiting amplifier includes circuitry that generates a loss-of-signal ($\overline{LOS}$) alarm when the input signal amplitude on RXDIN falls below an externally controlled threshold. The Si5530 can be configured to drive the $\overline{LOS}$ output low when the differential input amplitude drops below a threshold set between ~10 mV and 50 mV pk-pk differential. Approximately 3 dB of hysteresis prevents unnecessary switching on $\overline{LOS}$.

The LOS threshold is set by applying a voltage between 0.20 V and 0.80 V to the LOSLVL input. The voltage present on LOSLVL maps to an input signal threshold as follows:

$$V_{LOS} = \frac{(V_{LOSLVL} - 0.4xVREF)}{15} + 30 \text{ mV}$$

V_{LOS} is the differential pk-pk LOS threshold referred to the RXDIN input, V_{LOSLVL} is the voltage applied to the LOSLVL pin, and VREF is reference voltage output on the VREF pin.

The LOS detection circuitry is disabled by tieing the LOSLVL input to the supply (VDD). This forces the LOS output high.

Slicing Level Adjustment

To support applications that require BER optimization, the limiting amplifier provides circuitry that supports adjustment of the 0/1 decision threshold (slicing level) over a range of ±20 mV when referred to the RXDIN input. The slicing level is set by applying a voltage between 0.20 V and 0.80 V to the SLICELVL input. The voltage present on SLICELVL sets the slicing level as follows:

$$V_{LEVEL} = \frac{(V_{SLICE} - 0.4xVREF)}{15}$$

V_{LEVEL} is the slicing level referred to the RXDIN input, V_{SLICE} is the voltage applied to the SLICE_LVL pin, and VREF is reference voltage output on the VREF pin.

The slicing level adjustment may be disabled by tieing the SLCLVL input to the supply (VDD). When slicing is disabled, the slicing offset is set to 0.0 V relative to internally biased input common mode voltage for RXDIN.

Clock and Data Recovery (CDR)

The Si5530 uses an integrated CDR to recover clock and data from a non-return to zero (NRZ) signal input on RXDIN. The recovered data clock is used to regenerate the incoming data by sampling the output of the limiting amplifier at the center of the NRZ bit period. The recovered clock and data is then deserialized by a 1:16 demultiplexer and output via a LVDS compatible low speed interface (RXDOUT[15:0], RXCLK1, and RXCLK2).

Sample Phase Adjustment

In applications where it is not desirable to recover data by sampling in the center of the data eye, the Si5530 supports adjustment of the CDR sampling phase across the NRZ data period. When sample phase adjustment is enabled, the sampling instant used for data recovery can be moved over a range of ±45° relative to the center of the incoming NRZ bit period. Adjustment of the sampling phase is desirable when data eye distortions are introduced by the transmission medium.

The sample phase is set by applying a voltage between 0.20 V and 0.80 V to the PHASEADJ input. The voltage present on PHASEADJ maps to sample phase offset as follows:

$$PhaseOffset = \frac{45° \times (V_{PHASE} - 0.4 \times VREF)}{0.30}$$

Phase Offset is the sampling offset in degrees from the center of the data eye, V_{PHASE} is the voltage applied to the PHASEADJ pin, and VREF is reference voltage output on the VREF pin. A positive phase offset will adjust the sampling point to lead the default sampling point at the center of the data eye, and a negative phase offset will adjust the sampling point to lag the default sampling point.

Data recovery using a sampling phase offset is disabled by tieing the PHASEADJ input to the supply (VDD). This forces a default phase offset of 0° to be used for data recovery.

Lock Detect

The Si5530 provides lock-detect circuitry that indicates whether the PLL has achieved frequency lock with the incoming data. This circuit compares the frequency of a divided down version of the recovered clock with the frequency of the supplied reference clock (REFCLK). If the recovered clock frequency deviates from that of the reference clock by the amount specified in Table 4 on page 7, the PLL is declared out of lock, and the loss-of-lock ($\overline{RXLOL}$) pin is asserted. In this state, the PLL will try to reacquire lock with the incoming data stream. During reacquisition, the recovered clock frequency (RXCLK1 and RXCLK2) will drift over a 1% range relative to the supplied reference clock. The $\overline{RXLOL}$ output will remain asserted until the recovered clock frequency is within the REFCLK frequency by the amount specified in Table 4 on page 7.

Lock-to-Reference

In applications where it is desirable to maintain a stable output clock during an alarm condition like loss-of-signal, the lock-to-reference input ($\overline{LTR}$) can be used to force a stable output clock. When $\overline{LTR}$ is asserted, the CDR is prevented from acquiring the data signal and the CDR will lock the RXCLKOUT1 and RXCLKOUT2 outputs to the provided REFCLK. In typical applications, the $\overline{LOS}$ output would be tied to the $\overline{LTR}$ input to force a stable output clock.

Reference Clock

The CDR within the Si5530 uses a reference clock to center the PLL frequency so that it is close enough to the data frequency to achieve lock. The device is designed to operate with reference clock sources that are either 1/16th or 1/64th the input data rate. The Si5530 will operate with data streams between 9.9 Gbps and 10.7 Gbps and the reference clock should be scaled accordingly. For example, to support 10.66 Gbps operation the REFCLK frequencies would be approximately 166 MHz or 666 MHz. The REFRATE input pin is used to configure the device for operation with one of the two supported reference clock submultiples of the data rate.

Deserialization

The Si5530 uses a 1:16 demultiplexer to deserialize the high-speed input. The deserialized data is output on a 16-bit parallel data bus RXDOUT[15:0] synchronous with the rising edge of RXCLK1. This clock output is derived by dividing down the recovered clock by a factor of 16.

Serial Input to Parallel Output Relationship

The Si5530 provides the capability to select the order in which the received serial data is mapped to the parallel output bus RXDOUT[15:0]. The mapping of the receive bits to the output data word is controlled by the RXMSBSEL input. If RXMSBSEL is tied low, the first bit received is output on RXDOUT0 and the following bits are output in order on RXDOUT1 through RXDOUT15. If RXMSBSEL is tied high, the first bit received is output on RXDOUT15, and the following bits are output in order on RXDOUT14 through RXDOUT0.

Auxiliary Clock Output

To support the widest range of system timing configurations, a second clock output is provided on RXCLK2. This output can be configured to provide a clock that is a 1/16th or 1/64th submultiple of the high speed recovered clock. The divide factor used to generate RXCLK2 is controlled via the RXCLKDIV2 input as described in "Pin Descriptions: Si5530" on page 13. In applications which do not use RXCLK2, this output can be powered down by forcing the RSCLK2DSBL input high.

Data Squelch

During some system error conditions, such as LOS, it may be desirable to force the receive data output to zero in order to avoid propagation of erroneous data into the downstream electronics. In these applications, the Si5530 provides a data squelching control input, RXSQLCH. When this input is active low, the data on RXDOUT will be forced to 0.

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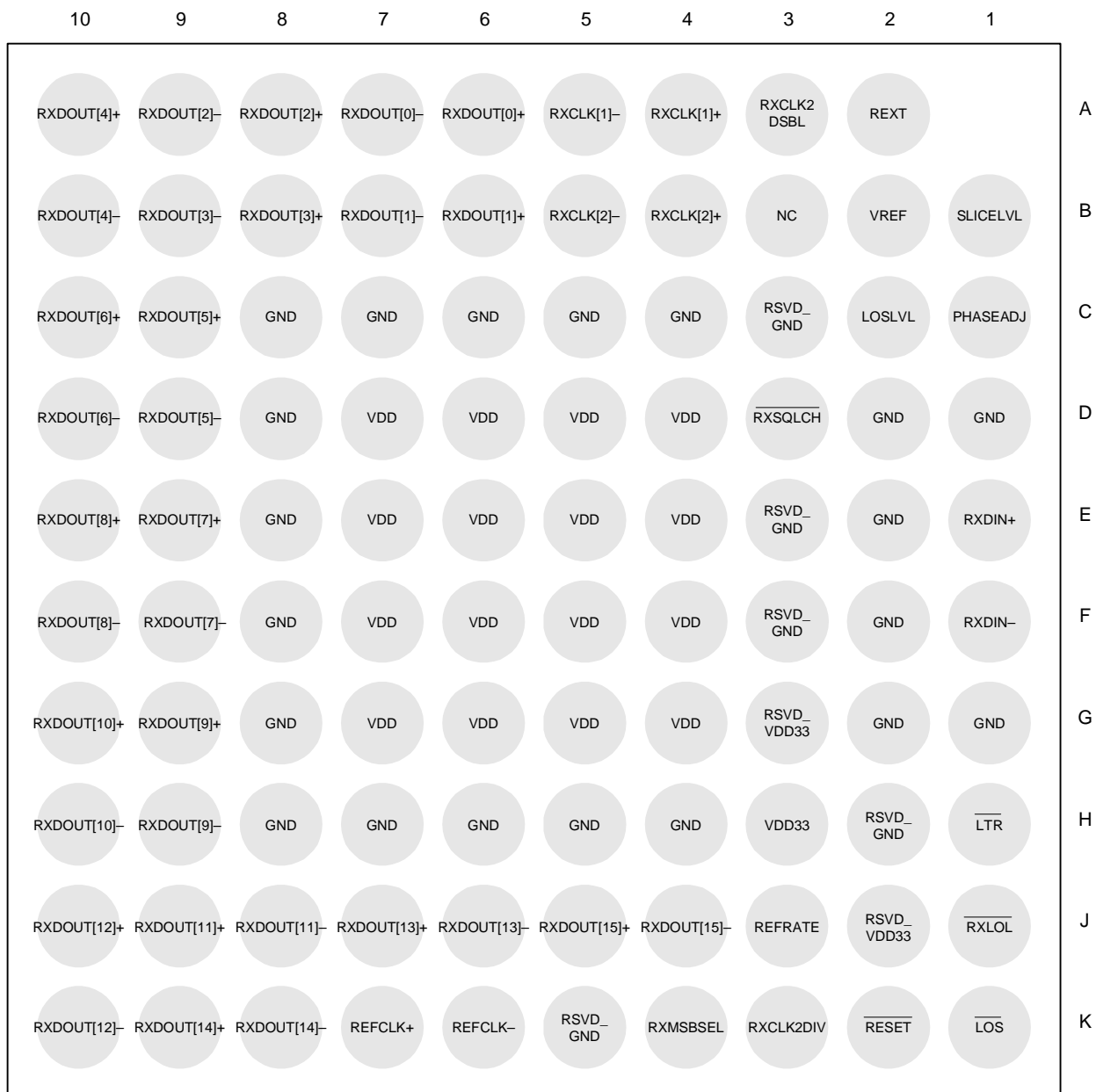
Bias Generation Circuitry

The Si5530 makes use of an external resistor to set internal bias currents. The external resistor allows precise generation of bias currents which significantly reduces power consumption versus traditional implementations that use an internal resistor. The bias generation circuitry requires a 3.09 kΩ (1%) resistor connected between REXT and GND.

Voltage Reference Output

The Si5530 provides an output voltage reference that can be used by an external circuit to set the LOS threshold, slicing level, or sampling phase adjust. One possible implementation would use a resistor divider to set the control voltage for LOSLVL, SLICELVL, or PHASEADJ. A second alternative would use a DAC to set the control voltage. Using this approach, VREF would be used to establish the range of a DAC output. The reference voltage is nominally 1.25 V.
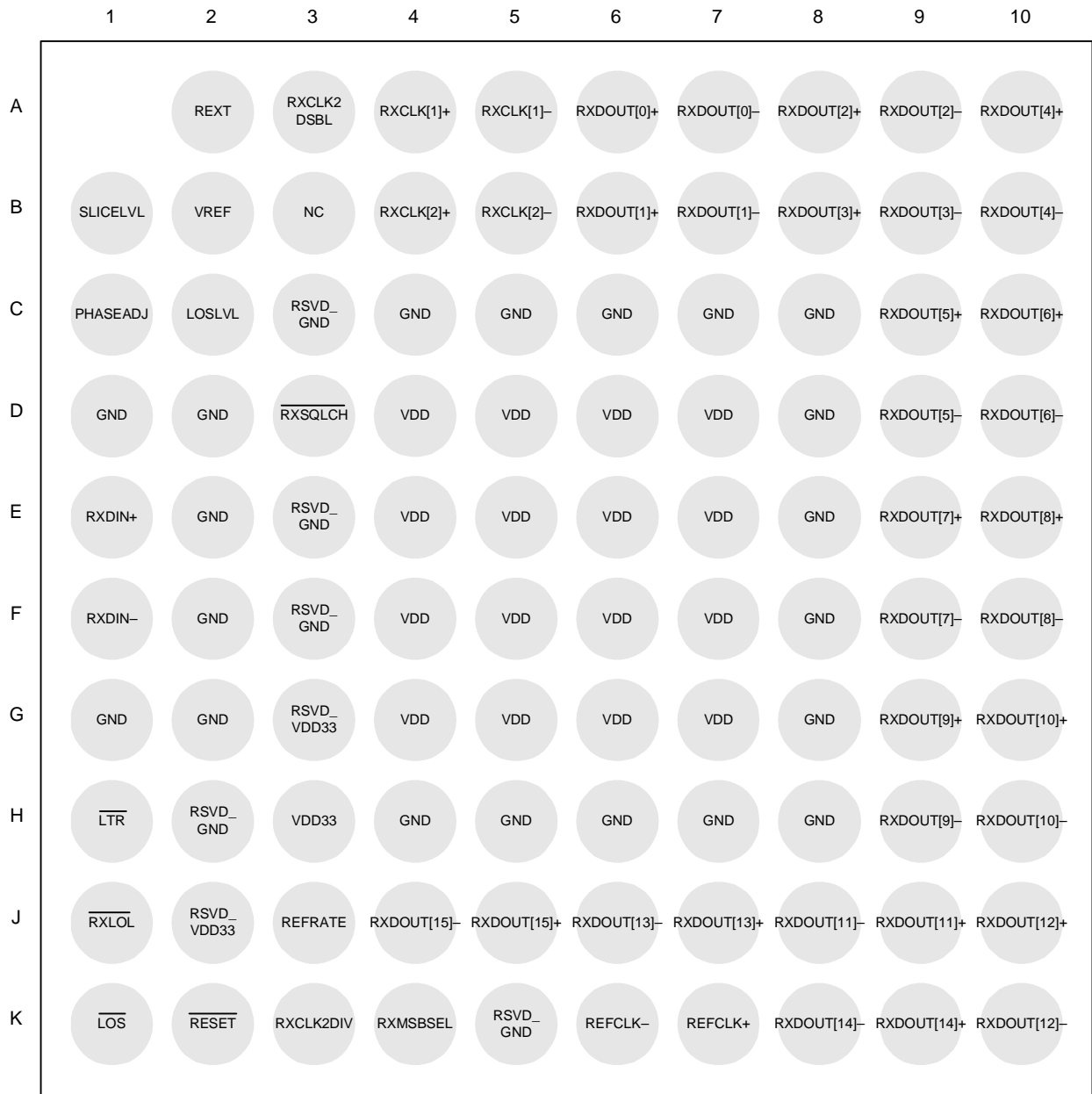
Si5530 Pinout: 99 BGA

	10	9	8	7	6	5	4	3	2	1	
A	RXDOUT[4]+	RXDOUT[2]–	RXDOUT[2]+	RXDOUT[0]–	RXDOUT[0]+	RXCLK[1]–	RXCLK[1]+	RXCLK2 DSBL	REXT		
B	RXDOUT[4]–	RXDOUT[3]–	RXDOUT[3]+	RXDOUT[1]–	RXDOUT[1]+	RXCLK[2]–	RXCLK[2]+	NC	VREF	SLICELVL	
C	RXDOUT[6]+	RXDOUT[5]+	GND	GND	GND	GND	GND	RSVD_GND	LOSLVL	PHASEADJ	
D	RXDOUT[6]–	RXDOUT[5]–	GND	VDD	VDD	VDD	VDD	$\overline{\text{RXSQLCH}}$	GND	GND	
E	RXDOUT[8]+	RXDOUT[7]+	GND	VDD	VDD	VDD	VDD	RSVD_GND	GND	RXDIN+	
F	RXDOUT[8]–	RXDOUT[7]–	GND	VDD	VDD	VDD	VDD	RSVD_GND	GND	RXDIN–	
G	RXDOUT[10]+	RXDOUT[9]+	GND	VDD	VDD	VDD	VDD	RSVD_VDD33	GND	GND	
H	RXDOUT[10]–	RXDOUT[9]–	GND	GND	GND	GND	GND	VDD33	RSVD_GND	$\overline{\text{LTR}}$	
J	RXDOUT[12]+	RXDOUT[11]+	RXDOUT[11]–	RXDOUT[13]+	RXDOUT[13]–	RXDOUT[15]+	RXDOUT[15]–	REFRATE	RSVD_VDD33	$\overline{\text{RXLOL}}$	
K	RXDOUT[12]–	RXDOUT[14]+	RXDOUT[14]–	REFCLK+	REFCLK–	RSVD_GND	RXMSBSEL	RXCLK2DIV	$\overline{\text{RESET}}$	$\overline{\text{LOS}}$	

Bottom View

Figure 4. Si5530 Pin Configuration (Bottom View)

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Top View

Figure 5. Si5530 Pin Configuration (Transparent Top View)

Pin Descriptions: Si5530

Pin Number(s)	Name	I/O	Signal Level	Description
C4–8, D8, D1–2, E8, E2, F8, F2, G8, G1–2, H4–8	GND	GND		**GND.**
K1	$\overline{\text{LOS}}$	O	LVTTL	**Loss-of-Signal.** This output is driven low when the peak-to-peak signal amplitude is below threshold set via LOSLVL.
C2	LOSLVL	I	—	**LOS Threshold Level.** Applying an analog voltage to this pin allows adjustment of the Threshold used to declare LOS. Tieing this input high disables LOS detection and forces the $\overline{\text{LOS}}$ output high.
H1	$\overline{\text{LTR}}$	I	LVTTL	**Lock-to-Reference.** This input forces a stable output clock by locking RXCLK1 and RXCLK2 to the provided reference. Driving LTR low activates this feature.
B3	NC			**No Connect.** Reserved for device testing leave electrically unconnected.
C1	PHASEADJ	I	—	**Sampling Phase Adjust.** Applying an analog voltage to this pin allows adjustment of the sampling phase across the data eye. Tieing this input high nominally centers the sampling phase.
K6–7	REFCLK–, REFCLK+	I	LVPECL	**Differential Reference Clock.** The reference clock sets the initial operating frequency used by the onboard PLL for clock and data recovery. The device will operate with reference frequencies that are 1/16th or 1/64th the input data rate (nominally 155 MHz or 622 MHz).
J3	REFRATE	I	LVTTL	**Reference Clock Select.** This input configures the Si5530 to operate with one of two reference clock frequencies. If REFSEL is held high, the device requires a reference clock that is 1/16 the input data rate. If REFSEL is low, a reference clock at 1/64 the input data rate is required.
K2	$\overline{\text{RESET}}$	I	LVTTL	**Device Reset.** Forcing this input low for a at least 1μs will cause a device reset. For normal operation, this pin should be held high.

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Pin Number(s)	Name	I/O	Signal Level	Description
A2	REXT			**External Bias Resistor.** This resistor is used by onboard circuitry to establish bias currents within the device. This pin must be connected to GND through a 3.09 kΩ (1%) resistor.
C3, E3, F3, H2, K5	RSVD_GND			**Reserved Tie to Ground.** Must tie directly to GND for proper operation.
G3, J2	RSVD_VDD33			**Reserved Tie to VDD33.** Must tie directly to VDD33 for proper operation.
A4–5	RXCLK1+, RXCLK1–	O	LVDS	**Differential Clock Output 1.** The clock recovered from the signal present on RXDIN is divided down by 16 and output on CLKOUT. In the absence of data, a stable clock on RXCLK1 can be maintained by asserting $\overline{LTR}$.
B4–5	RXCLK2+, RXCLK2–	O	LVDS	**Differential Clock Output 2.** An auxiliary output clock is provided on this pin that may be a divided down version of the high speed clock recovered from the signal present on RXDIN. The divide factor used in generating RXCLK2 is set via RXCLK2DIV.
K3	RXCLK2DIV	I	LVTTL	**Clock Divider Select.** This input selects the divide factor used to generate the RXCLK2 output. When this input is driven low, RXCLK2 is 1/16th the recovered high-speed clock. When driven high, RXCLK2 is 1/64th the recovered high speed clock rate.
A3	RXCLK2DSBL	I	LVTTL	**RXCLK2 Disable.** Driving this input high will disable the RXCLK2 output. This would be used to save power in applications that do not require an auxiliary clock.
E1, F1	RXDIN+, RXDIN–	I	High Speed Differential	**Differential Data Input.** Clock and data are recovered from the high speed data signal present on these pins.
A6–10, B6–10, C9–10, D9–10, E9–10, F9–10, G9–10, H9–10, J4–10, K8–10	RXDOUT[15:0]–, RXDOUT[15:0]+	O	LVDS	**Differential Parallel Data Output.** The data recovered from the signal present on RXDIN is demultiplexed and output as a 16-bit parallel word via RXDOUT[15:0]. These outputs are updated on the rising edge of RXCLK1.
J1	$\overline{RXLOL}$	O	LVTTL	**Loss-of-Lock.** This output is driven low when the recovered clock frequency deviates from the reference clock by the amount specified in Table 4.

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Pin Number(s)	Name	I/O	Signal Level	Description
K4	RXMSBSEL	I	LVTTL	**Data Bus Receive Order.** This determines the order of the received data bits on the output bus. For RXMSBSEL = 0, the first data bit received is output on RXDOUT[0] and following data bits are output on RDOUT[1] through RXDOUT[15]. For RXMSBSEL = 1, the first data bit is output on RXDOUT[15] and following data bits are output on RXDOUT[14] through RXDOUT[0].
D3	RXSQLCH	I	LVTTL	**Data Squelch.** When this input is low, the data on RXDOUT is forced to 0. Set RXSQLCH high for normal operation.
B1	SLICELVL	I	—	**Slicing Level Adjustment.** Applying an analog voltage to this pin allows adjustment of the slicing level applied to the input data eye. Tieing this input high nominally sets the slicing offset to 0.
D4–7, E4–7, F4–7, G4–7,	VDD	VDD	1.8 V	**Supply Voltage.** Nominally 1.8 V.
H3	VDD33	VDD33	1.8 V or 3.3 V	**Digital Output Supply.** Must be tied to either 1.8 V or 3.3 V. When tied to 3.3 V, LVTTL compatible output voltage swings on RXLOL and LOS are supported.
B2	VREF	O	Voltage Ref	**Voltage Reference.** The Si5600 provides an output voltage reference that can be used by an external circuit to set the LOS threshold, slicing level, or sampling phase adjustment. The equivalent resistance between this pin and GND should not be less than 10 kΩ. The reference voltage is nominally 1.25 V.

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Si5530

Ordering Guide

Table 7. Ordering Guide

Part Number	Package	Temperature
Si5530-BC	99 BGA	−40°C to 85°C

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Package Outline

Figure 6 illustrates the package details for the Si5530. Table 8 lists the values for the dimensions shown in the illustration.
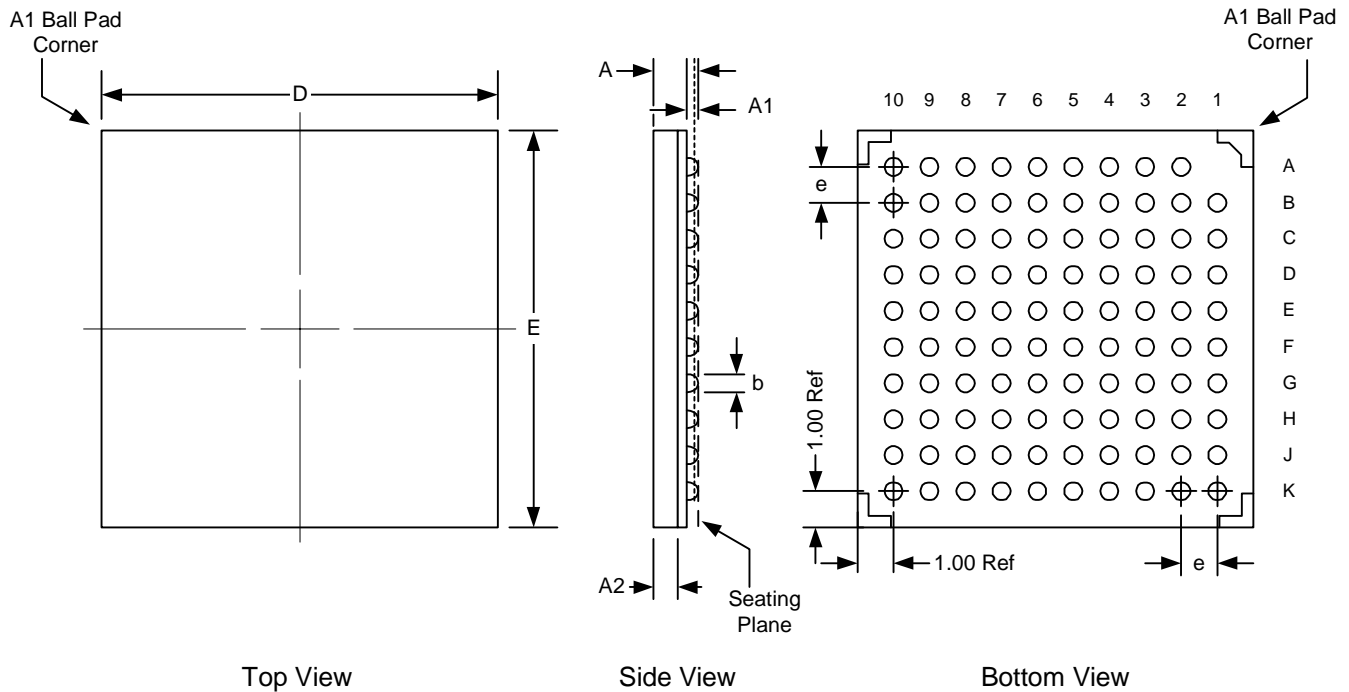

Figure 6. 99-Ball Grid Array (BGA)

Table 8. Package Diagram Dimensions

Symbol	Millimeters		
	Min	Nom	Max
A	1.30	1.40	1.50
A1	0.31	0.36	0.41
A2	0.65	0.70	0.75
b	—	0.46	—
D	—	11.00	—
E	—	11.00	—
e	—	1.00	—

SILICON LABORATORIES

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