

### 3.3V CMOS 1-TO-10 CLOCK DRIVER

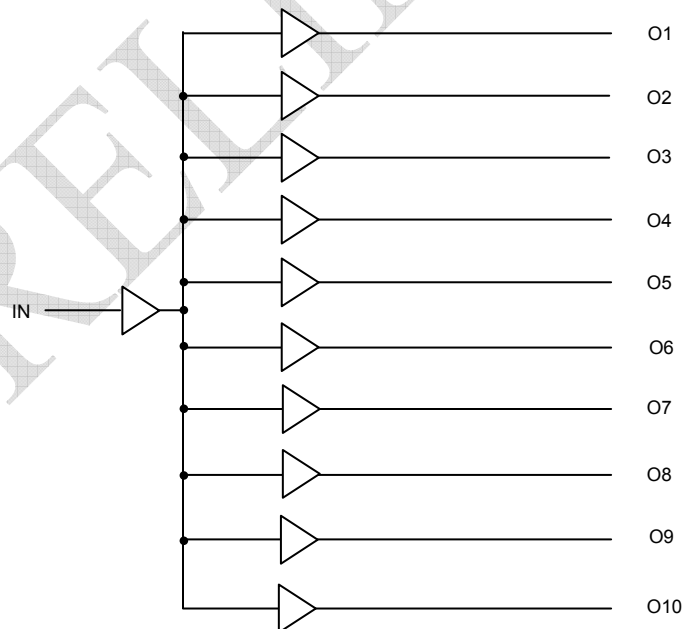
#### Features

- 0.5 MICRON CMOS Technology
- Guaranteed low skew < 350pS (max.)
- Very low duty cycle distortion < 350pS (max.)
- High speed: propagation delay < 3nS (max.)
- Very low CMOS power levels
- TTL compatible inputs and outputs
- 1:10 fanout
- Maximum output rise and fall time < 1.5nS (max.)
- Low input capacitance: 4.5pF typical
- Operates with 3.3V ± 0.3V Supply
- Inputs can be driven from 3.3V or 5V components
- Available in SSOP, SOIC, and QSOP Packages

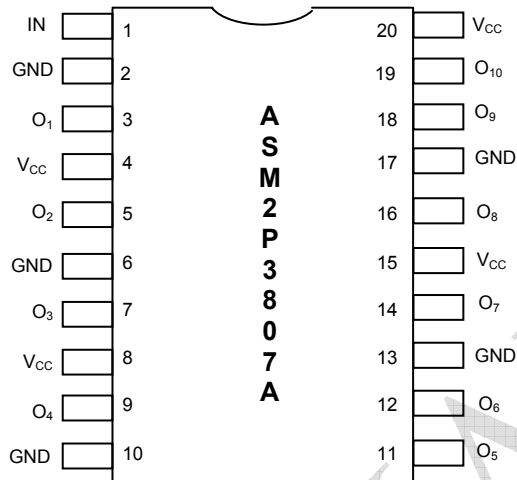
#### Product Description

The ASM2P3807A 3.3V clock driver is built using advanced dual metal CMOS technology. This low skew clock driver offers 1:10 fanout. The large fanout from a single input reduces loading on the preceding driver and provides an efficient clock distribution network. The ASM2P3807A offers low capacitance inputs with hysteresis for improved noise margins. Multiple power and grounds reduce noise. Typical applications are clock and signal distribution.

#### Block Diagram



**Pin Configuration**



SOIC / SSOP / QSOP Packages  
TOP VIEW

**Pin Description**

Pin#	Pin Names	Description
1	IN	Clock Inputs
3,5,7,9,11,12,14,16,18,19	O 1-O10	Clock Outputs
2,6,10,13,17	GND	Ground
4,8,15,20	Vcc	Power

**Absolute Maximum Ratings**

Symbol	Description	Max	Unit
$V_{TERM}^1$	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
$V_{TERM}^2$	Terminal Voltage with Respect to GND	-0.5 to +7	V
$V_{TERM}^3$	Terminal Voltage with Respect to GND	-0.5 to $V_{CC}+0.5$	V
$T_{STG}$	Storage Temperature	-65 to +150	° C
$I_{OUT}$	DC Output Current	-60 to +60	mA

Note: These are stress ratings only and are not implied for functional use. Exposure to absolute maximum ratings for prolonged periods of time may affect device reliability.

NOTES:

1.  $V_{CC}$  terminals.
2. Input terminals.
3. Outputs and I/O terminals.

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Capacitance ( $T_A = +25^\circ\text{C}$ ,  $f = 1.0\text{MHz}$ )

Symbol	Parameter <sup>1</sup>	Conditions	Typ	Max	Unit
$C_{IN}$	Input Capacitance	$V_{IN} = 0V$	4.5	6	pF
$C_{OUT}$	Output Capacitance	$V_{OUT} = 0V$	5.5	8	pF

Note: 1. This parameter is measured at characterization but not tested.

Power Supply Characteristics

Symbol	Parameter	Test Conditions <sup>1</sup>	Min	Typ <sup>2</sup>	Max	Unit
$\Delta I_{CC}$	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = V_{CC} - 0.6V^3$		10	30	$\mu\text{A}$
$I_{CCD}$	Dynamic Power Supply Current <sup>4</sup>	$V_{CC} = \text{Max.}$ Input toggling 50% Duty Cycle Outputs Open $V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$		0.31	0.45	mA/ MHz
$I_C$	Total Power Supply Current <sup>6</sup>	$V_{CC} = \text{Max.}$ Input toggling 50% Duty Cycle Outputs Open $V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$ $f_i = 50\text{MHz}$		15.5	22.8 <sup>5</sup>	mA

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.

2. Typical values are at  $V_{CC} = 3.3V$ ,  $+25^\circ\text{C}$  ambient.

3. Per TTL driven input ( $V_{IN} = V_{CC} - 0.6V$ ); all other inputs at  $V_{CC}$  or GND.

4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

5. Values for these conditions are examples of the  $I_C$  formula. These limits are guaranteed but not tested.

6.  $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$

$$I_C = I_{CC} + \Delta I_{CC} \text{ DHNT} + I_{CCD} (f_i)$$

$$I_{CC} = \text{Quiescent Current } (I_{CCL}, I_{CCH} \text{ and } I_{CCZ})$$

$$\Delta I_{CC} = \text{Power Supply Current for a TTL High Input } (V_{IN} = V_{CC} - 0.6V)$$

$$D_H = \text{Duty Cycle for TTL Inputs High}$$

$$N_T = \text{Number of TTL Inputs at } D_H$$

$$I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$$

$$f_i = \text{Input Frequency}$$

All currents are in milliamps and all frequencies are in megahertz.

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DC Electrical Characteristics over Operating Range

Following Conditions Apply Unless Otherwise Specified

Commercial:  $T_A = 0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$ , Industrial:  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$

Symbol	Parameter	Test Conditions <sup>1</sup>		Min	Typ	Max	Unit
$V_{IH}$	Input HIGH Level (Input pins)	Guaranteed Logic HIGH Level		2		5.5	V
	Input HIGH Level (I/O pins)			2		$V_{CC} + 0.5$	
$V_{IL}$	Input LOW Level (Input and I/O pins)	Guaranteed Logic LOW Level		-0.5		0.8	V
$I_{IH}$	Input HIGH Current (Input pins)	$V_{CC} = \text{Max}$	$V_I = 5.5\text{V}$			$\pm 1$	
	Input HIGH Current (I/O pins)		$V_I = V_{CC}$			$\pm 1$	$\mu\text{A}$
$I_{IL}$	Input LOW Current (Input pins)	$V_{CC} = \text{Max}$	$V_I = \text{GND}$			$\pm 1$	
	Input LOW Current (I/O pins)		$V_I = \text{GND}$			$\pm 1$	
$I_{OZH}$	High Impedance Output Current	$V_{CC} = \text{Max}$	$V_O = V_{CC}$			$\pm 1$	$\mu\text{A}$
$I_{OZL}$	(3-State Output Pins)		$V_O = \text{GND}$			$\pm 1$	
$V_{IK}$	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}$			-0.7	-1.2	V
$I_{ODH}$	Output HIGH Current	$V_{CC} = 3.3\text{V}, V_{IN} = V_{IH}$ or $V_{IL}, V_O = 1.5\text{V}^3$		-36	-60	-110	mA
$I_{ODL}$	Output LOW Current	$V_{CC} = 3.3\text{V}, V_{IN} = V_{IH}$ or $V_{IL}, V_O = 1.5\text{V}^3$		50	90	200	mA
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min.}, V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -0.1\text{mA}$	$V_{CC} - 0.2$			V
			$I_{OH} = -8\text{mA}$	$2.4^5$	3		
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{Min.}, V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 0.1\text{mA}$			0.2	V
			$I_{OL} = 16\text{mA}$		0.2	0.4	
			$I_{OL} = 24\text{mA}$		0.3	0.5	
$I_{OFF}$	Input Power Off Leakage	$V_{CC} = 0\text{V}, V_{IN} = 4.5\text{V}$				$\pm 1$	$\mu\text{A}$
$I_{OS}$	Short Circuit Current <sup>4</sup>	$V_{CC} = \text{Max.}, V_O = \text{GND}^3$		-60	-135	-240	mA
$V_H$	Input Hysteresis	-			150		mV
$I_{CCL}$ $I_{CCH}$ $I_{CCZ}$	Quiescent Power Supply Current	$V_{CC} = \text{Max.}, V_{IN} = \text{GND}$ or $V_{CC}$			0.1	10	$\mu\text{A}$

NOTES:

1. For conditions shown as Max or Min, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at  $V_{CC} = 3.3\text{V}, +25^{\circ}\text{C}$  ambient.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not tested.
5.  $V_{OH} = V_{CC} - 0.6\text{V}$  at rated current.

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Switching Characteristics Over Operating Range – Commercial<sup>3,4</sup>

Symbol	Parameter	Conditions <sup>1</sup>	ASM2P3807A		Unit
			Min <sup>2</sup>	Max	
t <sub>PLH</sub>	Propagation Delay	50Ω to V <sub>CC</sub> /2 C <sub>L</sub> = 10pF (See figure 1) or 10Ω AC termination, C <sub>L</sub> = 50pF (See figure 2) f ≤ 100MHz Outputs connected in groups of two	1.5	3	nS
t <sub>PHL</sub>					
t <sub>R</sub>	Output Rise Time		1.5	nS	
t <sub>F</sub>	Output Fall Time		1.5	nS	
t <sub>SK(O)</sub>	Output skew: skew between outputs of same package (same transition)		0.35	nS	
t <sub>SK(P)</sub>	Pulse skew: skew between opposite transitions of same output ( t <sub>PHL</sub> – t <sub>PLH</sub>  )		0.35	nS	
t <sub>SK(T)</sub>	Package skew: skew between outputs of different packages at same power supply voltage, temperature, package type and speed grade	0.65	nS		

PRELIMINARY

Symbol	Parameter	Conditions <sup>1</sup>	ASM2P3807A		Unit
			Min <sup>2</sup>	Max	
t <sub>PLH</sub>	Propagation Delay	C <sub>L</sub> = 30pF f ≤ 67MHz (See figure 3)	1.5	4	nS
t <sub>PHL</sub>					
t <sub>R</sub>	Output Rise Time		1.5	nS	
t <sub>F</sub>	Output Fall Time		1.5	nS	
t <sub>SK(O)</sub>	Output skew: skew between outputs of same package (same transition)		0.45	nS	
t <sub>SK(P)</sub>	Pulse skew: skew between opposite transitions of same output ( t <sub>PHL</sub> - t <sub>PLH</sub>  )		0.45	nS	
t <sub>SK(T)</sub>	Package skew: skew between outputs of different packages at same power supply voltage, temperature, package type and speed grade		0.75	nS	

Symbol	Parameter	Conditions <sup>1</sup>	ASM2P3807A		Unit
			Min <sup>2</sup>	Max	
t <sub>PLH</sub>	Propagation Delay	C <sub>L</sub> = 50pF f ≤ 40MHz (See figure 4)	1.5	4.3	nS
t <sub>PHL</sub>					
t <sub>R</sub>	Output Rise Time		1.5	nS	
t <sub>F</sub>	Output Fall Time		1.5	nS	
t <sub>SK(O)</sub>	Output skew: skew between outputs of same package (same transition)		0.35	nS	
t <sub>SK(P)</sub>	Pulse skew: skew between opposite transitions of same output ( t <sub>PHL</sub> - t <sub>PLH</sub>  )		0.35	nS	
t <sub>SK(T)</sub>	Package skew: skew between outputs of different packages at same power supply voltage, temperature, package type and speed grade		0.75	nS	

NOTES:1. See test circuits and waveforms.

2. Minimum limits are guaranteed but not tested on Propagation Delays.

3. t<sub>PLH</sub>, t<sub>PHL</sub>, t<sub>SK(O)</sub> are production tested. All other parameters guaranteed but not production tested.

4. Propagation delay range indicated by Min. and Max. limit is due to V<sub>CC</sub>, operating temperature and process parameters. These propagation delays limits do not imply skew.

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Switching Characteristics Over Operating Range - Industrial<sup>3,4</sup>

Symbol	Parameter	Conditions <sup>1</sup>	ASM2P3807A		Unit	
			Min <sup>2</sup>	Max		
t <sub>PLH</sub>	Propagation Delay	50Ω to V <sub>CC</sub> /2 C <sub>L</sub> = 10pF (See figure 1) or 50Ω AC termination, C <sub>L</sub> = 10pF (See figure 2) f ≤ 100MHz Outputs connected in groups of two	1.5	3	nS	
t <sub>PHL</sub>						
t <sub>R</sub>	Output Rise Time			1.5	nS	
t <sub>F</sub>	Output Fall Time			1.5	nS	
t <sub>SK(O)</sub>	Output skew: skew between outputs of same package (same transition)				0.45	nS
t <sub>SK(P)</sub>	Pulse skew: skew between opposite transitions of same output ( t <sub>PHL</sub> - t <sub>PLH</sub>  )				0.45	nS
t <sub>SK(T)</sub>	Package skew: skew between outputs of different packages at same power supply voltage, temperature, package type and speed grade				0.65	nS

Symbol	Parameter	Conditions <sup>1</sup>	ASM2P3807A		Unit	
			Min <sup>2</sup>	Max		
t <sub>PLH</sub>	Propagation Delay	C <sub>L</sub> = 30pF f ≤ 67MHz (See figure 3)	1.5	4	nS	
t <sub>PHL</sub>						
t <sub>R</sub>	Output Rise Time			1.5	nS	
t <sub>F</sub>	Output Fall Time			1.5	nS	
t <sub>SK(O)</sub>	Output skew: skew between outputs of same package (same transition)				0.45	nS
t <sub>SK(P)</sub>	Pulse skew: skew between opposite transitions of same output ( t <sub>PHL</sub> - t <sub>PLH</sub>  )				0.45	nS
t <sub>SK(T)</sub>	Package skew: skew between outputs of different packages at same power supply voltage, temperature, package type and speed grade				0.75	nS

Symbol	Parameter	Conditions <sup>1</sup>	ASM2P3807A		Unit	
			Min <sup>2</sup>	Max		
t <sub>PLH</sub>	Propagation Delay	C <sub>L</sub> = 50pF f ≤ 40MHz (See figure 4)	1.5	4.3	nS	
t <sub>PHL</sub>						
t <sub>R</sub>	Output Rise Time			1.5	nS	
t <sub>F</sub>	Output Fall Time			1.5	nS	
t <sub>SK(O)</sub>	Output skew: skew between outputs of same package (same transition)				0.45	nS
t <sub>SK(P)</sub>	Pulse skew: skew between opposite transitions of same output ( t <sub>PHL</sub> - t <sub>PLH</sub>  )				0.45	nS
t <sub>SK(T)</sub>	Package skew: skew between outputs of different packages at same power supply voltage, temperature, package type and speed grade			0.75	nS	

NOTES:1. See test circuits and waveforms.

2. Minimum limits are guaranteed but not tested on Propagation Delays.

3. t<sub>PLH</sub>, t<sub>PHL</sub>, t<sub>SK(O)</sub> are production tested. All other parameters guaranteed but not production tested.

4. Propagation delay range indicated by Min and Max limit is due to V<sub>CC</sub>, operating temperature and process parameters. These propagation delay limits do not imply skew.



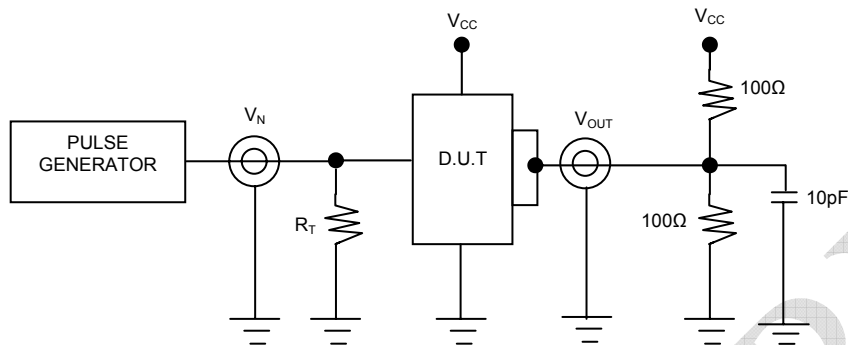


Figure 1.  $Z_o = 50\Omega$  to  $V_{cc}/2$ ,  $C_L = 10pF$

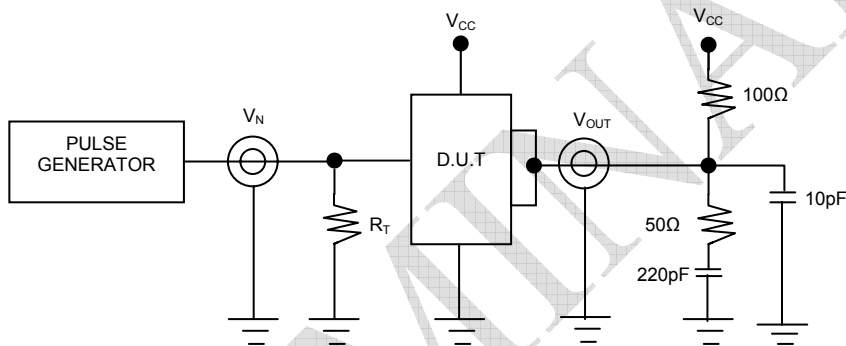


Figure 2.  $Z_o = 50\Omega$  AC Termination,  $C_L = 10pF$

The capacitor value for ac termination is determined by the operating frequency. For very low frequencies a higher capacitor value should be selected.

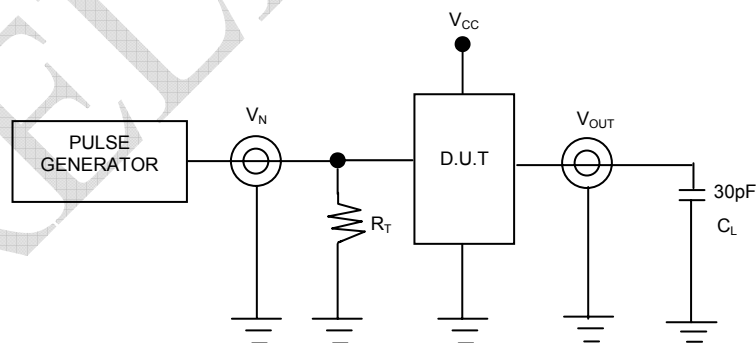
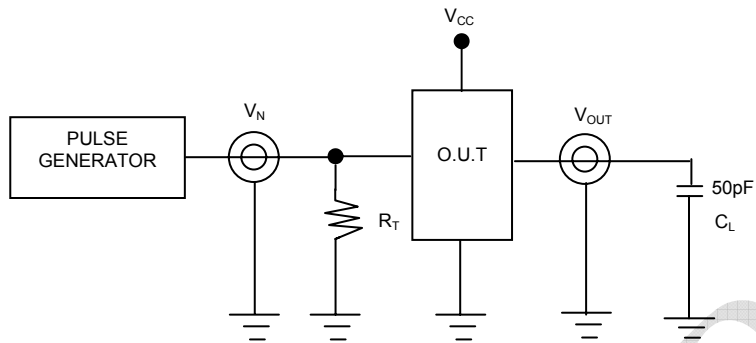
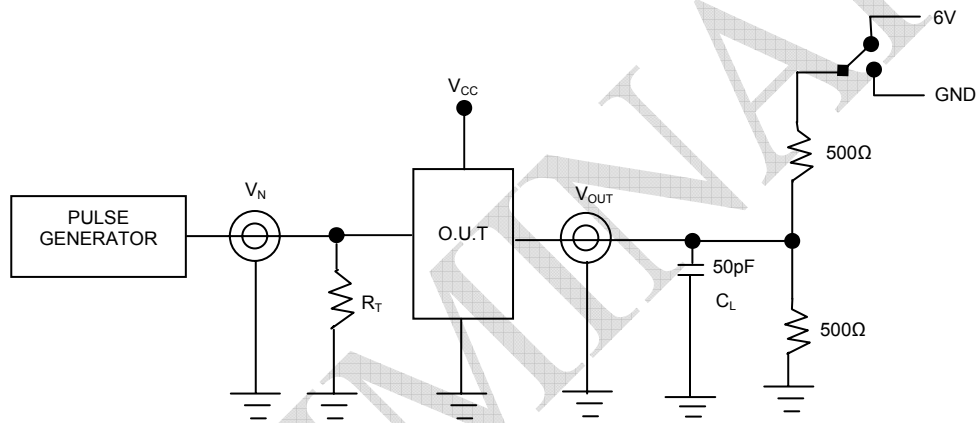


Figure 3.  $C_L = 30pF$  Circuit



**Figure 3.  $C_L = 50\text{pF}$  Circuit**



**Figure 5. Enable and Disable Time Circuit**

Enable and Disable Time

Switch Position

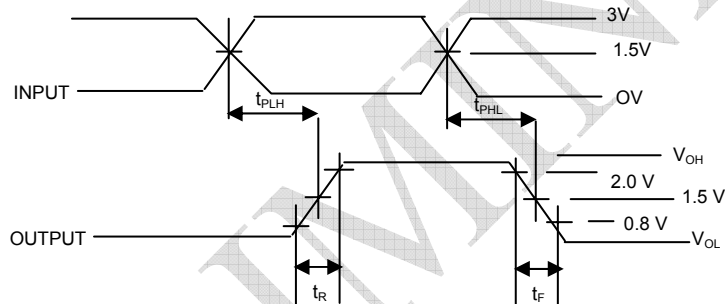
Test	Switch
Disable LOW	6V
Enable LOW	
Disable HIGH	GND
Enable HIGH	

DEFINITIONS:

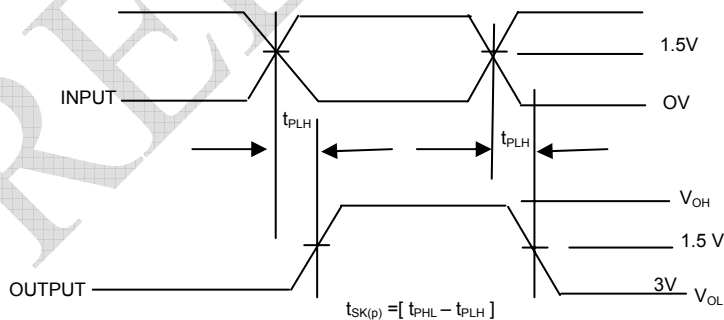
$C_L$  = Load capacitance: includes jig and probe capacitance.

$R_T$  = Termination resistance: should be equal to  $Z_{OUT}$  of the Pulse Generator.

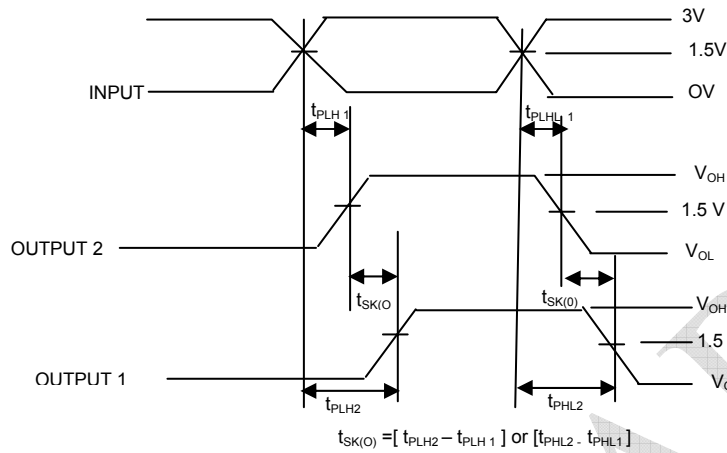
Test Waveforms



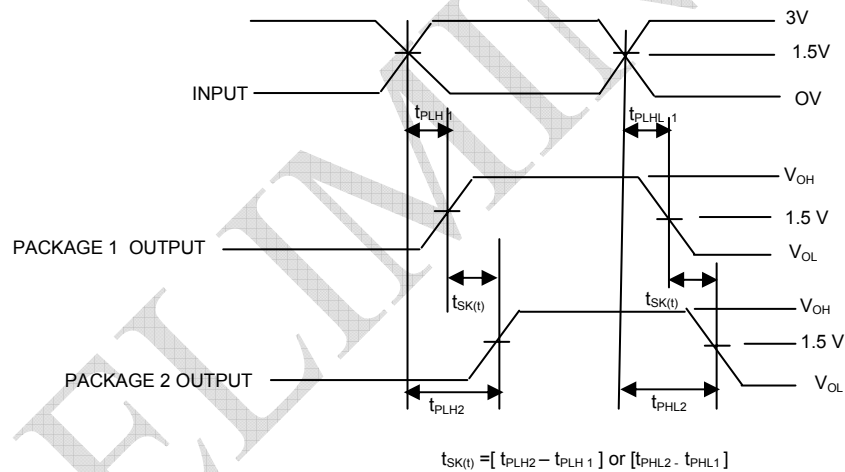
Package Delay



Pulse Skew -  $t_{SK(P)}$

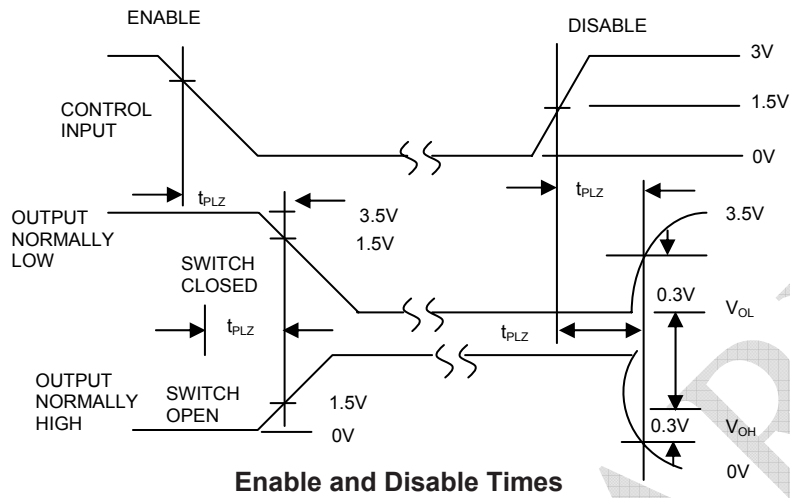


**Output Skew -  $t_{SK(O)}$**



**Package Skew -  $t_{SK(T)}$**

Package 1 and Package 2 are same device type and speed grade



- NOTES: 1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH  
 2. Pulse Generator for All Pulses:  $f \leq 1.0\text{MHz}$ ;  $t_f \leq 2.5\text{nS}$ ;  $t_r \leq 2.5\text{nS}$

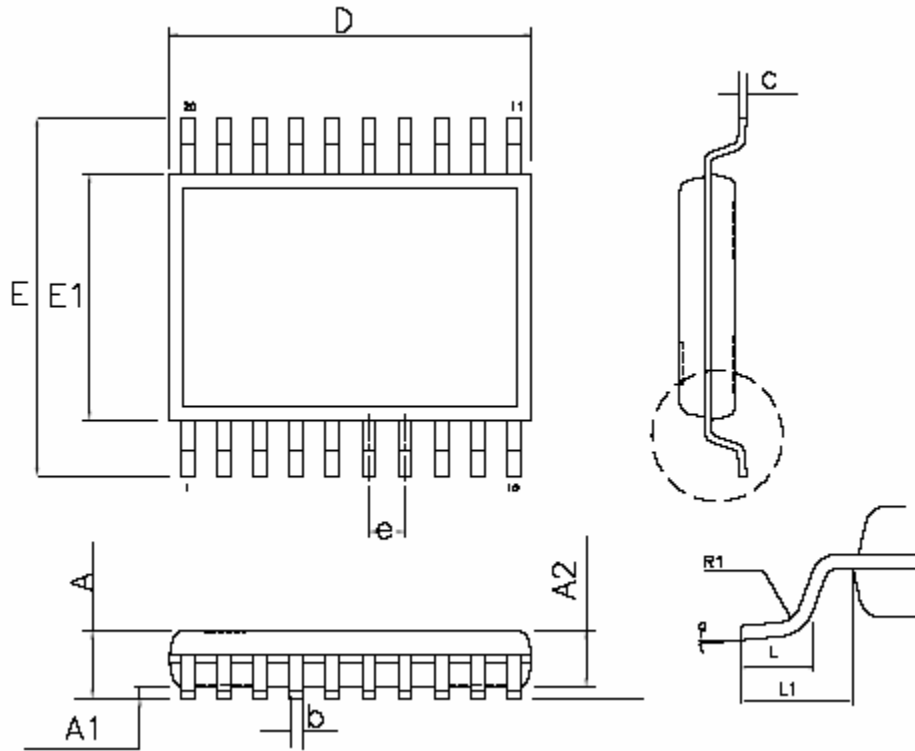
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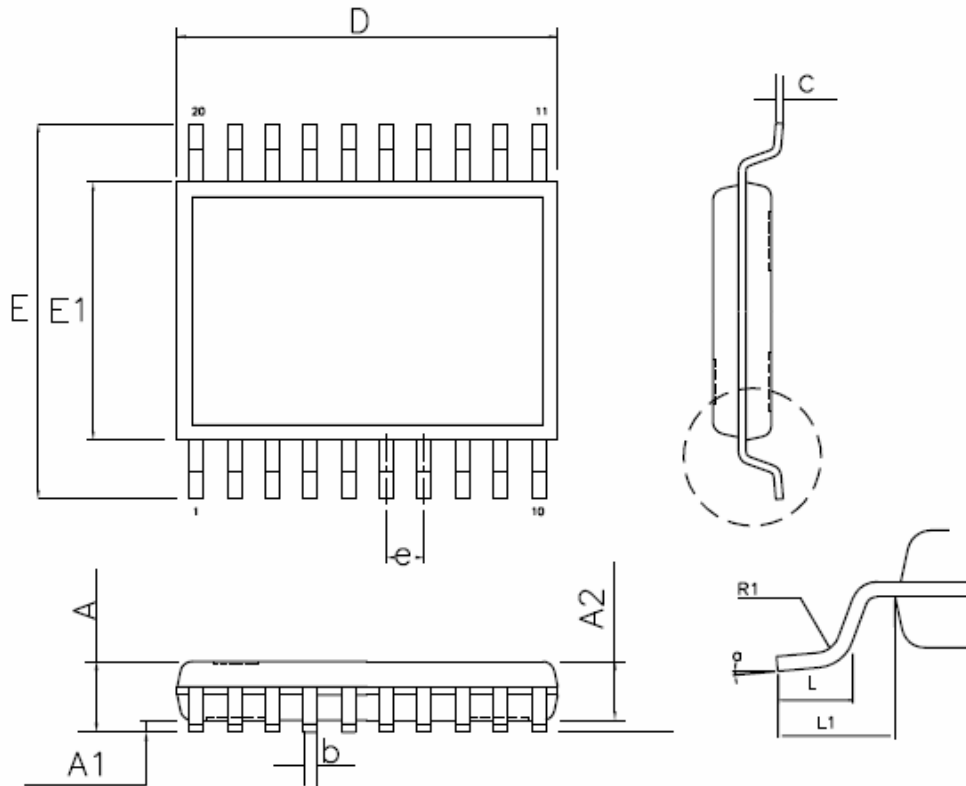
Package Information

20-lead SSOP ( 150 mil )



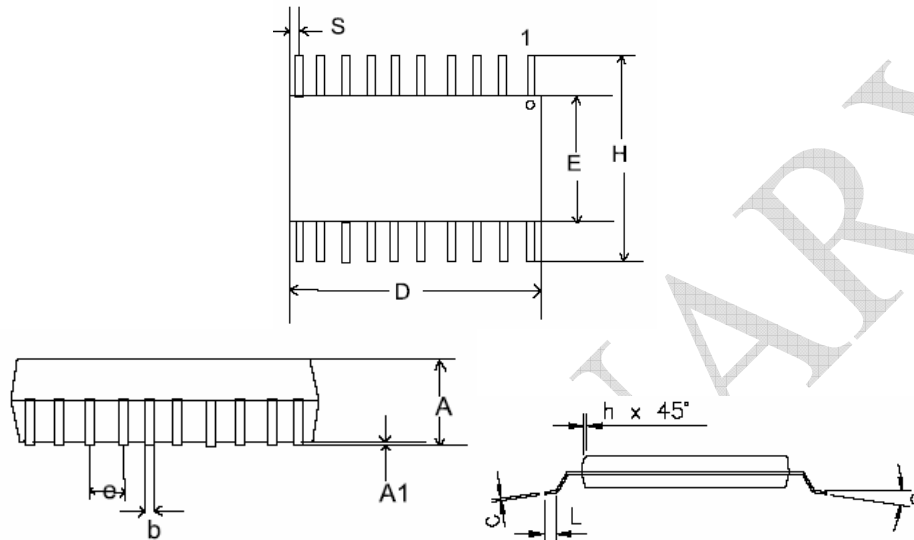
Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	0.053	0.069	1.346	1.753
A1	0.004	0.010	0.102	0.254
A2	....	0.059	....	1.499
D	0.337	0.344	8.560	8.738
c	0.007	0.011	0.178	0.274
E	0.228	0.244	5.791	6.198
E1	0.150	0.157	3.810	3.988
L	0.016	0.035	0.406	0.890
L1	0.010 BASIC		0.254 BASIC	
b	0.008	0.014	0.203	0.356
R1	0.003	....	0.08	....
a	0°	8°	0°	8°
e	0.025 BASIC		0.635 BASIC	

20L SOIC Package (300 mil)



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
A2	0.088	0.094	2.25	2.40
D	0.496	0.512	12.60	13.00
L	0.016	0.050	0.40	1.27
E1	0.291	0.299	7.40	7.60
R1	0.003	....	0.08	.....
b	0.013	0.022	0.33	0.56
c	0.009	0.015	0.23	0.38
E	0.394	0.419	10.00	10.65
e	0.050 BSC		1.27 BSC	
a	0°	8°	0°	8°

20-lead QSOP Package



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	0.060	0.068	1.52	1.73
A1	0.004	0.008	0.10	0.20
b	0.009	0.012	0.23	0.30
c	0.007	0.010	0.18	0.25
D	0.337	0.344	8.56	8.74
E	0.150	0.157	3.81	3.99
e	0.025 BSC		0.64 BSC	
H	0.230	0.244	5.84	6.20
h	0.010	0.016	0.25	0.41
L	0.014	0.030	0.35	0.75
S	0.056	0.060	1.42	1.52
a	0°	8°	0°	8°



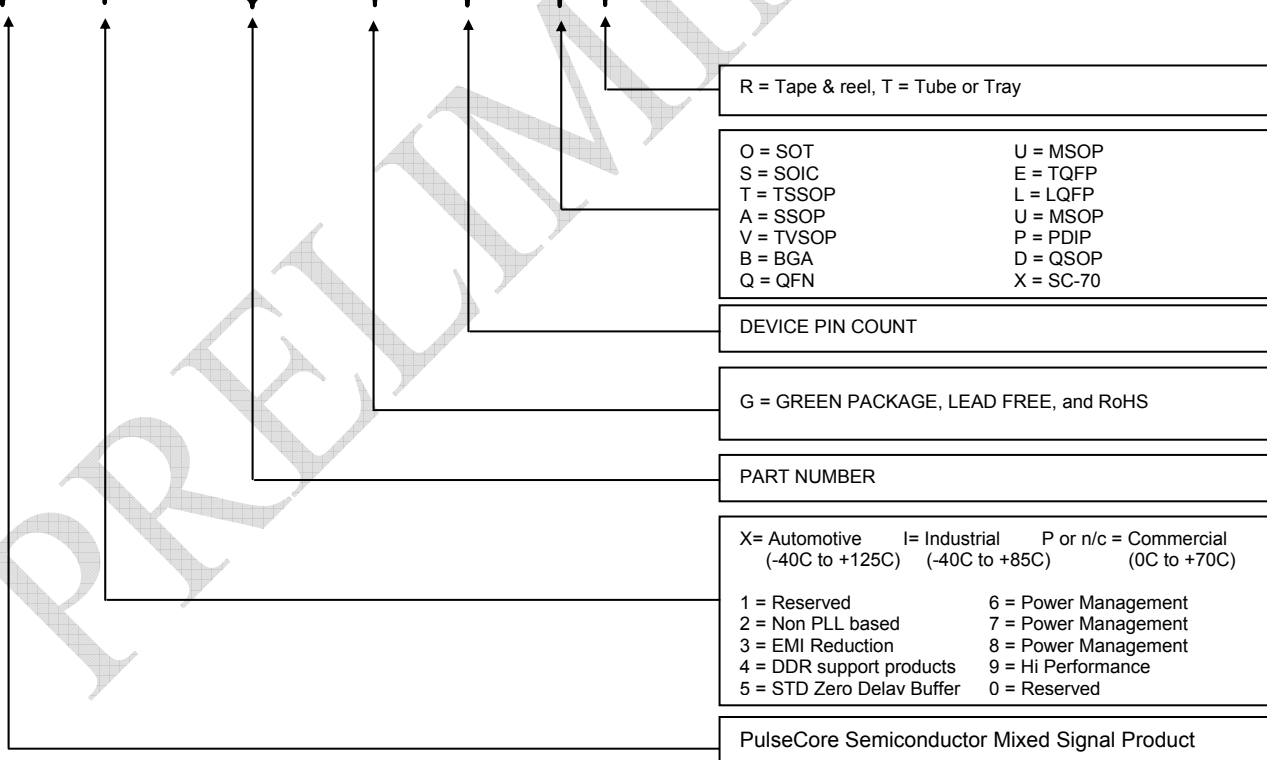
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Ordering Information

Part Number	Marking	Package Type	Temperature
ASM2P3807AG-20-AR	2P3807AG	20-Pin SSOP, TAPE & REEL, Green	Commercial
ASM2P3807AG-20-AT	2P3807AG	20-Pin SSOP, TUBE, Green	Commercial
ASM2P3807AG-20-DR	2P3807AG	20-Pin QSOP, TAPE & REEL, Green	Commercial
ASM2P3807AG-20-DT	2P3807AG	20-Pin QSOP, TUBE, Green	Commercial
ASM2P3807AG-20-SR	2P3807AG	20-Pin SOIC, TAPE & REEL, Green	Commercial
ASM2P3807AG-20-ST	2P3807AG	20-Pin SOIC, TUBE, Green	Commercial
ASM2I3807AG-20-AR	2I3807AG	20-Pin SSOP, TAPE & REEL, Green	Industrial
ASM2I3807AG-20-AT	2I3807AG	20-Pin SSOP, TUBE, Green	Industrial
ASM2I3807AG-20-DR	2I3807AG	20-Pin QSOP, TAPE & REEL, Green	Industrial
ASM2I3807AG-20-DT	2I3807AG	20-Pin QSOP, TUBE, Green	Industrial
ASM2I3807AG-20-SR	2I3807AG	20-Pin SOIC, TAPE & REEL, Green	Industrial
ASM2I3807AG-20-ST	2I3807AG	20-Pin SOIC, TUBE, Green	Industrial

Device Ordering Information

A S M 2 P 3 8 0 7 A G - 2 0 - A T



Licensed under US patent Nos 5,488,627 and 5,631,920.



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Preliminary Information  
Part Number: ASM2P3807A  
Document Version: v0.3

Note: This product utilizes US Patent # 6,646,463 Impedance Emulator Patent issued to PulseCore Semiconductor, dated 11-11-2003

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