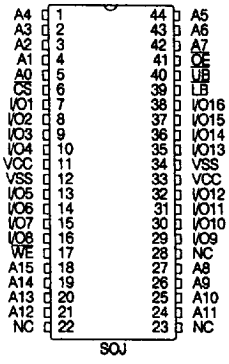
DESCRIPTION

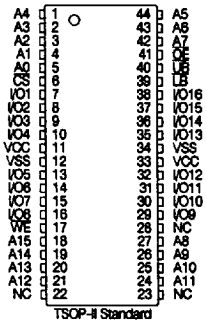
The HY6316100 is a 1,048,576-bit high-speed Static Random Access Memory organized as 65,536 words by 16 bits. The HY6316100 uses sixteen common input and output lines and has an output enable pin which operates faster than address access time at read cycle. The device is fabricated using HYUNDAI's advanced CMOS process and designed for high-speed circuit technology. It is particulary well suited for used in high-density high speed system applications.

FEATURES

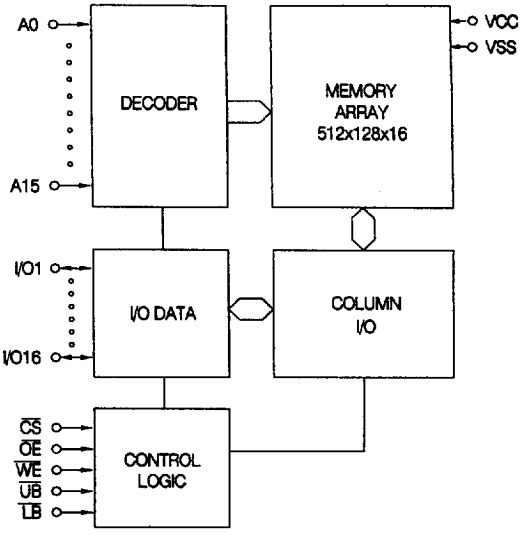
- **High speed - 15/17/20/25ns**
- **Low power consumption**
  - **HY6316100S**
    Active : 260mA(Max.)
    Standby(TTL) : 50mA(Max.)
    (CMOS) : 2mA(Max.)
  - **HY6316100L**
    Active : 260mA(Max.)
    Standby(TTL) : 50mA(Max.)
    (CMOS) : 100μA (Max.)
- **Single 5V±10% Power Supply**
- **TTL compatible inputs and outputs**
- **400-mil 44-pin plastic SOJ packaging**
- **400-mil 44-pin plastic TSOP-II packaging**

PIN CONNECTION





BLOCK DIAGRAM



PIN DESCRIPTION

A0 - A15	Address Input
I/O1 - I/O16	Data Input/Output
$\overline{CS}$	Chip Select Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
$\overline{LB}$, $\overline{UB}$	Data Byte Control Input
Vcc	Power(+5V)
Vss	Ground
NC	No Connection

ABSOLUTE MAXIMUM RATING (1)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}, V_{IN}, V_{OUT}	Power supply, Input/Output Voltage	-0.5 to7.0	V
T_A	Operating Temperature	0 to 70	°C
T_{BIAS}	Temperature Under Bias	-10 to 125	°C
T_{STG}	Storage Temperature	-65 to 150	°C
P_D	Power Dissipation	1.0	W
I_{OUT}	Data Output Current	50	mA
T_{SOLDER}	Lead Soldering Temperature & Time	260 • 10	°c • sec

Note:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliablity.

RECOMMENDED OPERATING TEMPERATURE & SUPPLY VOLTAGE

TEMPERATURE	Vss	Vcc
0°C to + 70°C	0V	5.0V ± 10%

RECOMMENDED DC OPERATING CONDITION

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Vcc	Supply Voltage	4.5	5.0	5.5	V
Vss	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	-	5.5	V
V_{IL}	Input Low voltage	-0.5	-	0.8	V

TRUTH TABLE

$\overline{OE}$	$\overline{WE}$	$\overline{CS}$	$\overline{UB}$	$\overline{LB}$	I/O 1-8	I/O 9-16	MODE
X	X	H	X	X	Hi - Z	Hi - Z	Standby
L	H	L	L	H	Hi - Z	Dout	Upper Byte Read (I/O 9-16)
L	H	L	H	L	Dout	Hi - Z	Lower Byte Read (I/O 1-8)
L	H	L	L	L	Dout	Dout	Word Read (I/O 1-16)
X	L	L	L	L	Din	Din	Word Write (I/O 1-16)
X	L	L	L	H	Hi - Z	Din	Upper Byte Write(I/O 9-16)
X	L	L	H	L	Din	Hi - Z	Lower Byte Write(I/O 1-8)
H	H	L	X	X	Hi - Z	HI - Z	Out disabled
X	X	L	H	H	Hi - Z	Hi - Z	

Note:
1. H=V_{IH}, L=V_{IL}, X=don't care
2. $\overline{UB}$, $\overline{LB}$(Upper, Lower Byte enable)
   These active LOW inputs allow indiviual bytes to be written or read.
   When $\overline{LB}$ is LOW, data is written or read to the lower byte, I/O 1 -I/O 8.
   When $\overline{UB}$ is LOW, data is written or read to the Upper byte, I/O 9 -I/O 16.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%)

SYMBOL	PARAMETER	TEST CONDITION	HY6316100S		HY6316100L		UNIT
I_{LI}	Input Leakage Current	Vcc=MAX.,Vin=Vss to Vcc	-	2	-	2	uA
I_{LO}	Output Leakage Current	Vcc=MAX.,$\overline{CS}$=Vih Vout=Vss to Vcc	-	2	-	2	uA
V_{OL}	Output Low Voltage	Iol = 8mA, Vcc = Min.	-	0.4	-	0.4	V
V_{OH}	Output High Voltage	Ioh = -4mA, Vcc = Min.	2.4	-	2.4	-	V

DC ELECTRICAL CHARACTERISTICS (1)

(V_{CC}=5.0V±10%, V_{IC}≤0.2V, V_{HC}≥V_{CC}-0.2V)

SYMBOL	PARAMETER	POWER	15, 17, 20, 25	UNIT
I_{CC}	Dynamic Operating Current $\overline{CS}$ = Vil Ii/o = 0mA, Vcc = Max. f= f_{MAX}(2)	S	260/260/230/200	mA
		L	260/260/230/200	mA
I_{SB}	Standby Power Supply Current(TTL Level) $\overline{CS}$ ≥ Vih, Vin = Vih or Vil Vcc = Max. f = f_{MAX}.(2)	S	50	mA
		L	50	mA
I_{SB1}	Full Standby Power Supply Current(CMOS Level) $\overline{CS}$ ≥ Vhc, Vin = Vhc or Vlc Vcc = Max., f = 0(2)	S	2	mA
		L	100	uA

Notes:
1. All values are maximum guaranteed values.
2. At f = fmax address and data inputs are cycling at the maximum frequency of read cycles of 1/trc.
   f = 0 means no input lines change.

AC CHARACTERISTICS

(TA=0°C to 70°C, VCC=5V ±10%, unless otherwise noted.)

#	SYMBOL	PARAMETER	15		17		20		25		UNIT
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
	READ CYCLE										
1	tRC	Read Cycle Time	15	-	17	-	20	-	25	-	ns
2	tAA	Address Access Time	-	15	-	17	-	20	-	25	ns
3	tACS	Chip Select Access Time	-	15	-	17	-	20	-	25	ns
4	tOE	Output Enable to Output Valid	-	8	-	9	-	10	-	12	ns
5	tBA	$\overline{UB}$, $\overline{LB}$ Acess Time	-	8	-	9	-	10	-	12	ns
6	tCLZ	Chip Select to Low -Z Output	3	-	3	-	3	-	3	-	ns
7	tOLZ	Output Enable to Low-Z Output	3	-	3	-	3	-	3	-	ns
8	tCHZ	Chip Disable to High -Z Output	-	8	-	8	-	8	-	8	ns
9	tOHZ	Output Disable to High -Z Output	-	8	-	8	-	10	-	10	ns
10	tOH	Output Hold from Address Change	3	-	3	-	3	-	3	-	ns
	WRITE CYCLE										
11	tWC	Write Cycle Time	15	-	17	-	20	-	25	-	ns
12	tCW	Chip Select to End of Write	11	-	12	-	13	-	15	-	ns
13	tAW	Address Valid to End of Write	11	-	12	-	13	-	15	-	ns
14	tBW	$\overline{UB}$, $\overline{LB}$ Valid to End of Write	11	-	12	-	13	-	15	-	ns
15	tAS	Address Set-up Time	0	-	0	-	0	-	0	-	ns
16	tWP	Write Plus Width	11	-	12	-	13	-	15	-	ns
17	tWR	Write Recovery Time	0	-	0	-	0	-	0	-	ns
18	tWHZ	Write to High-Z Output	0	8	0	8	0	10	0	15	ns
19	tDW	Data to Write Time Overlap	8	-	10	-	10	-	15	-	ns
20	tDH	Data Hold from Write Time	0	-	0	-	0	-	0	-	ns
21	tOW	Output Active from End of Write	3	-	3	-	3	-	3	-	ns

CAPACITANCE (1)

(Temp = 25°c, f= 1.0MHz)

SYMBOL	PARAMETER	MAX.	UNIT
CIN	Input Capacitance(Add., $\overline{CS}$, $\overline{WE}$, $\overline{OE}$, $\overline{UB}$, $\overline{LB}$)	6	pF
COUT	Ouput Capacitance(I/O)	10	pF

Notes:
1. This parameter is determined by device characterization but is not production tested.

AC TEST CONDITIONS

Input pulse levels ..... Vss to 3.0V
Input rise and fall times 3ns
Input timing reference levels 1.5V
Output reference levels 1.5V
Output load ..... See figures 1 and 2

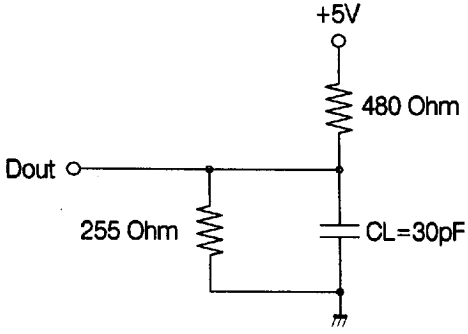


Figure 1
Output Load Equivalent

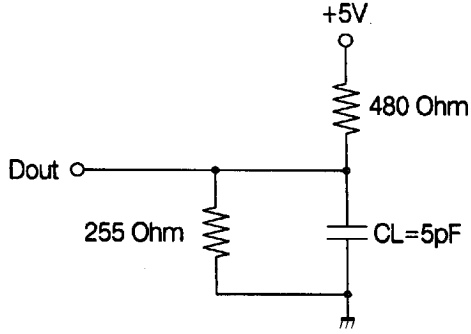
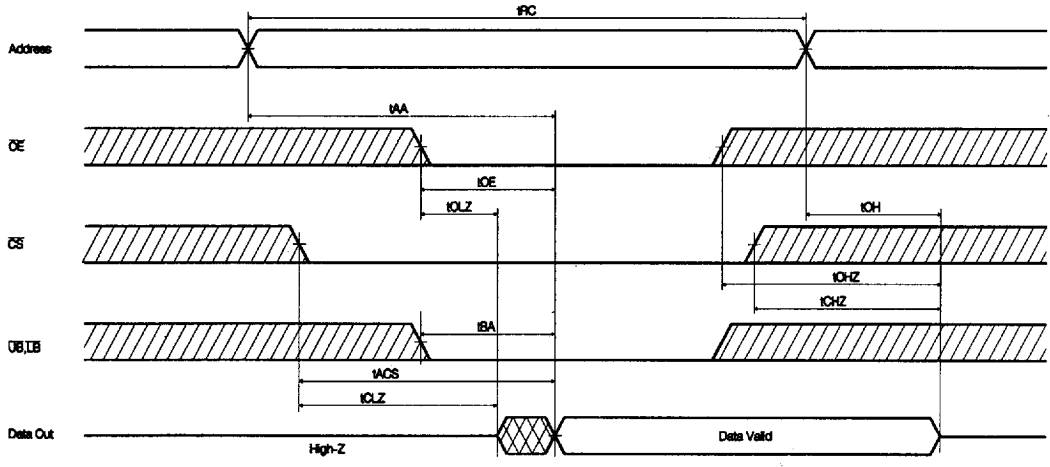


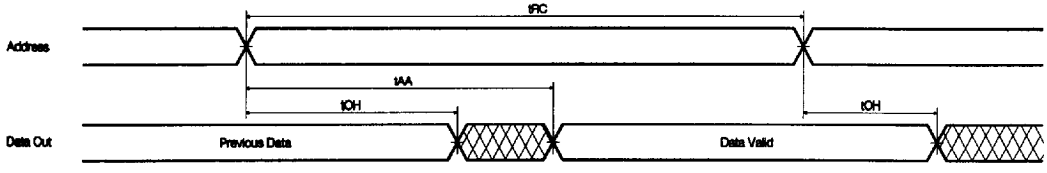
Figure 2
(for t_{CHZ}, t_{CLZ},t_{OHZ},t_{OLZ}, t_{WHZ} & t_{OW})

TIMING DIAGRAMS

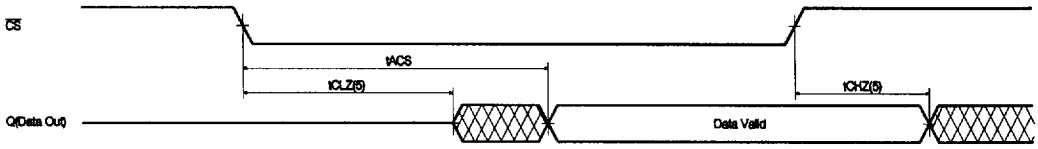
READ CYCLE 1 NOTE 1



READ CYCLE 2 NOTE 1,2,4

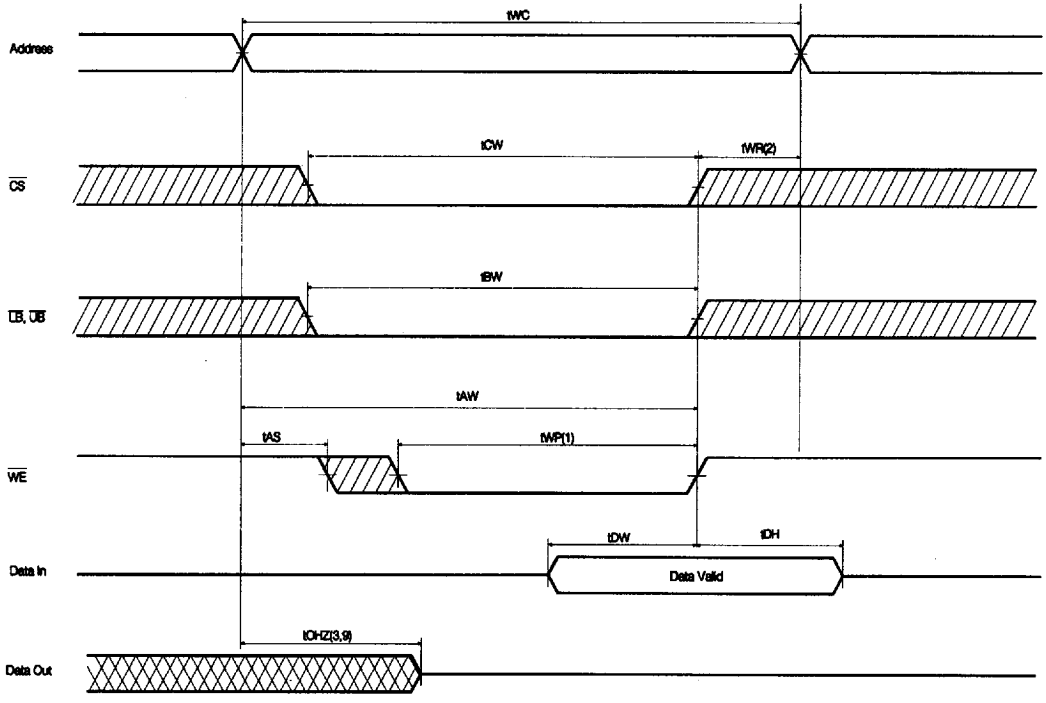


READ CYCLE 3 NOTE 1,3,4

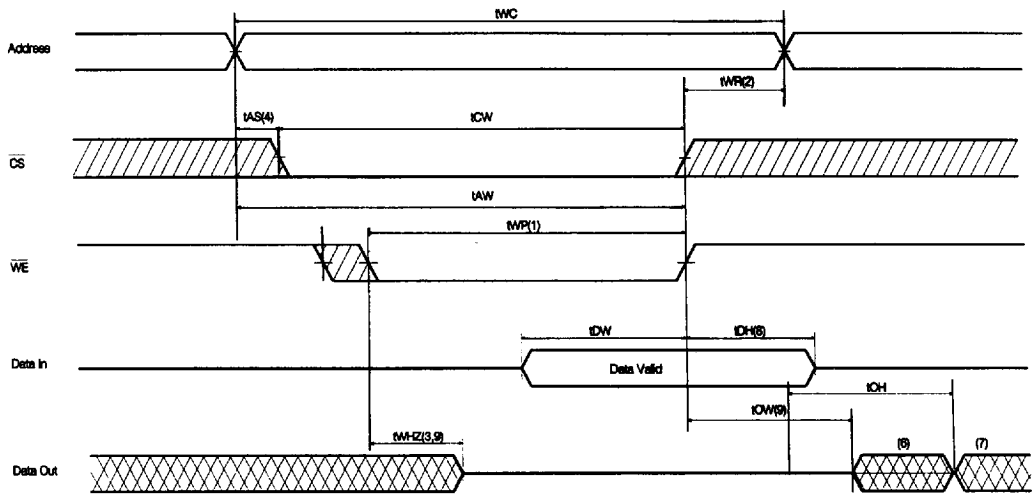


Notes:
1. $\overline{WE}$ is high for Read Cycle.
2. Device is continuously selected. $\overline{CS}$ = Vil
3. Address valid prior to or coincident with $\overline{CS}$ transition low
4. $\overline{OE}$ = Vil
5. Transition is measured ± 500mV form steady state voltage.
   This parameter is sampled and not 100% tested.

WRITE CYCLE 1



WRITE CYCLE 2 NOTE 5

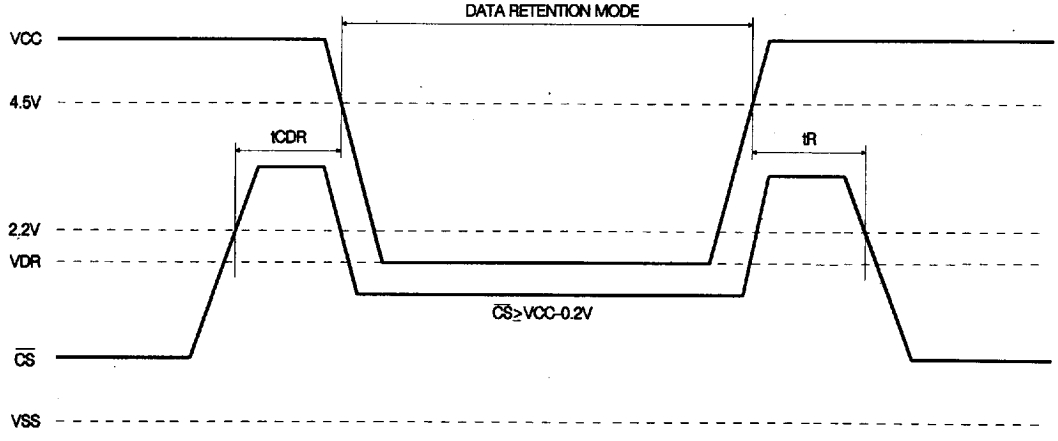


Notes:
1. A write occurs during the overlap(tWP) of a low $\overline{CS}$ and low $\overline{WE}$.
2. tWR is measured from the earlier of $\overline{CS}$, $\overline{LB}$, $\overline{UB}$, or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the output must not be applied.
4. If the $\overline{CS}$, $\overline{LB}$, $\overline{UB}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition. Outputs remain in a high impedance state.
5. $\overline{OE}$ is continuously low($\overline{OE}$=Vil)
6. Q(data out) is the same phase of write data of this write cycle.
7. Q(data out) is the read data of next address.
8. If $\overline{CS}$ is low during this period, I/O pins are in the output state.
   Then the data input signals of opposite phase to the outputs must not be applied to them.
9. Transition is measured +500mV from steady state.
   This parameter is sampled and not 100% tested.

DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

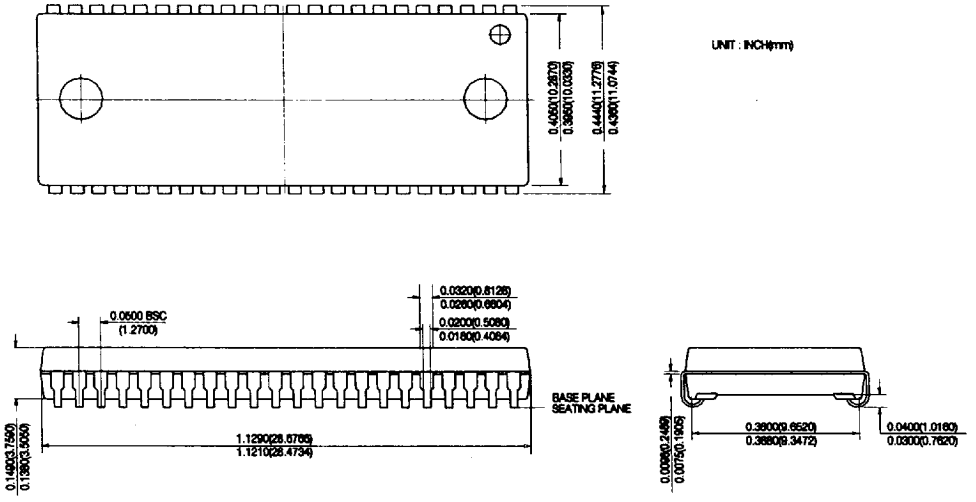
SYMOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DR}	Vcc for Retention Current	$\overline{CS} \geq V_{CC}-0.2V$, $V_{SS} \leq V_{IN} \leq V_{CC}$	2	-	-	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{CC}-0.2V$ Vcc=2V $V_{IN} \geq V_{CC}-0.2$ or $\leq 0.2V$ Vcc=3V	- -	- -	50 70	µA
t_{CDR}	Chip Deselect to Data Retention Time	See the Data Retertion Timming Diagram	0	-	-	ns
t_R	Operation Recovery Time		tRC	-	-	ns

DATA RETENTION TIMING DIAGRAM 1.

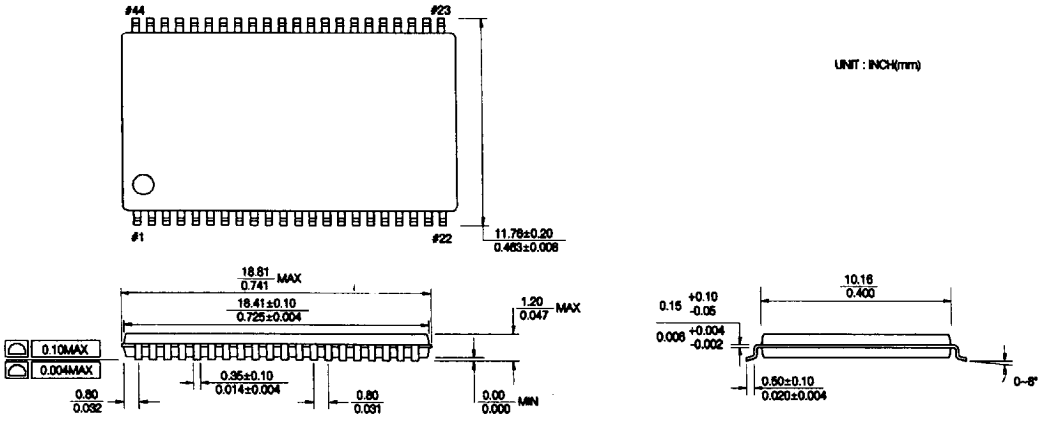


PACKAGE INFORMATION

400 mil 44 pin Small Outline J-form Package (J)



400 mil 44 pin Thin Small Outline Package (T2)



ORDERING INFORMATION

PART NO.	SPEED	POWER	PACKAGE
HY6316100AJ	15/17/20/25		44pin SOJ
HY6316100ALJ	15/17/20/25	L-Part	44pin SOJ
HY6316100AT2	15/17/20/25		44pin TSOP-II
HY6316100ALT2	15/17/20/25	L-Part	44pin TSOP-II
HY6316100AR2	15/17/20/25		44pin TSOP-II(R)
HY6316100ALR2	15/17/20/25	L-Part	44pin TSOP-II(R)