凌陽科技 SUNPLUS

Preliminary

SPC122A

SOUND CONTROLLER WITH 128KB FLASH MEMORY

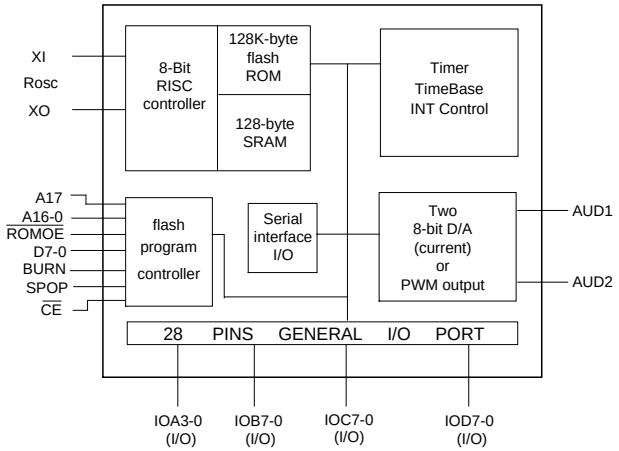
GENERAL DESCRIPTION

The SPC122A is a CPU based two-channel speech/melody synthesizer including CMOS 8-bit microprocessor with 69 instructions, 128K-bytes of Flash ROM for speech and melody data (Speech is compressed by a 4-bit ADPCM with approx. 36 sec speech duration @ 7KHz sampling rate) and 128-byte working SRAM. Its external memory is capable of being extended up to 256K. It provides Multi-Duty-Cycle output that can be implemented for remote-control purposes. It includes two Timer/Counters, 28 Software Selectable I/Os, 2 audio current D/A outputs (or one PWM audio output) and serial interface I/O port. Volume control is also provided. For audio processing, melody and speech can be mixed into one output. It operates over a wide voltage range of 2.4V - 5.5V. In addition, the SPC122A has a Clock Stop mode for power savings. The power savings mode saves the RAM contents, but freezes the oscillator, causing all other chip functions to be inoperative. The Max. CPU clock frequency is 6.0MHz. It has an Instruction Cycle Rate of 2 clock cycles (min.) – 6 clock cycles (max.). The SPC122A includes, not only the latest technology, but also the full commitment and technical support of Sunplus.

FEATURES

- 8-bit microprocessor
- **Provides 128K-byte Flash ROM for program and audio data**
- **128-byte working SRAM**
- Software-based audio processing
- Wide operating voltage: 2.4V – 3.4V @ 2.0MHz
  3.6V – 5.5V @ 6.0MHz
- Supports Crystal Resonator or Rosc (with bonding option)
- Max. CPU clock: 2.0MHz @ 3V, 6.0MHz @ 5V
- Standby mode (Clock Stop mode) for power savings. Max. 2μA @ 5V
- 500ns instruction cycle time @ 4.0MHz CPU clock
- **Provides 28 general I/Os**
- Two 12-bit timer/counters
- 6 INT sources
- Key wake-up function
- **Approx. 36 sec speech @ 7KHz sampling rate with ADPCM**
- **Two 8-bit D/A output**
- **One PWM audio output (single speaker)**
- **Volume control function**
- **Multi-Duty-Cycle outputs (1/2, 1/3, 1/4 duty)**

BLOCK DIAGRAM



APPLICATION FIELD

- Intelligent education toys
  Ex. Pattern to voice (animal, car, color, etc.)
  Spelling (English or Chinese)
  Math
- High end toy controller
- Talking instrument controller
- General speech synthesizer
- Industrial controller

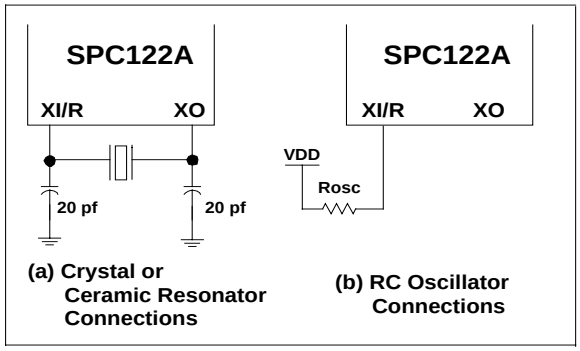
FUNCTION DESCRIPTIONS

■ CPU

The SPC122A 8-bit microprocessor is a high performance processor equipped with Accumulator, Program Counter, X Register, Stack pointer and Processor Status Register (this is the same as the 6502 instruction structure). SPC122A is able to perform with 6.0MHz (max.) depending on the application specifications.

■ OSCILLATOR

The SPC122A supports AT-cut parallel resonant oscillated Crystal / Resonator or RC Oscillator or external clock sources by using the bonding option (select one from those three types). The design of application circuit should follow the vendors' specifications or recommendations. The diagrams listed below are typical X'TAL/ROSC circuits for most applications:



■ BONDING OPTION

The SPC122A has the following bonding option:

- Supports Crystal Resonator or Rosc (with bonding option).

■ ROM AREA

The SPC122A provides a 122AK-byte of Flash ROM that can be defined as the program area, audio data area, or both. To access ROM, users should program the BANK SELECT Register, choose bank, and access address to fetch data. The combination of $\overline{CE}$ and Burn pins is capable of programming the Flash ROM as parallel mode. In contrast, using $\overline{CE}$ and STOP pins can program the Flash ROM as serial mode. In addition, pin AD17 and $\overline{CE}$ can be used to extend the memory from 128K to 256K with external memory.

■ RAM AREA

The SPC122A total RAM consists of 128 bytes (including Stack) at locations from $80 through $FF.

■ MAP OF MEMORY AND I/Os

*I/O PORT:

- PORT IOA $0002
  IOB $0003
  IOC $0004
  IOD $0005
- I/O CONFIG $0000
  $0001

*NMI SOURCE:

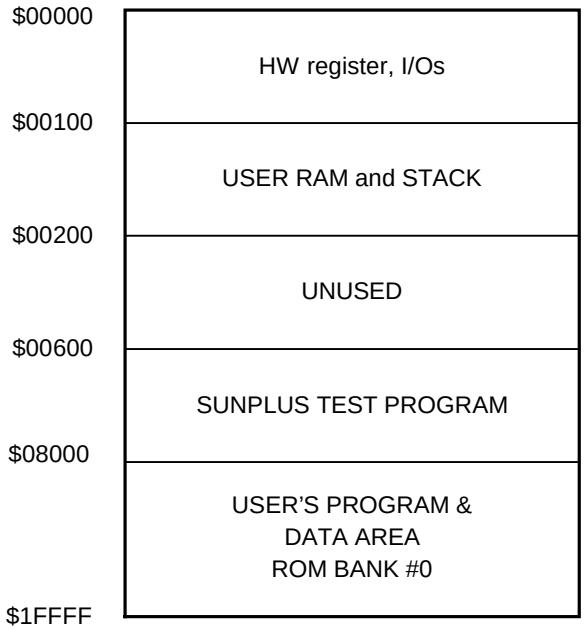
- INTA (from TIMER A)

*INT SOURCE:

- INTA (from TIMER A)
- INTB (from TIMER B)
- CPU CLK / 1024
- CPU CLK / 8192
- CPU CLK / 65536
- EXT INT

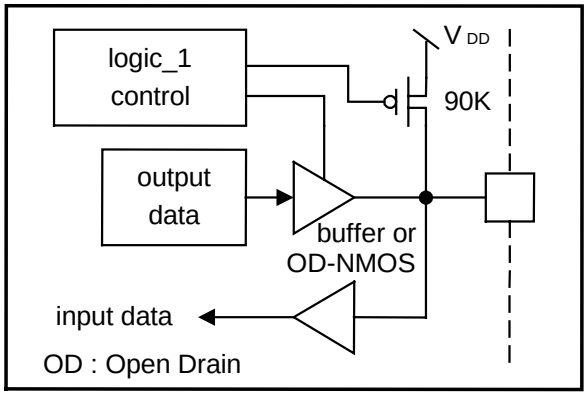
- Capable of being extended to 256K with external memory

*MEMORY MAP (From ROM view)

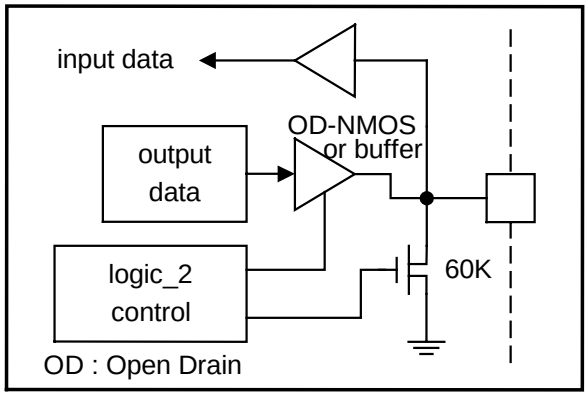


■ I/O PORT CONFIGURATION*

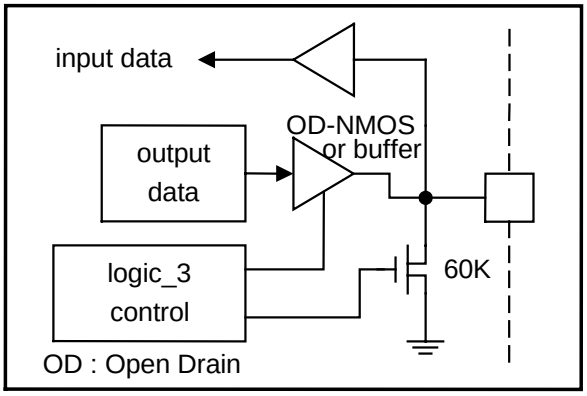
Input/Output IOA port : IOA3 - 0



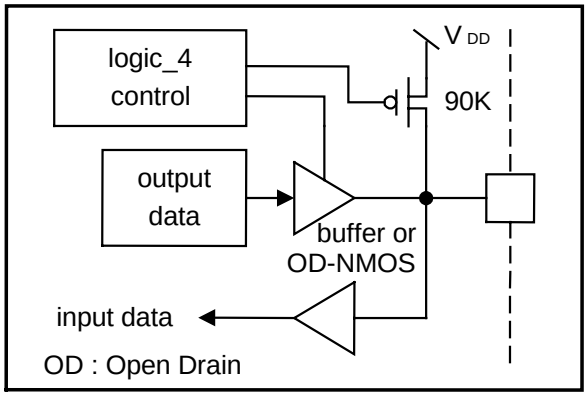
Input/Output IOB port : IOB2 - 0



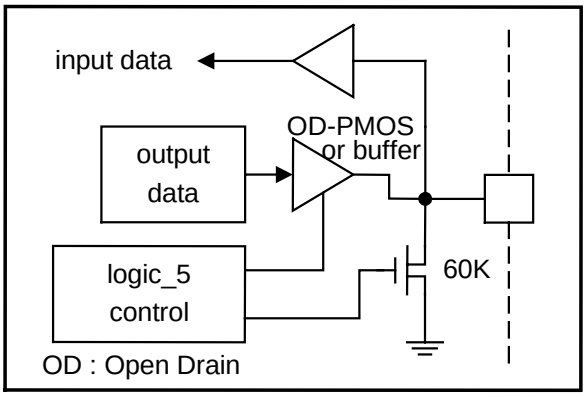
Input/Output IOB port : IOB5 - 4



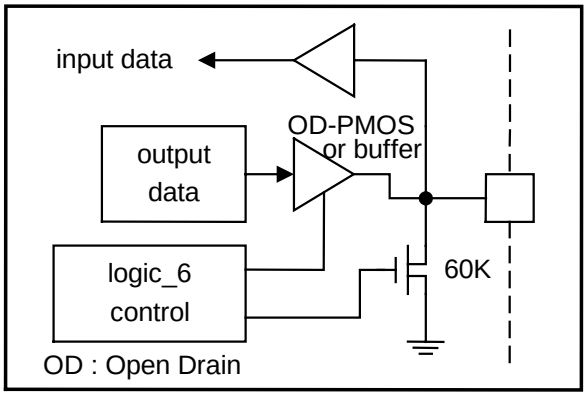
Input/Output IOC port : IOC3 - 0



Input/Output IOD port : IOD3 - 0



Input/Output IOD port : IOD7 - 4



*Values shown are for VDD = 5.0V test conditions only.

■ POWER SAVINGS MODE

The SPC122A provides a power savings mode (Standby mode) for those applications that require very low stand-by current. To enter standby mode, the Wake-Up Register should be enabled and then stop the CPU clock by writing the STOP CLOCK Register. The CPU will then go to the stand-by mode. In such a mode, RAM and I/Os will remain in their previous states until being awakened. Port IOD7-0 is the only wake-up source in the SPC122A. After the SPC122A is awakened, the internal CPU will go to the RESET State (Tw ≧ 65536 x T1) and then continue processing the program. Wakeup Reset will not affect RAM or I/Os (See FIG.1).

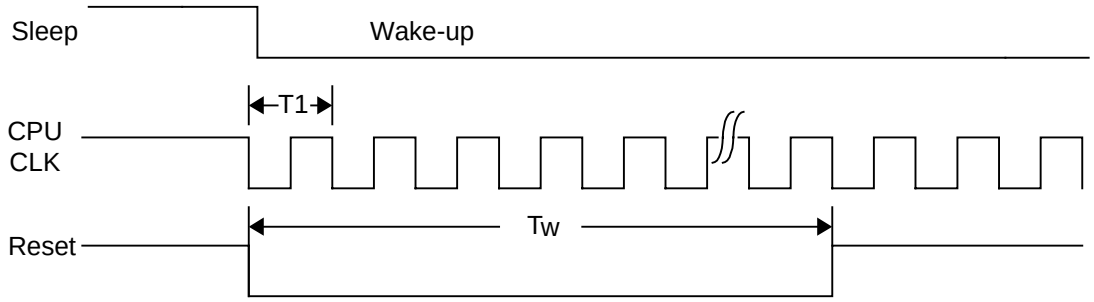


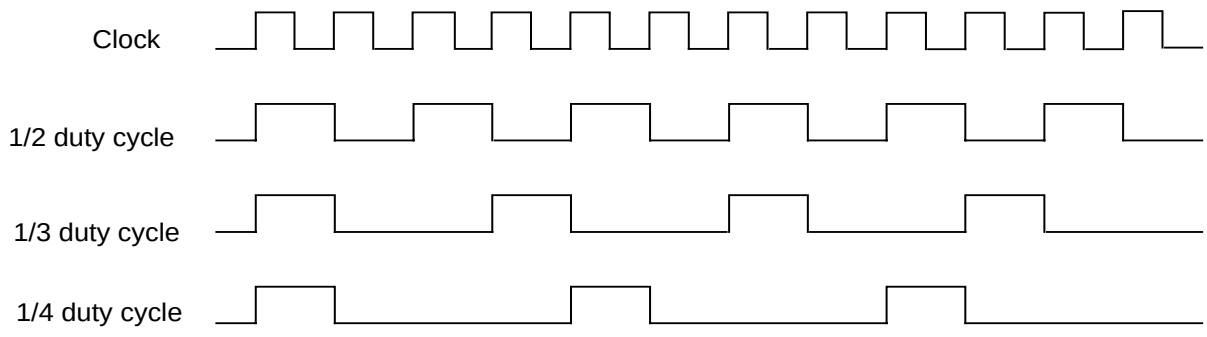
FIG. 1

T1 = 1 / (F_{CPU}), Tw ≧ 65536 x T1

■ MULTI-DUTY CYCLE MODE

The SPC122A provides three output waveforms, 1/2, 1/3, and 1/4 duty cycles. The Control Register should be used to select 1/2, 1/3, or 1/4 duty cycle and the IOA2 should be programmed as the multi-duty cycle output port. Users can use the combinations of these duty cycles for remote-control purpose.

■ 1/2, 1/3, 1/4 DUTY CYCLE OUTPUTS



■ SERIAL INTERFACE I/O

The SPC122A provides serial interface I/O mode for those applications required large ROM/RAM. Serial Interface I/O Port can be used to read/write data from/to extra memory. The interface I/O Register is the control register for programming interface I/O.

■ TIMER/COUNTER

The SPC122A contains two 12-bit timer/counters, TMA and TMB respectively. TMA can be specified as a timer or a counter, but TMB can only be used as a timer. In the timer mode, TMA and TMB are re-loaded up-counters. When timer overflows from $0FFF to $0000, the carry signal will make the timer automatically reload to the user's pre-set value and be up-counted again. At the same time, the carry signal will generate the INT signal if the corresponding bit is enabled in the INT ENABLE Register. If TMA is specified as a counter, users can reset by loading #0 into the counter. After the counter has been activated, the value of the counter can also be read from the counters at the same time.

Timer/Counter Clock source can be selected as follows:

Timer/Counter		Clock Source
TMA	12-BIT TIMER	CPU CLOCK (T) or T/4
	12-BIT COUNTER	T/64, T/8192, T/65536 or EXT CLK
TMB	12-BIT TIMER	T or T/4
MODE SELECT REGISTER		TMA only, select timer or counter
TIMER CLOCK SELECTOR		Select T or T/4

■ SPEECH AND MELODY

Since the SPC122A provides a large ROM and wide range of CPU operation speeds, it is most suitable for speech and melody synthesis.

For speech synthesis, the SPC122A can provide NMI for accurate sampling frequency. Users can record or synthesize the sound and digitize it into the ROM. The sound data can be played back in the sequence of the control functions as designed by the user's program. Several algorithms are recommended for high fidelity and compression of sound including PCM, LOG PCM, and ADPCM.

For melody synthesis, the SPC122A provides the dual tone mode. After selecting the dual tone mode, users only need to fill either TMA or TMB, or both TMA and TMB to generate expected frequency for each channel. The hardware will toggle the tone wave automatically without entering into an interrupt service routine. Users are able to simulate musical instruments or sound effects by simply controlling the envelope of tone output.

■ VOLUME CONTROL FUNCTION

The SPC122A contains a volume control function that provides an 8-step volume controller to control current D/A or PWM output. A volume control function selector (Enable/Disable) register and controller register is provided.

Differences between SPC121A and SPC122A

	SPC121A	SPC122A
1. Work range	2.4V - 5.5V	3.6V - 5.5V
2. ROM type	Mask	Flash
3. ROM SIZE	120K	128K
4. I/O port	21	28
5. SIO	×	✓
6. PWM Output	×	✓
7. Multiphase Output	×	✓
8. Volume Control	×	✓

PIN DESCRIPTIONS*

Mnemonic	PIN No.	Type	Description
VDD	5 29 34 45 57	I	Positive supply for logic and I/O pins
VSS	17 27 50 66	I	Ground reference for logic and I/O pins
XI	32	I	Oscillator crystal input or RESISTOR (Resistor should be connected to VDD)
XO	31	O	Oscillator crystal output
OPT*	30	I	For ROSC option, OPT should be connected to $V_{DD.}$
BURN	15	I	Burn, This pin is an active high to select the flash ROM program function
$\overline{CE}$	16	I	This pin is an active low to select this chip as a 1Mbits memory
$\overline{ROMOE}$	14	I/O	Data Output enable
SPOP	18	I	Serial program option
A17	4	O	Extended Memory Enable
RESET	19	I	This pin is an active low reset to the chip.
TEST	36	I	TEST MODE
AUD1 AUD2	33 35	O O	AUDIO OUTPUT
D7 – 0	6-13	I/O	Data Bus
A13 – 0 A16 – 14	74-60 3-1	I/O	Address Bus
IOA0 IOA1 IOA2 IOA3	46 47 48 49	I/O I/O I/O I/O	Port A is an 8-bit bi-directional programmable Input / Output port with Pull-high or Open-drain option. As inputs, Port A can be in either the Pure or Pull-high states. As outputs, Port A can be either Buffer or Open-drain NMOS types (Sink current). IOA0: Serial programming clock output IOA2: Multi-duty cycle output **See note 1 and 2 below.

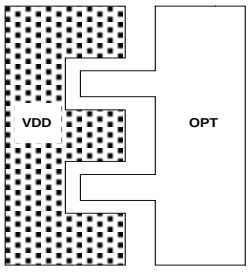
Mnemonic	PIN No.	Type	Description
IOB0	59	I/O	Port B is an 8-bit bi-directional Input / Output port with Pull-low or Open-drain option. As inputs, Port B can be in either the Pure or Pull-low states. As outputs, Port B can be either Buffer or Open-drain NMOS types (Sink current).
IOB1	58	I/O	
IOB2	56	I/O	
IOB4	54	I/O	
IOB5	53	I/O	
IOB6	52	I/O	
IOB7	51	I/O	**See note 1 and 2 below.
IOC0	28	I/O	Port C is an 8-bit bi-directional Input / Output port with Pull-high or Open-drain option. As inputs, Port C can be in either the Pure or Pull-high states. As outputs Port C can be a Buffer or Open-drain NMOS type (sink current). IOC0: Serial programming Data IOC1: EXT INT PIN IOC2: EXT COUNT IN
IOC1	26	I/O	
IOC2	25	I/O	
IOC3	24	I/O	
IOC4	23	I/O	
IOC5	22	I/O	
IOC6	21	I/O	
IOC7	20	I/O	**See note 1 and 2 below.
IOD0	44	I/O	Port D is an 8-bit bi-directional Input / Output port with Pull-low or Open-drain option. As inputs, Port D can be either Pure or Pull-low states. As outputs, Port D can be either Buffer or Open-drain PMOS (send current). (Port D can be software programmed for wake up I/O)
IOD1	43	I/O	
IOD2	42	I/O	
IOD3	41	I/O	
IOD4	40	I/O	
IOD5	39	I/O	
IOD6	38	I/O	
IOD7	37	I/O	**See note 1 and 2 below.

* Refer to SPC Programming Guide for complete information.

**Note: 1.) Two input states can be specified; Pure Input, Pull-High or Pull Low.

2.) Three output states can be specified as Buffer output, Open Drain PMOS output (send), or Open Drain NMOS output (sink).

***OPT is the selection pin for ROSC or X'TAL using the bonding option. The shape looks like the figure at the right. When ROSC is selected, OPT is connected to VDD. If X'TAL is selected, OPT is floating. The reason OPT is near VDD is that when ROSC is selected, it is easy to make the connection between VDD and OPT.



ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 7V
Input Voltage Range	V_{IN}	-0.5V to V+ + 0.5V
Operating Temperature	T_A	0℃ to +60℃
Storage Temperature	T_{STO}	-50℃ to +150℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

AC CHARACTERISTICS (TA = 25 ℃)

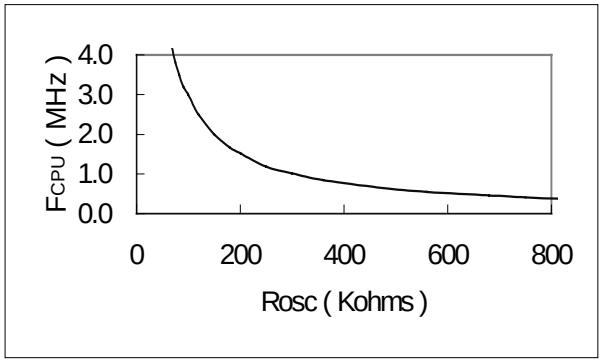
Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
OSC Frequency	F_{CPU}	-	1.0	2.0	MHz	VDD = 3V
		-	4.0	6.0	MHz	VDD = 5V
CPU Clock	F_{CPU}	-	-	6.0	MHz	$F_{CPU} = F_{OSC2}$ @5V

DC CHARACTERISTICS (TA = 25 ℃, VDD = 5V)

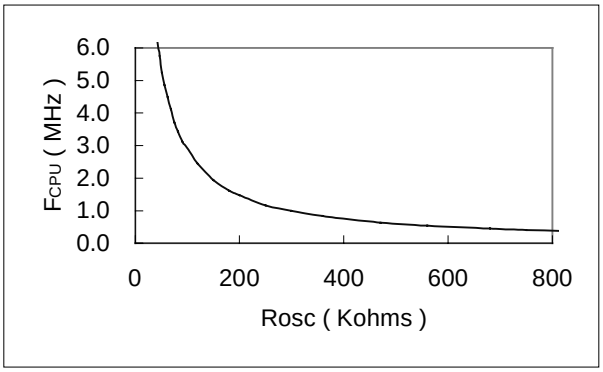
Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	V_{DD}	3.6	-	5.5	V	For 3-battery
Operating Current	I_{OP}	-	6.5	8.0	mA	F_{CPU} = 4.0MHz@5V, no load
Standby Current	I_{STBY}	-	-	2.0	μA	VDD = 5V
Audio output current	I_{AUD}	-	-3.0	-	mA	VDD = 5V
Input high level	V_{IH}	3.0	-	-	V	VDD = 5V
Input Low level	V_{IL}	-	-	0.8	V	VDD = 5V
Output high I IOA, IOB, IOD	I_{OH}	-1.0	-	-	mA	VDD = 5V V_{OH} = 4.2V
Output sink I IOA, IOB, IOD	I_{OL}	4.0	-	-	mA	VDD = 5V V_{OL} = 0.8V
Input resistor IOA, IOB, IOC, IOD	R_{IN}	-	60	-	kohm	Pull Low VDD = 5V

The relationship between the Rosc and the Fosc

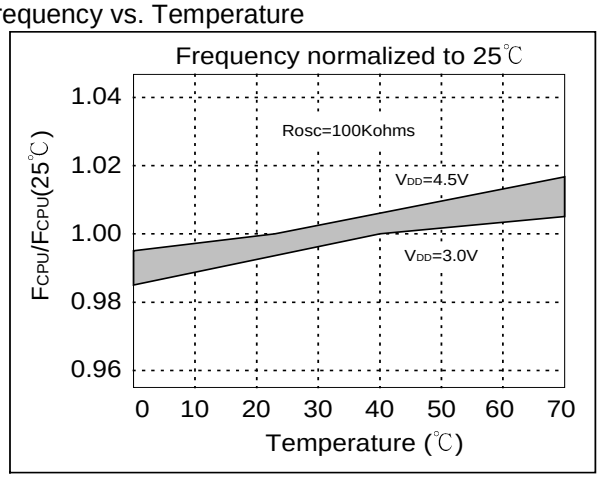
VDD = 3.0V , Ta = 25℃



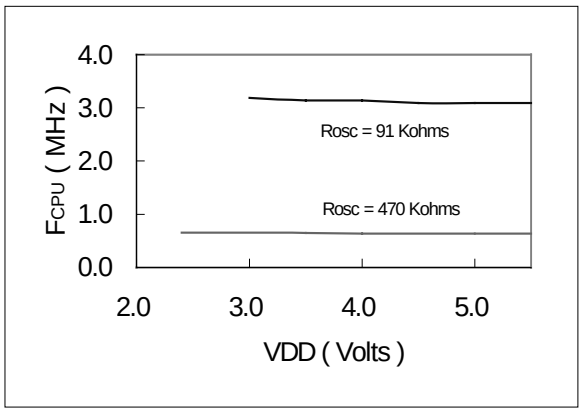
VDD = 4.5V , Ta = 25℃



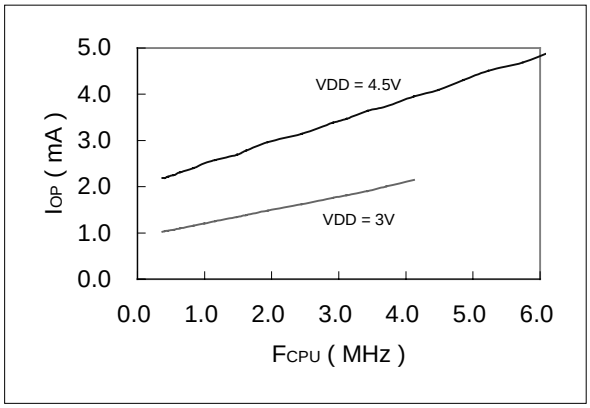
Frequency vs. Temperature



Frequency vs. VDD

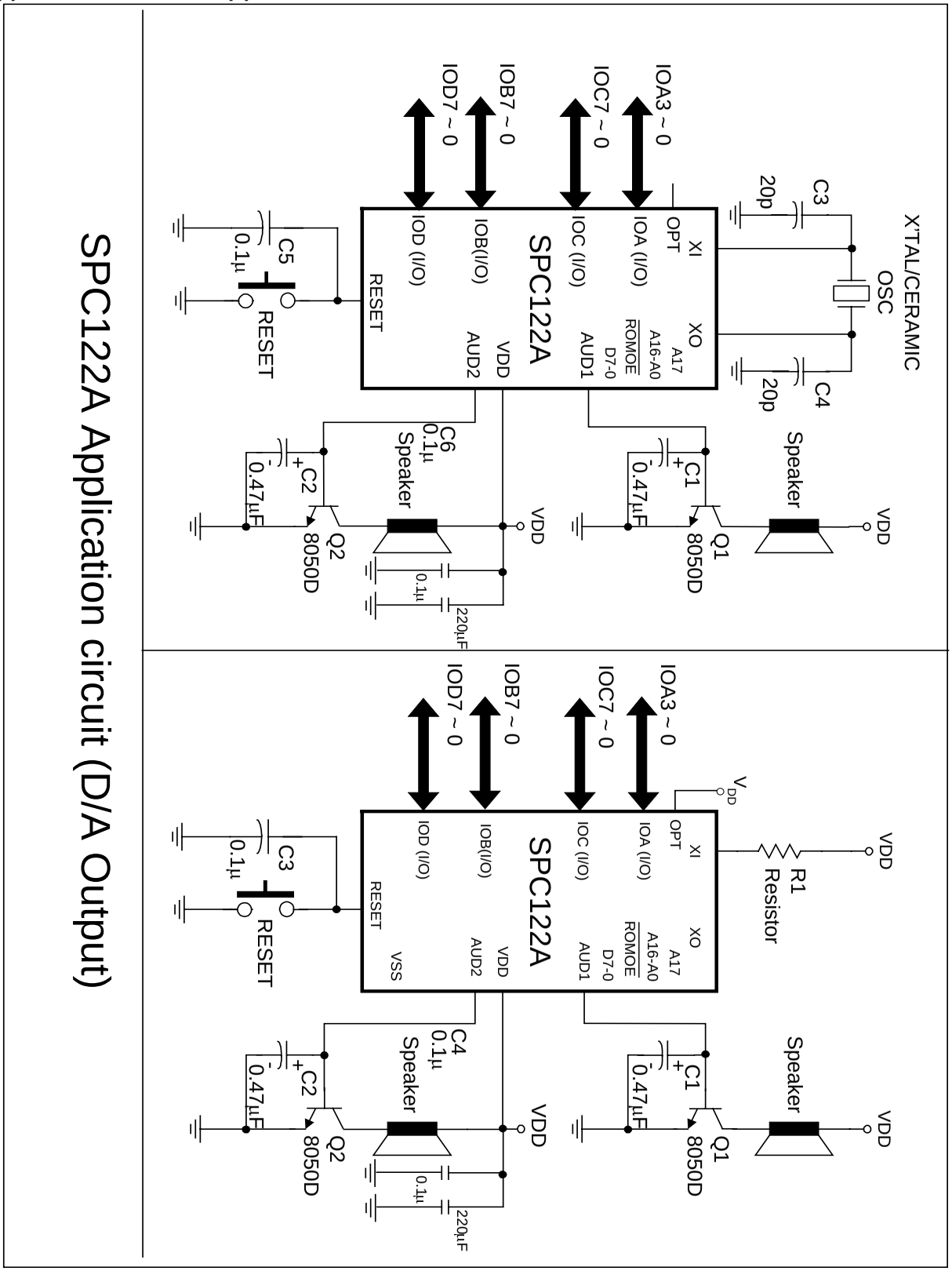


Operating current vs. Frequency vs. VDD

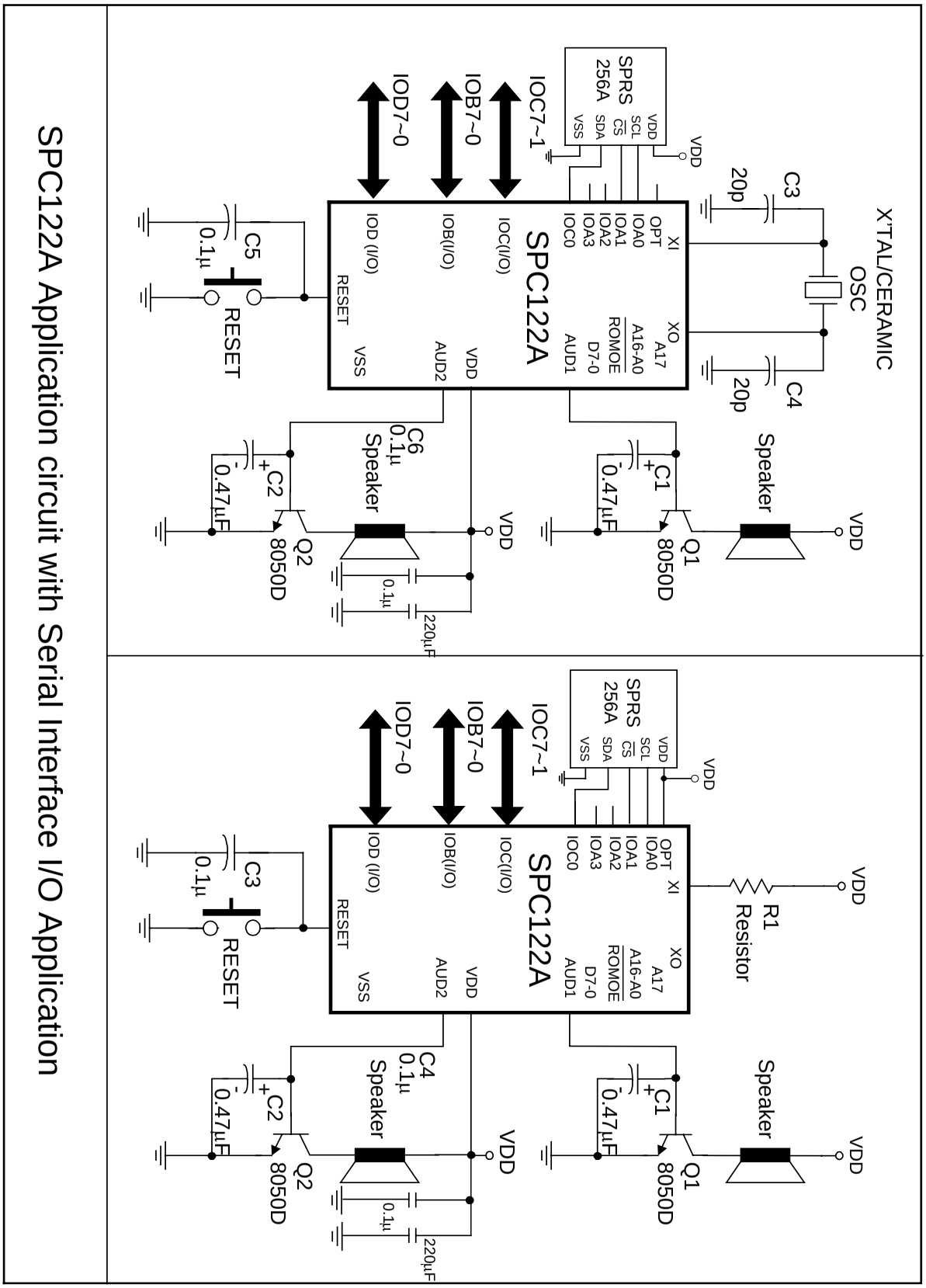


APPLICATION CIRCUIT NOTES

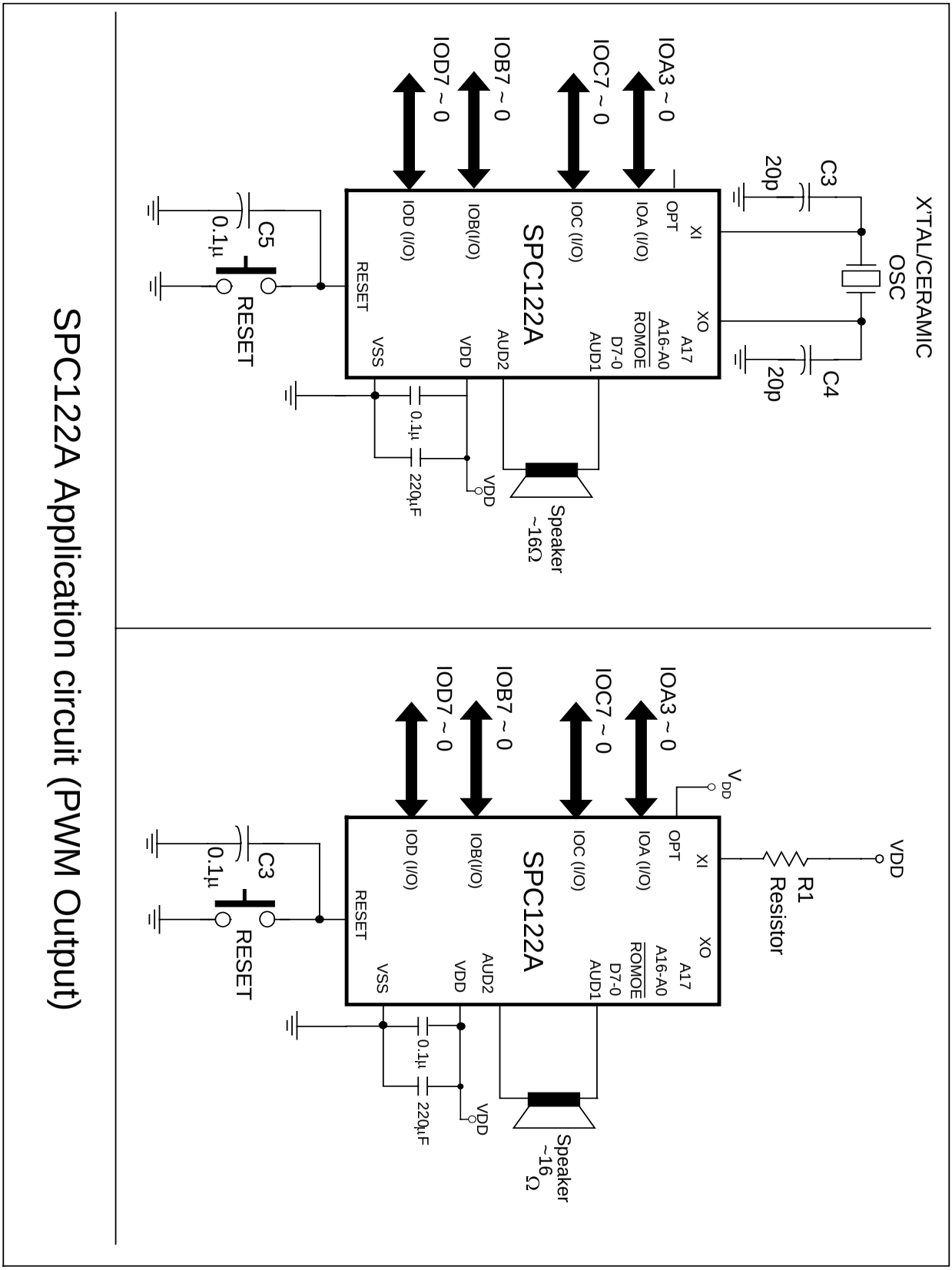
■ **Application Circuit Note (1)**



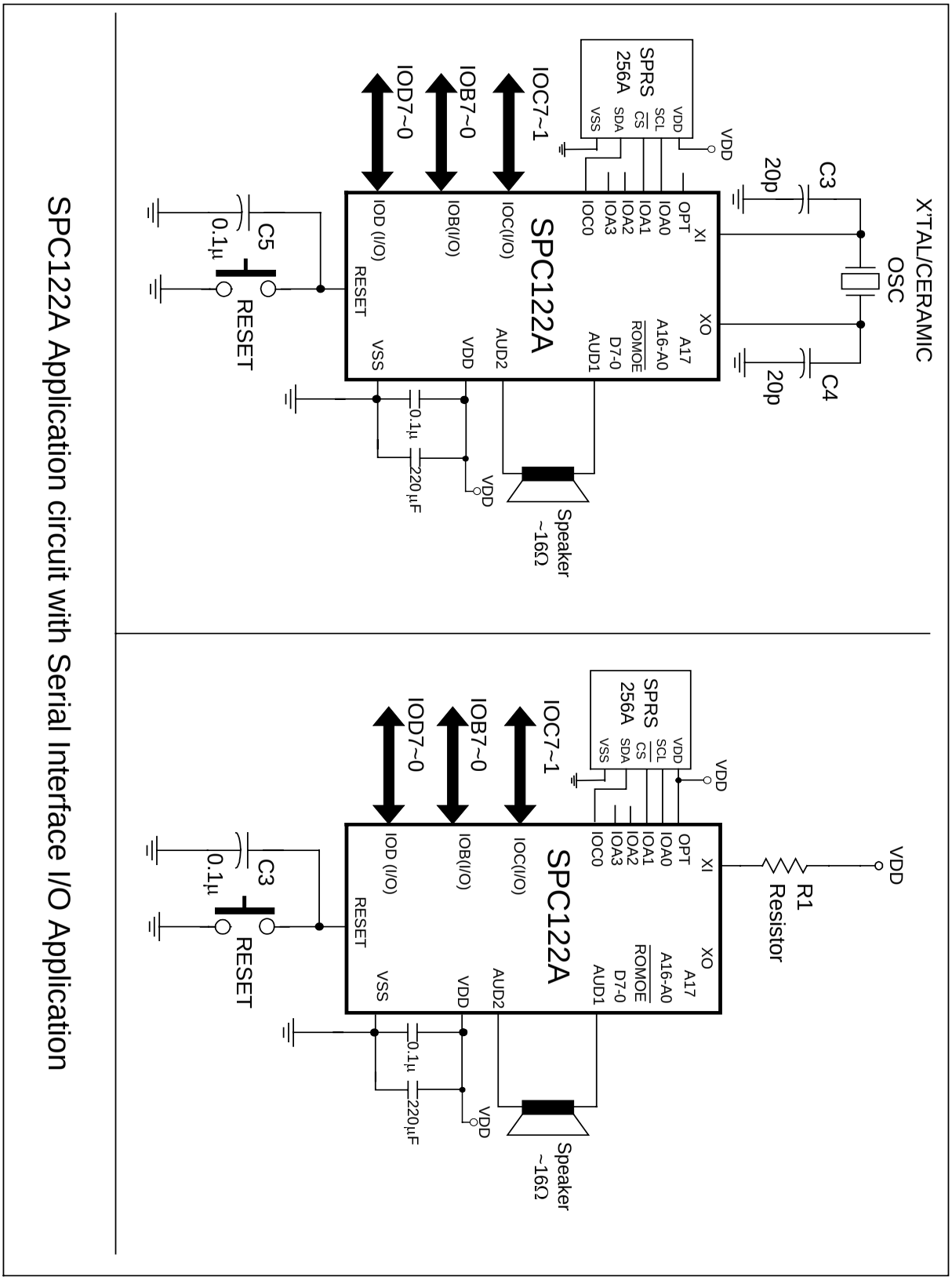
■ **Application Circuit Note (2)**



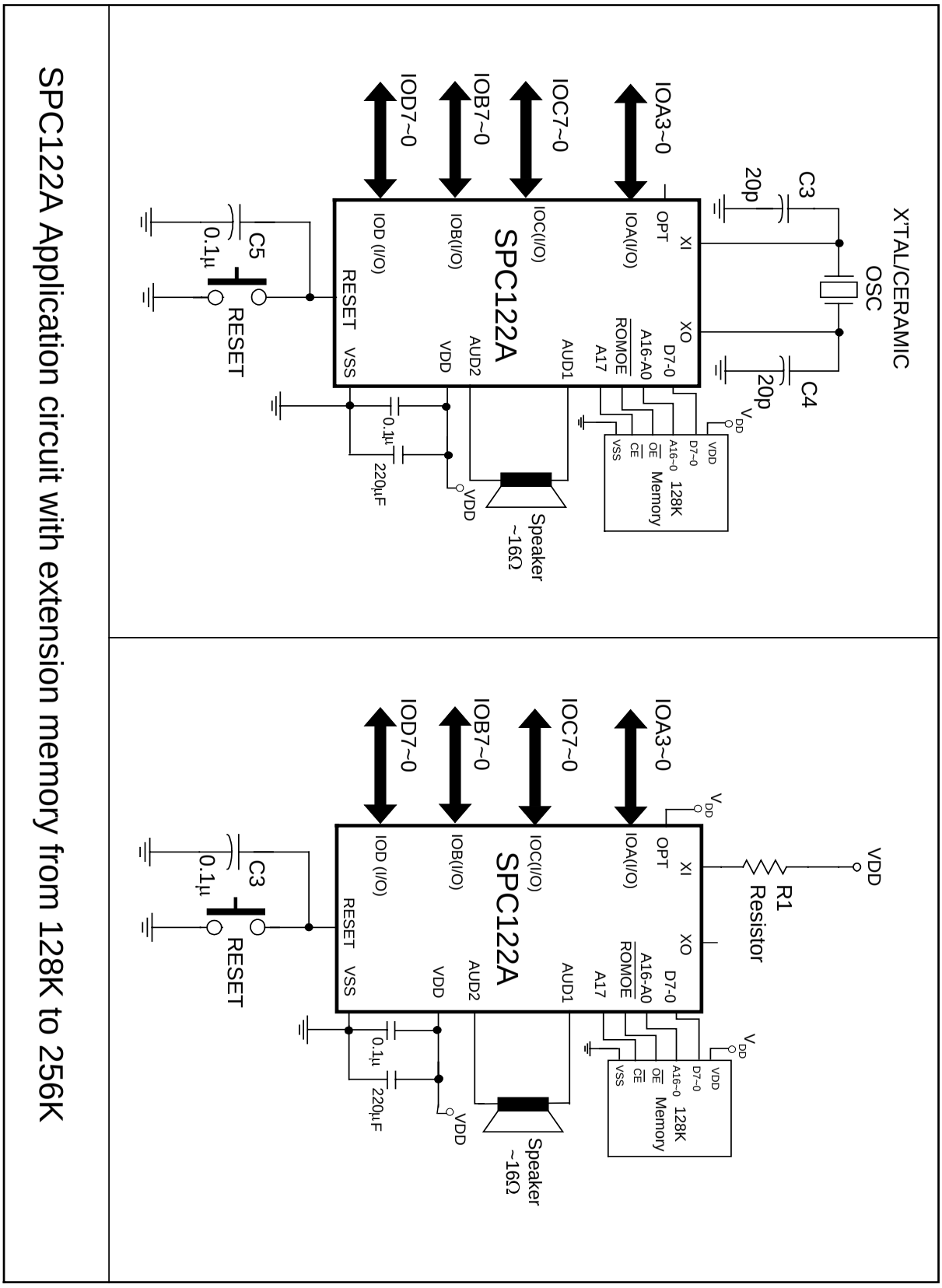
■ **Application Circuit Note (3)**



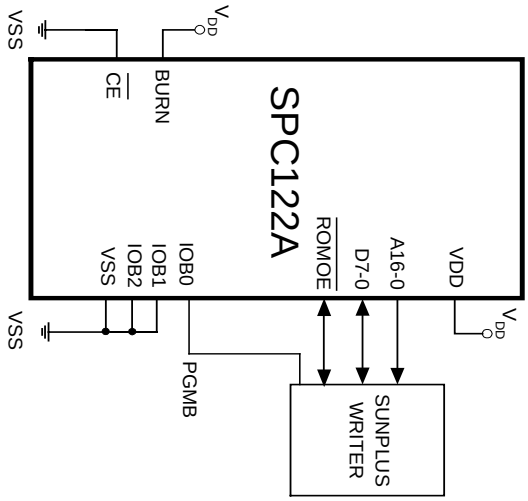
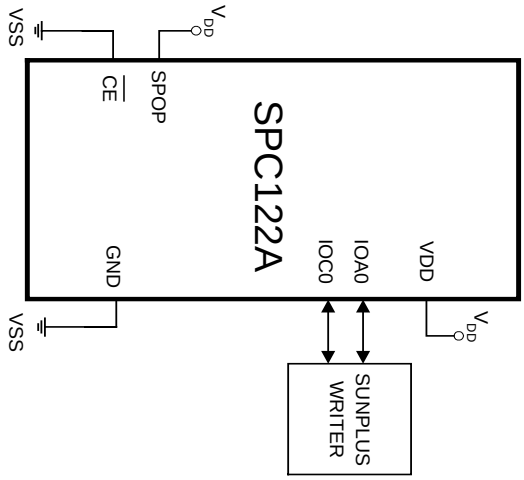
■ **Application Circuit Note (4)**



■ **Application Circuit Note (5)**

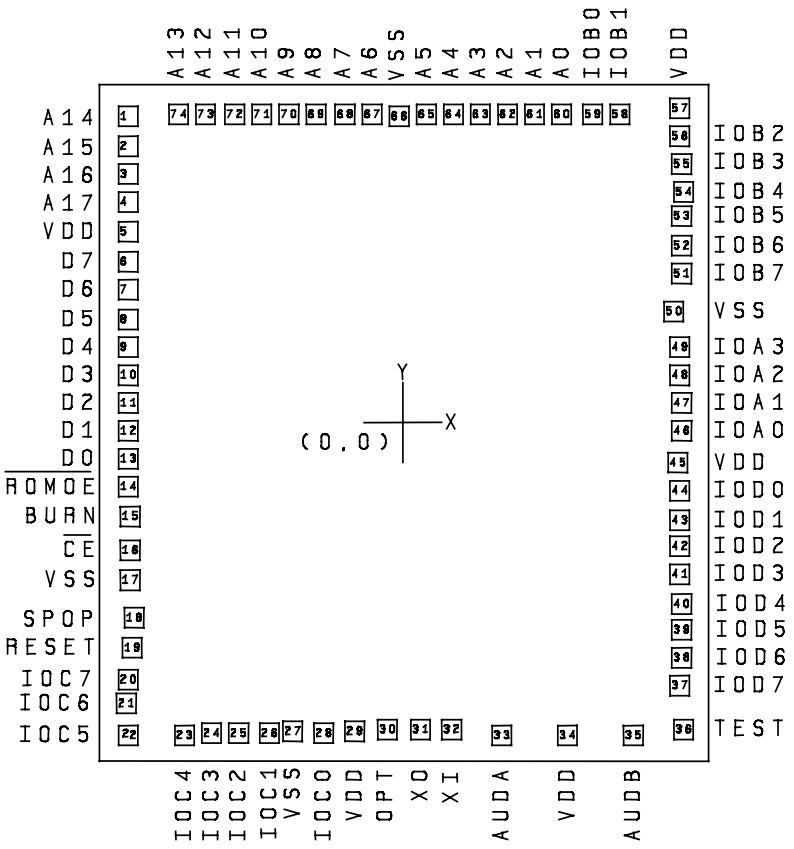


■ **Application Circuit Note (6)**

PARALLEL PROGRAMMING METHOD	
SERIAL PROGRAMMING METHOD	

PAD ASSIGNMENT AND LOCATIONS

■ PAD Assignment



Chip Size: 3250μm x 3500μm

This IC substrate should be connected to VSS

Note: To ensure that the IC function properly, bond all VDD, VSS, AVDD and AVSS pins.

Ordering Information

Product Number	Package Type
SPC122A-nnnnV-C	Chip form

Note1: Code number (nnnnV) is assigned for customer.

Note2: Code number (nnnn = 0000 - 9999); version (A = A - Z).

NOTE: SUNPLUS TECHNOLOGY CO., LTD reserves the right to make changes at any time without notice in order to improve the design and performance and to supply the best possible product.

■ **PAD Locations**

Pad No	Pad Name	X	Y	Pad No	Pad Name	X	Y
1	A14	-1429	1538	31	XO	81	-1542
2	A15	-1429	1388	32	XI	247	-1542
3	A16	-1429	1247	33	AUD1	508	-1574
4	A17	-1429	1107	34	VDD	847	-1574
5	VDD	-1424	956	35	AUD2	1186	-1574
6	D7	-1429	806	36	TEST	1441	-1542
7	D6	-1429	666	37	IOD7	1426	-1320
8	D5	-1429	525	38	IOD6	1432	-1182
9	D4	-1429	385	39	IOD5	1432	-1038
10	D3	-1429	245	40	IOD4	1434	-906
11	D2	-1429	104	41	IOD3	1426	-759
12	D1	-1429	-36	42	IOD2	1427	-620
13	D0	-1429	-176	43	IOD1	1427	-485
14	$\overline{\text{ROMOE}}$	-1429	-316	44	IOD0	1424	-342
15	BURN	-1417	-466	45	VDD	1416	-197
16	$\overline{\text{CE}}$	-1417	-641	46	IOA0	1433	-43
17	VSS	-1417	-791	47	IOA1	1433	98
18	SPOP	-1397	-979	48	IOA2	1426	238
19	RESET	-1401	-1126	49	IOA3	1428	381
20	IOC7	-1422	-1285	50	VSS	1400	564
21	IOC6	-1433	-1412	51	IOB7	1432	754
22	IOC5	-1424	-1570	52	IOB6	1437	895
23	IOC4	-1134	-1568	53	IOB5	1432	1040
24	IOC3	-994	-1557	54	IOB4	1443	1164
25	IOC2	-851	-1558	55	IOB3	1440	1303
26	IOC1	-699	-1559	56	IOB2	1426	1441
27	VSS	-573	-1547	57	VDD	1421	1582
28	IOC0	-416	-1562	58	IOB1	1113	1547
29	VDD	-259	-1549	59	IOB0	972	1547
30	OPT	-81	-1541	60	A0	816	1547
61	A1	675	1547	68	A7	-309	1547
62	A2	535	1547	69	A8	-458	1547
63	A3	394	1547	70	A9	-598	1547
64	A4	254	1547	71	A10	-739	1547

Pad No	Pad Name	X	Y	Pad No	Pad Name	X	Y
65	A5	113	1547	72	A11	-879	1547
66	VSS	-29	1537	73	A12	-1020	1547
67	A6	-169	1547	74	A13	-1160	1547

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