SGS-THOMSON MICROELECTRONICS

L6239

12V DISK DRIVE SPINDLE DRIVER

PRODUCT PREVIEW

General

- 12V OPERATION
- REGISTER BASED ARCHITECTURE
- SLEEP AND IDLE MODES FOR LOW POWER CONSUMPTION
- SERIAL INTERFACE

Spindle Driver

- BEMF PROCESSING FOR SENSOR-LESS MOTOR COMMUTATION
- INTERNAL POWER DEVICES
- PROGRAMMABLE SLEW-RATE FOR REDUCED E.M.I.
- 20 FOR ANY HALF BRIDGE WORST CASE (1Ω PER DEVICE)
- B.E.M.F. DETECTION READABLE FROM REGISTER OR PIN
- NO SNUBBERS REQUIRED FOR LOOP COMPENSATION OR E.M.I. CONTROL

Other Functions

- POWER UP SEQUENCING
- POWER DOWN SEQUENCING
- PWM OPERATION
- LOW VOLTAGE SENSE
- DYNAMIC BRAKE
- THERMAL WARNING
- THERMAL SHUTDOWN
- NEGATIVE VOLTAGE REGULATOR SUPPORT

DESCRIPTION

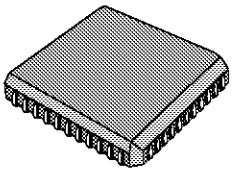
The L6239 is a single chip sensorless (DC) spindle motor controller including power stages suitable for use in disk drives.

The device has a serial interface for a microprocessor running up to 10 mega bits per second. There are registers on chip to allow the setting of the desired operating modes No external components are required in the sensor-less operation as the control functions are integrated on chip (e.g. B.E.M.F. processing & digital masking).

When a power On Reset (P.O.R.) is accepted, the internal registers are reset, the spindle power circuitry is tri-stated, and dynamic braking of the spindle is applied.

This device is built in BCD II technology allowing dense digital/analog circuitry to be combined with high power DMOS output stage.

MULTIPOWER BCD TECHNOLOGY



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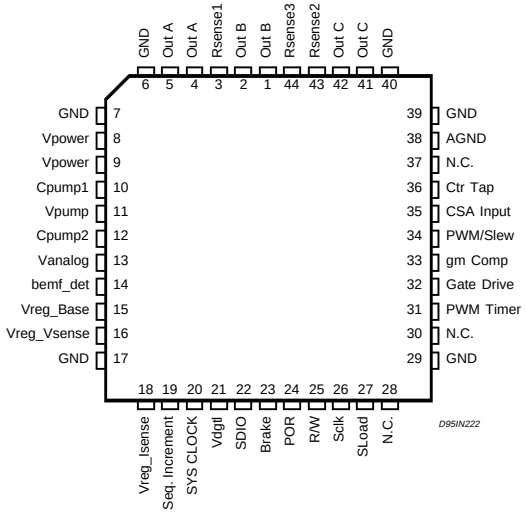
ORDERING NUMBER: L6239

PIN CONNECTION



FEATURES

General

- POWER UP MICROPROCESSOR RESET SEQUENCING
  - POWER UP RESET AND DELAY
  - INTERNAL REGISTER INITIALIZATION
- OVER TEMPERATURE PROTECTION
- MASKING ON CHIP
- COMMUTATION EXTERNALLY CONTROL-LED
- NEGATIVE VOLTAGE SUPPORT CIRCUITRY

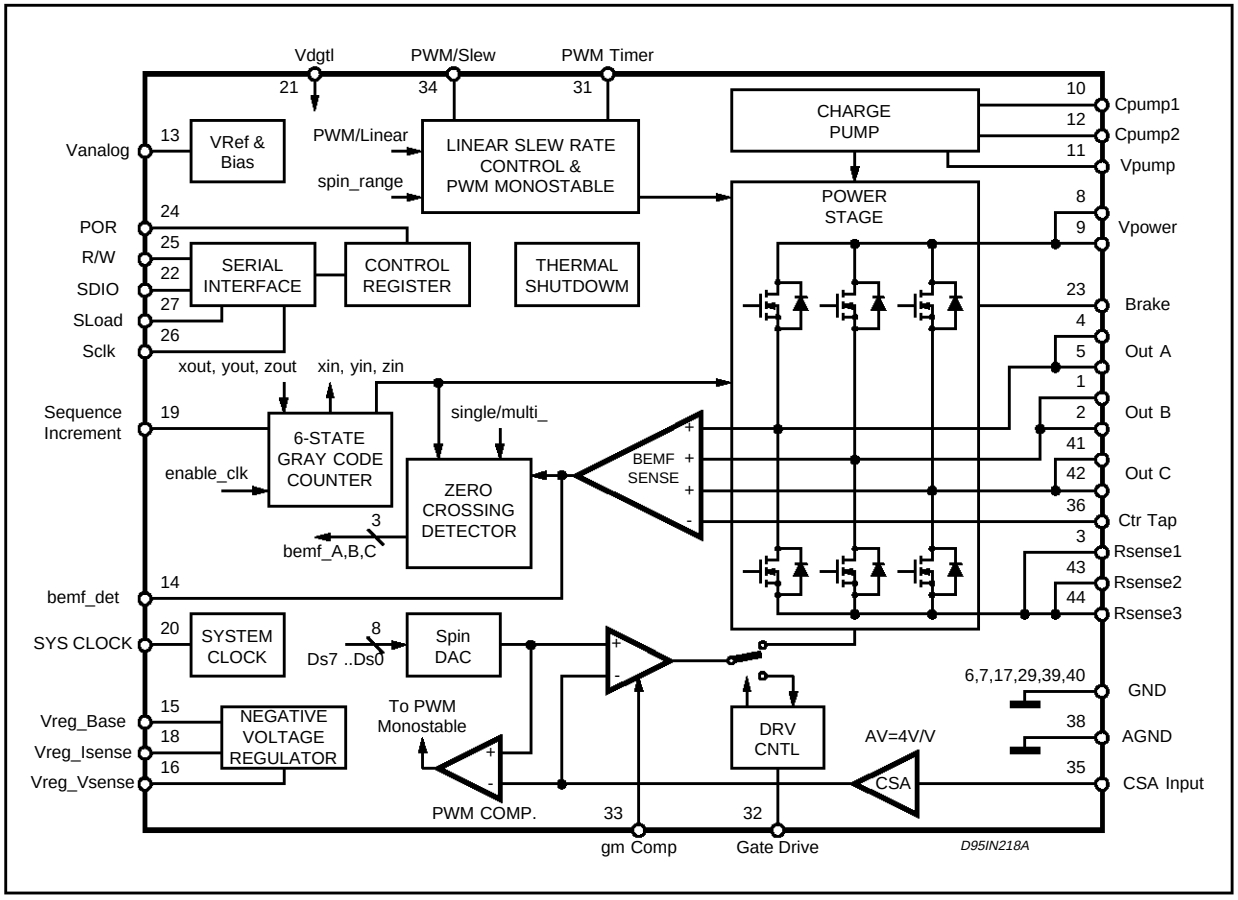
Interface

- SERIAL SYNCHRONOUS
  - SCLK, SLOAD, SDIO, R/W
  - UP TO 10 MEGABIT DATA RATE

Spindle Driver

- INTERNAL POWER DEVICES
- THREE PHASE BRIDGE PLUS BIPOLAR DRIVER
  - MICROPROCESSOR SPIN-UP & SPEED CONTROL
  - MICROPROCESSOR INITIATED STARTUP
  - SPEED COMPENSATION BY EXTERNAL RC NETWORK
  - NO SNUBBERS REQUIRED FOR CURRENT LOOP COMPENSATION OR EMI CONTROL
  - MICROPROCESSOR ACCELERATION CONTROL VIA DAC (FOR SMOOTH TRANSITION TO AT SPEED CONTROL)
  - GRAY CODE COUNTER FOR COMMUTATION CONTROL (INCREMENTED BY SPIN_CLOCK PIN).
  - BEMF DETECTION READABLE FROM REGISTERS (A,B OR C PHASES) OR PIN (BEMF_DET).
- AUTOMATIC CLAMPING OF OUTPUT TO PREVENT SUBSTRATE CURRENT
- PROGRAMMABLE SLEW RATE CONTROL (LINEAR MODE ONLY)
- 8 BIT RESOLUTION SPINDLE DAC FOR MICROPROCESSOR ACCELERATION CONTROL
- DYNAMIC BRAKING BY COMMAND

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Maximum Supply Voltage (Vanalog, power max)	15	V
V_S	Maximum Supply Voltage (Vdigital max)	7	V
V_{Imax}	Maximum Input Voltage	Vdigital ± 0.3	V
$V_{I\ min}$	Minimum Input Voltage	GND - 0.5	V
I_{peak}/I_{dc}	Peak Sink/Source Output Current/DC Sink Source Output Current	2.2	A
P_{tot}	Maximum Total Power Dissipation	3	W
T_{stg}, T_j	Maximum Storage and Junction Temperature Range	-40 to 150	°C

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient (standard PCB mounted)	27	°C/W

Note:
This standard board construction includes: A 4 layer board, for 1cm2 hest copper area best sinks located at the chips vertices each with 4 rows of 4 columns of plated vias (od = 0.104cm, diameter = 0.0584cm) through to the ground plane.

PIN DESCRIPTION

Pin Types: I = Input, O = Output, P = Power, A = Analog (passive)

N.	Name	Function	Pin Type
POWER			
6, 7, 17, 29, 40	Ground	Power Ground	AI
38	Analog Ground	Analog Signal Return	AI
8, 9,37	VPower	Driver Power Supply (12V)	AI
13	VAnalog	Analog Supply (12V)	AI
21	Vdgtl	Logic Supply (5V)	AI
SERIAL INTERFACE, DIGITAL & TEST PINS			
22	SDIO	Serial Port Data I/O	DI/O
25	R/W	Serial Port Read/Write Input	DI
27	SLoad	Serial Port Chip Select. Port is selected when low	DI
26	SCLK	Serial Port Clock	DI
19	Sequence Increment	Increments the spindle commutation on low to high transition	DI
23	Brake	Applies braking (all low side drivers energized) after the timedefined by Brake_time. Active low	DI
24	POR	Resets the controller on receipt of POR low	DI
14	BEMF det	Post masching BEMF zero crossing signal	DO
20	SYS CLK	Sistem clock	DI
28	TP out1	Test pin 1	TO
30	TP out2	Test pin 2	TO
ANALOG PINS			
4, 5	Coil A	Motor Coil Driver for phase A. This pin is also used for sensing the BEMF	AI/O
1, 2	Coil B	As above for phase B	AI/O
41, 42	Coil C	As above for phase C	AI/O
36	Center Tap	Center tap motor connection	AI/O
3, 43, 44	Rsense	Sense Resistor Pins	AI/O
35	CSA Input	Current Sense Amplifier Input for sensing of voltage across the external sense resistor.	AI/O
33	GM Comp	A series RC network to ground that defines the compensation for the Transconductance Loop	AO
32	Gate Drive (NOTE 1)	For external PMOS applications	AI/O
10	Cpump 1	Positive terminal of the pump capacitor	A/O
12	Cpump 2	Negative terminal of the pump capacitor	A/O
11	Vpump	Charge pump output	A/O
34	PWM/ Slew	An RC network to GND defines the slew ate from this pin	AO
31	PWM Timer	Masking for PWM (max)	AO
15	Vreg Base	Negative voltage regulator - Base	A/O
18	Vreg Isense	Negative voltage regulator - Current input	AI
16	Vreg Vsense	Negative voltage regulator - Regulator	AI

NOTE 1: for internal mode, this pin must be grounded. For external mode, connect this pin to the external PMOS.

ELECTRICAL CHARACTERISTICS (T_{amb} = 0 to 70°C; V_A = V_{power} = 12V; $V_{digital}$ = 5V, unless otherwise specified. Parameters market with an * are guaranteed by design, but not 100% tested in production)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
GENERAL						
$V_{analog, Power}$	Supply Voltage Range		10	12	13.6	V
$V_{digital}$	Supply Voltage Range		4.5	5	5.5	V
$I_{ready12}$	Quiescent Current	Spindle Enabled			15	mA
$I_{sleep12}$	Quiescent Current	Spindle Disabled			1000	µA
I_{ready5}	Quiescent Current	Spindle Enabled			5	mA
I_{sleep5}	Quiescent Current	Spindle Disabled			1000	µA
THERMAL SHUTDOWN						
*Th_{Warn}	Thermal Warning		130	150	170	°C
*$Th_{Sh\ Dwn}$	Thermal Shutdown		155	175	195	°C
SPINDLE DRIVER SECTION						
I_o	Maximum Output Current		2.2			A
dv/dt on	Voltage Sew Rate	Turn on	0.2		2.0	V/µs
		Turn off	0.1*		1.0*	V/µs
$R_{DS(on)}$ Total	Total Output On Resistance (Sink + Source)	Tj = 25°C, Tj = 125°C, Iload = 2.0A		1.0	2.0	Ω
$R_{DS(on)}$ Device	Sink Output On Resistance	Tj = 25°C, Tj = 125°C, Iload = 2.0A		0.5	1.0	Ω
$I_{o\ (LEAK)}$	Output Leakage Current				1	mA
V_F	Body Diode Forward Drop	Im = 2.0A			1.5	V
		I_m = 100mA			0.9	V
dV_o/dt	Output Slew Rate	R_{slew} = 100KΩ		0.30	0.35	V/µs

* Yet to be confirmed

DAC ACCELERATION CONTROL / SENSE AMPLIFIER						
RES	Resolution	Full scale			8	bits
NL	Differential Non-linearity	0-1 bit excluded			0.5	LSB
INL	Integral Non- linearity				1.5	LSB
FS	Full Scale Accuracy				5	%
CT	Conversion Time				10	µs
FSCT	Full Scale Temp Coefficient	0 to 125°C			250	ppm/°C
Gain	Curr. Sense Gain Ratio 4:1 or 20:1	1% resistence tolerance (0.5Ω)			TBD	%
DAC_{out}	DAC Output		0		2	V
OFFSET	Input Offset of Sense Amp		0	7	15	mV
LOGIC SECTION (All digital inputs are CMOS compatible)						
V_{ih}	High Level Input Voltage		3.5			V
V_{il}	Low Level Input Voltage				1.5	V
V_{oh}	High Level Output Voltage	I_{out} = 1.0mA	4.5			V
V_{ol}	Low Level Output Voltage	I_{out} = 1.0mA			0.4	V
I_{in}	Input Leakage Current	Tj = 125°C, 1	-1		1	mA
I_{wsi}	Minimum Sequence Increment High Time		Note 1			
F_{sys}	System Clock Frequency				10.0	MHz

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
C_{in}	Logic Input Capacitance (except Serial Port Clock)	All inputs except SCLK			5	pF
C_{in}	Serial Port Clock Input Capacitance (Logic Level Low)	SCLK			10	pF
POR_{IN}	POR Pulse Width		1			µs

Note1: The minimum time that the Sequence Increment pin must be held high during eternal sequence incrementing is equal to $\left(\frac{4}{SysCk}\right)$

BEMF AMPLIFIER						
I_{Ampin}	Input Bias Current				10.0	µA
V_{BEMF}	Minimum Bemf (Pk-Pk)		60			mV
V_{OFF_HYST}	Voltage Offset Hysteresis		11	18	25	mV
BRAKE						
T_{brake}	Time from POR signal receipt to expected receipt of Brake signal		0.01		500	ms
I_{brlk}	Brake Leakage Current				10	µA
I_{brin}	Brake Low Input Current		100			µA
NEGATIVE VOLTAGE REGULATOR - CURRENT SENSE COMPARATOR						
I_{bias}	Input Bias Current	0.3V input			2	µA
T_{resp}	Response Time	20mV overdrive			1	µs
$High_{Th}$	High hysteresis threshold		0.336		0.464	V
Low_{Th}	Low Hysteresis Threshold		0.033		0.046	V
NEGATIVE VOLTAGE REGULATOR - VOLTAGE SENSE COMPARATOR						
I_{bias}	Input Bias Current	0.3V input			2	µA
T_{resp}	Response Time	20mV overdrive			1	µs
V_{Th}	Comparator Threshold		1.20	1.27	1.333	V
V_{Hys}	Comparator Hysteresis		5		20	mV
NEGATIVE VOLTAGE REGULATOR - DRIVER OUTPUT						
I_{low}	Low Output Current	V_O < 3.5V	4			mA
V_{high}	Output High Voltage	I = 0.1mA; (V_{Dig} = 5V)	4.8			V
V_{low}	Output Low Voltage	I = -4mA	3.5			V
LOOP BACK COMPARATOR						
V_{th}	Switching Threshold		0.45	0.50	0.55	V

INTERNAL REGISTER DEFINITION

Spin Control Register (Reg 0)

The first (bits 0-8) is to program the current to the spindle motor to allow motor control and to present the "at speed" voltage for the charge pump. Often this will be used to limit the start-up current.

Reg: 0

Type: Write only.

BIT	LABEL	DESCRIPTION	@POR_ LOW
0	SPIN DAC BIT 0	Spindle current limit LSB	0
1	SPIN DAC BIT 1		0
2	SPIN DAC BIT 2		0
3	SPIN DAC BIT 3		0
4	SPIN DAC BIT 4		0
5	SPIN DAC BIT 5		0
6	SPIN DAC BIT 6		0
7	SPIN DAC BIT 7	Spindle current limit MSB	0
8	SPIN RANGE	Spindle transconductance loop gain range select, 0 = 4:1, 1= 20:1	0

System Input Register (Reg 1)

Reg: 1

Type: Write only.

BIT	LABEL	DESCRIPTION	@POR_ LOW
0	SLEEP	A0 puts the spindle into a high impedance state	0
1	BRAKE	A1 turns on all lower spindle drivers to brake the spindle	0
2	PWM/$\overline{\text{LINEAR}}$	Selects either PWM (1) or Linear (0) modes of operation	0
3	SINGLE/$\overline{\text{MULTI}}$	1 selects phase. A for zero crossings, 0 selects all three phases	0
4	ENABLE CLK	Enables (1) the SPIN CLK pulses to increment the spindle counter	0
5	RESPHASE	Logic low to reset spindle counter	0
6	TRIST di	Logic low to tristate BEMF DET output.	0
7	CLKDIV2	Logic low - sys clk; logic high - half system clock	0
8	ENABLE NEG	Enables Negative Voltage circuitry (when set to 1).	0
9	TIME2X	Logic low - masking time equal to 512 cycles of sys clk. Logic high - masking time equal to 1024 cycles of sys clk.	0
10	TEST PIN1	Test pin	0
11	TEST PIN2	Test pin	0

System Input Register (Reg 2)

Reg: 2

Type: Read only.

BIT	LABEL	DESCRIPTION	@POR
0	BEMF A	Phase A zero crossing detected	0
1	BEMF B	Phase B zero crossing detected	0
2	BEMF C	Phase C zero crossing detected	0
3	IN X	Grey code counter bit X	0
4	IN Y	Grey code counter bit Y	0
5	IN Z	Grey code counter bit Z	0
6	THERM_WARN	Thermal shutdown warning. This occurs approximately 25°C before the device goes into thermal shutdown.	0
7	LOOP_BACK	If PWM bit is set to 0, this bit represent the status of the loopback comparator	0

Register Select Table

INPUT: A3 - A0	REGISTER SELECTED	TYPE
0000	0	WRITE
0001	1	WRITE
0010	2	READ

CIRCUIT OPERATION

General

This device includes a sensorless spin driver, power sequencing with dynamic braking and serial interface for a microprocessor. The device is register based to eliminate single point interconnects where ever possible.

It is designed to operate with a 12V power supply.

POR

When POR goes low, the L6239 resets itself and all registers to the "@POR" state (see register description).

The L6239 assumes that a separate brake command must be issues to brake the spindle.

Serial Interface

The serial interface is designed to be compatible with the Intel 80196 (and other similar micros) serial interface but is capable of faster data rates, up to 10MHz.

All read and write operations must consists of 16 bits, with the 80196 this would be two 8 bit accesses.

The first four bits are address and the next 12 are data. If the address is a read register, then the L6239 will use the SCLK from the system to shift out 12 bits of data from the addressed register.

The system must provide 16 SCLK pulses to insure that the read operation completes. The SDIO line is capable of driving a 60pf load.

Symbol	Description	Min.	Typ.	Max.	Unit
t_{RWS}	R/$\overline{W}$ setup time to SCLK going high	100			ns
t_{SLS}	SLOAD setup time to SCLK going high	100			ns
t_{RWH}	R/$\overline{W}$ hold time after SCLK going high	100			ns
t_{SLH}	SLOAD hold time after SCLK going high	100			ns
t_{SCKD}	SCLK high to Data Valid	10	30	50	ns
t_{RWD}	R/$\overline{W}$ High to Data Valid Data bit D [0] valid from HiZ	10	30	50	ns
t_{AS}	Address setup time to SCLK going high	30			ns
t_{DS}	Data setup time to SCLK going high	30			ns
t_{AH}	Address hold after SCLK going high	10			ns
t_{DH}	Data hold time after SCLK going high	10			ns
t_{SDZ}	SDIO tri-state after SLOAD going high	30			ns
t_{RWZ}	SDIO tri-state afterR/$\overline{W}$ going low	30			ns
t_{PER}	Minimum SCLK period	100			ns
t_{REC} (*)	Recycle - Time between successive accesses	100			ns
t_{DUT}	Clock duty cycle	40	50	60	%
t_{SCLK}	SCLK Clock timing	100	0.1		µs

(*) For 10MHz system clock operation (in other words, 1 or more clock cycles of SCLK).

Serial Interface Truth Table

R/$\overline{W}$	SLOAD	SDIO	DIRECTION
1	1	Tri-state (Port un-selected)	Tri-state
0	1	Tri-state (Port un-selected)	Tri-state
0	0	Address/Data input	Input
1	0	Data output	Output

Figure 1: Serial Write Timing Diagram

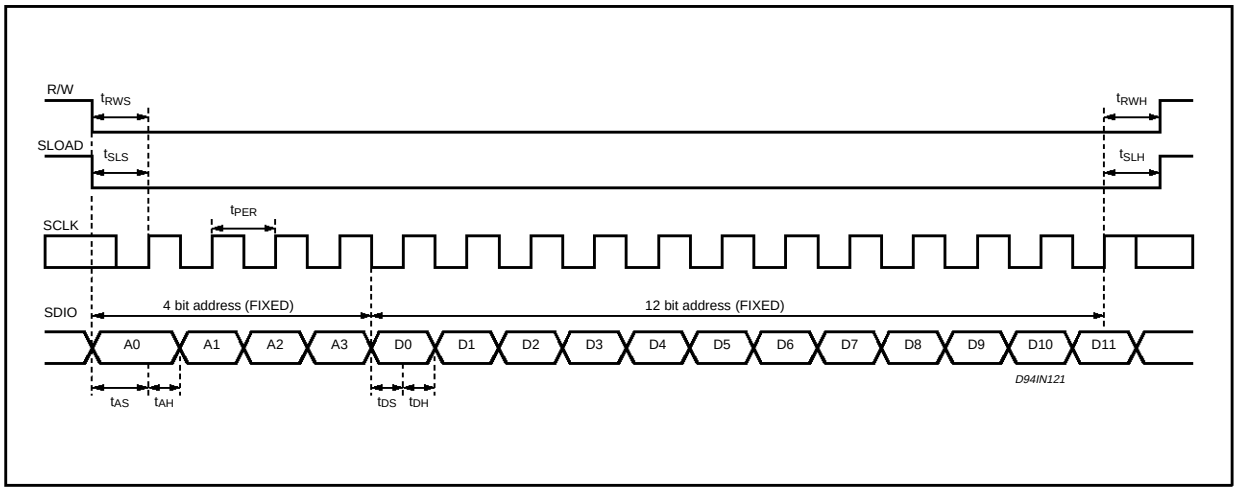
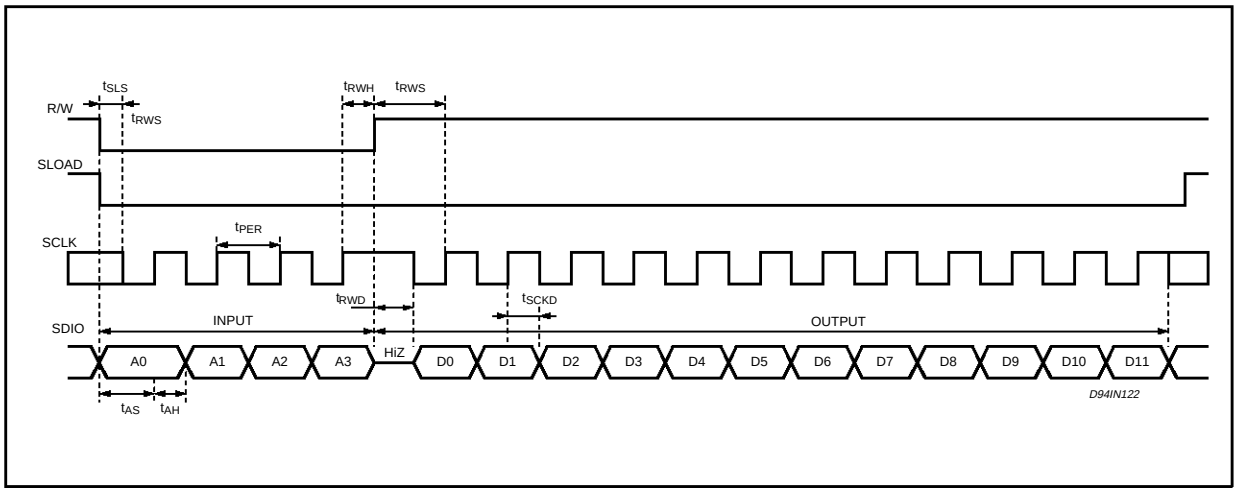


Figure 2: Serial Read Timing Diagram



The write cycle has a fixed address and data length. Four bits of address and 12 bits of data must be clocked in to allow the data to be loaded into the desired register.

The write cycle is initiated by setting SLOAD and R/W low. Setting R/W low causes the SDIO line to be tristated for data input. SLOAD low enables the internal counter to increment on the rising edge of SCLK. The address and data are clocked into the chip serially on each rising edge of SCLK as shown above. when both the 4 bits of address and the 12 bits of the data have been clocked in, then the address register will be written to with the provided data.

Setting SLOAD high will clear theinternal logic and tri-state the SDIO line. This also provides a way of safely aborting a write by simply forcing SLOAD high.

NOTE:
SLOAD must be kept low during the entire duration of the 16 write clocks.

The read cycle is initiated by setting SLOAD low and clocking in a valid read address.

Only four bits of address are necessary, if more than four bits are clocked in, the four MSBs will be ignored (i.e. only the first four bits will be used).

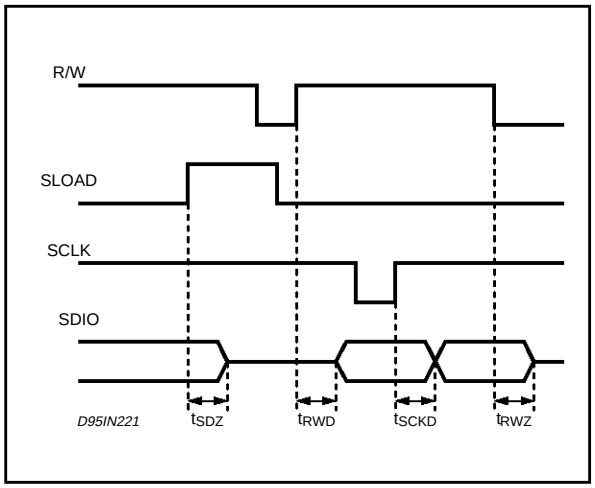
If a valid address is detected, the rising edge of R/W will liad the desired register into the internal serial/parallel register is then serially clocked out on every rising edge of SCLK (LSB is clocked out first). Additional padded bits clocked out will be zero.

NOTE:
If SLOAD is set low with R?W high, the current contents of the internal shift register can be clocked out. This is useful for a ”read back” of the data last written into the required register.

Figure 3, illustrates the case where the serial port is deselected while reading data.

During a read mode, the mP is in tri-state and the L6239 is writing data on to the SDIO pin. If the

Figure 3



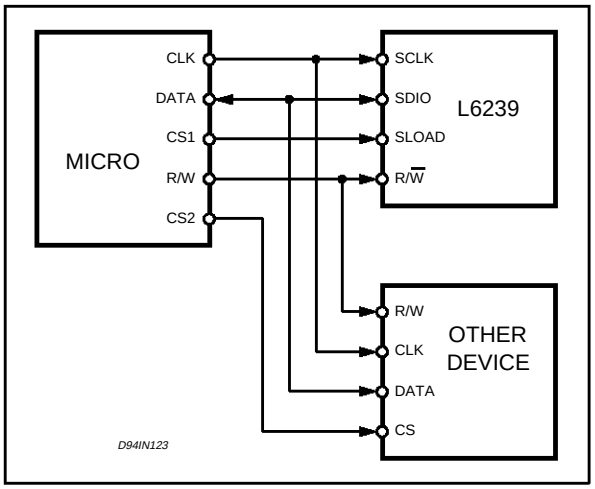
L6239 is deselected by bring SLOAD high, the serial port stops writing and assumes a tri-state condition after time t_{STZ}.

When R/W goes low, the Serial Port stops writing to SDIO. This is actually a transparent operation, since SDIO is already tri-stated.

Next, SLOAD goes low, selecting the L6239, but SDIO remains low since R/W is still low. When R/W goes high, the L6239 starts to write to SDIO with the data valid after time, t_{RWD}.

At the end of the read operation, R/W goes low and SDIO goes into tristate condition after time t_{RWZ}.

Figure 4: System Level Interface



drive is in bipolar mode (Unipolar is not supported).

S_A_L, S_B_L and S_C_L are the lower spindle drive transistors. They are active in bipolar drive. In linear mode the active transistor's gate drive is controlled so as to bring the current in the motor to the level set by the speed control compensation circuit or the current limit DAC. Activating the BRAKE mode turns on all the lower drivers.

RESET places the state machine into a known state (see @POR column of register definitions).

To increment the commutation state either Spin_Clock signal is clocked.

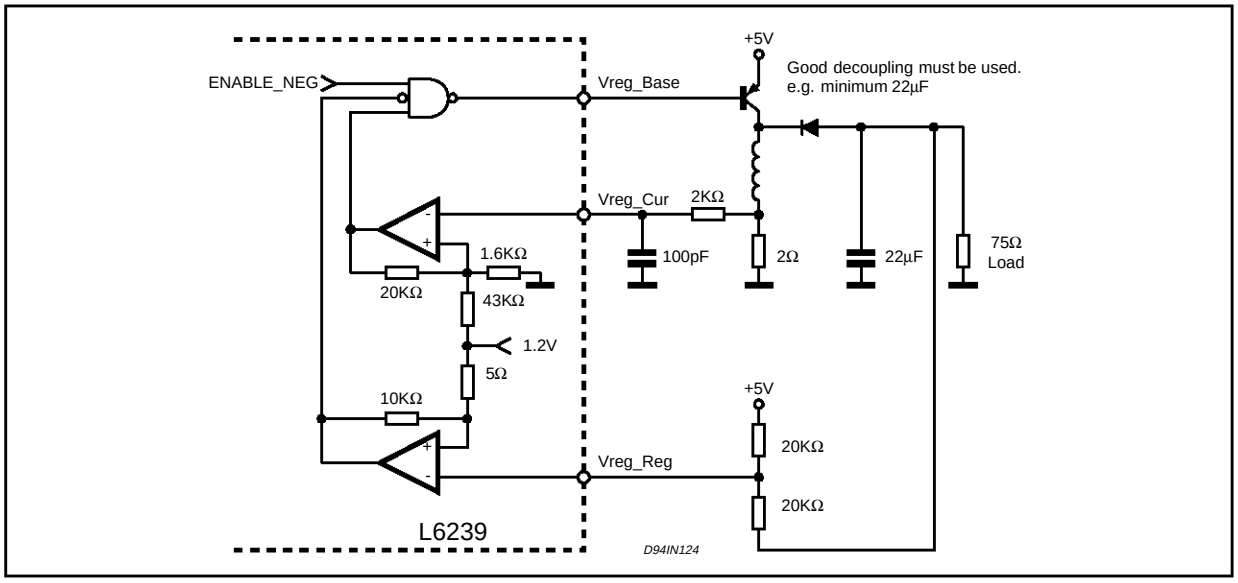
Power Devices/Spindl State Machine

S_AU, S_B_U and S_C_U are the upper spindle drive transistors. They are active whenever the

Thermal Warning & Shutdown

The Thermal (Shutdown) Warning is designed to allow the system to take any actions required

Figure 5



prior to the L6239 shut down at the Thermal Shutdown level.

Once the Thermal SHutdown is triggered the spindle is tristated and the chip is reset (although the serial interface can still be used). No braking function taken place.

The chip remains in this state with the serial interface available for access

Once the device falls below the Thermal Warning temperature, the L6239 output stage is no longer tristated.

If there is still sufficient motion in the motor, the µP has the opportunuty to resynchronize the output

Negative Voltage Regulator Support

This device includes support for a negative voltage supply. The regulator uses a regulation technique, that generates an external negative voltage, but does not require an negative power supply. the diagram below shows the circuitry included in the L6239 to support the Regulator.

The more lightly colored circuitry is the recommended external circuitry that actually creates the negative voltage.

The circuit has been designed so that all external componentsa can be inexpensive. For example, the transistor needs only to be a 2N@()&A and the diode a 1N4148.

PLCC44 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	17.4		17.65	0.685		0.695
B	16.51		16.65	0.650		0.656
C	3.65		3.7	0.144		0.146
D	4.2		4.57	0.165		0.180
d1	2.59		2.74	0.102		0.108
d2		0.68			0.027	
E	14.99		16	0.590		0.630
e		1.27			0.050	
e3		12.7			0.500	
e4			1.98			0.078
F		0.46			0.018	
F1		0.71			0.028	
G			0.101			0.004
M		1.16			0.046